AN-6083

Highly Integrated, Dual-PWM Combination Controller

Introduction

This application note shows the step-by-step process to design a high-performance power supply which includes a flyback converter for standby power and a single forward converter for main power. Design considerations and mathematical equations are presented, as well as guidelines for a printed-circuit-board (PCB) layout.

The complete power-supply circuits shown in Figure 1 demonstrate the FAN6791's ability to manage high-output power while complying with international requirements regarding AC line quality.

The FAN6791 is designed for the power supplies to achieve high efficiency. The highly integrated FAN6791 dual-PWM combination controller provides several features to enhance the performance of converters. To minimize standby power consumption, a proprietary green-mode function provides off-time modulation to linearly decrease the switching frequency at light-load conditions. With the internal high-voltage startup circuitry, the power loss due to bleeding resistors is also eliminated. The built-in synchronized slope compensation of FAN6791 achieves stable peak-current-mode control. The proprietary internal line compensation ensures constant output-power limit.

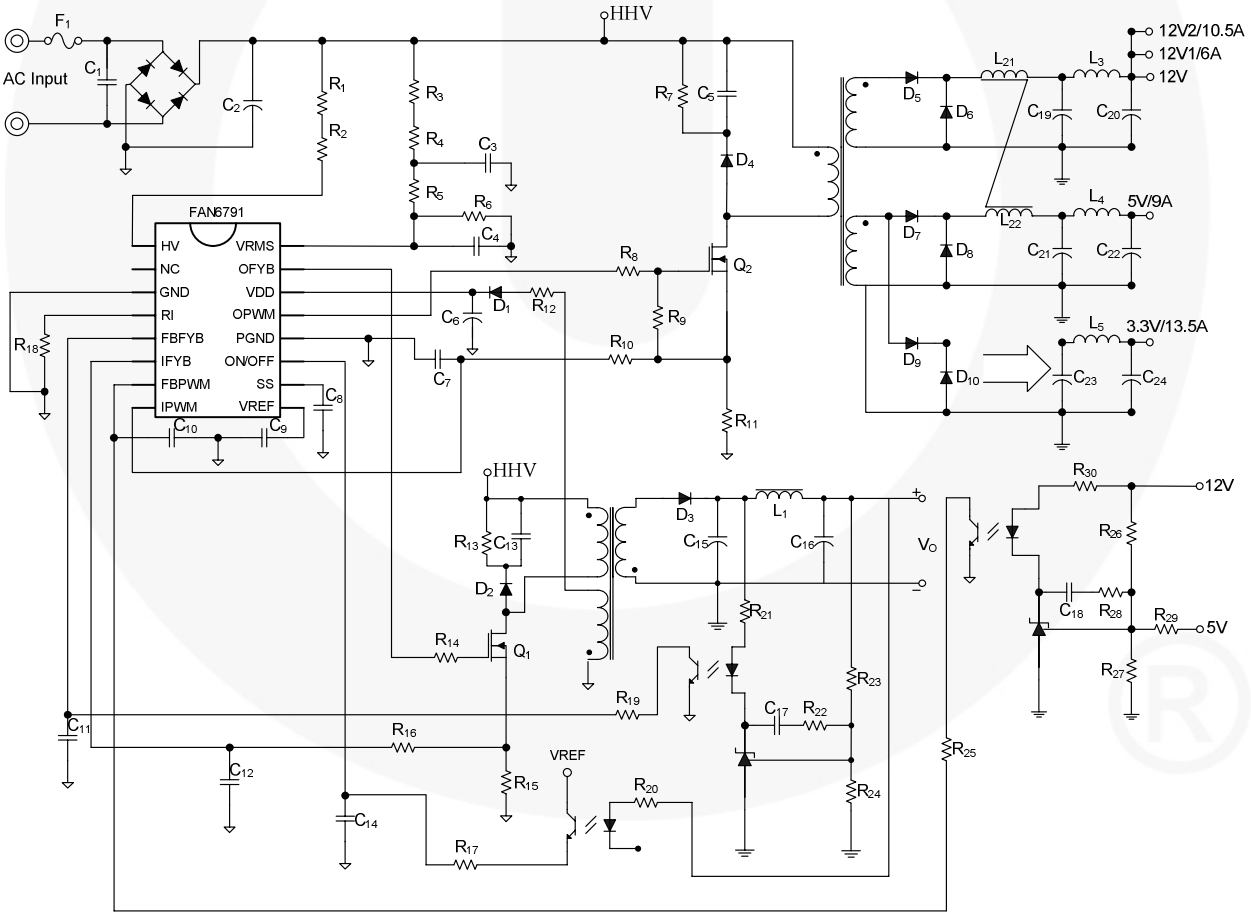

Figure 1. Typical Application

Startup Circuitry

When the power is turned on, the internal current source (typically 2.5mA) charges the hold-up capacitor C_6 through a startup resistor R_{HV}. During the startup sequence, the V_{AC} from the bulk capacitor provides a startup current of about 2.5mA and charges the capacitor C_6. R_{HV} can be directly connected by V_{AC} to the HV pin. As the VDD pin reaches the start threshold voltage V_{TH-ON}, the FAN6791 activates and signals the MOSFET. The high-voltage source current is switched off, and the supply current is drawn from the auxiliary winding of the main transformer.

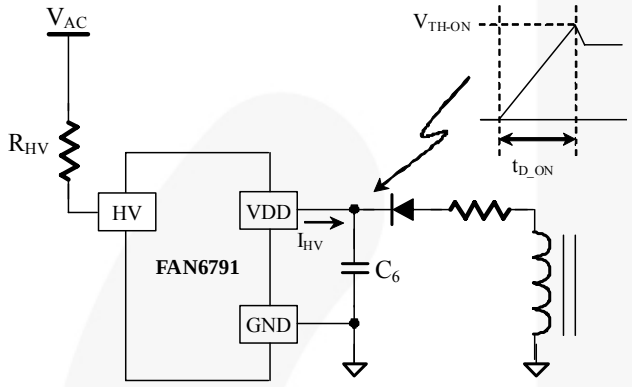

Figure 2. Startup Circuit for Power Transfer

The minimum power-on delay time is determined as:

$$t_{D\_ON} = \frac{\left(C_6 \times V_{TH-ON}\right)}{2.5\text{mA}} \quad \textbf{(1)}$$

where V_{TH-ON} is the turn-on threshold voltage and t_{D_ON} is the power-on delay time of the power supply.

Due to the low startup current, a large $R_{HV,}$ such as 100kΩ, can be used. With a hold-up capacitor of 22μF, the power-on delay t_{D_ON} is less than 300ms for $90V_{AC}$ input.

When the supply current is drawn from the transformer, it draws a leakage current of about 10μA from pin HV.

The power dissipation of the R_{HV} is:

$$P_{HV} = I_{HV-CS}{}^2 \times R_{HV} \quad \textbf{(2)}$$

where I_{HV-CS} is the supply current drawn from the HV pin.

Under-Voltage Lockout (UVLO)

FAN6791 has a voltage detector on the VDD pin to ensure that the chip has enough power to drive the MOSFET. Figure 3 shows a hysteresis of the turn-on and turn-off threshold levels and an open-loop-release voltage.

The turn-on and turn-off thresholds of the FAN6791 are internally fixed at 16V and 10V, respectively. During startup, the V_{DD} capacitor must be charged to 16V to enable the IC. The capacitor continues to supply the V_{DD} until the energy can be delivered from the auxiliary winding of the main transformer. The V_{DD} must not drop below 10V during the startup sequence.

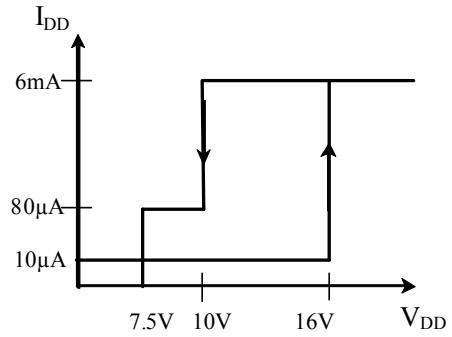

Figure 3. UVLO Specification

If the secondary output short circuits or the feedback loop is open, the FB pin voltage rises rapidly toward the open-loop voltage, V_{FB-OLP}. Once the FB voltage remains above V_{FB-OLP} for t_{OLP}, the FAN6791 stops emitting output pulses. To further limit the input power under a short-circuit or open-loop condition, a special two-step UVLO mechanism prolongs the discharge time of the VDD capacitor. Figure 4 shows the traditional UVLO method with the special two-step UVLO method. In the two-step UVLO mechanism, an internal sinking current, I_{TH-OLP}, pulls the V_{DD} voltage toward the V_{TH-OLP}. This sinking current is disabled after the V_{DD} drops below V_{TH-OLP}; after which, the V_{DD} voltage is charged towards V_{TH-ON}. With the addition of the two-step UVLO mechanism, the average input power during short-circuit or open-loop condition is greatly reduced and overheating doesn't occur.

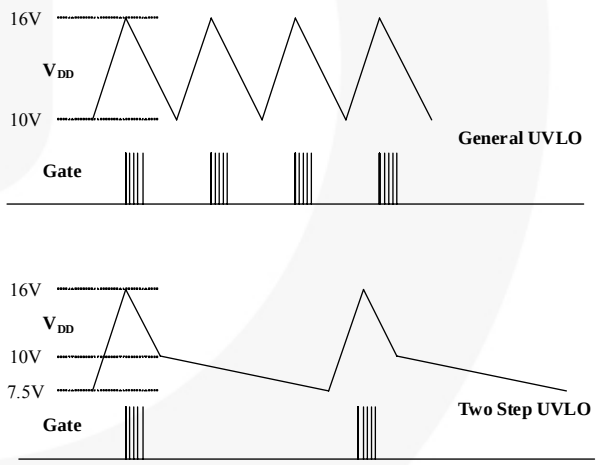

Figure 4. UVLO Effect

Oscillator and Green Mode

Resistor R_I programs the frequency of the internal oscillator. A 24kΩ resistor R_I generates 50μA reference current I_I and determines the PWM frequency as 65KHz:

$$I_I(\text{mA}) = \frac{1.2}{R_I(\text{k}\Omega)} \quad \textbf{(3)}$$

$$f_{OSC}(\text{kHz}) = \frac{1560}{R_I(\text{k}\Omega)} \quad \textbf{(4)}$$

The range of the PWM oscillation frequency is designed as 33KHz ~ 130KHz. FAN6791 integrates frequency hopping

function internally. The frequency variation ranges from around 61KHz to 69KHz for a center frequency 65KHz. The frequency hopping function helps reduce EMI emission of a power supply with minimum line filters.

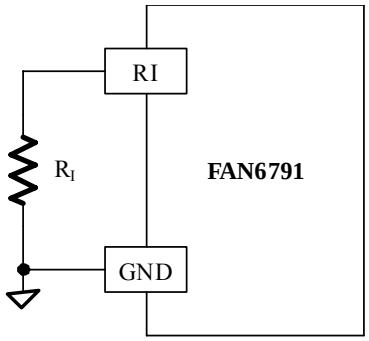

Figure 5. Setting the PWM Frequency

For power saving, flyback PWM stage has a green mode function. Frequency linearly decreases when V_{FBFYB} is within V_G and V_N. Once V_{FBFYB} is lower than V_G, switching frequency disables, and it enters burst mode.

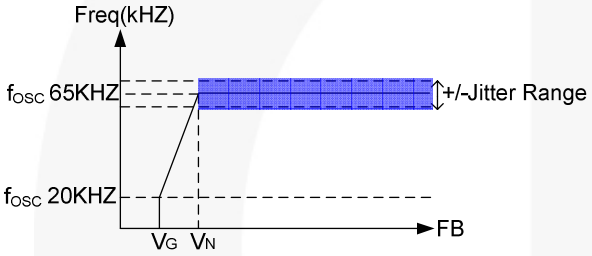

Figure 6. Oscillation Frequency in Green Mode

Line Voltage Detection (V_{RMS})

Xxx Figure 7 shows a resistive divider with low-pass filtering for line-voltage detection on VRMS pin. The V_{RMS} voltage is used for brownout protection: when V_{RMS} drops below 0.8V, OPWM turns off.

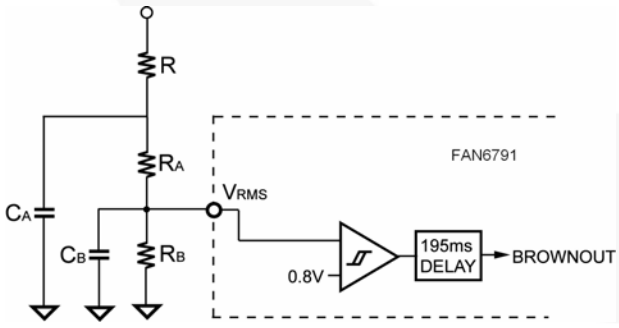

Figure 7. Line-Voltage Detection on VRMS Pin

Remote On/Off

Figure 8 shows the remote on / off function. When the supervisor FPO pin pulls down and enables the system by connecting an opto-coupler, V_{REF} applies to the ON/OFF pin to enable forward PWM stage.

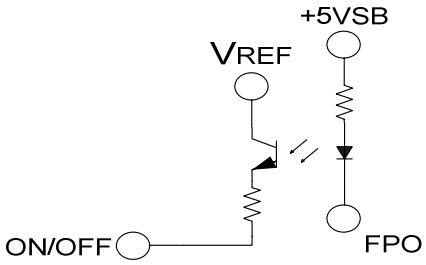

Figure 8. Remote On/Off

Interleave Switching

The FAN6791 uses interleaved switching to synchronize the stand-by PWM / forward PWM stages. This reduces switching noise and spreads the EMI emissions. Figure 9 shows off-time t_{OFF} is inserted in between the turn-off of the stand-by gate drives and the turn-on of the forward PWM.

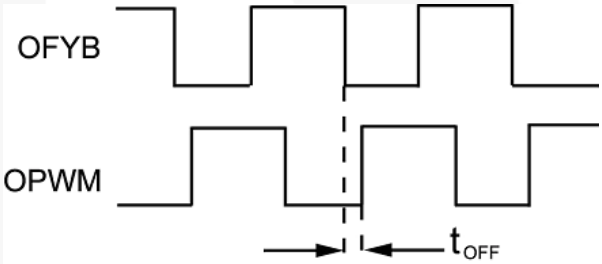

Figure 9. Interleaved Switching

FBFYB and FBPWM

The FAN6791 is designed for peak-current-mode control. A current-to-voltage conversion is done externally with a current-sense resistor R_S. Under normal operations, the peak inductor is controlled by an FBFYB level as:

$$I_{PEAK} = \frac{V_{FBFYB} - 1.3}{3.2 \times R_S} \quad \textbf{(5)}$$

when V_{FBFYB} is less than 1.3V, the FAN6791 terminates the output pulses.

Figure 10 is a typical feedback circuit consisting mainly of a shunt regulator and an opto-coupler. R_1 and R_2 form a voltage divider for the output voltage regulation. R_3 and C_1 are adjusted for control-loop compensation. A small-value RC filter (e.g. R_{FB} = 47Ω, C_{FB} = 1nF) placed on the FB pin to the GND can further increase the stability.

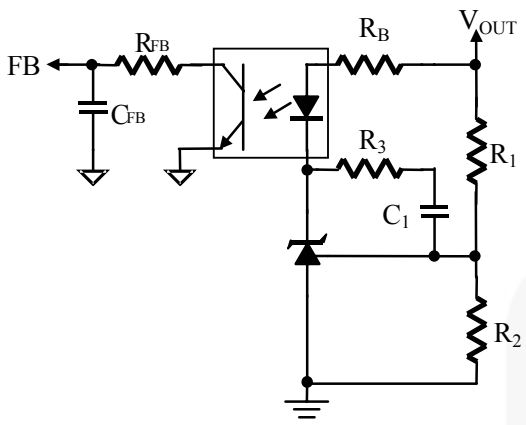

Figure 10.Feedback Circuit

The maximum sourcing current of the FB pin is 1.04mA. The phototransistor must be capable of sinking this current to pull FB level down at no load. The value of the biasing resistor R_B is determined as:

$$\frac{V_{OUT} - V_D - V_Z}{R_B} \times K \geq 2mA \quad \textbf{(6)}$$

where:
V_D is the drop voltage of photodiode, approximately 1.2V;
V_Z is the minimum operating voltage, 2.4V of the shunt regulator; and
K is the current transfer rate (CTR) of the opto-coupler.

For output voltage V_{OUT} = 5V, with CTR = 100%, the maximum value of R_B is 560Ω.

Built-In Slope Compensation

A flyback converter can be operated in either discontinuous current mode (DCM) or continuous current mode (CCM). There are many advantages to operating the converter in CCM. With the same output power, a converter in CCM exhibits a smaller peak inductor current than in DCM; therefore, a small-sized transformer and a low-rated MOSFET can be applied. On the secondary side of the transformer, the RMS output current of DCM can be twice that of the CCM. Larger wire gauge and output capacitors with larger ripple-current ratings are required. DCM operation also results in higher output-voltage spikes. A large LC filter has to be added. A flyback converter in CCM achieves better performance with a lower component cost.

Despite the above advantages of CCM operation, there is one concern—stability. In CCM operation, the output power is proportional to the average inductor current, while the peak current remains controlled. This causes sub-harmonic oscillation when the PWM duty cycle exceeds 50%. Adding slope compensation (reducing the current-loop gain) is an effective way to prevent oscillation. The FAN6791 introduces a synchronized positive-going ramp (V_{SLOPE}) in every switching cycle to stabilize the current loop. Therefore, the FAN6791 can be used to design a cost effective, highly efficient, compact flyback power supply operating in CCM without additional external components.

The positive ramp added is:

$$V_{SLOPE} = \Delta V_{SLOPE} \times D \quad \textbf{(7)}$$

where ΔV_{SLOPE} = 0.37V and D = duty cycle.

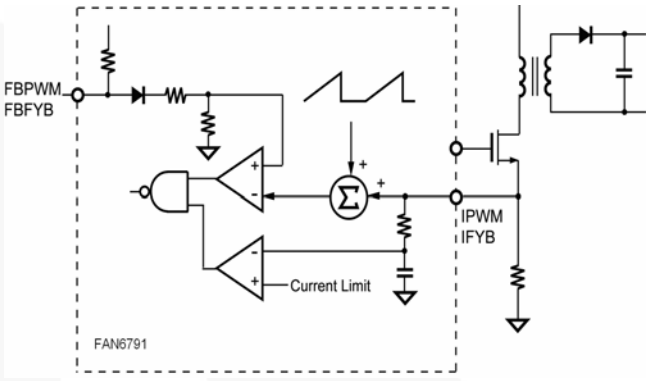

Figure 11.Synchronized Slope Compensation

Constant Power Control

To limit the output power of the converter constantly, a power-limit function is included. Sensing the converter input voltage through the VRMS pin, the power limit function generates a relative peak-current-limit threshold voltage for constant power control, as shown in Figure 12.

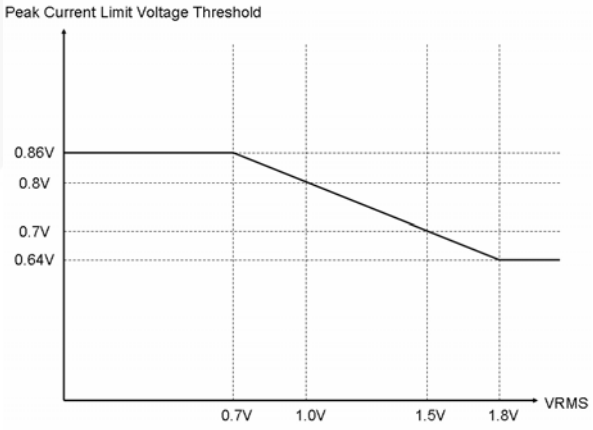

Figure 12. Constant Power Compensation

Leading Edge Blanking (LEB)

A voltage signal proportional to the MOSFET current develops on the current-sense resistor R_S. Each time the MOSFET is turned on, a spike is induced by the diode reverse recovery and by the output capacitances of the MOSFET and diode, inevitably appearing on the sensed signal. Inside the FAN6791, a leading-edge blanking time of about 270ns is introduced to avoid premature termination of MOSFET by the spike. Only a small-value RC filter (e.g. 100Ω + 470pF) is required between the SENSE pin and R_S. Still, a non-inductive resistor for the R_S is recommended.

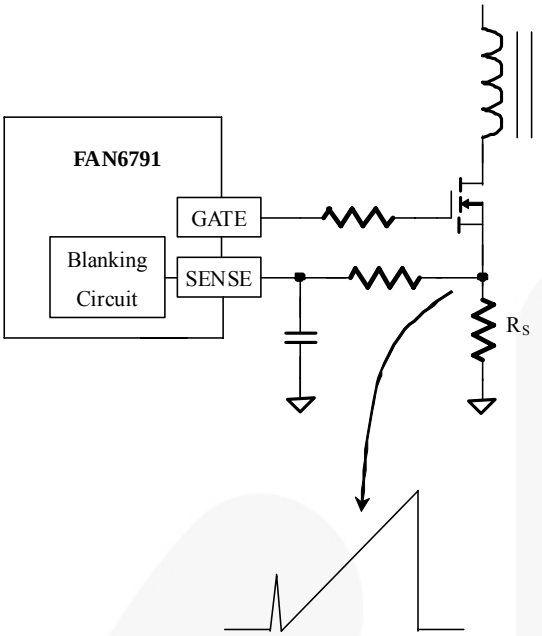

Figure 13.Turn-On Spike

Sense Pin Short-Circuit Protection

FAN6791 provides safety protection for power supply production. When a sense resistor is shorted by soldering in production, the pulse-by-pulse current limiting loses efficacy to provide an over-power protection of the unit. The unit may malfunction when the loading is larger than original maximum load. To protect against a short circuit across the current-sense resistor, the controller immediately shuts down if a continuously low voltage (around 0.15V) for 180µs on the SENSE pin is detected.

Output Driver / Soft Driving

The output stage is a fast totem-pole gate driver capable of directly driving an external MOSFET. An internal Zener diode clamps the driver voltage under 18V to protect the MOSFET against over-voltage. By integrating circuits to control the slew rate of switch-on rising time, the external resistor R_G may not be necessary to reduce switching noise, improving EMI performance.

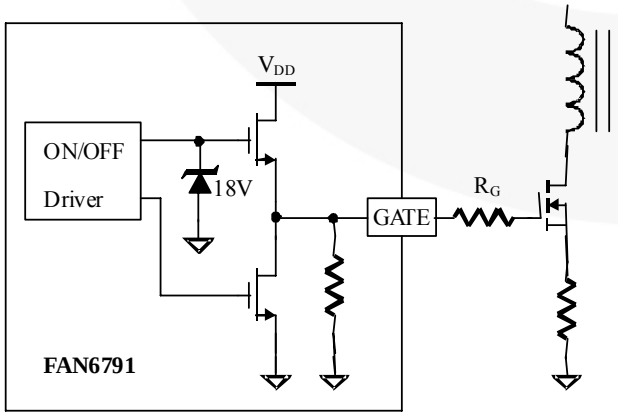

Figure 14. Gate Drive

Open-Loop Protection

FAN6791's OCP & SCP are based on the detection of feedback signal on FBPWM pin. As shown in Figure 15, when over current or short circuit occurs, FBPWM is pulled to a high voltage through the feedback loop. After a 95ms debounce time, FAN6791 is turned off. The 600ms time-out signal prevents FAN6791 from being latched off when the input voltage is fast on/off.

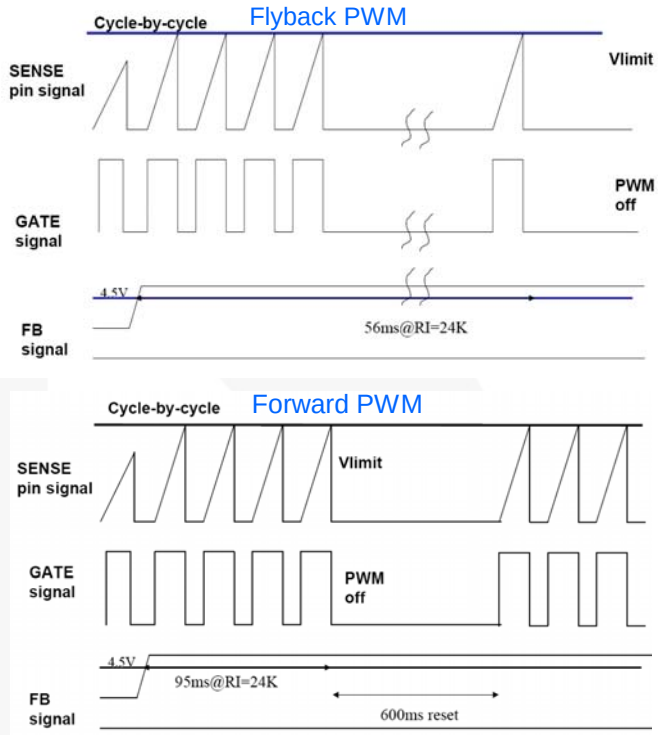

Figure 15.Timing for OCP & SCP

Forward Transformer

The topology used in this application note is dual switch forward, so the maximum duty cycle must be limited to less than 50%. To address transient load, efficiency, and hold-up time considerations, 30% duty cycle is chosen for determining the turn ratio of the transformer.

The secondary voltage of 12V, 5V should be:

$$V_{SEC(12V)} = \frac{V_{12}}{D} + V_{FD12} \quad \textbf{(8)}$$

$$V_{SEC(5V)} = \frac{V_5}{D} + V_{FD5} \quad \textbf{(9)}$$

Where, V_{FD12} and V_{FD5} are the forward voltage of rectifier diodes of 12V and 5V outputs. D is the duty cycle of the switching signal for steady-state operation. Assume V_{FD12} and V_{FD5} are 0.5V and D is 30% duty cycle, $V_{SEC\ (12V)}$ is 40.5V and $V_{SEC\ (5V)}$ is 17.17V.

The turn ratio is given as:

$$\frac{N_{PRI(VOUT)}}{N_{SEC(12V)}} = \frac{V_{OUT}}{V_{SEC(12V)}} \quad \textbf{(10)}$$

$$\frac{N_{PRI(VOUT)}}{N_{SEC(5V)}} = \frac{V_{OUT}}{V_{SEC(5V)}} \quad \textbf{(11)}$$

If V_{OUT} is 400V, the turn ratio is 69:7:3. The primary winding turns is calculated by Faraday's Law:

$$V_{OUT} \cdot \frac{N_{PRI(VOUT)} \times \Delta B_{MAX} \times Ae}{\Delta t} = \frac{N_{PRI(VOUT)} \times \Delta B_{MAX} \times Ae}{D / f} \quad \textbf{(12)}$$

$$N_{PRI(VOUT)} = \frac{400\text{V} \times 0.3 / 65\text{kHz}}{2500\text{G} \times 1.07\text{cm}^2} \times 10^8 = 69 \quad \textbf{(13)}$$

Choose ERL35 and the turn ratio is 69:7:3. If the topology is a single-switch forward, the maximum duty cycle can be designed around 40%~45% for the steady-state operation. The turns of the transformer can be calculated using the above equations.

Lab Note

Before modifying or soldering/de-soldering the power supply, discharge the primary capacitors through the external bleeding resistor. Otherwise, the PWM IC may be destroyed by external high voltage during the process.

This device is sensitive to electrostatic discharge (ESD). To improve the production yield, the production line should be ESD protected as required by ANSI ESD S1.1, ESD S1.4, ESD S7.1, ESD STM 12.1, and EOS/ESD S6.1 standards.

Printed Circuit Board Layout

High-frequency switching current/voltage makes PCB layout a very important design issue. Good PCB layout minimizes excessive EMI and helps the power supply survive during surge/ESD tests.

Guidelines

To improve EMI performance and reduce line frequency ripples, the output of the bridge rectifier should be connected to capacitor C_2 first, then to the switching circuits *(see Figure 16)*.

- The high-frequency current loop is in C_2 – Transformer – MOSFET – R_S – GND – C_2. The area enclosed by this current loop should be as small as possible. Keep the traces (especially **4→1**) short, direct, and wide. High-voltage traces related to the drain of the MOSFET and RCD snubber should be kept far way from control circuits to prevent unnecessary interference. If a heatsink is used for the MOSFET, connect this heatsink to ground.
- As indicated by **3**, the control-circuit ground should be connected first, then to other circuitry.
- As indicated by **2**, the area enclosed by the transformer auxiliary winding, D_1 and C_6 should also be kept small. Place C_6 close to the FAN6791 for good decoupling.

Two options with different pros and cons for ground connections are recommended:

- GND**3**→**2**→**1**→**4**: Potentially better for ESD testing where a ground is not available for the power supply. The ESD-discharge charges go from secondary through the transformer stray capacitance to the GND**2** first. Then charges go from GND**2** to GND**1** and back to the mains. Control circuits should not be placed on the discharge path. Point discharge for common choke can decrease high-frequency impedance and help increase ESD immunity.
- Should a Y-cap between primary and secondary be required, the Y-cap should be connected to the positive terminal of the C_2. If this Y-cap is connected to the primary GND, it should be connected to the negative terminal of the C_2 (GND1) directly. Point discharge of the Y-cap also helps with ESD. However, according to safety requirements, the creepage between the two pointed ends should be at least 5mm.

Isolating the interference between the dual-PWM stages is also important. The GND 5 provides the single-forward-signal ground. It should be connected directly to the decoupling capacitor C_6 and/or to the GND pin of the FAN6791. The ground in the output capacitor C_2 is the major ground reference for power switching, providing a good ground reference and reducing the switching noise of both the dual-PWM stages.

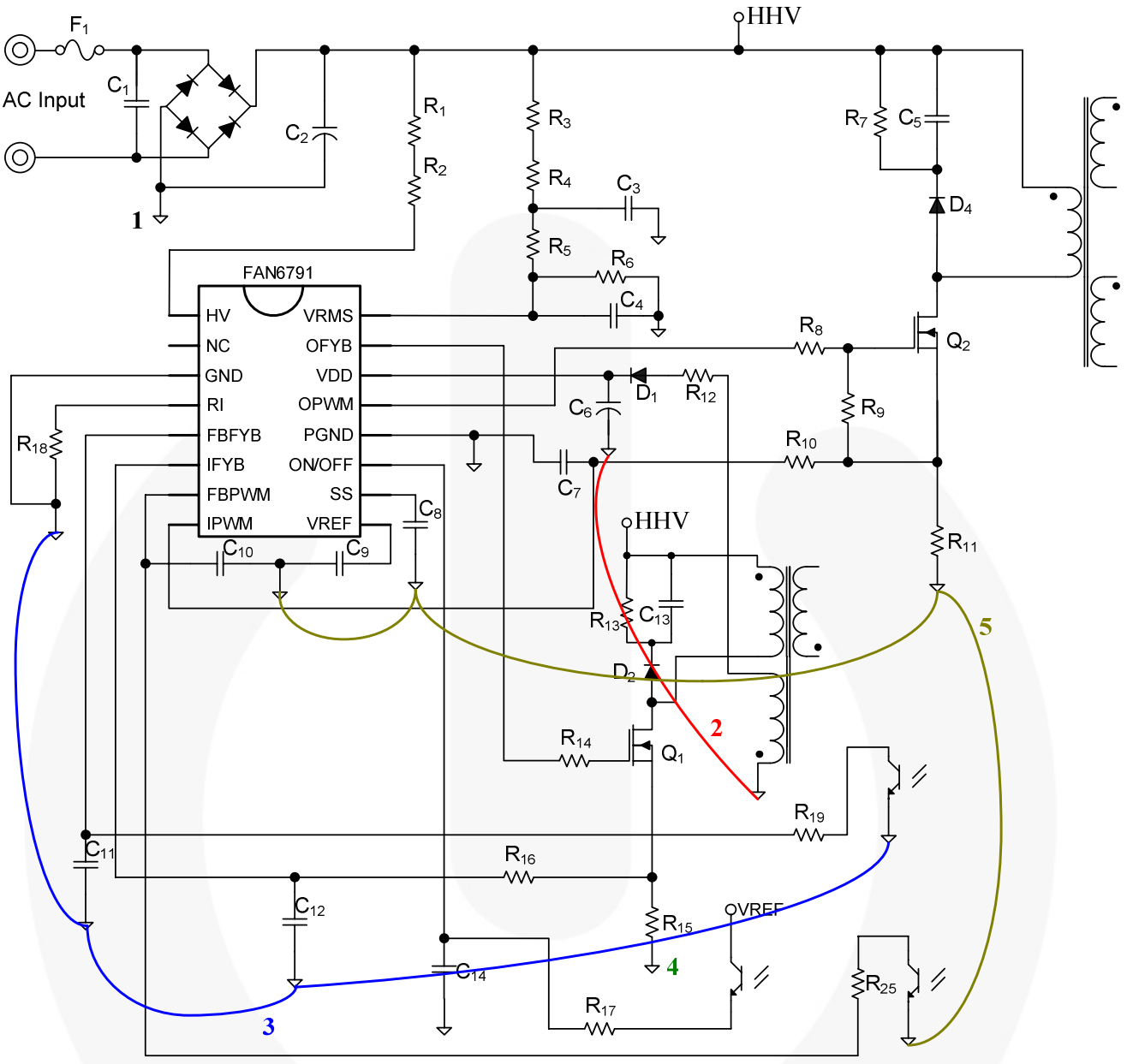

Figure 16. Layout Considerations

Reference

FAN6791 — Highly Integrated, Dual-PWM Combination Controller

AN-6741 — Flyback Power Supply Control with the SG6741

AN-6932 — Applying SG6932 to Control a PFC and Forward/PWM Power Supply