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TEA1713 resonant power supply control IC with PFC

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Document information

Info	Content
Keywords	TEA1713, PFC, burst mode, adapter, LCD TV, Plasma TV, resonant, converter.
Abstract	The TEA1713 integrates a controller for Power Factor Correction (PFC) and a controller for a half-bridge resonant converter (HBC). It provides the drive function for the discrete MOSFET for the up-converter and for the two discrete power MOSFETs in a resonant half-bridge configuration. The resonant controller part is a high voltage controller for a zero voltage switching LLC resonant converter. The resonant controller part of the IC includes a high voltage level shift circuit and several protection features such as overcurrent protection, open loop protection, capacitive mode protection and a general purpose latched protection input. In addition to the resonant controller, the TEA1713 also contains a Power Factor Correction (PFC) controller. The efficient operation of the PFC is obtained by functions such as quasi-resonant operation at high power levels and quasi-resonant operation with valley skipping at lower power levels. Overcurrent protection, overvoltage protection and demagnetization sensing, ensures safe operation in all conditions. The proprietary high voltage BCD Powerlogic process makes direct start-up possible from the rectified universal mains voltage in an efficient way. A second low voltage Silicon-On-Insulator (SOI) IC is used for accurate, high speed protection functions and control. The combination of PFC and a resonant controller in one IC makes the TEA1713 very suitable for power supplies in LCD TV, plasma televisions, PC power supplies, high power office equipment and adapters. This application note discusses the TEA1713 functions for applications.

Table 1. Revision history

Rev	Date	Description
01	20100322	First release

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1. Introduction

1.1 Scope and setup

This application note discusses the TEA1713 functions for applications in general. Because the TEA1713 provides extensive functionality, there are a large number of subjects discussed.

This document is setup in such a way, that a chapter or paragraph of a selected subject can be read as a standalone explanation with a minimum of cross-references to other document parts or the datasheet. This will lead to some repetition of information within the application note and to descriptions or figures that are similar to those published in the TEA1713 datasheet. In most cases typical values are given to enhance the readability.

Section 1 “Introduction” -

Section 2 “TEA1713 highlights and features”

Section 3 “Pin overview with functional description” - An overview of the TEA1713 pins with a summary of the functionality.

Section 4 “Application diagram”

Section 5 “Block diagram”

Section 6 “Supply functions” - In this and the following four sections, the main functions of the TEA1713 are discussed providing an in-depth explanation of the issues relating to the subject. The functions are written from an application point of view.

Section 7 “MOSFET drivers GATEPFC, GATELS and GATEHS” - Refer to the explanation for Section 6.

Section 8 “PFC functions” - Refer to the explanation for Section 6.

Section 9 “HBC functions” - Refer to the explanation for Section 6.

Section 10 “Burst mode operation” - Refer to the explanation for Section 6.

Section 11 “Protection functions” - An overview of the protection functions of the TEA1713 with an extended explanation and related issues on the subject. These functions are described and seen from an applications point of view.

Section 12 “Miscellaneous advice and tips” - A collection of subjects related to PCB design and debugging are discussed, including proposals for the way of working.

Section 13 “Application examples and topologies” - This section contains examples of applications (circuit diagrams) and possible topologies.

Please note that all values provided throughout this document are typical values unless otherwise stated.

1.2 Related documents

Additional information and tools can be found in other TEA1713 documents such as:

- Data sheet
- Calculation sheet
- User manual of demo board

2. TEA1713 highlights and features

2.1 Resonant conversion

Today's market demands high-quality, reliable, small, lightweight and efficient power supplies.

In principle, the higher the operating frequency, the smaller and lighter the transformers, filter inductors and capacitors can be. On the other hand, the core, switching and winding losses of the transformer will increase at higher frequencies and become dominant. This effect reduces the efficiency at a high frequency, which limits the minimum size of the transformer.

The corner frequency of the output filter usually determines the bandwidth of the control loop. A well-chosen corner frequency allows high operating frequencies to achieve a fast dynamic response.

Pulse Width Modulated (PWM) power converters, such as flyback, up and down converters, are widely used in low and medium power applications. A disadvantage of these converters is that the PWM rectangular voltage and current waveforms cause turn-on and turn-off losses that limit the operating frequency. The rectangular waveforms also generate broadband electromagnetic energy that can produce ElectroMagnetic Interference (EMI).

A resonant DC-DC converter produces sinusoidal waveforms and reduces the switching losses, which provides the possibility of operation at higher frequencies.

Recent environmental considerations have resulted in a need for high efficiency performance at low loads. Burst-mode operation of the resonant converter can provide this if the converter is required to remain active as is the case for adapter applications.

Why resonant conversion?

- High power.
- High efficiency.
- EMI friendly.
- Compact.

2.2 Power factor correction conversion

Most switch mode power supplies result in a non-linear impedance (load characteristic) to the mains input. Current taken from the mains supply occurs only at the highest voltage peaks and is stored in a large capacitor. The energy is taken from this capacitor storage, in accordance with the switch mode power supply operation characteristics.

Government regulations dictate special requirements for the load characteristics of certain applications. Two main requirements can be distinguished:

1. Mains harmonics requirements EN61000-3-2.
2. Power factor (real power/apparent power).

The requirements work towards a more resistive characteristic of the mains load.

To fulfill these requirements, measures need to be taken regarding the input circuit of the power supply. Passive (often a series coil) or active (often a boost converter) circuits can be used to modify the mains load characteristics accordingly.

An additional market requirement for the added mains input circuit is that it should work with a good efficiency and have a low cost.

Using a boost converter to meet these requirements provides the benefit of a fixed DC input voltage when combined with a resonant converter. The fixed input voltage provides easier design of the resonant converter (specially for wide mains input voltage range applications) and the possibility to reach a higher efficiency.

2.3 TEA1713 resonant power supply control IC with PFC

The TEA1713 integrates two controllers, one for Power Factor Correction (PFC) and one for a half-bridge resonant converter (HBC). It provides the drive function for the discrete MOSFET for the up-converter and for the two discrete power MOSFETs in a resonant half-bridge configuration.

The resonant controller part is a high voltage controller for a zero voltage switching LLC resonant converter.

The resonant controller part of the IC includes a high voltage level shift circuit and several protection features such as overcurrent protection, open-loop protection, capacitive mode protection and a general purpose latched protection input.

In addition to the resonant controller, the TEA1713 also contains a Power Factor Correction (PFC) controller. The efficient operation of the PFC is obtained by functions such as quasi-resonant operation at high power levels and quasi-resonant operation with valley skipping at lower power levels. Overcurrent protection, overvoltage protection and demagnetization sensing ensures safe operation in all conditions.

The proprietary high-voltage BCD Powerlogic process makes direct start-up possible from the rectified universal mains voltage in an efficient way. A second internal low-voltage SOI die is used for accurate, high-speed protection functions and control.

The topology of a PFC and a resonant converter controlled by the TEA1713 is very flexible and enables a broad range of applications for wide input (85 V to 264 V) AC mains voltages. The combination of PFC and resonant controller in one IC makes the TEA1713 very suitable for compact power supplies with a high level of integration and functionality.

2.4 Features

General features

- Integrated power factor controller and resonant controller.
- Universal mains supply operation.
- High level of integration, resulting in a low external component count and a cost effective design.
- Enable input. Also allows enabling of PFC only.
- On-chip high voltage start-up source.
- Standalone operation or IC supply from external DC supply.

Power factor controller features

- Boundary mode operation with on-time control for highest efficiency.
- Valley/zero voltage switching for minimum switching losses.
- Frequency limitation to reduce switching losses.
- Accurate boost voltage regulation.
- Burst mode switching with soft-start and soft-stop.

Resonant half-bridge controller features

- Integrated high-voltage level shifter.
- Adjustable minimum and maximum frequency.
- Maximum 500 kHz half-bridge switching frequency.
- Adaptive non-overlap timing.
- Burst mode switching.

Protection features

- Safe restart mode for system fault conditions.
- General latched protection input for output overvoltage protection or external temperature protection.
- Protection timer for time-out and restart.
- Over-temperature protection.
- Soft (re)start for both converters.
- Undervoltage protection for mains (brownout), boost, IC supply and output voltage.
- Overcurrent regulation and protection for both converters.
- Accurate overvoltage protection for boost voltage.
- Capacitive mode protection for resonant converter.

2.5 Protection

The TEA1713 provides several protection functions that combine detection with a response to solve the problem. By regulating the frequency as a reaction to, for example, over-power or bad half-bridge switching, the problem can be solved or operation kept safe until it is decided to stop and restart (timer function).

2.6 Typical areas of application

- LCD television.
- Plasma television.
- High power adapters.
- Slim notebook adapters.
- PC power supplies.
- Office equipment.

3. Pin overview with functional description

Table 2. Pinning overview

Pin	Name	Functional description
1	COMPPFC	Frequency compensation for the PFC control-loop. Externally connected filter with typical values: 150 nF (33 kΩ + 470 nF)
2	SNSMAINS	Sense input for mains voltage. Externally connected to resistive divided mains voltage. This pin has 4 functions: 1. Mains enable level: Vstart(SNSMAINS) = 1.15 V 2. Mains stop level (brownout): Vstop(SNSMAINS) = 0.9 V 3. Mains-voltage compensation for the PFC control-loop gain bandwidth 4. Fast latch reset: Vrst(SNSMAINS) = 0.75 V The mains enable and mains stop level will enable and disable the PFC. Enabling and disabling of the resonant controller is based on the voltage on SNSBOOST. The voltage on the SNSMAINS pin must be an averaged DC value, representing the AC line voltage. The pin should not be used for sensing the phase of the mains voltage. Open pin detection is included by an internal current source (33 nA).
3	SNSAUXPFC	Sense input from an auxiliary winding of the PFC coil for demagnetization timing and valley detection to control the PFC switching. It is −100 mV level with a time-out of 50 μs. The auxiliary winding needs to be connected via an impedance to the pin (recommended is a 5.1 kΩ series resistor) to prevent damage of the input during surges (e.g. lightning). Open pin detection is included by an internal current source (33 nA).
4	SNSCURPFC	Current sense input for PFC. This input is used to limit the maximum peak-current in the PFC core. The PFCSENSE is a cycle-by-cycle protection. The PFC MOSFET is switched off when the level reaches 0.5 V. Internally, there is a 60 μA current source connected to the pin, which is controlled by the internal logic. This current source is used to implement a soft-start and soft-stop function for the PFC to prevent audible noise in burst mode. The pin is also used to enable the PFC. The PFC will only start when the internal current source (60 μA) is able to charge the soft-start capacitor to a voltage of 0.5 V. A minimum soft-start resistor of 12 kΩ is required to guarantee enabling of the PFC. The value of the capacitor on SNSCURPFC provides the soft-start and soft-stop timing in combination with the parallel resistor value.
5	SNSOUT	Input for indirectly sensing the output voltage of the resonant converter. It is normally connected to an auxiliary winding of HBC and is also an input for the burst mode of HBC or PFC + HBC. This pin has 4 functions related to internal comparators: 1. Overvoltage protection: SNSOUT > 3.5 V, latched 2. Under voltage protection: SNSOUT < 2.3 V, protection timer 3. Hold HBC: SNSOUT < 1.0 V, stop switching HBC (burst mode) 4. Hold HBC + PFC: SNSOUT < 0.4 V, stop switching HBC and PFC (burst mode) The pin also contains an internal current source of 100 μA that, initially, will generate a voltage up to 1.5 V across an external impedance (> 20 kΩ recommended) to avoid unintended burst mode operation.

Table 2. Pinning overview *…continued*

Pin	Name	Functional description
6	SUPIC	IC voltage supply input and output of the internal HV start-up source. All internal circuits are directly or indirectly (via SUPREG) supplied from this pin, with the exception of the high-voltage circuit. The buffer capacitor on SUPIC can be charged in several ways: 1. Internal high-voltage (HV) start-up source 2. Auxiliary winding from HBC transformer or capacitive supply from switching half-bridge node 3. External DC supply, for example a standby supply The IC will enable operation when the SUPIC voltage has reached the start level of 22 V (for HVstart) or 17 V (for external supply). It will stop operation below 15 V and a shutdown reset will be activated at 7 V.
7	GATEPFC	Gate driver output for PFC MOSFET.
8	PGND	Power ground. Reference (ground) for HBC low-side and PFC driver.
9	SUPREG	Output of the internal regulator: 10.9 V. The supply made by this function is used by internal IC functions such as the MOSFET drivers. It can also be used to supply an external circuit. SUPREG can provide a minimum of 40 mA. SUPREG will become operational after SUPIC has reached its start level. The IC will start full operation when SUPREG has reached 10.7 V. UVP: If SUPREG drops below 10.3 V after start, the IC will stop operating and the current from SUPIC will be limited to 5.4 mA, to allow recovery.
10	GATELS	Gate driver output for low side MOSFET of HBC.
11	n.c.	Not connected, high-voltage spacer.
12	SUPHV	High-voltage supply input for internal HV start-up source. In a standalone power supply application, this pin is connected to the boost voltage. SUPIC and SUPREG will be charged with a constant current by the internal start-up source. SUPHV will operate at a voltage above 25 V. Initially the charging current is low (1.1 mA). When the SUPIC exceeds the short-circuit protection level of 0.65 V, the generated current increases to 5.1 mA. The source is switched off when SUPIC reaches 22 V which initiates a start operation. During start operation, an auxiliary supply will take over the supply of SUPIC. If the takeover is not successful, the SUPHV source will be reactivated and a restart is made (SUPIC below 15 V).
13	GATEHS	Gate driver output for high-side MOSFET of HBC.
14	SUPHS	High-side driver supply connected to an external bootstrap capacitor between HB and SUPHS. The supply is obtained using an external diode between SUPREG and SUPHS.
15	HB	Reference for the high-side driver GATEHS. It is an input for the internal half-bridge slope detection circuit for adaptive non-overlap regulation and capacitive mode protection and is externally connected to a half-bridge node between the MOSFETs of HBC.
16	n.c.	Not connected, high-voltage spacer.

Table 2. Pinning overview *…continued*

Pin	Name	Functional description
17	SNSCURHBC	Sense input for the momentary current of the HBC. In case of too high voltage level (that represents the primary current), internal comparators determine to regulate to a higher frequency (SNSCURHBC = ±0.5 V) or protect (SNSCURHBC = ±1 V) by switching immediately to maximum frequency. Variations on protection level, caused by HBC input voltage variations, can be compensated by the provided additional current from SNSCURHBC. This current leads to a voltage offset across the external series resistance value. This series resistance is normally provided by the current measurement resistor and an extra series resistance which has a typical value of 1 kΩ.
18	SGND	Signal ground, reference for IC.
19	CFMIN	Oscillator pin. The value of the external capacitor determines the minimum switching frequency of the HBC. In combination with the resistor value on RFMAX, it sets the operating frequency range. To facilitate switching timing, a triangular waveform is generated on the CFMIN capacitor Vlow(CFMIN) = 1 V and Vhigh(CFMIN) = 3 V). The minimum frequency is determined by a fixed minimum (dis)charging current of 150 μA. During special conditions, the (dis)charging current is reduced to 30 μA to temporarily slow down the charging. An internal function limits the operating frequency to 670 kHz.
20	RFMAX	Oscillator frequency pin. The value of the resistor connected between this pin and ground, determines the frequency range. Both the minimum and maximum frequencies of the HBC are preset. The minimum frequency is set by CFMIN and the absolute maximum frequency is internally limited to 670 kHz. The voltage on RFMAX and the value of the resistor connected to it, determine the variable part (in addition to the fixed 150 μA) of the (dis)charging current of the CFMIN-capacitor. The voltage on RFMAX can vary between 0 V (minimum frequency) and 2.5 V (maximum frequency). The RFMAX voltage (running frequency) is driven by SNSFB- and SSHBC/EN- function. The protection timer is started when the voltage level is above 1.88 V. An error is assumed when the HBC is operating at high frequency for a longer time.
21	SNSFB	Sense input for HBC output regulation feedback by voltage. Sinking a current from SNSFB creates the feedback voltage on SNSFB. The regulation voltage is produced by feeding this current through a 1.5 kΩ internal resistor which is internally connected to 8.4 V. The regulation voltage range is from 4.1 V to 6.4 V and it corresponds with the maximum and minimum frequencies that are controlled by SNSFB. The SNSFB range is limited to 65% of the maximum frequency preset by RFMAX. The provision of open loop detection activates the protection timer when SNSFB is (remains) above 7.7 V.

Table 2. Pinning overview *…continued*

Pin	Name	Functional description
22	SSHBC/EN	Combined soft-start/protection frequency control of HBC and IC enable input (PFC or PFC + HBC). Externally connected to a soft-start capacitor and an enable pull-down function. This pin has 3 functions: 1. Enable PFC (>1 V) and PFC + HBC (> 2 V) 2. Frequency sweep during soft-start from 3.2 V to 8 V 3. Frequency control during protection between 8 V to 3.2 V Seven internal current sources operate the frequency control, depending on which of the following actions is required: 1. Soft-start + OverCurrent Protection: high/low charge (160 μA/40 μA) + high/low discharge (160 μA/40 μA) 2. Capacitive mode regulation: high/low discharge (1800 μA/440 μA) 3. General: bias discharge (5 μA)
23	RCPROT	Timer presetting for time-out and restart.The timing is determined by the values of an externally connected resistor and capacitor. Protection timer During certain protection, the timer is activated by a 100 μA charge current: 1. Overcurrent regulation (SNSCURHBC) 2. High frequency protection (RFMAX) 3. Open loop protection (SNSFB) 4. Undervoltage protection (SNSOUT) When the level of 4 V is reached the protection is activated. The resistor discharges the capacitor and at a level of 0.5 V, a restart is made. Restart timer In the case of SCP (SNSBOOST), the RCPROT capacitor is quickly charged by 2.2 mA. After it reaches the 4 V level, the capacitor will be discharged after which a new start is initiated.
24	SNSBOOST	Sense input for boost voltage regulation (output voltage of the PFC stage). It is externally connected to a resistive divided boost voltage. This pin has 4 functions: 1. Pin SNSBOOST short detection: VSCP(SNSBOOST) ≤ 0.4 V 2. Regulation of PFC output voltage: Vreg(SNSBOOST) = 2.5 V 3. PFC soft OVP (cycle-by-cycle): VOVP(SNSBOOST) ≥ 2.63 V 4. Brownout function for HBC: converter enable voltage: Vstart(SNSBOOST) = 2.3 V and converter disable voltage: VUVP(SNSBOOST) = 1.6 V

4. Application diagram

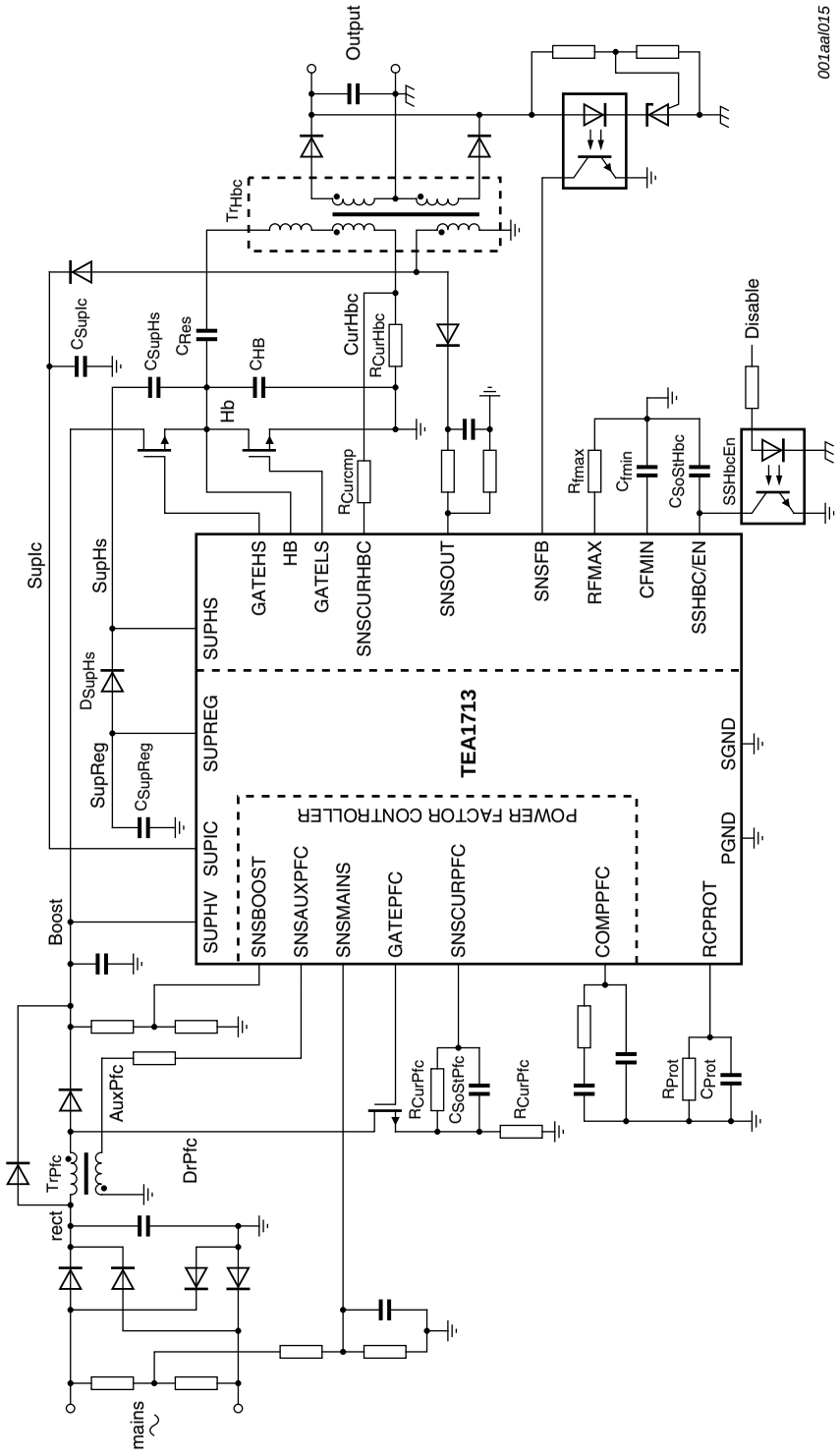

Fig 1. Basic application diagram TEA1713

5. Block diagram

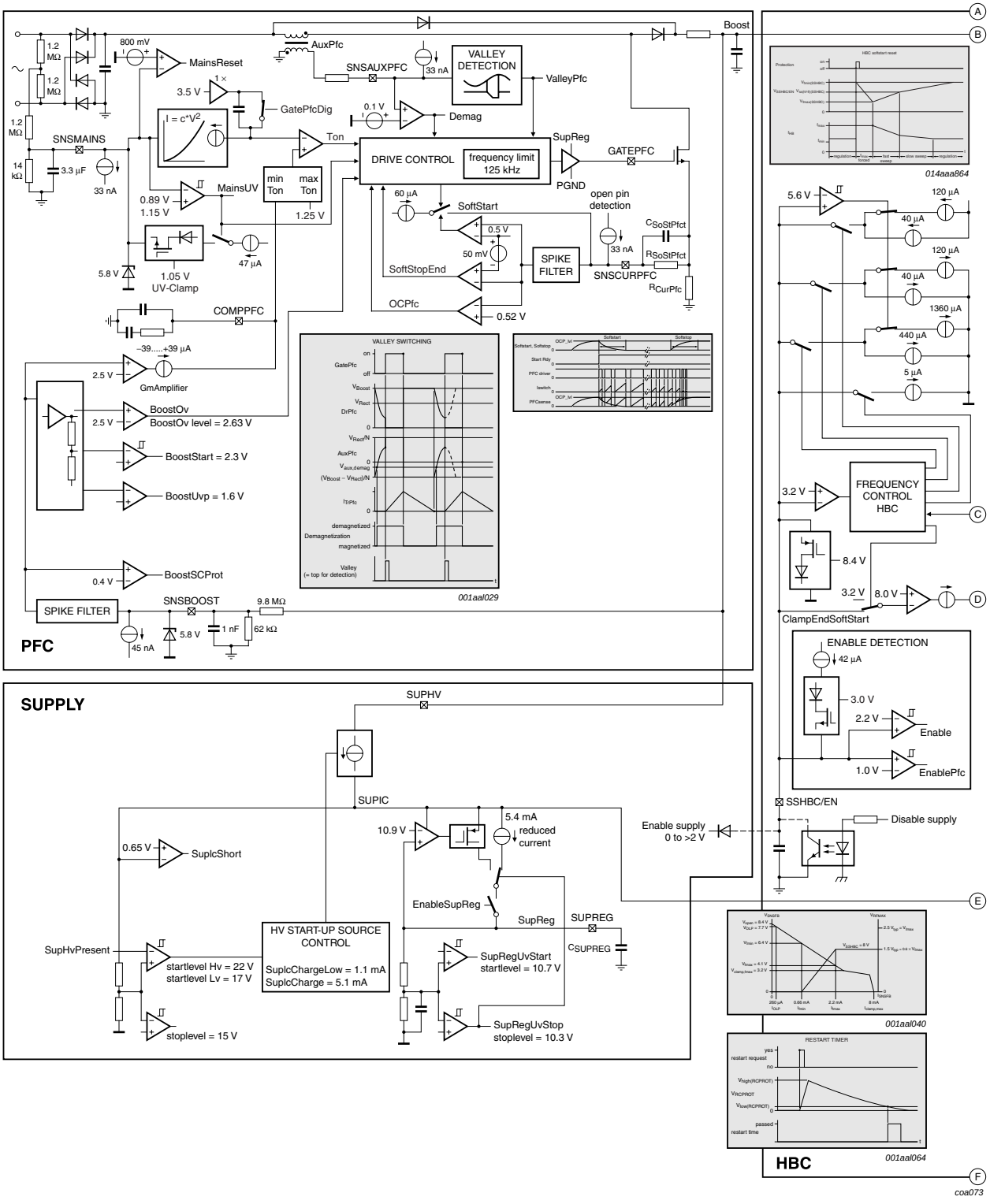

Fig 2. Block diagram TEA1713

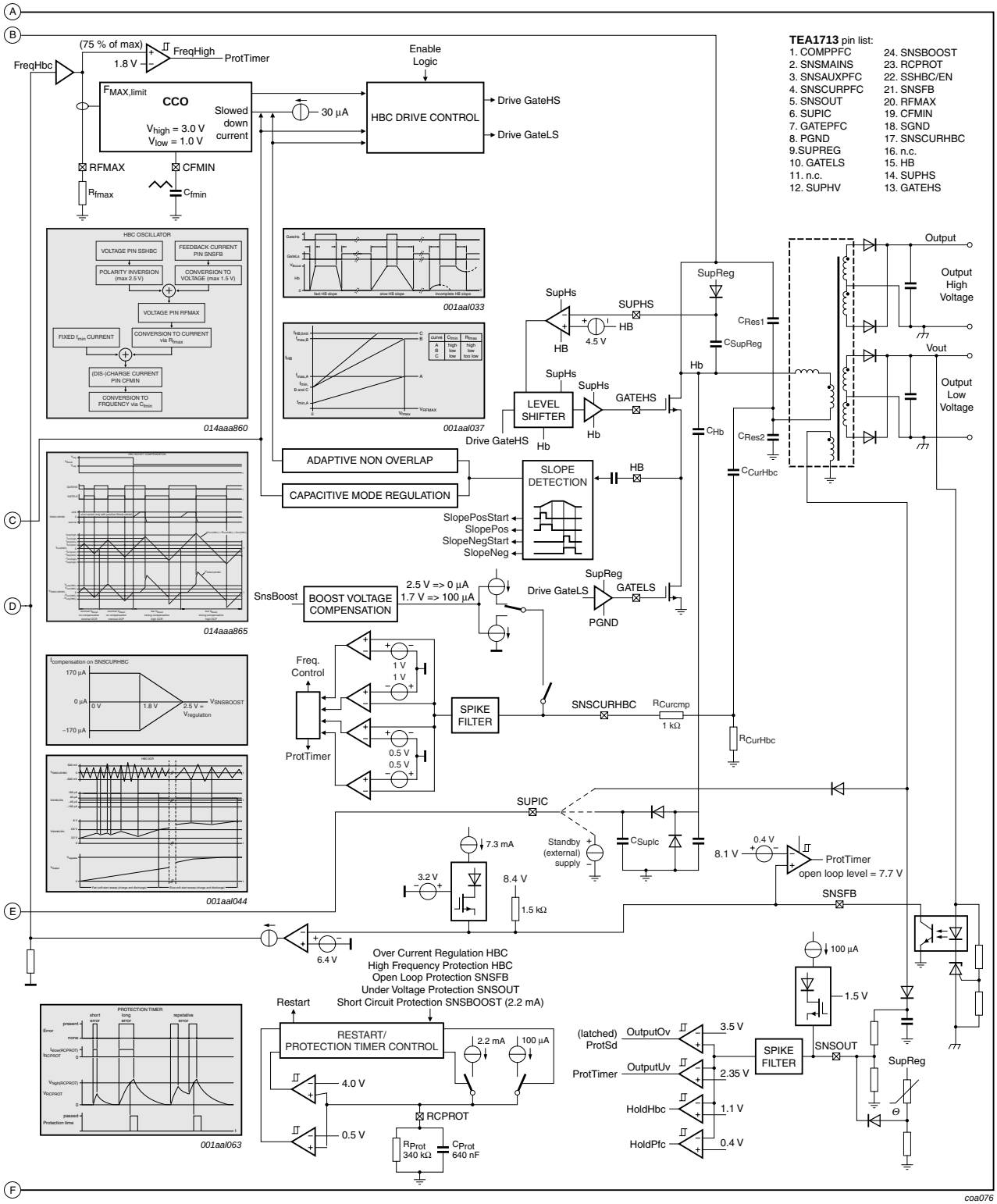

Fig 3. Block diagram TEA1713

6. Supply functions

6.1 Basic supply system overview

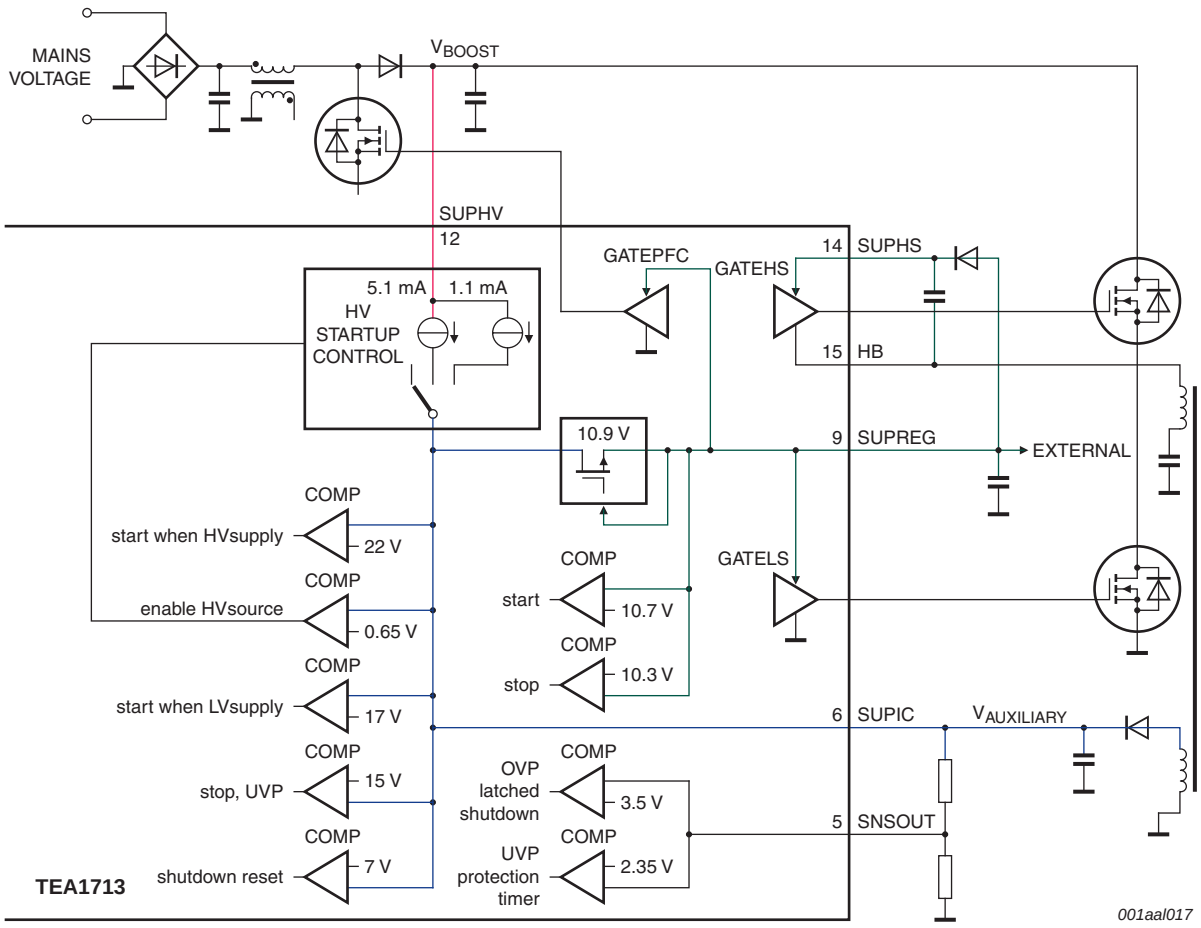

Fig 4. Basic overview internal IC supplies

6.1.1 TEA1713 supplies

The main supply for the TEA1713 is SUPIC.

SUPHV can be used to charge SUPIC for starting the supply. During operation a supply voltage is applied to SUPIC and the SUPHV source is switched off. The SUPHV source is only switched on again at a new start-up.

The internal regulator SUPREG will generate a fixed voltage of 10.9 V to supply the internal MOSFET drivers: GATEPFC, GATELS and GATEHS. To supply GATEHS a bootstrap function with an external diode is used to make supply SUPHS.

SUPIC and SUPREG also supply other internal TEA1713 circuits.

6.1.2 Supply monitoring and protection

The supply voltages are internally monitored to determine when to initiate certain actions: starting, stopping or protection.

In several applications (e.g. when using an auxiliary winding construction) the SUPIC voltage can also be used to monitor the HBC output voltage by protection input SNSOUT.

6.2 SUPIC - the low voltage IC supply

SUPIC is the main IC supply. With the exception of the SUPHV circuit, all internal circuits are either directly or indirectly supplied from this pin.

6.2.1 SUPIC start-up

SUPIC needs to be connected to an external buffer capacitor. This buffer capacitor can be charged in several ways:

1. Internal high-voltage (HV) start-up source
2. Auxiliary supply, e.g. from a winding on the HBC transformer
3. External DC supply, e.g. from a standby supply

The IC will start operating when the SUPIC and SUPREG voltage have reached the start level. The start level value of SUPIC depends on the condition of the SUPHV pin.

SUPHV $\geq$ 25 Vmax

This is the case in a standalone application where SUPIC is initially charged by the HV start-up source. The SUPIC start level will be 22 V. The large difference between start level and stop level (15 V) is used to allow discharge of the SUPIC capacitor until the auxiliary supply can take over the IC supply.

SUPHV not connected/used

This is the case when the TEA1713 is supplied from an external DC supply. The SUPIC start level is now 17 V. During start-up and operation the IC is continuously supplied by the external DC supply. For this kind of application the SUPHV pin should not be connected.

6.2.2 SUPIC stop, UVP and short circuit protection

The IC will stop operating when the SUPIC voltage drops below 15 V which is the UnderVoltage Protection (UVP) of SUPIC. While in the process of stopping, the HBC will continue until the low-side MOSFET is active, before stopping the PFC and HBC operation.

SUPIC has a low level detection at 0.65 V to detect a short circuit to ground. This level also controls the current source from the SUPHV pin.

6.2.3 SUPIC current consumption

The SUPIC current consumption depends on the state of the TEA1713.

1. **Disabled IC state:** When the IC is disabled via the SSHBC/EN pin, the current consumption is low at 250 μA.
2. **SUPIC charge, SUPREG charge, thermal hold, restart and shutdown state:** During the charging of SUPIC and SUPREG before start-up, during a restart sequence or during shutdown after activation of protection, only a small part of the IC is active. The PFC and HBC are disabled. The current consumption from SUPIC in these states is small at 400 μA.
3. **Boost charge state:** PFC is switching and HBC is still off. The current from the high voltage start-up source is large enough to supply SUPIC, so current consumption is below the maximum current (5.1 mA) that SUPHV can deliver.
4. **Operating supply state:** Both PFC and HBC are switching. The current consumption is larger. The MOSFET drivers are dominant in the current consumption (see Section 6.5.5), especially during soft-start of the HBC, when the switching frequency is high, and also during normal operation. Initially the SUPIC current will be delivered by the stored energy in the SUPIC capacitor that after a short time is taken over by the supply source on SUPIC during normal operation.

6.3 SUPIC supply using HBC transformer auxiliary winding

6.3.1 Start-up by SUPHV

In a standalone power supply application, the IC can be started by a high voltage source such as the rectified mains voltage. For this purpose the high voltage input SUPHV can be connected to the boost voltage (PFC output voltage).

The SUPIC and SUPREG will be charged by the internal HV start-up source which delivers a constant current from SUPHV to SUPIC. SUPHV will be operational at a voltage > 25 V.

As long as the voltage at SUPIC is below the short circuit protection level (0.65 V), the current from SUPHV is low (1.1 mA). This is to limit the dissipation in the HV start-up source when SUPIC is shorted to ground.

During normal conditions, SUPIC will quickly exceed the protection level and the HV start-up source will switch to normal current (5.1 mA). The HV start-up source switches off when SUPIC has reached the start level (22 V). The current consumption from SUPHV will be low (7 μA) when switched off.

When SUPIC has reached the start level (22 V), SUPREG will be charged. When SUPREG reaches the level of 10.7 V, it enables operation of HBC and PFC.

The auxiliary winding supply of the HBC transformer must take over the supply of SUPIC before it is discharged to the SUPIC under voltage stop level (15 V).

6.3.2 Block diagram for SUPIC start-up

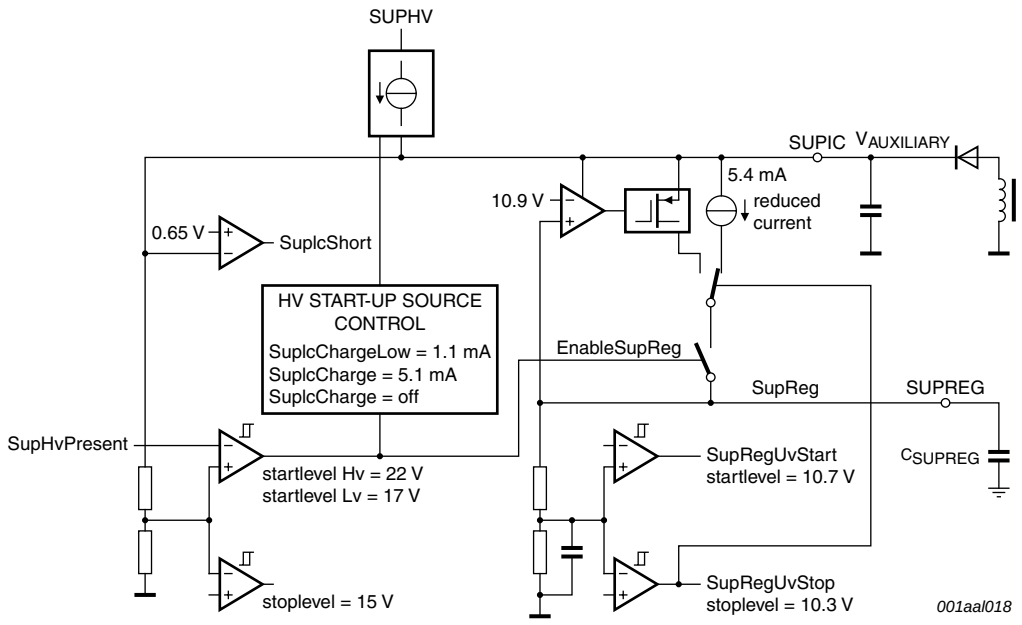

Fig 5. Block diagram: SUPIC and SUPREG start-up with SUPHV and auxiliary supply

6.3.3 Auxiliary winding on the HBC transformer

An auxiliary winding on the HBC transformer can be used to obtain a supply voltage for SUPIC during operation. As SUPIC has a wide operational voltage range (15 V to 38 V), this is not a critical parameter.

But:

- For low power consumption, the voltage on SUPIC should be low.
- To use the voltage from the auxiliary winding for IC supply **and** HBC output voltage measurement (by SNSOUT), the auxiliary supply must be made accurately representing the output voltage. To ensure good coupling, this winding needs to be placed on the secondary (output) side.
- When mains insulation is included in the HBC transformer, it can impact the construction of the auxiliary winding. Triple insulated wire is needed when the auxiliary winding is placed on the mains-insulated area of the transformer construction.

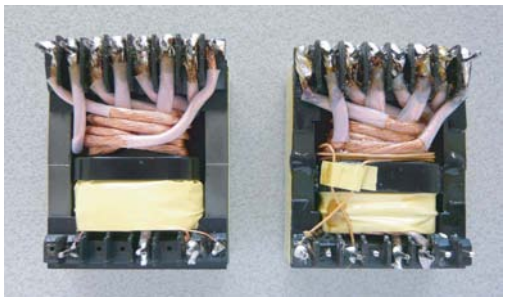

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Fig 6. Auxiliary winding on primary side (left) and secondary side (right)

6.3.3.1 SUPIC and SNSOUT by auxiliary winding

The SNSOUT input provides a combination of 4 functions:

1. Overvoltage protection: SNSOUT > 3.5 V, latched
2. Under voltage protection: SNSOUT < 2.35 V, protection timer
3. Hold HBC: SNSOUT < 1.1 V, stop switching HBC (for burst mode)
4. Hold HBC + PFC: SNSOUT < 0.4 V, stop switching HBC and PFC (for burst mode)

Remark: A more detailed explanation of the SNSOUT functions can be found in Section 11.3.1 “OverVoltage Protection (OVP) output” and (Section 11.3.2 “Under Voltage Protection (UVP) output”)

Often, a circuit is used which combines SUPIC and the output voltage monitoring by SNSOUT, with one auxiliary winding on the HBC transformer. But an independent construction for SUPIC and SNSOUT is also possible. This could be in a situation where SUPIC is supplied by a separate standby supply and an auxiliary winding is only used for output voltage sensing. It is also possible not to use SNSOUT for output sensing but as a general purpose protection input. For more details, refer to Section 11.3.3 “OVP and UVP combinations”.

In case of a combined function of SUPIC and SNSOUT by an auxiliary winding on the HBC transformer, some issues need to be addressed to obtain a good representation of the output voltage for SNSOUT measurement.

The advantage of a good coupling/representation of the auxiliary winding with the output windings is also that a stable auxiliary voltage is obtained for SUPIC. A low SUPIC voltage value can be designed more easily for lowest power consumption.

6.3.3.2 Auxiliary supply voltage variations by output current

At high (peak) current loads, the voltage drop across the series components of the HBC output stage (resistance and diodes) is compensated by regulation. This results in a higher voltage on the windings at higher output currents due to the higher currents causing a larger voltage drop across the series components. An auxiliary winding supply will show this variation caused by the HBC output.

6.3.3.3 Voltage variations by auxiliary winding position: primary side component

Due to a less optimal position of the auxiliary winding, the voltage for SNSOUT and/or SUPIC can contain a certain amount of undesired primary voltage component. This can seriously endanger the feasibility of the SNSOUT sensing function.

To avoid a primary voltage component on the auxiliary voltage, the coupling of the auxiliary winding with the primary winding should be as small as possible. To obtain this, the auxiliary winding should be placed on the secondary winding(s) and as physically remote as possible from the primary winding. See differences in results given by comparison on secondary side position in Figure 7.

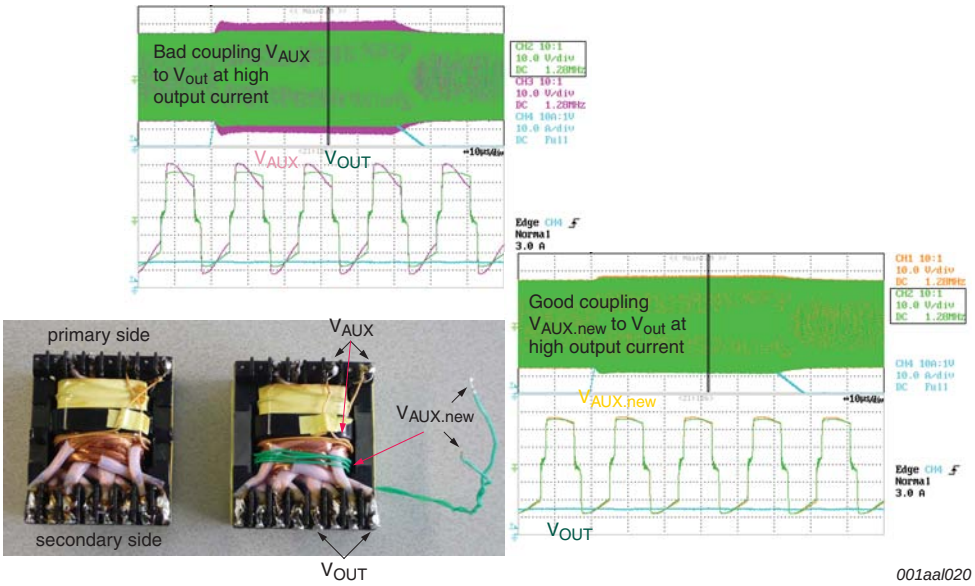


Fig 7. Position the auxiliary winding for good output coupling

6.3.4 Difference between UVP on SNSOUT and SNSCURHBC OCP/OCR

In a system that uses output voltage sensing by means of the SNSOUT function, there can be an overlap in functionality in an over power or short-circuit situation. In such a situation, often both the SNSOUT UVP and the OCP/OCR on SNSCURHBC, will activate the protection timer.

There are basic differences between both functions:

- OCP/OCR monitors the **power** in the system by sensing the primary current in detail
- SNSOUT monitors (indirectly) the HBC output **voltage** or another external protection circuit (such as NTC temperature measurement)

SNSOUT is a more general usable protection input while SNSCURHBC is specifically designed for HBC operation.

In addition, SNSOUT also offers three other functions: OVP (latched), hold HBC and hold HBC + PFC (for burst mode).

6.4 SUPIC supply by external voltage

6.4.1 Start-up

When the TEA1713 is supplied by an external DC supply, the SUPHV pin can remain unconnected. The SUPIC start level is now 17 V.

When the SUPIC exceeds 17 V the internal regulator will be activated and charge SUPREG.

At SUPREG ≥ 10.7 V, GATELS is switched on for the bootstrap function to charge SUPHS. And at the same time the PFC operation is internally enabled. When all enable conditions are met, the TEA1713 will start the PFC function and as soon as V_{boost} reaches approximately 90 % (SNSBOOST ≥ 2.3 V) of its nominal value, the HBC will be started.

6.4.2 Stop

Operation of the TEA1713 can be stopped by switching off the external source for SUPIC. As soon as the voltage level on SUPIC drops below 15 V, operation is stopped.

In case of shutdown (because of protection), this state is reset by internal logic as soon as the SUPIC voltage drops below 7 V.

6.5 SUPREG

SUPIC has a wide voltage range for easy application. Because of this, SUPIC cannot be directly used to supply the internal MOSFET drivers as this would exceed the allowed gate voltage of many external MOSFETs.

To avoid this issue (and create a few other benefits), the TEA1713 contains an integrated series stabilizer. The series stabilizer generates an accurate regulated voltage on SUPREG on the external buffer capacitor.

This stabilized SUPREG voltage is used for:

- Supply of internal PFC driver.
- Supply of internal low-side HBC driver.
- Supply of internal high-side driver via external components.
- Reference voltage for optional external circuits.

The series stabilizer for SUPREG is enabled after SUPIC has been charged. In this way optional external circuitry at SUPREG will not consume from the start-up current during the charging of SUPIC. The capacitor on SUPIC acts as a buffer at charge of SUPREG and start-up of the IC.

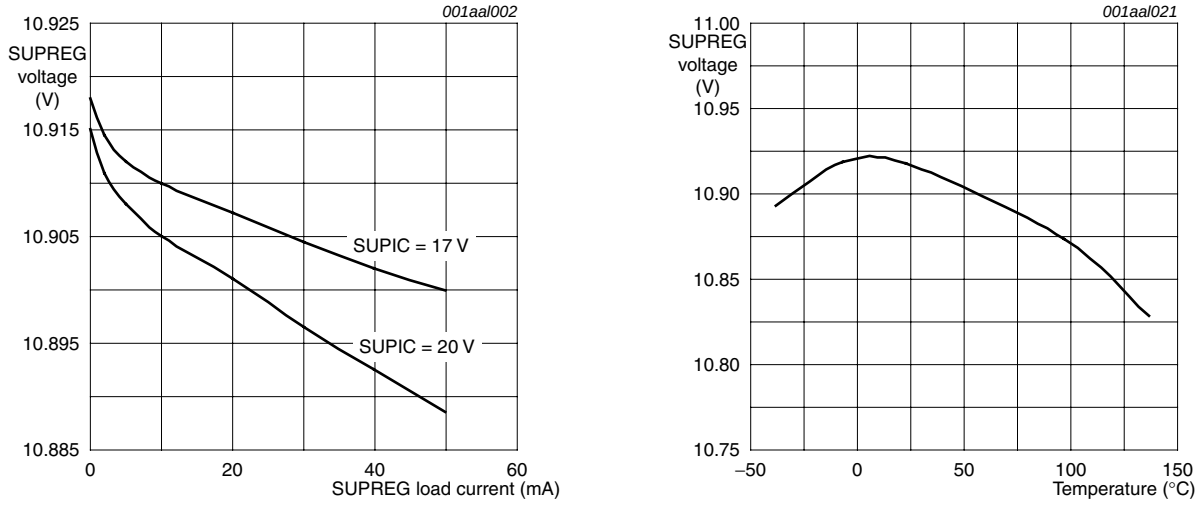
To ensure that the external MOSFETs receive sufficient gate drive, the SUPREG voltage must first reach the Vstart(SUPREG) level before the IC will start operating, provided that the SUPIC voltage has also reached the start level.

The SUPREG has an UnderVoltage Protection. When the SUPREG voltage drops below the 10.3 V two actions take place:

1. The IC will stop operating to prevent unreliable switching due to too low gate driver voltage. The PFC controller will stop switching immediately, but the HBC will continue until the low-side stroke is active.
2. The maximum current from the internal SUPREG series stabilizer is reduced to 5.4 mA. In case of an overload at SUPREG in combination with an external DC supply for SUPIC, this action will reduce the dissipation in the series stabilizer.

It is important to realize that in principle, SUPREG can only source current.

The drivers of GATELS and GATEPFC are supplied by this voltage and draw current from it during operation depending on the operating condition. Some change in value can be expected due to current load and temperature:



Voltage characteristics for load

Voltage characteristics for temperature

Fig 8. Typical SUPREG voltage characteristics for load and temperature

6.5.1 Block diagram of SUPREG regulator

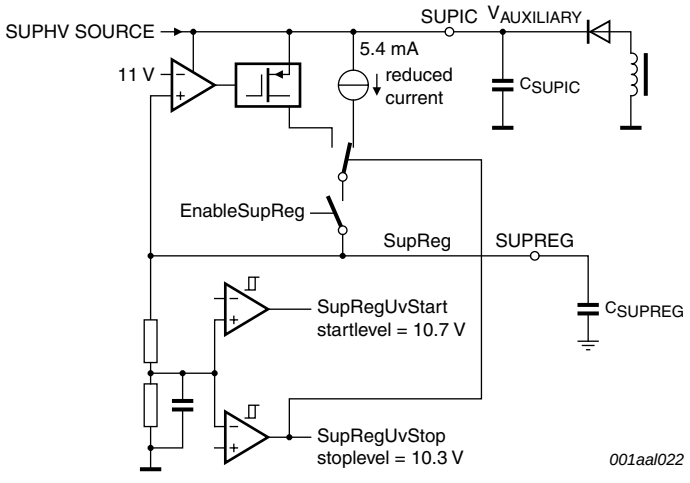


Fig 9. Block diagram of internal SUPREG regulator

6.5.2 SUPREG during start-up

SUPREG is supplied by SUPIC. SUPIC is the unregulated external power source that provides the input voltage for the internal voltage regulator that provides SUPREG.

At start-up SUPIC needs to reach a specific voltage level before SUPREG is activated:

1. Using the internal HV supply, SUPREG is activated when SUPIC ≥ 22 V.
2. Using an external low voltage supply, SUPREG is activated when SUPIC ≥ 17 V.

6.5.3 Supply voltage for the output drivers: SUPREG

The TEA1713 has a powerful output stage for GATEPFC and GATELS to drive large MOSFETs. These internal drivers are supplied by SUPREG that provides a fixed voltage.

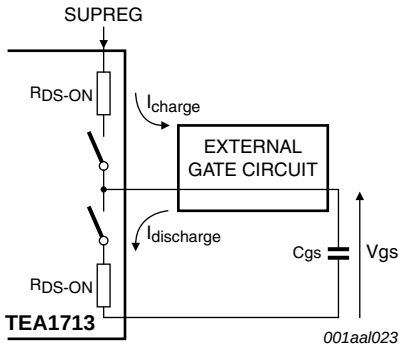


Fig 10. Simplified model of MOSFET drive

It can be seen from Figure 10 that current is taken from SUPREG when the external MOSFET is switched on by charging the gate to a high voltage.

The shape of the current from SUPREG at switch on is related to:

- the supply voltage for the internal driver (10.9 V).
- the characteristic of the internal driver.
- the gate capacitance to be charged.
- the gate threshold voltage for the MOSFET to switch on.
- the external circuit to the gate.

Be aware that the switching moments of GATEPFC and GATELS are independent in time. The charging of SUPHS for GATEHS is synchronized in time with GATELS but has a different shape because of the bootstrap function.

6.5.4 Supply voltage for the output drivers: SUPHS

The high-side driver is supplied by an external bootstrap buffer capacitor. The bootstrap capacitor is connected between the high-side reference pin HB and the high-side driver supply input pin SUPHS. This capacitor is charged by an external diode from SUPREG during the time that HB is low. By selecting a suitable external diode, the voltage drop between SUPREG and SUPHS can be minimized. This is especially important when using a MOSFET that needs a large amount of gate charge and/or when switching at high frequencies.

Instead of using SUPREG as the power source for charging SUPHS, another supply source can be used. In such a construction it is important to check for correct start/stop sequences and to prevent the voltage exceeding the maximum value of HB +14 V.

Be aware that the current taken from SUPREG to charge SUPHS differs, (in time and shape) from the current taken by drivers GATEPFC and GATELS, for each cycle.

6.5.4.1 Initial charging of SUPHS

At start-up, SUPHS is charged by the bootstrap function by setting GATELS high to switch on the low side MOSFET. While SUPHS is being charged, GATELS is switched on for charging and the PFC operation is started. The time between start charging and start HBC operation is normally sufficient to charge SUPHS completely. Start HBC operation is when SNSBOOST reaches 2.3 V which is approximately 90 % of nominal V_{boost}.

6.5.4.2 Current load on SUPHS

The current taken from SUPHS consists of two parts:

1. Internal MOSFET driver GATEHS.
2. Internal circuit to control GATEHS (37 μA, quiescent current).

It can be seen from Figure 11 that the current taken by the driver GATEHS occurs at switch on. The shape of the current from SUPHS at switch on is related to:

- the value of the supply voltage for the internal driver.
- the characteristic of the internal driver.
- the gate capacitance to be charged.
- the gate threshold voltage for the MOSFET to switch on.
- the external circuit to the gate.

The voltage value of SUPHS can vary.

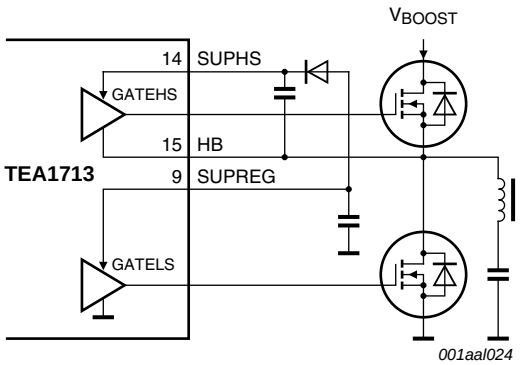


Fig 11. Typical application of SUPHS

6.5.4.3 Lower voltage on SUPHS

During normal operation, each time the half-bridge node (HB) is switched to ground level, the SUPHS capacitor is charged by the bootstrap function. Because of the voltage drop across the bootstrap diode, the value of SUPHS will normally be lower than SUPREG (or other bootstrap supply input).

The voltage drop across the bootstrap diode is directly related to the amount of current that is needed to charge SUPHS. The resultant SUPHS voltage also has a relation to the time available for charging.

A large voltage drop will occur when an external MOSFET with a large gate capacitance has to be switched at high frequency (high current + short time).

Also, during burst mode operation, a low voltage on SUPHS can occur. In burst mode there will be (long) periods of not switching, and therefore no charging of SUPHS. During this time the circuit supplied by SUPHS will slowly discharge the supply voltage capacitor. At the moment a new burst starts, the SUPHS voltage will be lower than during normal operation. During the first switching cycles SUPHS will be recharged to its normal level. During burst mode, at low output power, the switching frequency is normally rather high which limits a fast recovery of the SUPHS voltage.

Although in most applications the voltage drop will be limited, it is an important issue to be evaluated. It can influence the selection of the best diode type for the bootstrap function and the value of the buffer capacitor on SUPHS.

6.5.5 SUPREG power consumed by MOSFET drivers

During operation the drivers GATEPFC, GATELS and GATEHS charging the gate capacitances of the external MOSFETs are a major part of the power consumption from SUPREG. The amount of energy needed for this in time is linear to the switching frequency. Often, for the MOSFETs used, the total charge is specified for certain conditions. With this figure an estimation can be made for the amount of current needed from SUPREG.

GATELS and GATEHS (driving a total of 2 MOSFETs):

$\Delta I_{SUPIC} = 2 \times Q_{gate} \times f_{bridge}$

For example, a MOSFET with Q_{gate} = 40 nC at a bridge frequency 100 kHz:

$\Delta I_{SUPIC} = 2 \times 40\ nC \times 100\ kHz = 8\ mA$

Note: The calculated value is generally higher than the practical value, because the switching operation deviates from the MOSFET specification for Q_{gate}.

GATEPFC:

$\Delta I_{SUPIC} = Q_{gate} \times f_{pfc}$

For example a MOSFET with Q_{gate} = 40 nC at a PFC frequency of 100 kHz:

$\Delta I_{SUPIC} = 40\ nC \times 100\ kHz = 4\ mA$

6.5.6 SUPREG supply voltage for other circuits

The regulated voltage of SUPREG can also be used as a regulated supply for an external circuit. The load of the external circuits has an effect on the start-up (time) and the total load (IC + external circuit) of SUPREG during operation.

Current available for supplying an external circuit from SUPREG

The total current available from SUPREG is a minimum of 40 mA. To determine how much current is available for an external circuit, it must be known how much the IC is using.

$I_{SUPREG\_for\_external} = 40\ mA - I_{SUPREG\_for\_IC}$

With respect to the IC, by far the most amount of current from SUPREG is consumed by the MOSFET drivers (GATELS, GATEHS and GATEPFC). Other circuit parts in the IC, consume a maximum of 3 mA.

$I_{SUPREG\_for\_IC} = I_{SUPREG\_for\_MOSFET\text{-}drivers} + I_{SUPREG\_for\_other\_IC\text{-}circuits}$

$I_{SUPREG\_for\_IC} = I_{SUPREG\_for\_MOSFET\text{-}drivers} + 4\ mA_{max}$

$I_{SUPREG\_for\_MOSFET\text{-}drivers}$ can be estimated by the method provided in Section 13

An estimation by measurement

The current used by SUPIC, while supplying the circuit from an external power supply, can be assumed as a first approximation of how much current the IC circuits take from SUPREG. Using this value, an estimation can be made of the power available for external circuits.

Be aware that the highest power consumption value is reached when the MOSFET drivers are switching at the highest frequency.

Example:

$I_{SUPIC(maximum\ measured)} = 18\ mA$

$I_{SUPREG(for\ IC\ circuits)} = I_{SUPIC(maximum\ measured)} = 18\ mA$

$I_{SUPREG(for\ externals)} = 40\ mA - I_{SUPREG(for\ IC\ circuits)} = 40\ mA - 18\ mA = 22\ mA$

Note: To maintain full functionality, SUPREG must remain above the undervoltage protection level of 10.3 V. During startup, high external current loads can lead to problems.

6.6 Value of the capacitors on SUPIC, SUPREG and SUPHS

Some practical examples are provided in Section 13.

6.6.1 Value of the capacitor on SUPIC

6.6.1.1 General

It is generally advisable to use two types of capacitors on SUPIC. An SMD ceramic type with a smaller value located close to the IC and an electrolytic type with the major part of the capacitance.

6.6.1.2 Start-up

When the supply is initially provided by an HV source, before being handled by an auxiliary winding, a larger capacitor is needed. The capacitor value should be large enough to handle the start-up before the auxiliary winding takes over the supply of SUPIC.

Example of a value estimation:

$I_{SUPIC(start\text{-}up)}$ = 10 mA

$\Delta V_{SUPIC(start\text{-}up)}$ = 22 V − 15 V = 7 V

$\Delta t_{Vaux>15V}$ = 70 ms

$$C_{SUPIC} > I_{SUPIC(start\text{-}up)} \times \frac{\Delta t_{Vaux > 15\ V}}{\Delta V_{SUPIC(statt\text{-}up)}} = 10\ mA \times \frac{70\ ms}{7\ V} = 100\ \mu F \quad (1)$$

6.6.1.3 Normal operation

For normal operation, the main purpose of the capacitors on SUPIC is to keep the current load variations (e.g. gate drive currents) local.

6.6.1.4 Burst mode operation

When burst mode operation is applied, the supply construction often uses an auxiliary winding and start-up from an HV source. While in the burst mode there is a long period during which the auxiliary winding is not able to charge the SUPIC because there is no HBC switching (time between two bursts). Therefore, the capacitor value on SUPIC should be large enough to keep the voltage above 15 V to prevent activating the SUPIC undervoltage stop level.

Example of a value estimation:

$I_{SUPIC(between\ 2\ bursts)}$ = 4 mA

$\Delta V_{SUPIC(burst)} = V_{aux\ burst} - 15\ V = 19\ V - 15\ V = 4\ V$

$\Delta t_{between\ 2\ bursts}$ = 25 ms

$$C_{SUPIC} > I_{SUPIC(start\text{-}up\ between\ 2\ bursts)} \times \frac{\Delta t_{between\ 2\ bursts}}{\Delta V_{SUPIC(burst)}} = 4\ mA \times \frac{25\ ms}{4\ V} = 25\ \mu F \quad (2)$$

6.6.2 Value of the capacitor for SUPREG

To support charging of SUPREG during an HV source start, the capacitor on SUPREG should not be larger than the capacitor on SUPIC. This is to prevent a severe voltage drop on SUPIC due to the charge of SUPREG. Should SUPIC be supplied by an external (standby) source, this is not important.

SUPREG is the supply for the current of the gate drivers. Keeping current peaks local can be achieved using an SMD ceramic capacitor supported by an electrolytic capacitor. This is necessary to provide sufficient capacitance to prevent voltage drop during high current loads. To prevent significant voltage drop, the value of the capacitor on SUPREG should be much larger than the (total) capacitance of the MOSFETs that need to be driven (including the SUPHS parallel load and capacitor bootstrap construction).

When considering the internal voltage regulator, the value of the capacitance on SUPREG should be ≥ 1 μF. Often a much larger value is used for the reasons mentioned previously.

6.6.3 Value of the capacitor for SUPHS

To support charging the gate of the high side MOSFET, the SUPHS capacitor should be much larger than the gate capacitance. This is to prevent a significant voltage drop on SUPHS by the gate charge. When burst mode is applied, SUPHS is discharged by 37 μA during the time between two bursts.

7. MOSFET drivers GATEPFC, GATELS and GATEHS

The TEA1713 provides 3 outputs for driving external high voltage power MOSFETs:

1. GATEPFC for driving the PFC MOSFET
2. GATELS for driving the low side of the HBC MOSFET
3. GATEHS for driving the low side of the HBC MOSFET

7.1 GATEPFC

The TEA1713 has a strong output stage for PFC to drive a high-voltage power MOSFET. It is supplied by the fixed voltage from SUPREG = 10.9 V.

7.2 GATELS and GATEHS

Both drivers have identical driving capabilities for the gate of an external high-voltage power MOSFET. The low-side driver is referenced to pin PGND and is supplied from SUPREG. The high-side driver is floating, referenced to HB, the connection to the midpoint of the external half-bridge. The high-side driver is supplied by a capacitor on SUPHS that is supplied by an external bootstrap function by SUPREG. The capacitor on SUPHS is charged by the bootstrap diode when the low-side MOSFET is on.

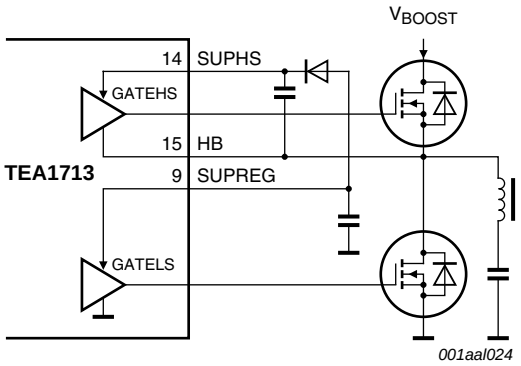


Fig 12. GATELS and GATEHS drivers

Both HBC drivers have a strong current source capability and an extra strong current sink capability. In general operation of the HBC, fast switch on of the external MOSFET is not critical, as the HB node will swing automatically to the correct state after switch off. Fast switch off however, is important to limit switching losses and prevent delay especially at high frequency.

7.3 Supply voltage and power consumption

For a description of the supply voltages and power consumption by the MOSFET drivers see Section 6.5.3 and Section 6.5.5.

7.4 General subjects on MOSFET drivers

Switch on

The time to switch on is dependent upon:

- the supply voltage for the internal driver.
- the characteristic of the internal driver.
- the gate capacitance to be charged.
- the gate threshold voltage for the MOSFET to switch on.
- the external circuit to the gate.

Switch off

The time to switch off is dependent upon:

- the characteristic of the internal driver.
- the gate capacitance to be discharged.
- the voltage on the gate just before discharge.
- the gate threshold voltage for the MOSFET to switch off.
- the external circuit to the gate.

Because the timing for switching off the MOSFET is more critical than switching it on, the internal driver can sink more current than it can source. At higher frequencies and/or short on-time, timing becomes more critical for correct switching. Sometimes a compromise must be made between fast switching and EMI effects. A gate circuit between the driver output and the gate can be used to optimize the switching behavior.

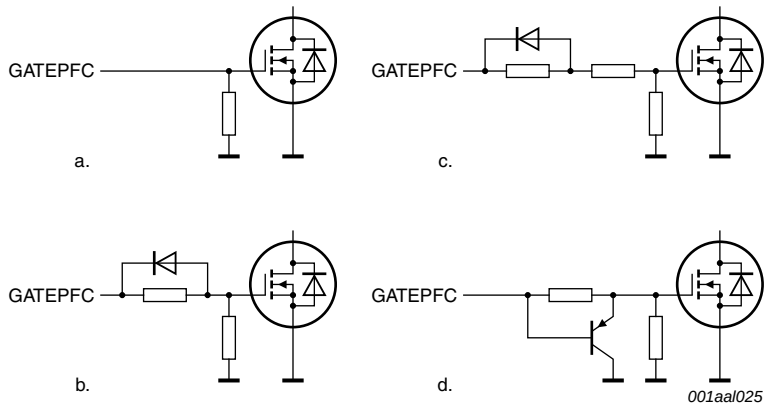


Fig 13. Gate circuits examples

Switching the MOSFETs on and off by the drivers can be approximated by alternating charge and discharge of a (gate-source) capacitance of the MOSFET through a resistor (R_{DS-ON} of the internal driver MOSFET).

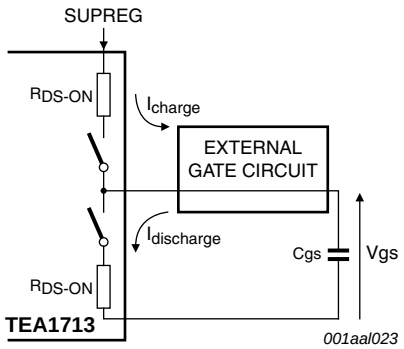


Fig 14. Simplified model of a MOSFET drive

7.5 Specifications

The main function of the internal MOSFET drivers is to source current and sink current to switch the external MOSFET switch on and off.

The amount of current that can be sunk and sourced is specified to show the capability of the internal driver.

The simplified model in Figure 14 demonstrates that the values of the charge current and discharge current are strongly dependant upon the conditions of the supply voltage and gate voltage. The value of the source current is highest when the supply voltage is highest and the gate voltage 0 V. The value of the sink-current is highest when the gate voltage is highest.

Table 3. PFC and HBC driver specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PFC driver (pin GATEPFC)						
$I_{source(GATEPFC)}$	source current on pin GATEPFC	$V_{GATEPFC}$ = 2 V	-	–0.5	-	A
$I_{sink(GATEPFC)}$	sink current on pin GATEPFC	$V_{GATEPFC}$ = 2 V	-	0.7	-	A
		$V_{GATEPFC}$ = 10 V	-	1.2	-	A
HBC high-side and low-side driver (pins GATEHS and GATELS)						
$I_{source(GATEHS)}$	source current on pin GATEHS	$V_{GATEHS} - V_{HB}$ = 4 V	-	–310	-	mA
$I_{source(GATELS)}$	source current on pin GATELS	$V_{GATELS} - V_{PGND}$ = 4 V	-	–310	-	mA
$I_{sink(GATEHS)}$	sink current on pin GATEHS	$V_{GATEHS} - V_{HB}$ = 2 V	-	560	-	mA
		$V_{GATEHS} - V_{HB}$ = 11 V	-	1.9	-	A
$I_{sink(GATELS)}$	sink current on pin GATELS	$V_{GATELS} - V_{PGND}$ = 2 V	-	560	-	mA
		$V_{GATELS} - V_{PGND}$ = 11 V	-	1.9	-	A

The supply voltage provided by SUPREG for GATEPFC and GATELS is constant at 10.9 V. The supply voltage for GATEHS will be lower and depends on the operating conditions (see Section 6.5.4).

7.6 Mutual disturbance of PFC and HBC

The charge and discharge currents for the MOSFET gate of the PFC and HBC, are independently driven in time. Due to these current peaks being high, they can give disturbance on control and sense signals. As both the PFC controller and the HBC controller are integrated in the TEA1713, the (large) driver currents of GATEPFC and GATELS can also give mutual disturbance on the operation of the controllers.

Gate circuits and PCB layout (see Section 12.1) must be designed to prevent this.

A construction similar to that provided by Figure 13(d) will help to keep the (fast and high) switch-off current local, for a high power PFC MOSFET.

8. PFC functions

The PFC operates in Quasi Resonant (QR) or Discontinuous Conduction Mode (DCM) with valley detection to reduce the switch-on losses. The maximum switching frequency of the PFC is limited to 125 kHz which reduces switching losses by valley skipping. This is mainly near the zero crossings of the mains voltage and very effective at low mains input voltage and medium/low output load condition.

The PFC is designed as a boost converter with a fixed output voltage. An advantage of such a fixed boost is that the HBC can be designed to a high input voltage. This makes the HBC design easier.

Another advantage of the fixed boost is the possibility to use a smaller boost capacitor value or to have a significant longer hold-up time.

In the TEA1713 system the PFC is always active. The PFC is switched on first when the mains voltage is present. The HBC is switched on after the boost capacitor is charged to approximately 90% of its normal value.

For improved efficiency at low output loads the system can be operated in burst-mode. During this mode the HBC determines the on/off sequences and the PFC can be made to burst simultaneously for even better efficiency results.

8.1 PFC output power and voltage control

The PFC of the TEA1713 is time controlled and therefore it is not necessary to measure the mains phase angle. For a given mains voltage and load condition the on time is kept constant during the half sine wave to obtain a good power factor (PF) and Mains Harmonics Reduction (MHR).

With a constant on time, the switching current to the PFC output will be proportional to the sine waveform input voltage.

An essential parameter for the PFC coil design is the highest peak current. This current occurs at the lowest input voltage with maximum power.

For a PFC operating in critical conduction mode the maximum peak current $I_{p(max)}$ can be calculated with the following equation:

$$I_{p(max)} = \frac{2 \times \sqrt{2} \times P_{in(max)}}{V_{ac(min)}} = \frac{2 \times \sqrt{2} \times \frac{P_{out(nameplate)}}{\eta}}{V_{ac(min)}} \quad (3)$$

Example:

Efficiency η = 0.9

$P_{out(nameplate)}$ = 250 W

$V_{ac(min)}$ = 90 V

$I_{p(max)}$ = 8.73 A

$I_{p(max)}$ + 10 % = 9.60 A(1)

(1) The TEA1713 PFC, operates in Quasi Resonant (QR) mode with valley detection providing good efficiency. Valley detection needs additional ringing time within every switching cycle. This time for ringing adds short periods of no power transfer to the output capacitor. The system must compensate this with a somewhat higher peak current. A rule of thumb is that the peak current in QR mode is a maximum of 10 % higher than the calculated peak current in critical conduction mode.

8.2 PFC regulation

8.2.1 Sensing V_{BOOST}

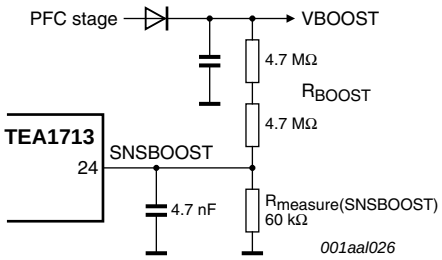


Fig 15. PFC output regulation example: SNSBOOST

The boost output voltage value is set with a resistor divider between the PFC output voltage and pin SNSBOOST. When in regulation, the SNSBOOST voltage is kept at 2.5 V.

To limit power loss, the resistor divider can have a total value up to 10 MΩ.

The measurement resistor between SNSBOOST and ground can be calculated with the following equation:

$$R_{measure(SNSBOOST)} = \frac{R_{BOOST} \times V_{reg(SNSBOOST)}}{V_{BOOST} - V_{reg(SNSBOOST)}} \quad (4)$$

Example:

$R_{measure(RBOOST)}$ = 4.7 MΩ + 4.7 MΩ = 9.4 MΩ

V_{BOOST} = 394 V

$$R_{measure(SNSBOOST)} = \frac{R_{BOOST} \times V_{reg(SNSBOOST)}}{V_{BOOST} - V_{reg(SNSBOOST)}} = \frac{9.4\ \text{M}\Omega \times 2.5\ \text{V}}{394\ \text{V} - 2.5\ \text{V}} = 60\ \text{k}\Omega \quad (5)$$

It is recommended to use a capacitor on SNSBOOST to prevent wrong measurements due to MOSFET switching noise, mains surge events or ESD events. Also, for this reason, the measurement resistor and the filtering capacitor should be placed close to the IC in the PCB layout.

8.2.2 SNSBOOST open and short-circuit pin detection

The PFC will not start switching until the voltage on SNSBOOST is above 0.4 V. This serves as short-circuit protection for the boost voltage and SNSBOOST pin itself.

An internal current source draws a small amount of current from SNSBOOST. This will prevent switching when the pin is left open as the voltage will remain lower than 0.4 V. This combination also creates an Open Loop Protection (OLP) when, for example, one of the resistors in the boost divider network is disconnected.

8.2.3 PFCCOMP in the PFC voltage control loop

The PFC output voltage is set and controlled by SNSBOOST. The internal error amplifier with a reference voltage of 2.5 V senses the voltage at SNSBOOST. The amplifier converts the input error voltage with a transconductance g_m=80 μA/V to its output. This output is available at COMPPFC for adding an external loop compensation network. The current from the error amplifier will result in a loop voltage at COMPPFC. This COMPPFC voltage, in combination with the voltage at pin SNSMAINS, determines the PFC switching-on time.

A compensation network, typically comprising one resistor and two capacitors at pin COMPPFC, is used to stabilize the PFC control loop.

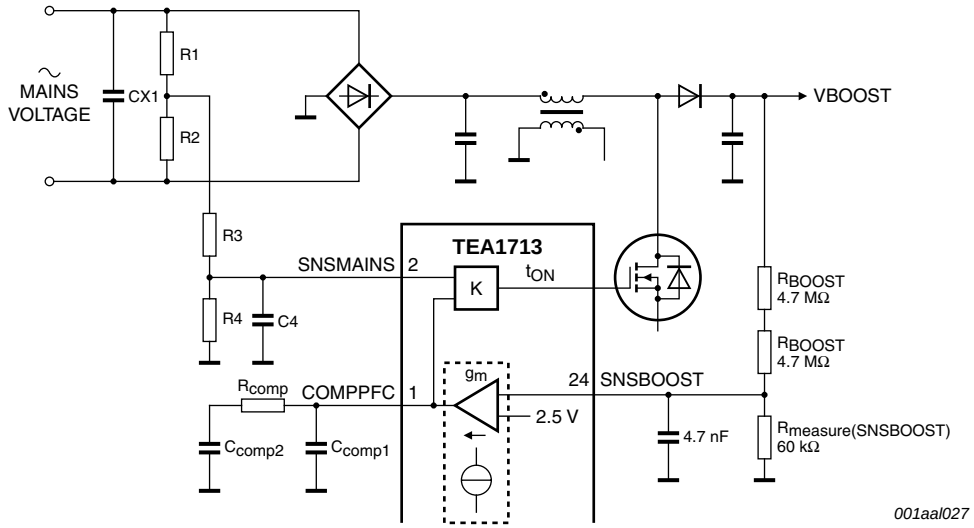


Fig 16. Basic PFC voltage control loop with PFCCOMP

The transfer function has a pole at 0 Hz, a zero by $R_{comp}C_{comp2}$ and a pole again by $C_{comp1}C_{comp2}$. The zero frequency should be set to 10 Hz while the next pole frequency is at 40 Hz. The zero point and pole frequencies of the compensation network can be calculated as follows:

$$fz = \frac{1}{2\pi \times R_{comp} \times C_{comp2}} \quad (6)$$

$$fp = \frac{C_{comp1} + C_{comp2}}{2\pi \times R_{comp} \times C_{comp1} \times C_{comp2}} \quad (7)$$

The choice also concerns a trade-off between power factor and transient behavior. A lower regulation bandwidth leads to a better power factor but the transient behavior becomes poorer. A higher regulation bandwidth leads to a better transient response but a poorer power factor.

8.2.4 Mains compensation in the PFC voltage control loop

The mathematical equation for the transfer function of a power factor corrector, contains the square of the mains input voltage.

$$K(V_{mains}) = \frac{A}{V_{mains}^2} \quad (8)$$

In a typical application this will result in a low bandwidth for low mains input voltages, while at high mains input voltages the MHR requirements may be hard to meet.

To compensate for the mains input voltage influence, the TEA1713 contains a correction circuit. The average mains voltage is measured by SNSMAINS and used for internal compensation. Figure 17 shows the relationship between the SNSMAINS voltage, COMPPFC voltage and the on-time. With this compensation it is possible to keep the regulation loop bandwidth constant over the complete mains input voltage range, yielding a fast transient response on load steps, while still complying with class-D MHR requirements.

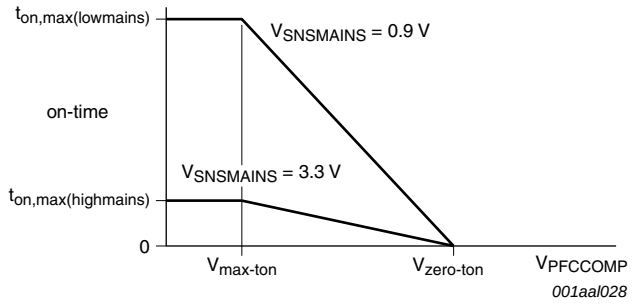


Fig 17. Relationship between on-time, SNSMAINS voltage and COMPPFC voltage

8.3 PFC demagnetization and valley sensing

To reduce switching losses and EMI, the PFC MOSFET is switched on for the next stroke if the voltage at the drain of the MOSFET is at its minimum (valley switching), see Figure 18.

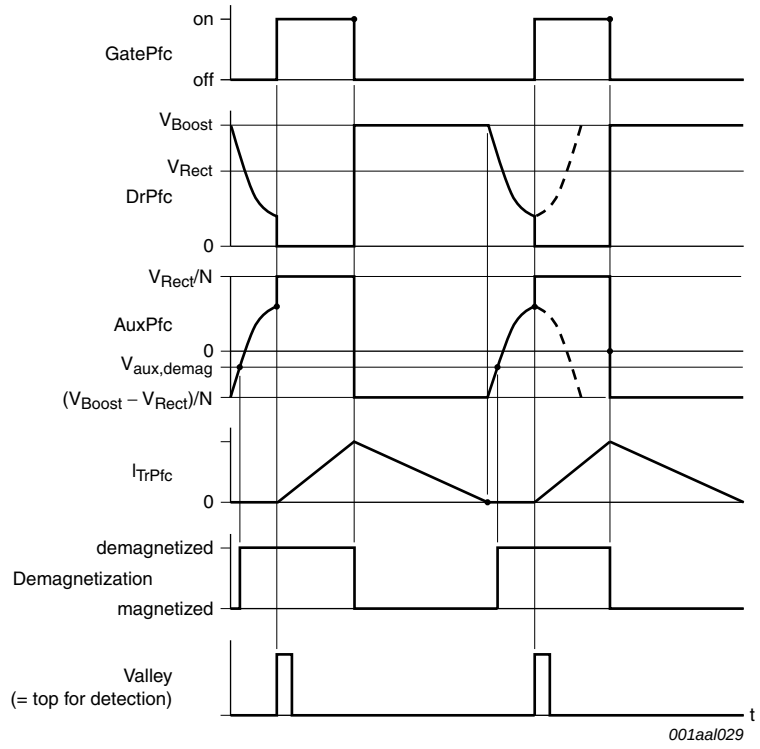


Fig 18. PFC demagnetization and valley sensing

The valleys are detected by SNSAUXPFC. An auxiliary winding on the PFC coil provides a measurement signal on SNSAUXPFC. It gives a reduced and inverted copy of the MOSFET drain voltage. When a valley of the drain voltage (top at SNSAUXPFC voltage) is detected, the MOSFET is switched on.

If no top (valley at the drain) is detected on SNSAUXPFC within 4 μs after demagnetization is detected, the MOSFET is forced to switch on.

8.3.1 PFC auxiliary sensing circuit

To protect the internal circuit of the IC against excessive voltage, for example during lightning surges, it is recommended to add a 5 kΩ series resistor to SNSAUXPFC. In the PCB layout, this resistor should be placed close to the IC to prevent disturbances causing incorrect switching.

It is important to maintain valley detection even at low ringing amplitudes. To reach this objective, the voltage at the SNSAUXPFC should be set as high as possible, while taking into account its absolute maximum rating of ±25 V.

The number of turns of the auxiliary winding on the PFC coil can be calculated using the following equation:

$$N_{aux(max)} = \frac{V_{SNSAUXPFC}}{V_{Lmax}} \times N_p = \frac{25\ \text{V}}{415} \times 52 = 3.13 \rightarrow 3\ turns \quad (9)$$

$V_{SNSAUXPFC}$ is the absolute maximum voltage rating, V_{Lmax} is the maximum voltage across the PFC primary winding and N_P is the number of turns on the PFC coil (for this example, a value of 52 is used).

The boost output voltage at OverVoltage Protection (OVP) determines the maximum voltage across the PFC primary winding and can be calculated using the following equation:

$$V_{Lmax} = \frac{V_{OVP(SNSBOOST)}}{V_{reg(SNSBOOST)}} \times V_{BOOST} = \frac{2.63\ \text{V}}{2.5\ \text{V}} \times 394V = 415\ \text{V} \quad (10)$$

In this example, a design value of 394 V is used for nominal V_{BOOST}.

When a PFC coil with a higher number of auxiliary turns is used, a resistor voltage divider can be placed between the auxiliary winding and SNSAUXPFC. The total resistive value of the divider should be less than 10 kΩ to prevent delay of the valley detection in combination with parasitic capacitances.

8.3.2 PFC frequency limit

For minimizing the switching losses, the switching frequency is limited to 125 kHz. If the frequency for quasi-resonant operation is above the 125 kHz limit, the system will switch over to discontinuous conduction mode. The PFC MOSFET is only switched on at a minimum voltage across the switch (valley switching). One or more valleys are skipped, when necessary, to keep the frequency below 125 kHz (valley skipping).

To ensure proper control of the PFC MOSFET in all circumstances, the minimum off-time is limited to 50 μs after the last PFC gate signal.

8.4 PFC OverCurrent Regulation/Protection (OCR/OCP)

The maximum peak current, switched by the external MOSFET, is limited cycle-by-cycle by sensing the voltage across a measurement resistor $R_{SENSE(PFC)}$ in the source of the MOSFET. The voltage is measured by SNSCURPFC and limited to 0.5 V. At this voltage level the MOSFET is switched off.

To avoid false triggering of the OCP, it is advised to take a small voltage margin into account.

The value of the measurement resistor $R_{SENSE(PFC)}$ can be determined by:

$$R_{SENSE(PFC)} = \frac{V_{OCR(SNSCURPFC)} - V_{margin}}{I_{P_{max}}} = \frac{0.52V - 0.1V}{8.73A} = 48\ m\Omega \quad (11)$$

The SNSCURPFC voltage will sense an initial voltage peak at the moment the PFC MOSFET switches on, because its (parasitic) capacitances are discharged. SNSCURPFC has a leading edge blanking of 310 ns to mask this event, so it will not react to this initial peak.

8.4.1 PFC soft-start and soft-stop

To prevent transformer noise/rattle at start-up or during burst mode operation, the PFC has a soft-start function and a soft-stop function. The soft-start slowly increases the primary peak current at the start of operation. The soft-stop function slowly decreases the transformer peak current before operation is stopped.

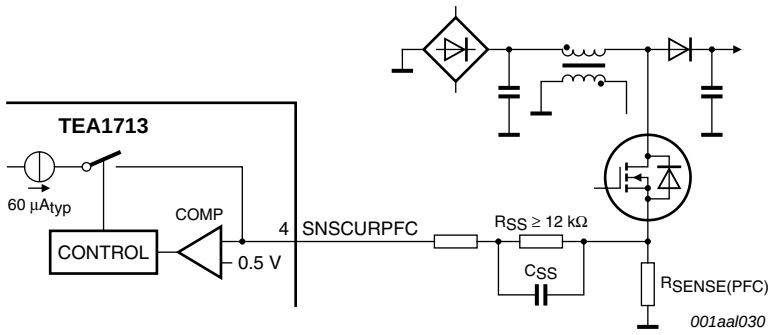


Fig 19. PFC soft-start and soft-stop setup

A resistor and capacitor between SNSCURPFC and the current sense resistor $R_{SENSE(PFC)}$ set both functions.

8.4.1.1 Soft-start

Before start of operation, an internal current source of 60 µA charges the capacitor to $V_{SNSCURPFC}$ = 60 µA x R_{SS}. As soon as SNSCURPFC exceeds the internal start voltage of 0.5 V, the operation can start. To ensure that the start voltage level is reached, it is recommended to choose $R_{SS} \geq 12$ kΩ. At starting, the current source is stopped and the voltage on SNSCURPFC will drop as R_{SS} discharges C_{SS}. During this discharge the peak current of each cycle will increase until C_{SS} is discharged completely and the normal peak current regulation level (OCR/OCP), set by $R_{SENSE(PFC)}$, is reached.

The soft-start period can be estimated by:

$$\tau = R_{SS} \times C_{SS} \quad (12)$$

8.4.1.2 Soft-stop

Soft-stop is achieved by switching on the internal current source of 60 µA again.

The current charges C_{SS} and the increasing capacitor voltage reduces the peak current. When SNSCURPFC reaches 0.5 V the operation is stopped.

To prevent measurement disturbances during soft-stop, the voltage is only measured during the off time of the PFC power switch.

8.4.2 SNSCURPFC open and short protection

When the SNSCURPFC pin is open, SNSCURPFC is charged to 0.5 V by the internal current source of 60 µA for soft-start. The PFC will not start switching because of OCP.

When the SNSCURPFC pin is short circuit to ground, the PFC cannot start operation as the start level of 0.5 V has not been reached.

8.5 PFC boost OverVoltage Protection (OVP)

To prevent boost overvoltage during load steps and mains transients, an overvoltage protection circuit is built in. As soon as the voltage on SNSBOOST exceeds 2.63 V, the switching of the power factor correction circuit is stopped. The PFC will resume switching when the voltage on SNSBOOST drops below 2.63 V.

When the resistor between pin SNSBOOST and ground is open, the overvoltage protection will also trigger. In this situation, an internal current source of 45 nA to ground can increase the voltage on SNSBOOST to the OVP protection level.

The voltage value at which PFC OVP will become active can be calculated with the following equation:

$$V_{OVP(BOOST)} = \frac{V_{OVP(SNSBOOST)}}{V_{reg(SNSBOOST)}} \times V_{BOOST} = \frac{2.63\ \text{V}}{2.5\ \text{V}} \times 394V = 415\ \text{V} \quad (13)$$

In the example, a design value of 394 V is used for nominal V_{BOOST}.

8.6 PFC mains UnderVoltage Protection (brownout protection)

To prevent the PFC operating at very low mains input voltages, the voltage on the SNSMAINS pin is sensed continuously. As soon as the voltage on this pin drops below 0.89 V, the switching of the PFC is stopped. This mains undervoltage protection is sometimes referred to brownout protection.

The voltage on pin SNSMAINS must be an average DC value that represents the mains input voltage. The system works best with a time constant of approximately 150 ms for pin SNSMAINS. When the voltage on SNSMAINS drops, it is internally clamped to a value of 1.05 V, which is 0.1 V below the start level of 1.15 V for SNSMAINS. This allows a fast restart as soon as the mains input voltage returns after a mains-dropout. The PFC (re)starts when the SNSMAINS voltage exceeds the start level of 1.15V.

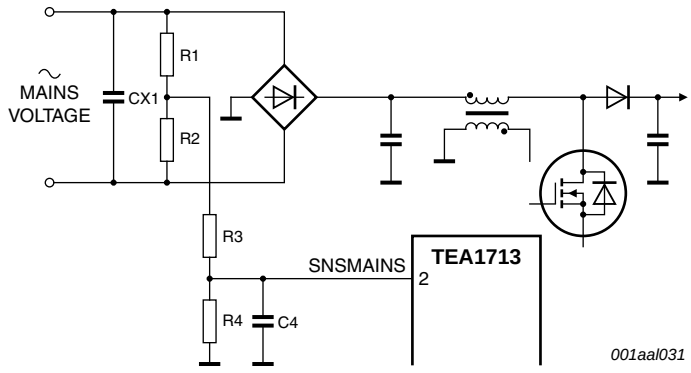


Fig 20. SNSMAINS circuitry

8.6.1 Under voltage or brownout protection level

The AC input voltage is measured via R1 and R2. Each resistor alternately senses half the sine cycle and as a result, both resistors have the same value.

For R1 and R2 a typical resistor value of 2 MΩ can be applied to keep the bleeder loss low.

The average voltage sensed is calculated as follows:

$$V_{AC_{average}} = \frac{2\sqrt{2}}{\pi} \times V_{AC_{rms}} \quad (14)$$

The SNSMAINS brownout protection (RMS) voltage level is calculated by:

$$R_v = \frac{R1 \times R2}{R1 + R2} \quad (15)$$

$$V_{BO} = 2 \times \frac{\pi}{2\sqrt{2}} \times V_{SNSMAINS(UVP)} \times \left(\frac{R_v + R3}{R4} + 1\right) \quad (16)$$

Example:

Required: V_{BO} = 66 V AC, with:

- $V_{SNSMAINS(UVP)}$ = 0.89 V
- R1 = R2 = 2 MΩ → R_V = 1 MΩ

$$V_{BO} = 2 \times \frac{\pi}{2\sqrt{2}} \times 0.89 \times \left(\frac{R_v + R3}{R4} + 1\right) \quad (17)$$

$$66 = 1.9771 \times \left(\frac{1\ \text{M}\Omega + R3}{R4} + 1\right) \quad (18)$$

R3 = 560 kΩ, R4 = 47 kΩ

For a recommended time constant of 150 ms, with C4 = 3300 nF, the time constant:

$T_{SNSMAINS}$ = R4 x C4 = 47 kΩ x 3300 nF = 155 ms.

8.6.2 Discharging the mains input capacitor

There is often an application requirement to discharge the X capacitors in the EMC input filtering within a certain time. The resistance to discharge the X capacitors in the input filtering is determined by the replacement value of R1, R2, R3 and R4. The replacement value can be calculated with the following equation:

$$R_{discharge} = R1 + \frac{R2 \times (R3 + R4)}{R2 + R3 + R4} \quad (19)$$

Example:

Required: $T_{discharge}$ < 600 ms, with:

- R1 = R2 = 2 MΩ
- R3 = 560 kΩ
- R4 = 47 kΩ

$$R_{discharge} = R1 + \frac{R2 \times (R3 + R4)}{R2 + R3 + R4} = 2\ \text{M}\Omega + \frac{2\ \text{M}\Omega \times (560\ \text{k}\Omega + 47\ \text{k}\Omega)}{2\ \text{M}\Omega + 560\ \text{k}\Omega + 47\ \text{k}\Omega} = 2465\ \text{k}\Omega \quad (20)$$

With:
C = 220 nF, the time constant $T_{discharge} = R_{discharge}$ x C = 2465 kΩ x 220 nF = 542 ms.

8.6.3 SNSMAINS open pin detection

The SNSMAINS pin, which senses the mains input voltage, has an integrated protection circuit to detect an open pin. When the pin is not connected, an internal current source of 33 nA will either pull the pin down below the stop level of 0.9 V or keep it below the start level of 1.15 V.

When the SNSMAINS pin is shorted to ground, the results will be similar.

9. HBC functions

9.1 HBC UVP boost

To ensure proper working of the HBC, the TEA1713 will begin operation when the input voltage is higher than approximately 90 % of the nominal boost voltage.

For this, the voltage on the SNSBOOST pin is sensed continuously. As soon as the voltage on SNSBOOST drops below 1.6 V, switching of the HBC is stopped at the moment the low-side MOSFET is on. The HBC (re)starts when the SNSBOOST voltage exceeds the start level of 2.3 V.

9.2 HBC switch control

The internal control for the MOSFET drivers, determines when the MOSFETs are switched on and off. It uses the input from several functions.

1. An internal divider is used to provide the **alternating switching** of high-side and low-side MOSFET for every oscillator cycle.
2. The **adaptive non-overlap** (see Section 9.3) sensing on HB determines the switch-on moment.
3. The **oscillator** (see Section 9.4) determines the switch-off moment.
4. Several **protection and enable** functions determine if the resonant converter is allowed to switch.

9.3 HBC adaptive non-overlap

9.3.1 Inductive mode (normal operation)

The high efficiency of a resonant converter is the result of Zero-Voltage Switching (ZVS) of the power MOSFETs, also called soft-switching. To allow soft-switching, a small non-overlap time (also called dead time) is required between the on-time of the high-side MOSFET and low-side MOSFET. During this non-overlap time, the primary resonant current (dis)charges the capacitance of the half-bridge between ground and boost voltage. After the (dis)charge, the body diode of the MOSFET starts conducting and because the voltage across the MOSFET is zero, there are no switching losses.

This mode of operation is called inductive mode because the switching frequency is above the resonance frequency and the resonant tank has an inductive impedance.

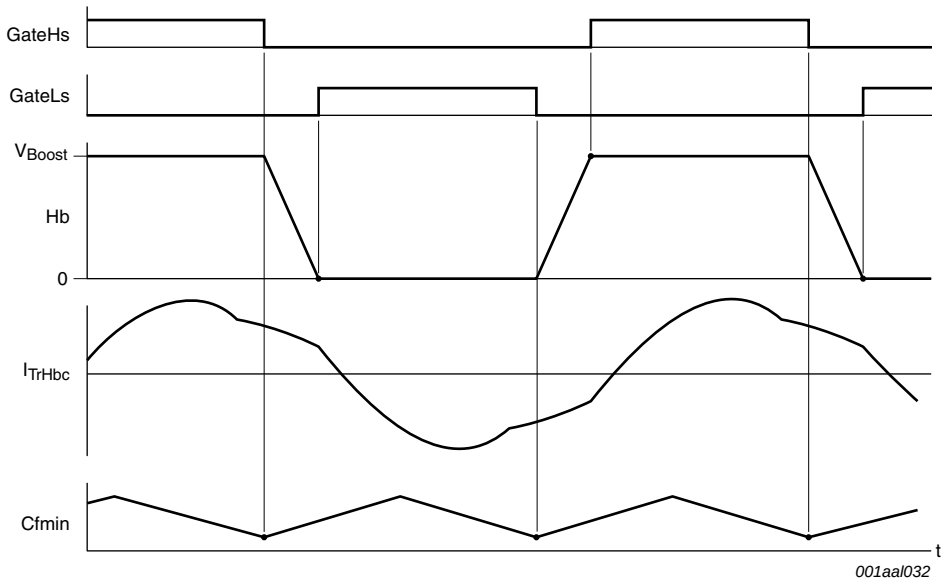


Fig 21. Inductive mode HBC switching

The time required for the transition of the HB depends on the amplitude of the resonant current at the moment of switching. There is a (complex) relationship between the amplitude, the frequency, the boost voltage and the output voltage. Ideally the IC should switch on the MOSFET as soon as the transition of the HB has reached its end value. To prevent a swing back of the HB voltage, it should not wait longer, especially at high output load.

The adaptive non-overlap function of the TEA1713 provides an automatic measurement and control function that decides when to switch on. As it uses actual measurement input the control will adapt for operation changes in time.

Because of this adaptive non-overlap function, it is not needed to preset a fixed non-overlap time, which is always a compromise between different operating conditions.

The adaptive non-overlap function senses the slope at HB after one MOSFET has been switched off. Normally the slope at the HB starts directly. Once the transition of the HB node is complete, the slope ends. This is detected by the adaptive non-overlap sensing and the other MOSFET is switched on. In this way the non-overlap time is automatically adjusted to the best value providing the lowest switching loss, even if the HB transition cannot be fully completed.

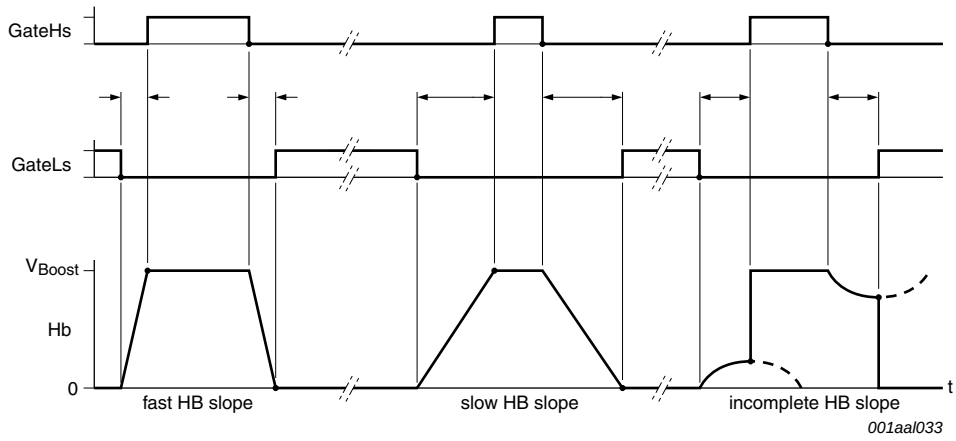


Fig 22. Adaptive non-overlap switching during normal operating conditions

The non-overlap time depends on the HB slope, but has an upper and lower time limit. An integrated minimum non-overlap time (160 ns_{max}) prevents accidental cross conduction in all conditions. The maximum non-overlap time is limited to the charging time of the oscillator. If the HB slope takes more time than the charging of the oscillator (25 % of HB switching period) the MOSFET is forced to switch on. In this case the MOSFET is not soft-switching. This limitation of the maximum non-overlap time ensures that at very high switching frequency the on-time of the MOSFET is at least 25 % of the HB switching period.

9.3.2 Capacitive mode

During error conditions (e.g. output short-circuit, load pulse too high) or special start-up conditions, the switching frequency can become lower than the resonance frequency. The resonant tank then has a capacitive impedance. In capacitive mode the HB slope doesn't start after the MOSFET has switched off. It is not preferred to just switch on the other MOSFET. The lack of soft-switching increases dissipation in the MOSFETs. The conducting body diode in the MOSFET at the switching moment can damage or even destroy the device very quickly.

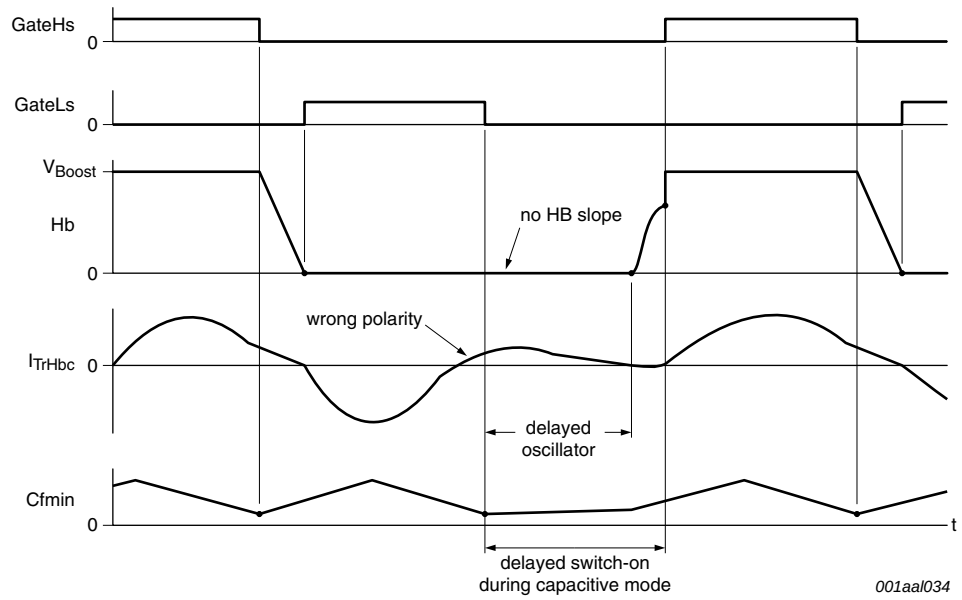


Fig 23. Capacitive mode HBC switching

The adaptive non-overlap system of the TEA1713 will always wait until the slope at the half bridge node starts. It guarantees safe/best switching of the MOSFETs in all circumstances. In capacitive mode, it can take half the resonance period before the resonant current changes back to the correct polarity and starts charging the half bridge node. To allow this relatively long waiting time, the oscillator remains in its slow charging current mode until the half bridge slope starts (see also Section 9.4.2 and Figure 27).

The MOSFET will be forced to switch-on when the half bridge slope doesn't start at all and the slowed-down oscillator reaches the high level.

To bring the converter from capacitive mode to inductive operation again, the oscillation frequency is increased by the capacitive mode regulation function.

9.3.3 Capacitive Mode Regulation (CMR)

The harmful switching in capacitive mode is prevented by the adaptive non-overlap function. However, to end the capacitive mode operation and return to inductive mode operation, an extra action is executed which results in the Capacitive Mode Regulation.

Capacitive mode is detected when the HB slope doesn't start shortly (690 ns) after the MOSFET is switched-off. At detection of capacitive mode, the switching frequency will be increased quickly. This is realized by discharging SSHBC/EN with a high current (1800 μA) from the moment $t_{no\text{-}slope}$ = 690 ns has passed before the half bridge slope starts. The resulting frequency increase regulates the HBC back to the border between capacitive and inductive mode.

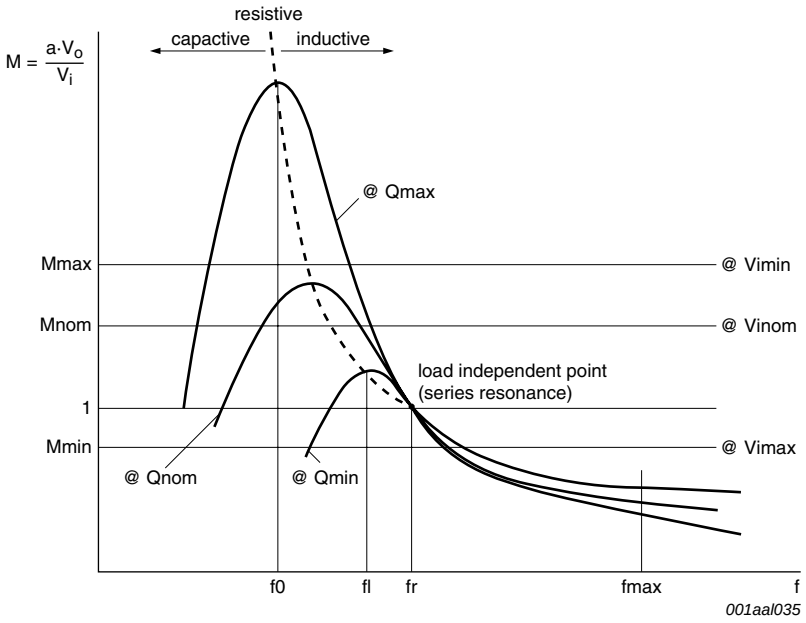
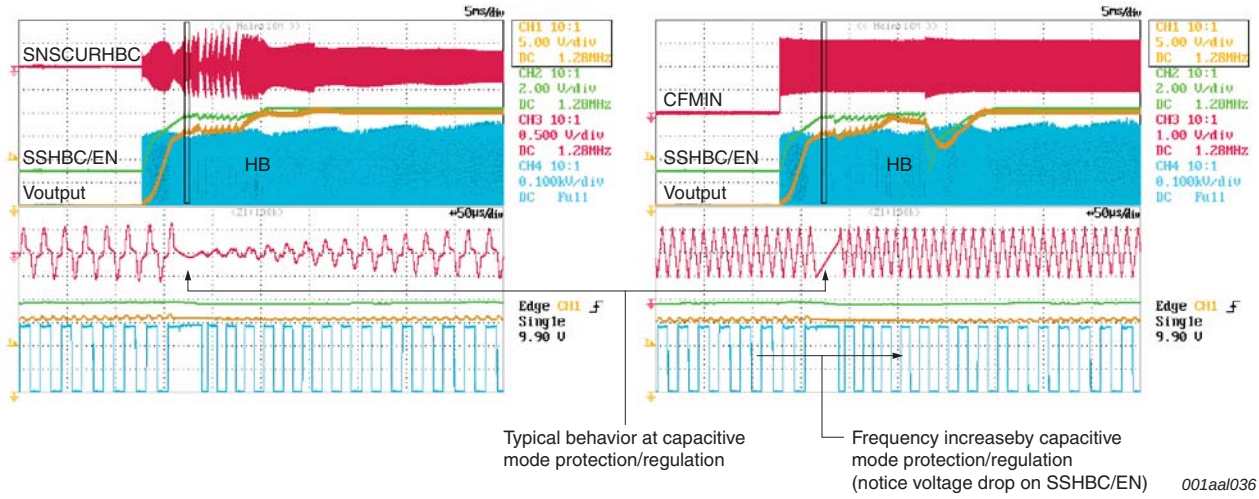


Fig 24. Capacitive/Inductive HBC operating frequencies

CMR of the TEA1713 can be recognized by the typical slowing of the oscillator in combination with the discharging of SSHBC/EN.



Oscilloscope traces contain normal time-base (top) and zoomed view (bottom)

Fig 25. Typical protection and regulation behavior in capacitive mode (during bad start-up)

9.4 HBC oscillator

The slope controlled oscillator determines the switching frequency of the half-bridge. The oscillator generates a triangular waveform at the external capacitor Cf_{min}.

9.4.1 Presettings

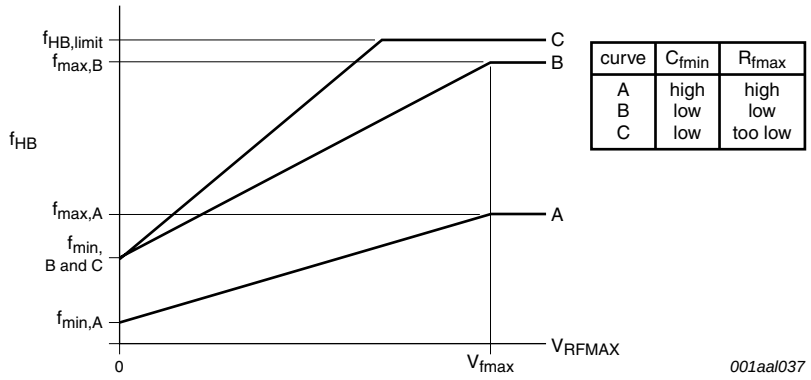
Two external components determine the frequency range:

1. Capacitor at CFMIN: Sets the minimum frequency in combination with an internally trimmed current source.
2. Resistor at RFMAX: Sets the frequency range and, in combination with CFMIN, the maximum frequency.

The oscillator frequency depends on the charge and discharge current of the capacitor on CFMIN. This (dis)charge current consists of a fixed part which determines the minimum frequency, and a variable part which depends on the value of the resistor on RFMAX and the voltage at pin RFMAX.

- The voltage on RFMAX is 0 V when the oscillator frequency is minimum.
- The voltage on RFMAX is 2.5 V when the oscillator frequency is maximum.
- The value of the resistor on RFMAX determines the relationship between VRFMAX and the frequency. It also determines the maximum frequency when RFMAX = 2.5 V.

The maximum frequency of the oscillator is independent of the settings on CFMIN and RFMAX and is limited internally to a minimum of 500 kHz. Figure 26 visualizes the relationship between VRFMAX and f_{HB} for three different values of C_{fmin} and R_{fmax}.



curve	C_{fmin}	R_{fmax}
A	high	high
B	low	low
C	low	too low

Fig 26. Frequency relationships

9.4.2 Operational control

During operation, the oscillator is controlled by the state of the half bridge node HB. To achieve this, an internal slope detection circuit monitors the voltage on HB.

The charge current of the oscillator is initially set to a low value of 30 μA. After the start of the half bridge slope has been detected, the charge current will be increased to the normal value that corresponds to the working frequency at that moment. The working

frequency is controlled by feedback on SNSFB. Normally, the half bridge slope starts directly after the switch-off of the MOSFET, the time with the low oscillator current (30 μA) being negligible.

The similarity between GATELS and GATEHS when switching, is that the oscillator signal determines the moment of switching off. The moment of switching on is determined by the HB sensing circuit.

As the moment of switching on is determined by the HB sensing (and therefore not fixed), the time between switching one MOSFET off and the other one on, is adaptive: adaptive non-overlap time (or dead time). This non-overlap time has no influence on the oscillator signal.

The frequency control by oscillator-frequency consists of determining the time between two moments of switching off (including a small period in which the oscillator current is only 30 μA).

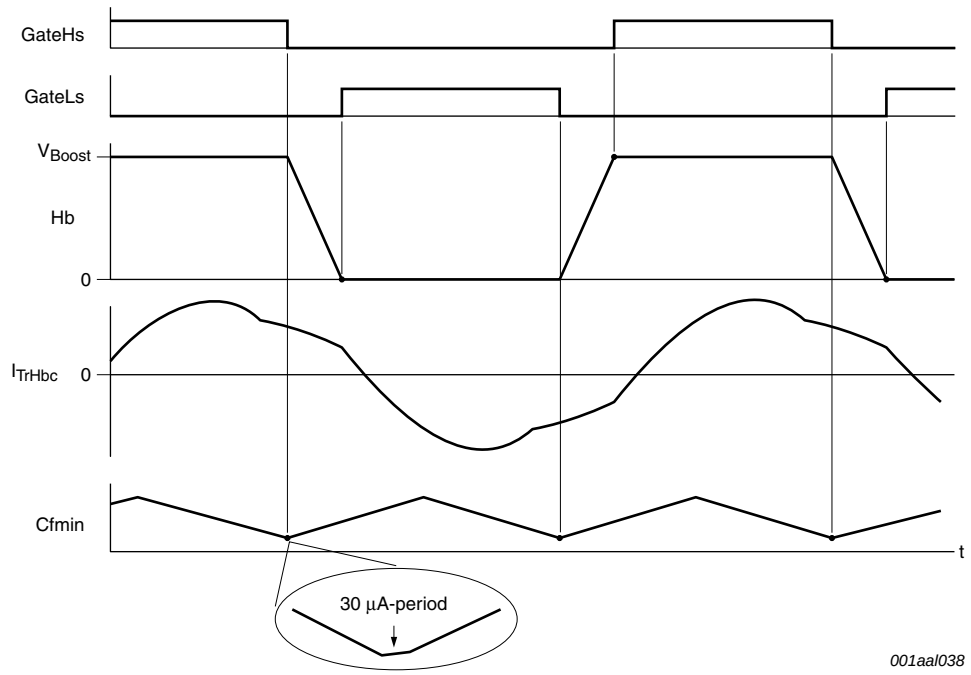


Fig 27. Timing overview of the oscillator and HBC drive

9.4.3 CFMIN and RFMAX

This section explains the method of calculating the values for the capacitor on CFMIN and the resistor on RFMAX.

9.4.3.1 Minimum frequency setting for CFMIN

$$f_{oscillator} = 2 \times f_{HB} \tag{21}$$

$$t_{charge} \approx t_{discharge} \approx \frac{t_{oscillator}}{2} \tag{22}$$

$$\Delta V_{oscillator} = V_{high(CFMIN)} - V_{low(CFMIN)} = 3\ V - 1\ V = 2\ V \tag{23}$$

$$I_{oscillator(min)} = 150\ \mu A \tag{24}$$

$$CFMIN = \frac{I_{oscillator(min)}}{2 \times 2 \times f_{HB(min)} \times \Delta V_{oscillator}} = \frac{150\ \mu A}{8 \times f_{HB(min)}} \tag{25}$$

Example:

Requirement: $f_{HB(min)}$ = 57 kHz

$$CFMIN = \frac{150\ \mu A}{2 \times 2 \times 57\ \text{kHz} \times 2} = \frac{0.00015}{456000} = 329\ \text{pF} \tag{26}$$

9.4.3.2 Maximum frequency setting for RFMAX

$$I_{oscillator(max)} = 4.7 \times I_{RFMAX(max)} + I_{oscillator(min)} \tag{27}$$

$$I_{RFMAX(max)} = \frac{V_{f(max)}}{RFMAX} \tag{28}$$

$$RFMAX = \frac{V_{f(max)}}{I_{RFMAX(max)}} = \frac{2.5\ \text{V}}{I_{RFMAX(max)}} \tag{29}$$

Analog to the situation with $I_{oscillator(min)}$:

$$f_{HB(max)} = \frac{I_{oscillator(max)}}{4 \times CFMIN \times \Delta V_{oscillator}} = \frac{4.7 \times I_{RFMAX(max)} + I_{oscillator(min)}}{4 \times CFMIN \times 2} \tag{30}$$

$$I_{RFMAX(max)} = \frac{8 \times CFMIN \times f_{HB(max)} - I_{oscillator(min)}}{4.7} \tag{31}$$

$$I_{RFMAX(max)} = \frac{8 \times CFMIN \times f_{HB(max)} - 150\ \mu A}{4.7} \tag{32}$$

$$RFMAX = \frac{2.5\ \text{V}}{I_{RFMAX(max)}} = \frac{11.75}{8 \times CFMIN \times f_{HB(max)} - 150\ \mu A} \tag{33}$$

Example:

Requirement: $f_{HB(max)}$ = 180 kHz and CFMIN = 330 pF

$$I_{RFMAX(max)} = \frac{8 \times 330\ \text{pF} \times 180\ \text{kHz} - 150\ \mu A}{4.7} = \frac{(475\ \mu A - 150\ \mu A)}{4.7} = 69.15\ \mu A \tag{34}$$

$$RFMAX = \frac{2.5\ \text{V}}{69.15\ \mu A} = 36\ \text{k}\Omega \tag{35}$$

Note: The average multiplication factor is 4.7. There will be a small deviation in value depending on other parameters and presetting conditions. Practical verification of the result is advised.

9.4.4 RFMAX and High Frequency Protection (HFP)

Normally the converter will not operate continuously at the preset maximum frequency. This maximum frequency will only be used for a short time during soft-start or temporary fault/overload conditions.

When the operating frequency remains at, or close to, maximum frequency for a longer period, a fault condition is assumed and a protection activated.

For this, the HFP senses the voltage at pin RFMAX. This voltage indicates the actual operating frequency. When the frequency is higher than approximately 75 % of the frequency range (RFMAX=1.83 V), the protection timer is started.

Note: During normal regulation, the maximum frequency will lead to only 60 % of the present range and the voltage at pin RFMAX will be 1.5 V maximum.

9.5 HBC feedback (SNSFB)

A typical power supply application contains mains insulation in the HBC. On the secondary (mains insulated) side, the output voltage is compared to a reference and amplified. The TEA1713 is normally placed on the primary side. The output of the error amplifier is transferred to the primary side via an OPTOcoupler. The output of the OPTOcoupler on the primary side can be connected directly to SNSFB.

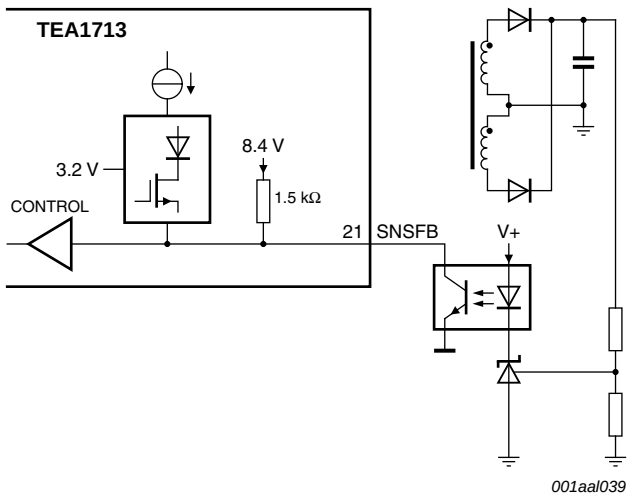


Fig 28. Typical basic SNSFB application

The SNSFB pin supplies the OPTOcoupler from an internal voltage source of 8.4 V via an internal series resistor of 1.5 kΩ. This internal series resistance allows spike filtering by an external capacitor at the pin if needed.

To ensure sufficient bias current for proper working of the optocoupler, the feedback input has a threshold current of 0.66 mA at which the frequency is minimum. The maximum frequency controlled by SNSFB is reached at 2.2 mA. Notice that this is approximately 60% of the total preset frequency range. The remaining upper part of the frequency range can only be reached by control of SSHBC/EN for soft-start or protection.

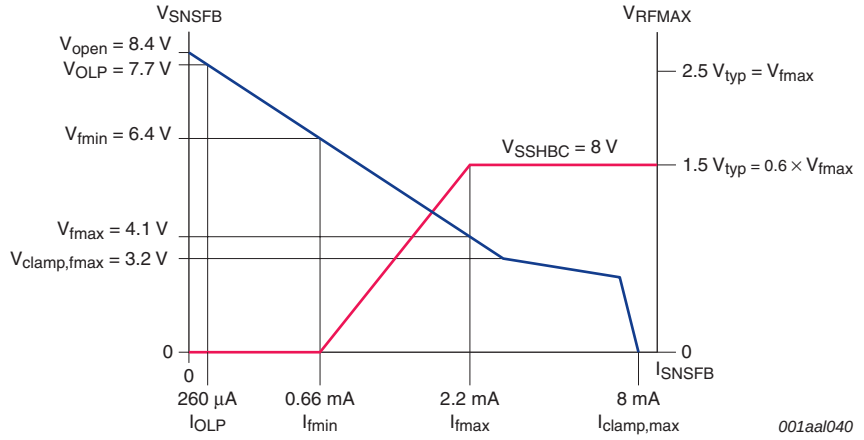
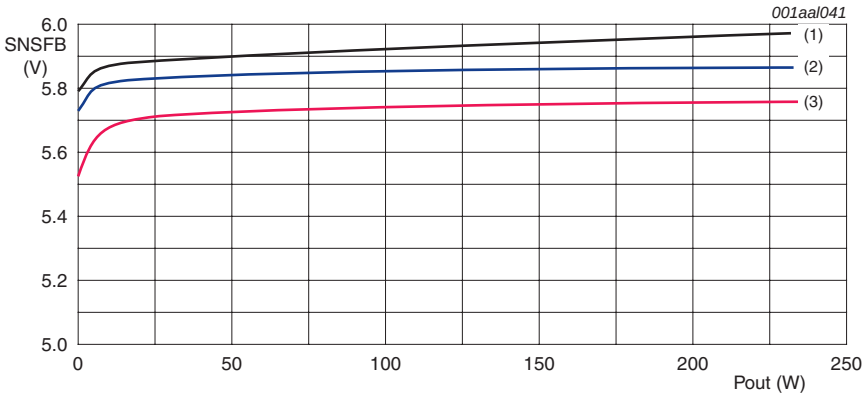


Fig 29. SNSFB V-I characteristics



1. V_{BOOST} = 310 V DC
2. V_{BOOST} = 350 V DC
3. V_{BOOST} = 390 V DC

Fig 30. SNSFB voltage to output power characteristics examples

9.5.1 HBC Open Loop Protection (OLP)

The resonant controller of the TEA1713 contains an Open-Loop Protection (OLP). This protection monitors the voltage on SNSFB. When it exceeds 7.7 V, the protection timer is started.

In normal operating conditions, the OPTOcoupler current is between 0.66 mA and 2.2 mA which pulls down the voltage at pin SNSFB. Due to an error in the feedback loop, the current can become less than 260 µA which leads to an open loop protection.

9.6 SSHBC/EN soft-start and enable

The SSHBC/EN pin provides the following three functions:

1. It enables the PFC (> 1.2 V) and PFC plus HBC (> 2.2 V).
2. It performs an HBC frequency sweep during soft-start from 3.2 V to 8 V.
3. It provides frequency control during protection.

Seven internal current sources operate the frequency control depending on the required action.

1. Soft-start + OverCurrent Protection: high/low charge (160 μA/40 μA) + high/low discharge (160 μA/40 μA).
2. Capacitive mode regulation: high/low discharge (1800 μA/440 μA).
3. General: bias discharge (5 μA).

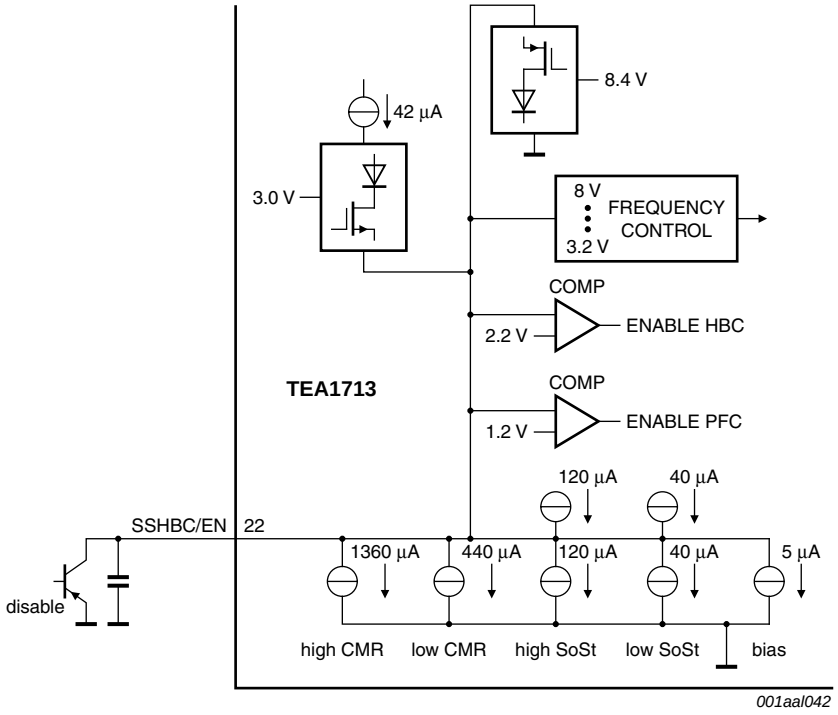


Fig 31. SSHBC: overview of sources, clamps and levels

9.6.1 Switching ON and OFF using an external control function

The SSHBC/EN can be used to switch the converters on and off using an external control function.

This function is often driven by a microcontroller from the secondary side of the OPTOcoupler. By doing this, the main power supply (PFC+HBC) can be switched off for standby mode and on for normal operation. In such a concept a separate standby supply is needed to supply the microcontroller functions during the standby. It is also possible to switch/keep off the HBC and only have the PFC operational.

The TEA1713 also offers the possibility to switch on/off using the SNSOUT function. This function is intended for burst-mode operation where the duration of the on- and off-states are short.

9.6.1.1 Switching ON and OFF using SSHBC/EN

When a voltage is present at pin SUPHV or at pin SUPIC, a current from the SSHBC/EN pin will charge the external capacitor. If the pin is not pulled-down, this current will increase the voltage to 8.4 V. Since this is above the level to enable the operation of PFC (1.2 V) and PFC + HBC (2.2 V), the IC will be completely enabled.

The IC can be completely disabled by pulling down the SSHBC/EN pin below 1.2 V. The PFC controller will stop switching immediately, but the HBC will continue until the low-side stroke is active. The pull-down current must be larger than the current capability from the internal soft-start clamp: i.e. 42 μA.

PFC only active

By pulling the SSHBC/EN voltage below the enable PFC + HBC operation level (2.2 V), but keeping it above the enable PFC operating level (1.2 V), only the HBC is disabled. This can be used when there is another power converter connected to the boost voltage of the PFC. The low-side power switch of the HBC will be on when the HBC is disabled via the SSHBC/EN pin.

HBC only active

The TEA1713 is not designed to provide this operation mode but it can be realized by forcing a voltage higher than 2.63 V (but below 5 V) on SNSBOOST. This way the output overvoltage protection of the PFC will be activated and the PFC operation stopped (put on hold). The HBC will operate because SNSBOOST exceeds its start level of 2.3 V (boost UVP).

This mode of operation is not likely to be needed by an application, but it can be useful for starting up and debugging purpose during analyses or evaluation.

9.6.1.2 Hold and continue

The SNSOUT function can be used to start and stop the PFC and HBC. This method is intended for burst-mode operation to switch off the converters for only a short time. It is possible to operate only the HBC in burst-mode or both HBC + PFC simultaneously. The possibilities are similar to SSHBC/EN with the main difference being that HBC will continue without soft-start. For more details see Section 10.1 on burst mode operation.

9.6.2 Soft-start HBC

The soft-start function for the resonant converter is provided by SSHBC/EN.

The relation between switching frequency and output current/power is not constant. It is highly dependent on output and boost voltage and the relationship can be complex. To ensure that the resonant converter starts or restarts with safe currents, the TEA1713 has a soft-start function.

This soft-start function forces a start at high frequency so that currents are acceptable in all conditions. The soft-start slowly decreases the frequency until the output voltage regulation has taken over the frequency control. The limitation of the output current during start-up also limits the output voltage rise and prevents an overshoot.

During soft-start, in parallel to the soft-start frequency sweep, the SNSCURHBC function monitors the primary current and can activate regulation in case of a (temporary) overpower situation.

The soft-start uses the voltage at pin SSHBC/EN. The timing (duration) of the soft-start event is set by an external capacitor on SSHBC/EN.

As the SSHBC/EN is also used as enable input, the soft-start functionality is above the enable related voltage levels (see Figure 32).

9.6.2.1 Soft-start voltage levels

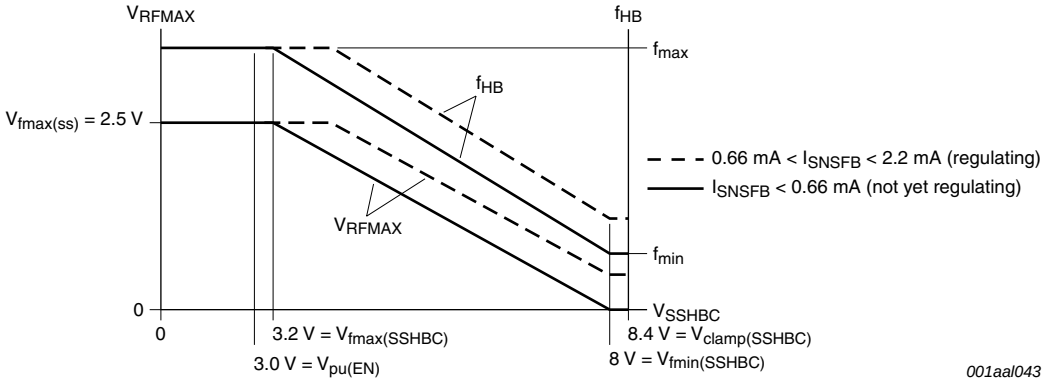


Fig 32. Operating frequencies related to SSHBC/EN voltage

At start-up, the SSHBC/EN voltage is low which corresponds to the maximum frequency. During the soft-start procedure, the external capacitor is charged, the SSHBC/EN voltage rises and the frequency decreases. The contribution of the soft-start function ends when SSHBC/EN is above 8 V.

The SSHBC/EN voltage is clamped at 8.4 V and will remain at that level during normal operation.

When the voltage on SSHBC/EN is reduced during protection or regulation, the voltage will be clamped at 3.0 V. This is to provide a quick response so that the operating frequency can be reduced again. Below 3.2 V the discharge current is reduced to 5 μA.

9.6.2.2 SSHBC/EN charge and discharge

Initially at start-up the soft-start external capacitor on SSHBC/EN is only charged to obtain a decreasing frequency sweep from maximum to operating frequency.

Besides the function to soft-start, SSHBC/EN is also used for regulation purposes such as overcurrent regulation. Therefore the voltage on the capacitor on SSHBC/EN can vary by charging and discharging it by internal current sources.

For example: in case of overcurrent regulation, a continuous alternation between charging and discharging of the SSHBC/EN capacitor occurs. The SSHBC/EN voltage can be regulated in this way, thereby overruling the signal on the feedback input SNSFB.

The (dis)charge current can have a high value ±160 μA or a low value ±40 μA. The two-speed soft-start sweep of the TEA1713 allows a combination of a short start-up time of the resonant converter and stable regulation loops such as overcurrent regulation.

In some cases there can be a situation where overcurrent regulation is activated during the soft-start sequence. This results in a feedback controlled or corrected soft-start.

The fast (dis)charge speed is used for the upper frequency range where VSSHBC/EN is below 5.6 V. In the upper frequency range the current and power in the converter do not react strongly to frequency variations.

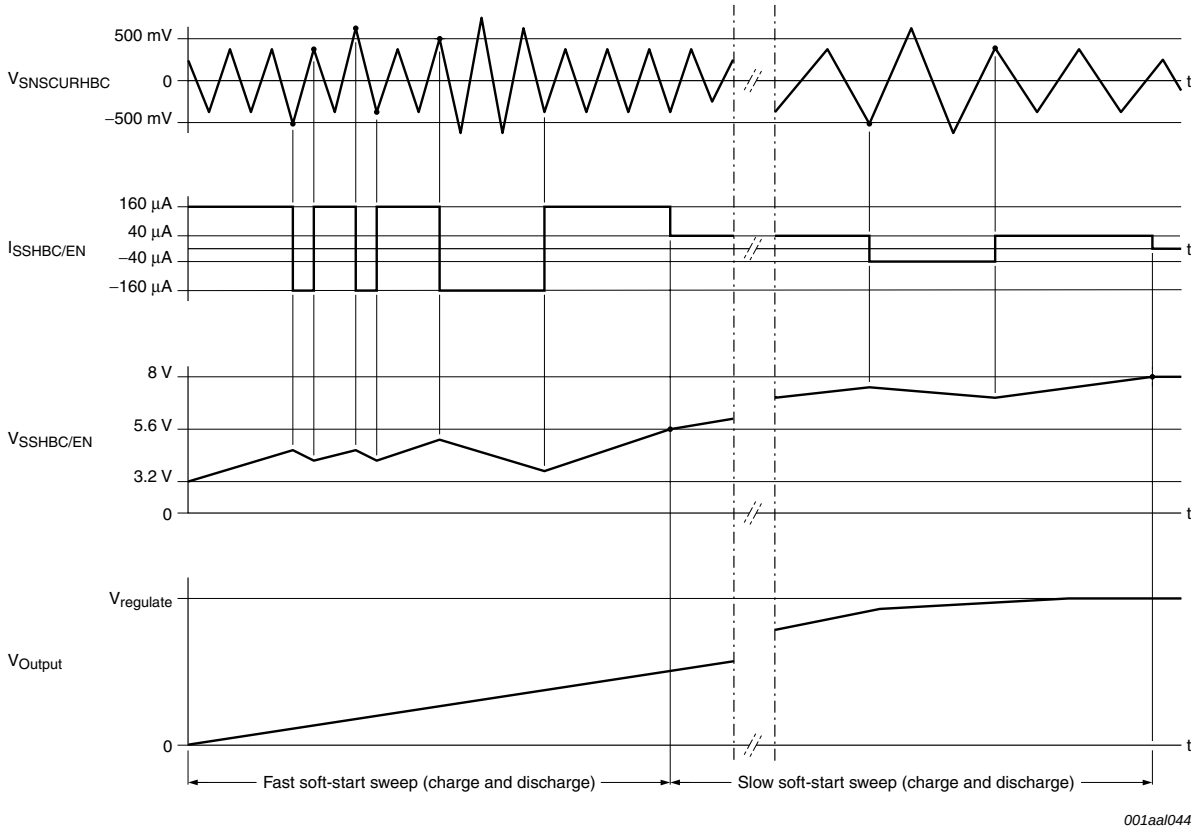


Fig 33. OverCurrent Regulation (OCR) during start-up

The slow (dis)charge speed is used for the lower frequency range where VSSHBC/EN is above 5.6 V. In the lower frequency range the current in the converter reacts strongly to frequency variations.

Burst mode

The soft-start capacitor is neither charged nor discharged during the no-operation time in burst mode operation. The soft-start voltage will not change during this time.

9.6.2.3 SNSFB, SSHBC/EN and soft-start reset - operating frequency control

The operating frequency can be controlled by the SNSFB and SSHBC/EN simultaneously. SSHBC/EN is dominant to provide protection and soft-start capability. Additionally, there is an internal soft-start reset mechanism that overrules both SNSFB and SSHBC/EN control inputs and immediately sets the frequency to maximum.

9.6.2.4 Soft-start reset

Some protection requires a fast correction of the operating frequency to the maximum value, but it is not needed to stop switching. The overcurrent protection is an example (see Table 4).

When this protection is activated, the control input of the oscillator is disconnected internally from the soft-start capacitor at pin SSHBC/EN and the switching frequency is immediately set to maximum. In most cases, the change to the maximum switching frequency will restore safe switching operation. Once the voltage at pin SSHBC/EN has reached 3.2 V, the control input of the oscillator reconnects to the pin and the normal soft-start sweep follows. Figure 34 shows the soft-start reset and the two-speed frequency downward sweep.

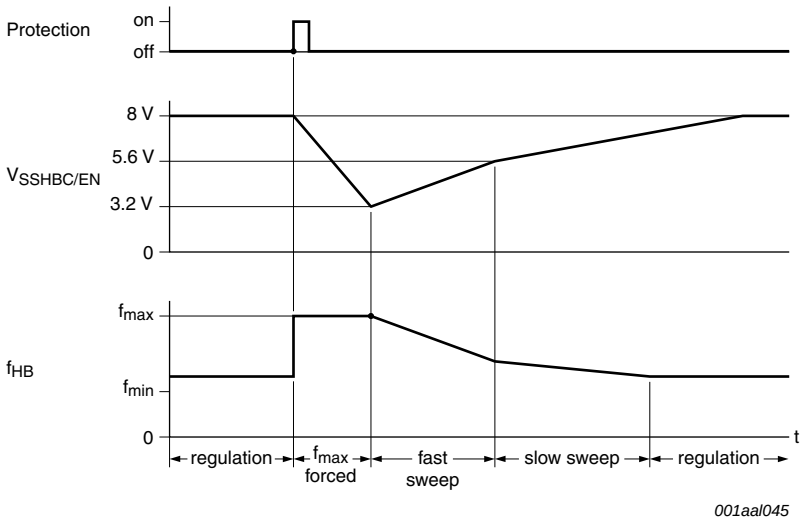


Fig 34. Soft-start reset and two-speed soft-start

The soft-start reset is also used to ensure a safe start-up at maximum frequency when the HBC is enabled by SSHBC/EN or after a restart. The soft-start reset is not used when the operation has been stopped for burst mode.

9.7 HBC overcurrent protection and regulation

Measurement of the primary resonant current indicates the level of output power that is being generated by the converter. In case of a fault or output overload condition, this current will often increase considerable. By monitoring this current and then taking appropriate action, the converter can remain operational during a temporary fault or overload condition.

The resonant controller of the TEA1713 has two functions when in an overcurrent condition:

1. OverCurrent Regulation (OCR) slowly increases the frequency and the protection timer is started.
2. OverCurrent Protection (OCP) steps to maximum frequency.

A boost voltage compensation function is included to reduce the variation in the preset protection level of the resonant current.

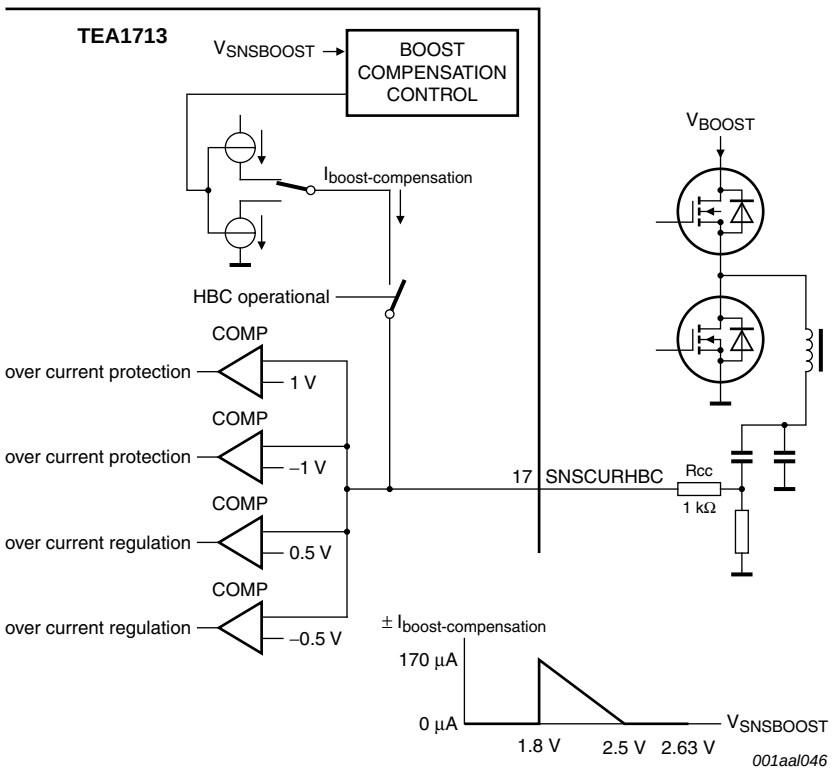


Fig 35. SNSCURHBC

9.7.1 HBC overcurrent regulation

The lowest comparator levels of ±0.5 V at the SNSCURHBC pin belong to the OverCurrent Regulation (OCR) level. There is a comparator for both the positive and negative polarity. If either level is exceeded, the frequency will be slowly increased. This is accomplished by discharging the soft-start capacitor. Every time the OCR level is exceeded, this state is latched until the next stroke and the soft-start discharge current is

enabled. When both the positive and negative OCR levels are exceeded, the soft-start discharge current will flow continuously. In this way the operating frequency is slowly increased until the resonant current value just reaches the value permitted by the preset.

The behavior during OCR can be observed on the SSHBC/EN pin as a resultant regulation voltage.

When an OCR situation is present for a long time, a serious fault condition is assumed. During OCR the protection timer is activated. The charging of the protection timer is active approximately a half period cycle after the ±0.5 V level is exceeded. If the detection levels are continuously exceeded, the timer will be charged continuously but, if the detection levels are only sometimes exceeded, the timer is charged accordingly (for details on charging/discharging of the protection timer refer to Section 11.3.3.4). The restart state is activated when RCPROT reaches the protection level of 4 V.

Start-up

The overcurrent regulation is very effective for limiting the output current during start-up. A smaller soft-start capacitor can be chosen which allows faster start-up. The small soft-start capacitor may sometimes result in an excessive output current but the OCR function can slow down the frequency sweep to keep the output current within the limits.

9.7.2 HBC overcurrent protection

In most cases the OverCurrent Regulation is able to keep the current below the set maximum values. For certain error conditions however, the OCR might not be fast enough to limit the current. To protect against those error conditions the OverCurrent Protection (OCP) is implemented.

The internal OCP level is set at ±1 V for SNSCURHBC. This is significantly higher than the OCR level of ±0.5 V. When the OCP level is reached the frequency will immediately jump to the maximum via a soft-start reset procedure, followed by a normal sweep down.

The maximum frequency value for soft-start must be chosen in order to sufficiently limit the output power under these conditions.

The behavior during OCP can be observed on the SSHBC/EN pin as a new soft-start. Depending on the (over)load or fault condition during this new soft-start, OCR or OCP can be reactivated.

9.7.3 SNSCURHBC boost voltage compensation

The primary current, also called resonant current, is sensed via pin SNSCURHBC. It senses the momentary voltage across an external current sense resistor. The use of the momentary current signal allows a fast OverCurrent Protection and simplifies the stability of the OverCurrent Regulation. The OCR and OCP comparators compare the SNSCURHBC voltage to the maximum positive and negative values.

For the same output power, the primary current is higher when the boost voltage is low. To reduce the dependency of the protected output current level for the boost voltage, a boost compensation is included. The boost compensation sources and sinks a current from the SNSCURHBC pin. This current creates a voltage drop across the series resistor Rcc. A typical value for this resistor is 1 kΩ.

The amplitude of the current depends linearly on the boost voltage. At nominal boost voltage the current is zero and the voltage across the current sense resistor is also present at the SNSCURHBC pin. At the boost start level SNSBOOST = 1.8 V and the current is maximum 170 μA. The direction of the current, sink or source, depends on the active gate signal. The voltage drop created across Rcc reduces the voltage amplitude at the pin, resulting in a higher effective current protection level. The amount of compensation is set by the value of Rcc.

9.7.4 Current measurement circuits

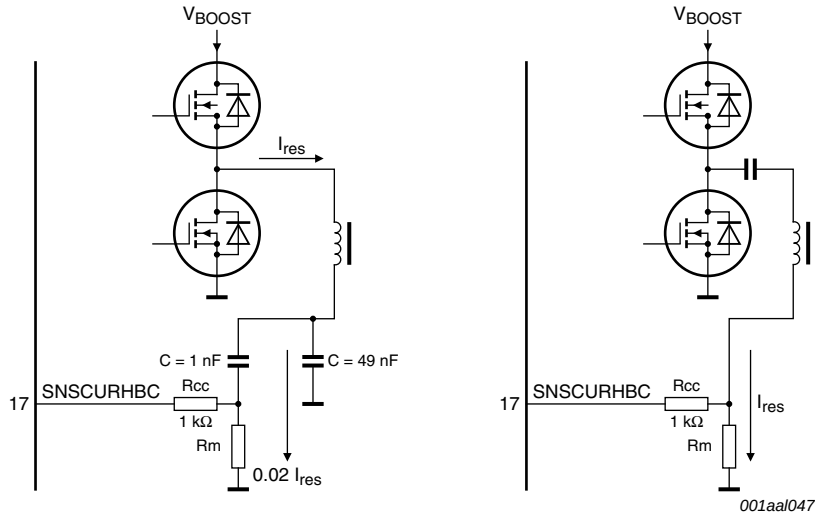


Fig 36. SNSCURHBC: resonant current measurement configurations

9.7.5 SNSCURHBC layout

Because the SNSCURHBC must be able to accurately sense the measurement signal cycle-by-cycle at higher frequencies, it is rather susceptible to disturbances. To prevent disturbances on this input, the series resistor Rcc should be placed close to the IC in order to reduce the length of the track that can pick up disturbing signals. As the impedance of the measurement resistor is normally low, the signal track between Rcc and the measurement resistor is not critical regarding disturbance.

10. Burst mode operation

Burst mode operation can be used to improve the efficiency at low output loads.

By temporarily interrupting the switching, losses during idle time are minimized. Because the average power needed for the output is very low, it is easy for the converter to deliver it during a short conversion time (a burst).

The burst mode operation of the TEA1713 is based on interrupting the switching while maintaining regulation. With an external comparator, the regulation voltage can be monitored to determine if it should stop switching and then continue. Stopping and starting again can be controlled via the SNSOUT pin. When starting again after interruption, no soft-start is applied as the system is still in regulation (close to the regular working point). The timing of switching on and off is determined by the regulation-loop of the system (normally by the output voltage). In this way, a small ripple on the output voltage is deliberately created during burst mode.

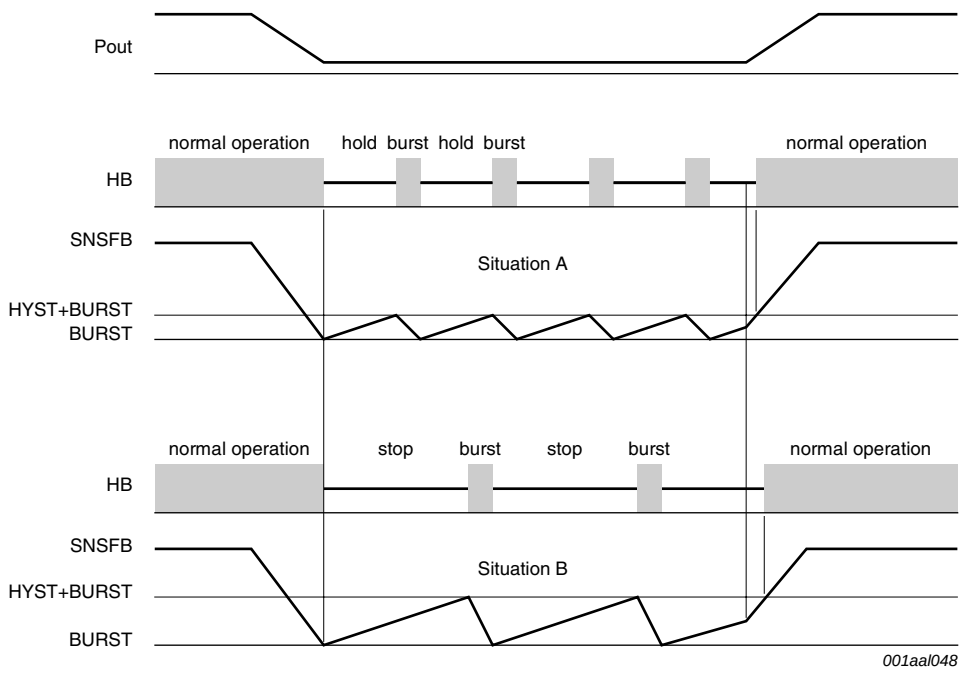


Fig 37. Principle of burst mode operation with SNSFB and comparator levels

10.1 Burst mode controlled by SNSOUT

The HBC and the PFC of the TEA1713 can be operated in burst mode. In burst mode the converters operate for a limited time, followed by a period of non-operation. Burst mode operation increases the efficiency during low load conditions.

A simple external circuit that uses the information from the feedback loop can detect the low load condition. To pause the operation of the TEA1713 for a burst off-time, the detection circuit will pull down the SNSOUT pin.

SNSOUT has two levels for burst mode operation:

1. Burst-off level for HBC = 1.1 V. Below this level, only the HBC will pause its operation. Both high-side and low-side power switches will be off and the PFC continues full operation. Above this level the HBC resumes operation and it will not execute a soft-start sequence.
2. Burst-off level for PFC = 0.4 V. Below this level, the PFC will also pause its operation via a soft-stop. The HBC will already be paused. Above this level the PFC resumes operation with a soft-start.

To avoid burst mode activation when the output voltage is not yet present, a current (100 μA) from the SNSOUT pin will keep the voltage at an internal clamp voltage of 1.5 V, which is above both burst mode levels. The impedance between the SNSOUT pin and ground should therefore be larger than 20 kΩ.

10.2 External comparator for burst mode implementation

Implementation of the burst mode can be done by a comparator circuit between SNSFB and SNSOUT.

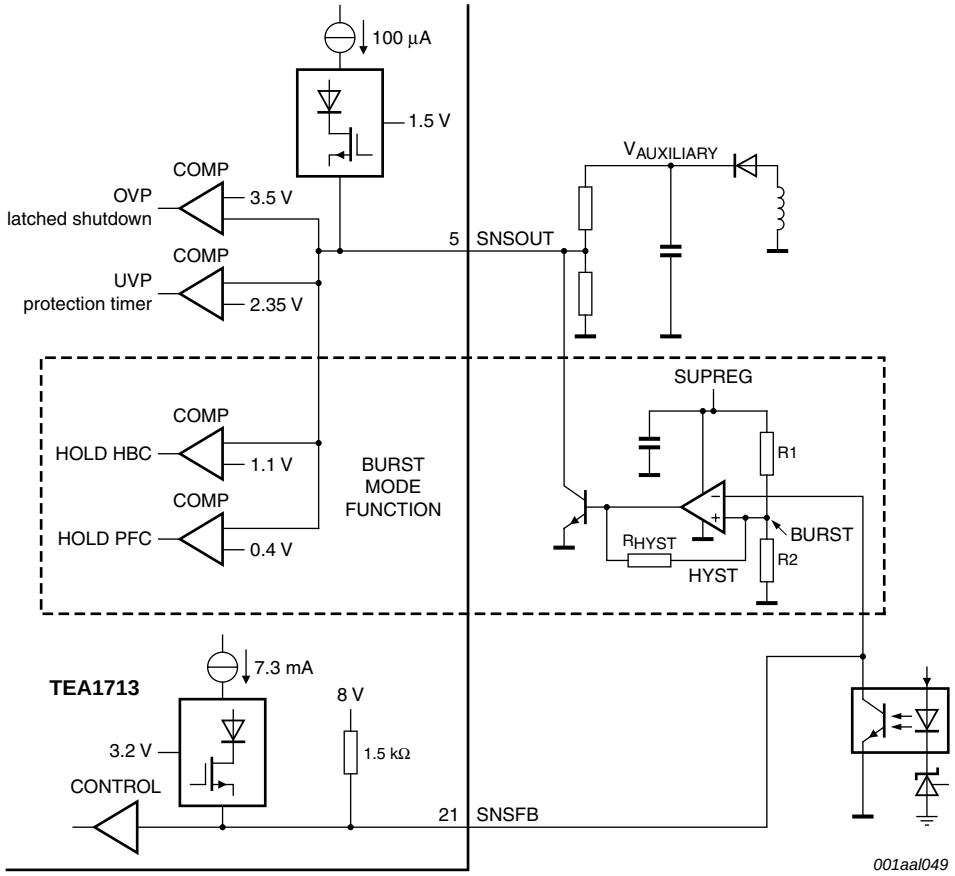


Fig 38. Principle of burst mode operation with SNSFB and comparator levels

The comparator input monitors the regulation voltage SNSFB to a preset burst voltage value by R1 and R2: BURST. When the HBC power output power is low, the regulation voltage decreases and when it reaches BURST the switching stops by switching SNSOUT to ground. When the switching stops, no energy is converted and the output voltage will drop. The regulation voltage will then increase again. As soon as the regulation voltage reaches BURST + HYST (voltage hysteresis set by R_{HYST}) the switching resumes.

When the power delivered during a burst is larger than needed for the output, the regulation voltage SNSFB quickly decreases, stopping the switching at BURST. The time needed for the regulation voltage to reach BURST, is mainly dependent on the output voltage and its load.

When the HBC output load increases to high levels, normal operation is resumed as the regulation voltage can no longer reach the BURST level.

10.3 Advantages of burst mode for HBC

The main reason of applying burst mode in a resonant converter is to improve the efficiency at low output power by reducing the power losses.

The graphs in Figure 39 and Figure 40 show the improvement principle in an example of a 250 W resonant converter including (non-bursting) PFC.

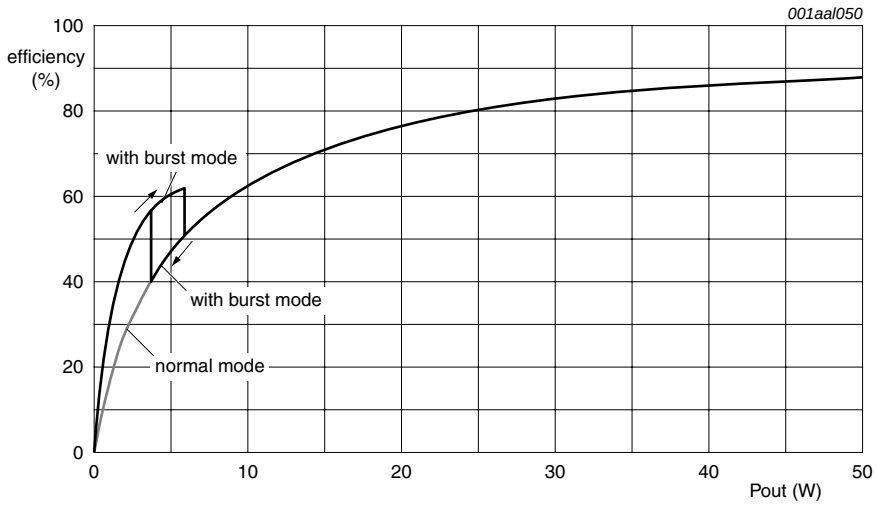


Fig 39. Improved efficiency by HBC burst mode in a 250 W converter

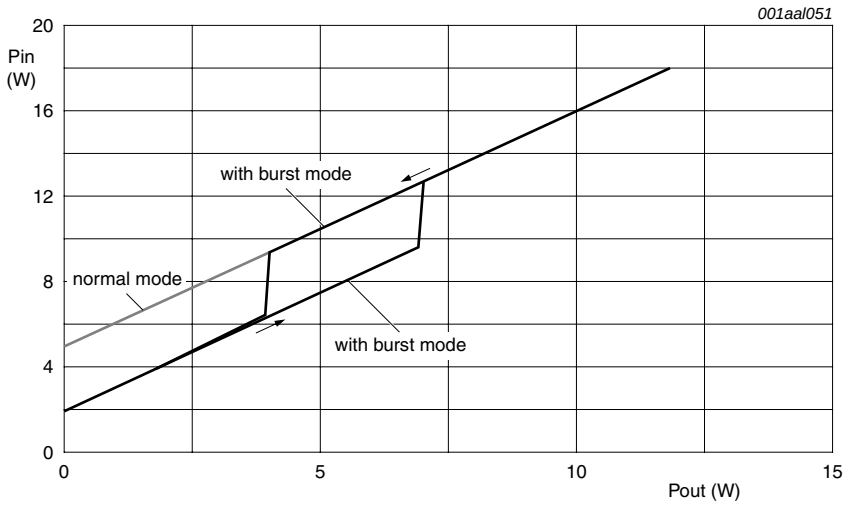


Fig 40. Reduced losses by HBC burst mode in a 250 W converter

10.4 Advantages of burst mode for HBC and PFC simultaneously

The TEA1713 provides a burst mode system that simultaneously switches the HBC and PFC. In this way, during the burst period, the power is transferred directly from the input to the output. The HBC determines the repetition time of the burst and the PFC follows. In the burst period, the PFC operates in normal regulation.

Extra reduction in power consumption is obtained by PFC bursting. Examples of results obtained are provided by Figure 41, Figure 42 and Figure 43.

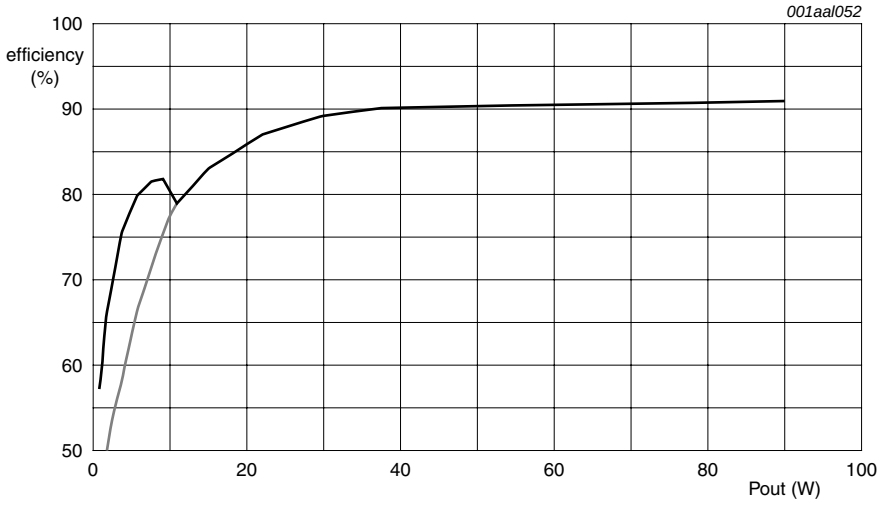


Fig 41. Increased efficiency at low output power in burst HBC and PFC (90 W adapter)

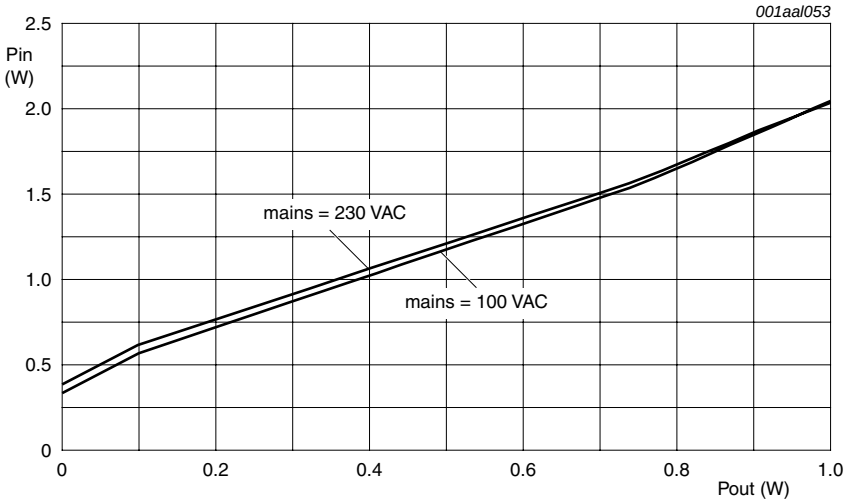


Fig 42. Remaining 90 W adapter losses in burst mode

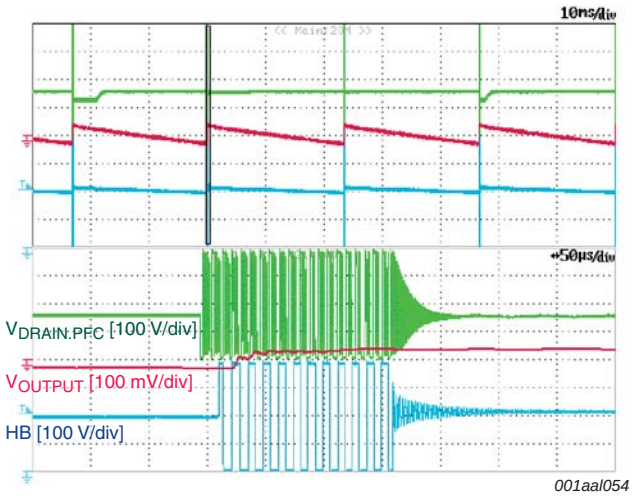


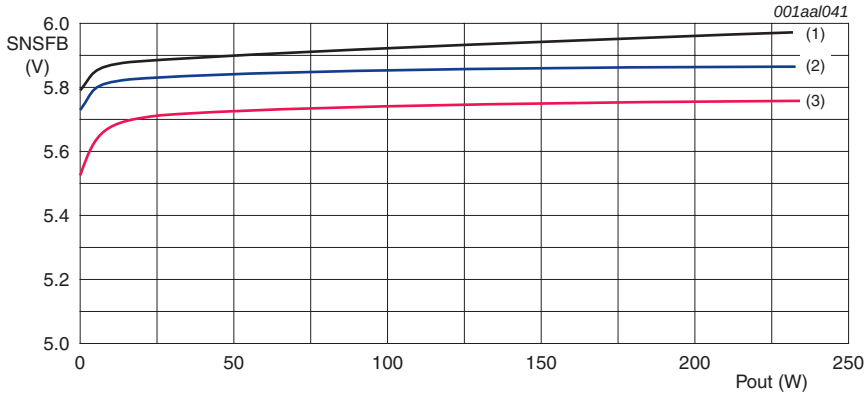
Fig 43. Simultaneous HBC and PFC burst mode operation (including output voltage ripple)

10.5 Choice of burst level and hysteresis level

For dimensioning the burst mode, the power levels for bursting must be set by an external comparator. A typical comparator circuit with hysteresis is given in Figure 38.

The basic choice for the voltage level at which the comparator must be active (BURST) can be made experimentally.

It is important to realize that the relationship between the HBC output power level and the SNSFB regulation voltage is strongly influenced by the input voltage of the resonant converter V_{boost} (see Figure 45)



1. V_{BOOST} = 310 V DC
2. V_{BOOST} = 350 V DC
3. V_{BOOST} = 390 V DC

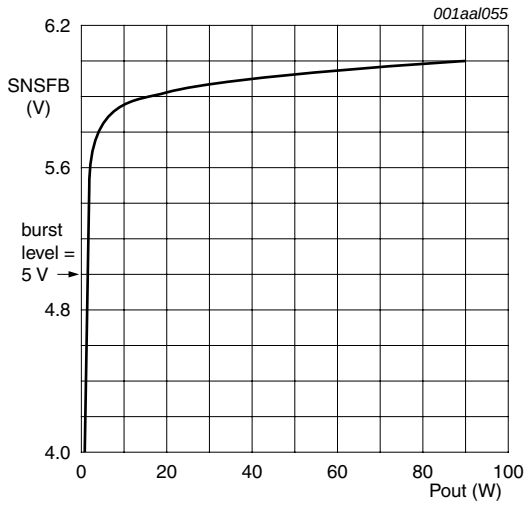
Fig 44. SNSFB voltage to output power characteristics examples

Aspects that influence the voltage levels (BURST and HYST) of burst mode:

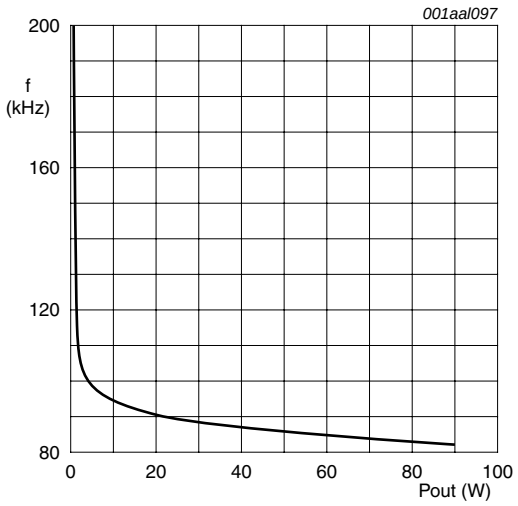
- Input voltage V_{boost}.
- SNSFB voltage regulation levels in combination with the preset frequency range of RFMAX and CFMIN.
- Dynamic behavior of the regulation during burst mode and during normal operation (large load variations).

10.6 Output power - operating frequency characteristics

As can be concluded from Figure 45, it is critical to make a design choice for a certain SNSFB voltage to start bursting. With this kind of characteristic there is a risk that, due to spread, the system can either remain in burst mode or never reach burst-mode operation at all. The dimensioning of the LLC can be made more suitable for burst mode. The standard approach is to design the system in such a way that it cannot regulate to no-load, even at the highest frequency. During the lowest loads, the frequency required for regulation must become infinite. A voltage level can then easily be chosen to ensure that burst mode will be activated at the lowest load and that the remaining load conditions will operate in normal mode. The burst mode will now enable the system to operate at no-load.



SNSFB - output power



Frequency - output power

Fig 45. Normal mode output power characteristics (Adapted for easy implementation of burst mode comparator level detection)

10.7 Lower SUPHS in burst

During the idle time SUPHS is not charged.

During normal operation, each time the half-bridge node HB is switched to ground level, the SUPHS capacitor is charged by the bootstrap function of the external diode between SUPHS and SUPREG. In burst mode there will be periods of non-switching, and therefore no charging of SUPHS. During this time, the circuit supplied by SUPHS will slowly discharge the supply voltage capacitor. At the moment a new burst starts, the SUPHS voltage will be lower than in normal operation. During the first switching cycles, the SUPHS will be re-charged to its normal level. It is important that, during these first recharge cycles, SUPREG does not drop below the protection level of 10.3 V.

10.8 Audible noise

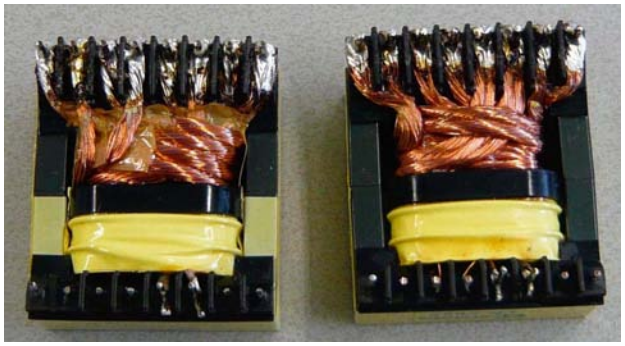
Because the burst mode is normally used when the output power is low, the converted energy will not contribute much to generate audible noise. The magnetization current however is still present during low loads and is the dominant energy during burst mode. Switching the converter sequences on and off continuously at a certain speed and duration can lead to audible noise. The main mechanism for producing noise is the interruption of magnetization current sequences leading to a mechanical force. This is especially the case on the core of the resonant transformer which starts acting as a loudspeaker.

When burst mode is applied during higher output power conditions, the converted energy also contributes and will lead to an increased risk of audible noise.

10.8.1 Measurements in the resonant transformer construction

To prevent problems with audible noise under specific conditions, it is necessary to adapt the mechanical transformer construction.

One measure is to adhere the core parts to each other using a material with damping (vibration absorbing) properties. A combination can be made with the air gap construction. Other vibration damping measures can also help when audible noise is a critical issue for a product.



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(1) Left-hand transformer with glue to reduce audible noise
(2) Right-hand transformer has standard construction

Fig 46. Transformer construction

10.8.2 Burst power dependent noise level

The amount of audible noise is strongly related to the amount of energy in each burst.

At low output power, the amount of energy is mainly determined by the magnetization current of the resonant converter. The amount of transferred energy is low. To avoid problems with audible noise, the burst mode should only be used at low power (a few watts output power). When the transition level between normal mode and burst mode is chosen at a higher output power, the level of audible noise will be larger.

Overshoot on feedback voltage

When the output load is increased, the system will revert to normal operation. The transition from burst mode to normal mode is based on the feedback voltage. In certain burst conditions the feedback voltage can overshoot, thereby keeping the system in burst mode at higher output power levels than intended. As the power level in this situation is larger, the amount of noise will also be larger.

10.9 PFC converter and resonant converter simultaneous bursting

When in the burst mode, PFC operation will stop during the time that the resonant converter is not switching. In most cases this will save extra energy consumption by reduced switching losses from the PFC converter.

The behavior of the total system (PFC and resonant) in burst mode may differ from the situation when only the resonant converter would operate in burst mode. Although this will result in good performance, there will be a number of interactions.

10.9.1 PFC output voltage variations

When bursting the PFC converter, the resonant control system determines the timing. This may result in a situation that the PFC cannot maintain a constant output voltage. The time during which the PFC can convert power is limited by the HBC operation and may be too short. The result will be either a lower or a varying output voltage. This also has consequences for the resonant converter as its input voltage is not the same. The working conditions change towards a new balance.

The resonant converter must be able to remain operational during these conditions.

It is important to check that the resonant controller has not been stopped because the input voltage provided by SNSBOOST is too low. This may cause an unacceptable voltage decrease in the output of the resonant converter.

10.9.2 PFC burst duration

Normally a square SNSOUT pulse leads to equal operation time for PFC and HBC (see Figure 43). If a longer PFC operating time is needed for correct balance, it can be achieved by adding a capacitor on SNSOUT to create a ramp signal. As the PFC starts at a voltage of 0.4 V, this will allow a longer PFC operating time.

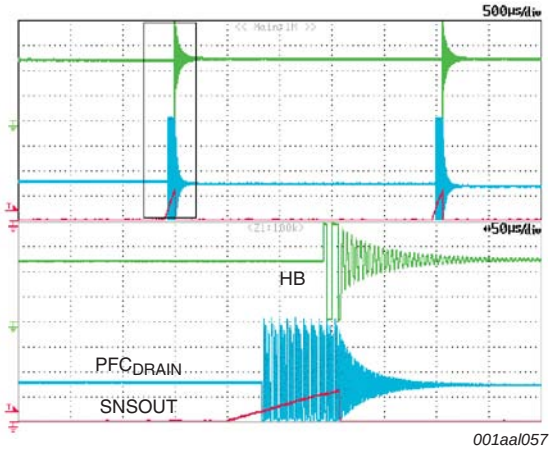

Fig 47. Example of longer burst time for PFC using ramp on SNSOUT

10.9.3 Switching between burst and normal operation

Interaction between the PFC converter and resonant converter in the burst mode can lead to a situation where the system alternates between burst mode and normal mode for certain output power conditions.

10.9.4 Audible noise during mode transition

As a result of the previously mentioned interactions, a stable situation can occur during the following operating modes, alternating in time:

- Resonant burst with short burst time without PFC burst (time too short to start).
- Resonant burst with long burst time and PFC burst.
- Normal operation for resonant and PFC bursts.

Transitions between modes and variations within a certain mode have a corresponding effect on audible noise.

10.10 Design guideline for burst mode operation

Design for a stable PFC (nominal) output voltage during burst mode.

Best efficiency is achieved when the number of cycles for each burst is as small as possible (only a few cycles).

Best efficiency is achieved by resistively tuning the comparator circuit to preset the SNSFB burst level and hysteresis.

System and component tolerances play a significant role in variations of performance in production.

The regulation feedback loop can be optimized for normal mode and any additional filtering can be done in the comparator circuit. However, this should be used moderately so that control of the situation can be maintained during burst mode operation.

10.11 Enable/disable burst mode

In micro-controller operated applications such as TV, a clear separation is made between normal operation and standby operation. To avoid the resonant converter going into burst during short periods of low load during normal operation, an enable/disable function can be added. This can be implemented by an extra enable/disable switch function in the comparator circuit.

10.12 Unused burst mode

When the burst mode is not required, it can be accommodated by not applying a circuit to switch SNSOUT thereby leaving the burst mode function inactive.

11. Protection functions

Most protection functions are discussed in the chapters of the systems of which they are a part. In the overview of Table 4, links are given to the corresponding places in this document. In the following paragraphs the remaining, more independent, protection functions are discussed.

11.1 Protection overview

Table 4. Overview of protection functions with links

Part	Symbol	Protection	Action	Link
IC	UVP-SUPIC	Under Voltage Protection	SUPIC IC disable	6.2.2
IC	UVP-SUPREG	Under Voltage Protection SUPREG	IC disable	6.5
IC	UVP supplies	Under Voltage Protection supplies	IC disable and reset	-
IC	SPC-SUPIC	Short Circuit Protection SUPIC	low HV start-up current	6.2.2
IC	OVP output	OverVoltage Protection output	IC shutdown	11.3.1
IC	UVP output	Under Voltage Protection output	IC restart after protection time	11.3.2
IC	OTP	Over-Temperature Protection	IC disable	11.2.1
PFC	OCR-PFC	OverCurrent Regulation PFC	PFC switch-off cycle-by-cycle	8.4
PFC	UVP-mains	UnderVoltage Protection mains	PFC hold switching	8.6.1
PFC	OVP-boost	OverVoltage Protection boost	PFC hold switching	8.5
PFC	SCP-boost	Short-Circuit Protection boost	IC restart	8.2.2
HBC	UVP-boost	UnderVoltage Protection boost	HBC disable	9.1
HBC	OLP-HBC	Open-loop protection HBC	IC restart after protection time	9.5.1
HBC	HFP-HBC	High Frequency Protection HBC	IC restart after protection time	9.4.4
HBC	OCR-HBC	OverCurrent Regulation HBC	HBC frequency increase IC restart after protection time	9.7.1
HBC	OCP-HBC	OverCurrent Protection HBC	HBC step to maximum frequency	9.7.2
HBC	CMR	Capacitive Mode Regulation	HBC increase frequency	9.3.2
HBC	ANO	Adaptive non-overlap	HBC prevent hazardous switching	9.3.1

11.2 IC protection

11.2.1 Over Temperature Protection (OTP)

The TEA1713 contains an accurate internal Over-Temperature Protection (OTP). When the junction temperature exceeds the over-temperature level of 140 °C, the IC will go to the Thermal hold state. The Thermal hold state is left as soon as the temperature has dropped by 10 °C.

The circuit will resume operation with a complete restart including a soft-start of PFC and HBC.

11.2.2 Latched protection

Only an overvoltage detection on SNSOUT leads to a latched shutdown protection state. To enter a latched shutdown state, the voltage on SNSOUT must exceed 3.5 V.

Resetting a latched protection shutdown state

When a latched protection shutdown state has occurred this state will be reset by one of the following actions:

1. SUPIC drops below 7 V **and** SUPHV is lower than 7 V.
2. SNSMAINS drops below 0.8 V and then rises above 0.85 V.
3. SSHBC/EN is pulled below 1.2 V (PFC enable level).

In most cases, a reset by the SNSMAINS voltage will be activated before a reset by SUPIC/SUPHV. This enables a restart before the V_{boost} voltage is discharged (fast shutdown reset).

When resetting by interrupting the mains input, some time is still needed to lower the SNSMAINS voltage below 0.8 V. The time depends on the component values used on the SNSMAINS circuit and the value of the mains voltage. An additional aspect is a possible leakage of the bridge rectifiers that allows the charging of SNSMAINS by the rectified mains voltage capacitor (reverse current through the diodes). At moderate rectifier temperature this may be neglected but at high temperature this is a significant parameter.

A reset possibility by external control (for example micro-controller) is available using the SSHBC/EN function.

11.3 SNSOUT protection

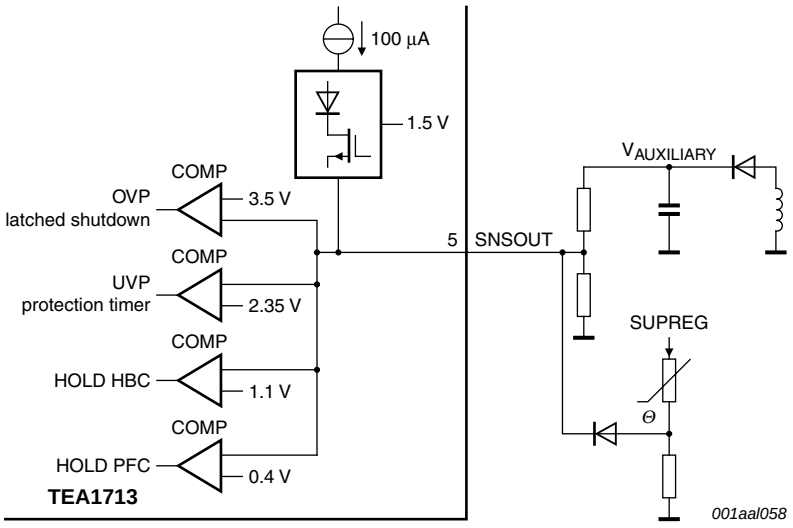

Fig 48. SNSOUT protection

11.3.1 OverVoltage Protection (OVP) output

The TEA1713 has an overvoltage protection intended for monitoring the HBC output voltage. It is one of the functions that is combined on the SNSOUT pin.

11.3.1.1 Auxiliary winding

When dealing with a mains insulated converter, the HBC output voltage can be measured via the auxiliary winding of the resonant transformer. To accurately measure the secondary voltage of the primary circuit auxiliary winding, a special transformer construction is needed.

To facilitate correct working, it is important that this winding has a good coupling with the secondary winding(s) and a minimum coupling with the primary winding. In this way, a good representation of the output voltage situation is obtained. For more details refer to Section 6.3.3.1 and Figure 6.

To meet the mains insulation requirements, triple insulated wire can be used.

11.3.1.2 Principle of operation

The voltage is sensed at the SNSOUT pin via an external rectifier and resistive divider. Overvoltage is detected when the SNSOUT voltage exceeds 3.5 V. After detecting OVP the TEA1713 will go to the latched protection shutdown state.

11.3.1.3 Connecting external measurement circuits

When latched protection is needed for other detection circuits, it can be added to SNSOUT by means of a series diode.

11.3.2 Under Voltage Protection (UVP) output

The TEA1713 has an undervoltage protection intended for monitoring the HBC output voltage. It is one of the functions that is combined on the SNSOUT pin.

11.3.2.1 Auxiliary winding

When dealing with a mains insulated converter, the HBC output voltage can be measured via the auxiliary winding of the resonant transformer. To accurately measure the secondary voltage of the primary circuit auxiliary winding, a special transformer construction is needed.

To facilitate correct working, it is important that this winding has a good coupling with the secondary winding(s) and a minimum coupling with the primary winding. This is to obtain a good representation of the output voltage situation. For more details refer to section 6.3.3.1 and Figure 6.

To meet the mains insulation requirements, triple insulated wire can be used.

11.3.2.2 Principle of operation

The voltage is sensed at the SNSOUT pin via an external rectifier and resistive divider. Undervoltage is detected when the SNSOUT voltage drops below 2.35 V. When detecting UVP the TEA1713 will start the protection timer by charging it with 100 μA.

When the undervoltage state remains until the timer reaches the protection level, the controller will stop and then be re-started by the restart timer.

At start-up, the SNSOUT voltage will normally start at a level lower than 2.35 V. To prevent undesired protection during start-up, the timer setting should allow sufficient time for start-up to charge the SNSOUT voltage to a value above 2.35 V.

In applications where the TEA1713 is supplied from an auxiliary winding (to SUPIC), the SUPIC monitoring can also activate a protection when an error condition results in a drop of the output voltage. See chapter 6.2.2.

11.3.2.3 Severe voltage drop

When the voltage on SNSOUT drops to a very low voltage, the HBC and PFC are stopped by the Hold HBC and Hold PFC functions on this input pin.

11.3.2.4 Connecting external measurement circuits

When restart protection is needed for other detection circuits, it can be added on SNSOUT by means of a series diode.

11.3.3 OVP and UVP combinations

11.3.3.1 Circuit configurations

The following list contains examples of configurations for which certain functionality on the SNSOUT pin is disabled.

- OVP functional and UVP disabled (refer to section 11.3.3.2)
- UVP functional and OVP disabled (refer to section 11.3.3.3)
- Both OVP and UVP disabled (refer to section 11.3.3.4)

Note that in the examples given, burst mode operation can still be implemented independent of the UVP and/or OVP functionality.

11.3.3.2 OVP functional and UVP disabled

In some applications it may be required to prevent the activation of the Under Voltage Protection on SNSOUT. To achieve this, it is necessary to disable UVP. This can be realized by adding a circuit that will prevent the voltage on SNSOUT from dropping below 2.35 V.

Practical example

The voltage on SNSOUT can be prevented from dropping below a preset voltage by externally adding a low impedance resistive divider, with a fixed voltage, and connecting it to SNSOUT via a diode. This simple circuit is not very accurate but it does provide the basic capability to disable the UVP function of SNSOUT. Note that for higher voltage values on SNSOUT, the diode is blocking so that the OverVoltage Protection is still functional.

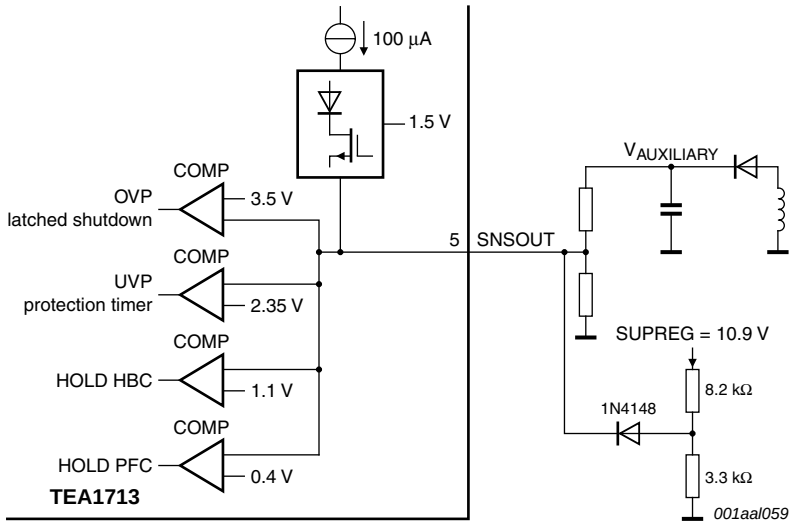

Fig 49. Example of disabling the UVP function of SNSOUT

11.3.3.3 UVP functional and OVP disabled

In some applications it may be required to prevent the activation of the overvoltage protection on SNSOUT. To achieve this, it is necessary to disable OVP. This can be realized by adding a circuit that will prevent the voltage on SNSOUT from exceeding 3.5 V.

Practical example

The voltage on SNSOUT can be prevented from exceeding the preset voltage by externally adding a low impedance resistive divider, with a fixed voltage, and connecting it to SNSOUT via a diode. This simple circuit is not very accurate but it does provide the basic capability to disable the OVP function of SNSOUT. Note that for lower voltage values on SNSOUT, the diode is blocking so that the Under Voltage Protection is still functional.

Another possibility is to add a zener diode function on SNSOUT to limit the voltage on this pin.

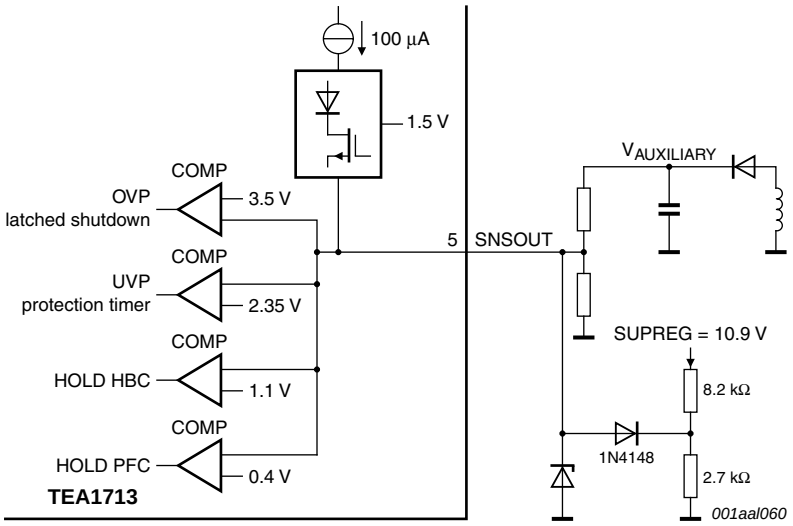

Fig 50. Example of disabling the OVP function of SNSOUT

11.3.3.4 Both OVP and UVP disabled

When neither OVP or UVP functionality is required, a fixed voltage between 2.35 V and 3.5 V can be applied to SNSOUT. This can be obtained from a resistive divider that is referenced to the SUPREG.

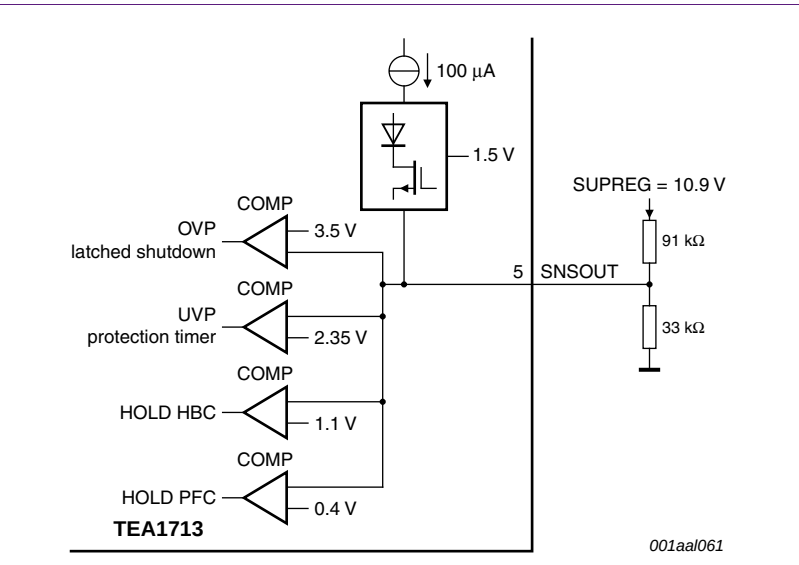

Fig 51. Example of disabling both the UVP and the OVP functions of SNSOUT

11.4 Protection timer

The TEA1713 has a programmable timer that is used for the timing of several forms of protection. The timer is basically used in two ways:

- As a protection timer.
- As a restart timer.

The values for both types of timer can be independently preset by an external resistor and capacitor connected to RCPROT.

11.4.1 Block diagram of the RCPROT function

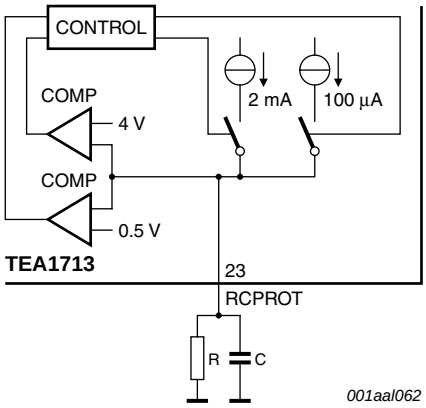

Fig 52. Block diagram of the RCPROT function

11.4.2 RCPROT working as protection timer

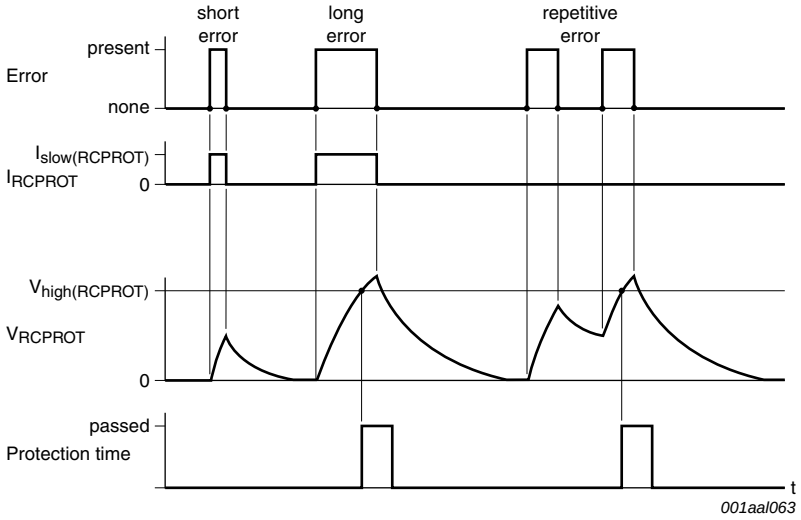

Fig 53. RCPROT protection timer operation

Figure 53 demonstrates the operation of the protection timer. When an error condition occurs, a fixed current of 100 μA flows from the RCPROT pin and charges the external capacitor. The voltage will rise exponentially due to the external resistor. The protection time is passed when the upper switching level of 4 V has been reached. At that moment, the appropriate protective action will be executed, the current source is stopped and RCPROT will be discharged by the external resistor.

In the case where the error condition ends before 4 V has been reached, the current source will be stopped and the pin will discharge through the external resistor and no further action will be taken.

If the error condition is permanent, the system will fluctuate between stop and restart.

The protection timer is activated by one of the following:

1. OverCurrent Regulation SNSCURHBC.
2. High Frequency Protection RFMAX.
3. Open Loop Protection SNSFB.
4. Under Voltage Protection SNSOUT.

It is allowed to force the activation of protection (and restart) by increasing the RCPROT voltage to above the 4 V (but no higher than +12 V) using an external circuit.

11.4.3 RCPROT utilized as a restart timer

During certain error conditions, it may be desirable to temporarily disable the IC. This is especially useful when an error can overheat components. A temporary disable will allow power supply components to cool down, after which the IC must automatically restart. The time to restart is determined by the restart timer.

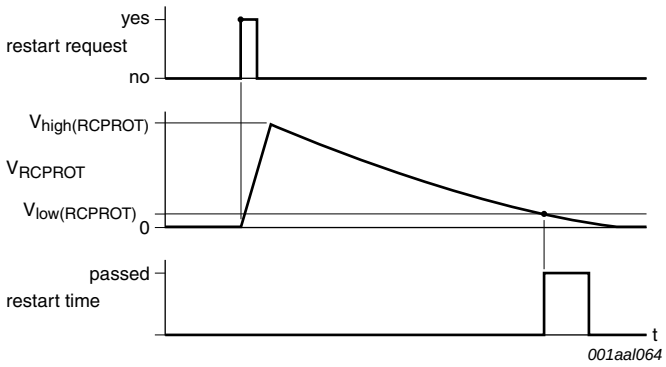

Fig 54. RCPROT operating as a restart timer

Normally, the capacitor is discharged to 0 V but when a restart is requested, the external capacitor is quickly charged by a current of 2.2 mA until it reaches the upper switching level of 4 V. After this, the RCPROT pin becomes high ohmic and the external resistor will discharge the external capacitor. The restart time is exceeded when the lower switching level of 0.5 V has been reached. At that moment, the IC will be restarted and the RCPROT pin will be further discharged. This condition is only activated in the case of short-circuit protection of the SNSBOOST.

11.4.4 Dimensioning the timer function

The required restart time $t_{restart}$ determines the time constant t_{RCPROT} made by the values of R and C.

$$t_{RCPROT} = \frac{-t_{restart}}{1n\left\langle \frac{V_{low(RCPROT)}}{V_{high(RCPROT)}} \right\rangle} = \frac{-t_{restart}}{1n\left\langle \frac{0.5}{4} \right\rangle} = 0.48 \times t_{restart} \quad (36)$$

With this time constant and the required protection time $t_{protection}$, the value of R and C can be calculated as follows:

$$R = \frac{V_{high(RCPROT)}}{I_{slow(RCPROT)} \times \left\langle 1 - e^{-\frac{t_{protection}}{t_{RCPROT}}} \right\rangle} = \frac{4}{100\ \mu A \times \left\langle 1 - e^{-\frac{t_{protection}}{t_{RCPROT}}} \right\rangle} \quad (37)$$

$$C = \frac{t_{RCPROT}}{R} \quad (38)$$

Example

$t_{restart}$ = 500 ms;

$t_{protection}$ = 30 ms;

t_{RCPROT} = 240 ms;

R = 341 kΩ;

C = 705 nF.

12. Miscellaneous advice and tips

12.1 PCB layout

12.1.1 General setup

The TEA1713 contains two largely independent converter controllers in one package. General advice is to physically separate the PFC and HBC circuits on the PCB to avoid mutual interference.

12.1.2 Grounding

SGND + PGND **must** be connected directly under the IC (on the ground plane if possible) to avoid false signal detection by driver current disturbance (see Figure 57).

A star grounding construction provides the lowest risk of mutual converter disturbance or signal detection disturbance. In this system, the central star point can be chosen at the V_{boost} capacitor ground.

High currents should be avoided on grounding tracks that are meant for signal measurement.

12.1.3 Current loops

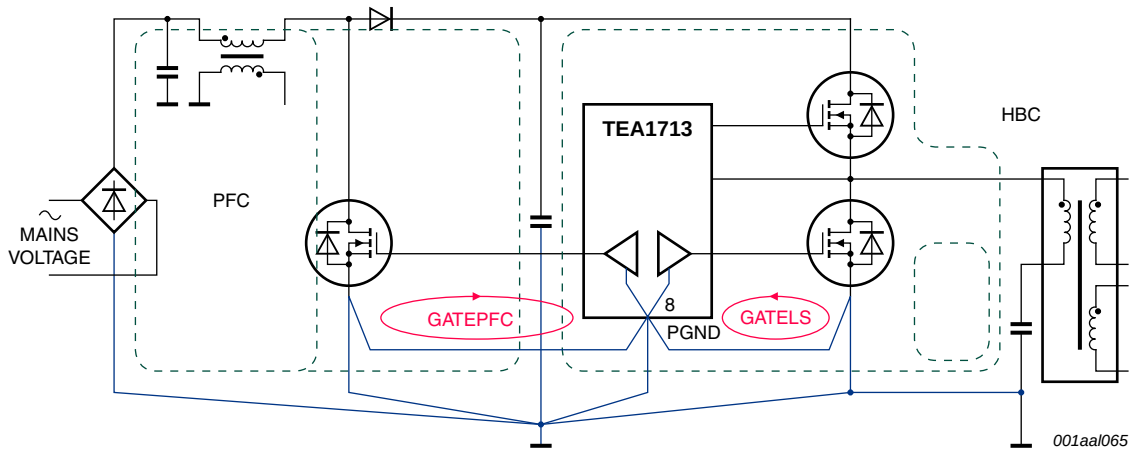

Fig 55. Grounding structure and current loops GATEPFC and GATELS

12.1.4 Grounding layout example

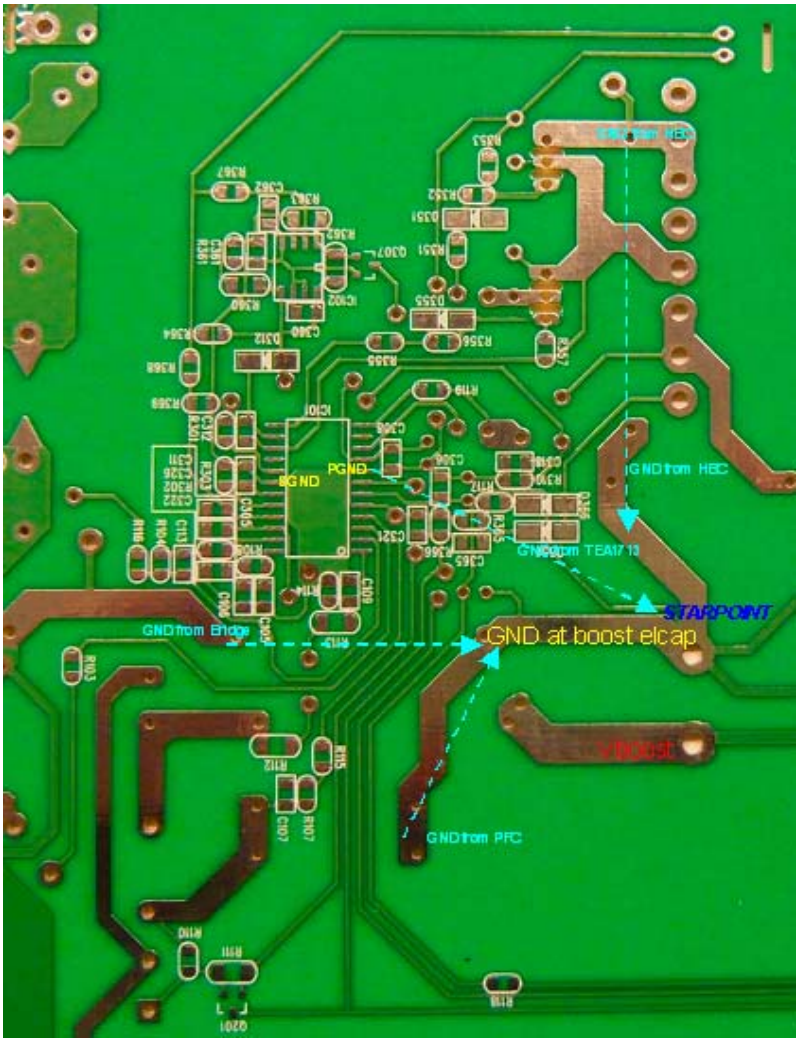

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Fig 56. Grounding layout example with star point at the boost capacitor

12.1.5 Miscellaneous

Connecting SNSCURHBC (pin 17)

Place a series resistor in the SNSCURHBC connection as close as possible to pin 17. This is important for avoiding disturbance pickup. Also avoid capacitive coupling between the connection to pin 17 and the HB track (to pin 15) that contains high dV/dt signals.

CFMIN (pin 19) and RFMAX (pin 20)

Connect the oscillator capacitor on CFMIN from pin 19 to SGND pin 18 with short tracks to prevent pickup of disturbances by an external field. Although less critical, a similar construction can be used for RFMAX.

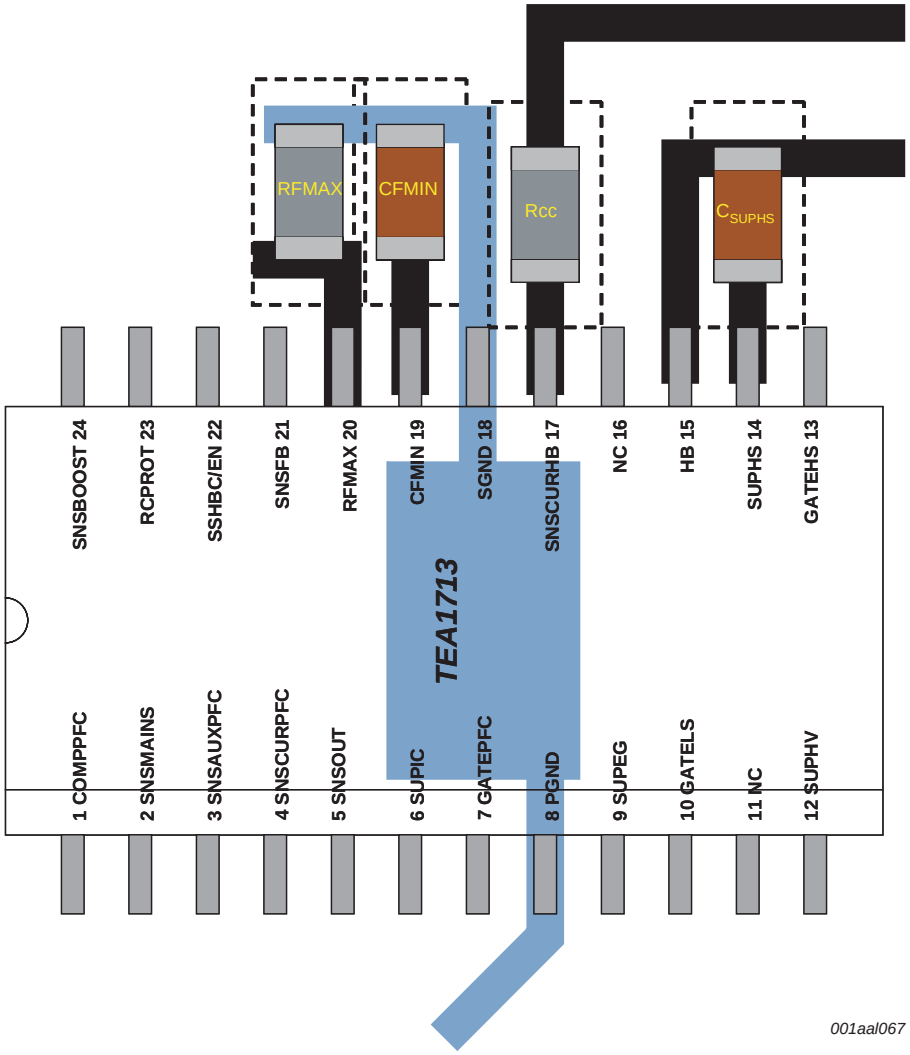


Fig 57. PCB layout connecting SGND, PGND, CFMIN, RFMAX and SNSCURHBC

12.2 Starting/debugging partial circuits

When starting a newly built application for the first time or when an error is observed during operation, it is possible to activate circuit parts step by step. This enables errors to be located more easily and an evaluation can be performed under conditions that restrict the influences from other circuit parts.

The following provides a step-by-step sequence for debugging:

1. HBC only, with protection disabled.
2. HBC only, with protection disabled and variable DC input voltage.
3. HBC only, with protection enabled.
4. PFC only.
5. PFC + HBC complete application.

The best approach is to check the HBC converter first and then the PFC converter.

12.2.1 HBC only

A proposal for the setup (temporary additions to the existing application to force operation) and the sequence for disabling/enabling the different functions is given in Figure 58. A moderate (current) load can be applied to the converters output to ascertain the correct functioning.

Be aware that a latching, overvoltage detection on SNSOUT (> 3.5 V), can still prevent operation.

CFMIN, GATELS, GATEHS and HB can be monitored to continuously assess the functioning of the converter/controller.

Practical tip: When the PFC function is disabled, V_{BOOST} can often be applied by simply applying a DC or AC voltage to the mains input connections.

Check the regulation by increasing the input voltage V_{BOOST} for the following situations in the sequence given:

1. Initially at V_{BOOST} = 0 V: the running frequency will be low with a short on-time and a long off-time. This is due to the HB detection not working properly at low voltage and the internal slope detection (HB) not detecting a proper (fast) slope. In this situation a quick check of the working of the PFC can be done by lowering the external supply voltage of 2.7 V on SNSMAINS and SNSBOOST to a value below 2.5 V. This will allow the gate-drive pulses on GATEPFC to be seen. Varying the voltage, shows changes in on-time. After this check, revert the voltage to 2.7 V to continue the HBC-only start-up. See Section 12.2.2.1.
2. Increasing the value of V_{BOOST}, at a certain input voltage the HB detection will work correctly and the frequency to drive maximum power, will be minimal. If the HB slope remains slow, the output current is probably low. Increasing the output current will probably result in proper HB switching.
3. When the V_{BOOST} input voltage has reached a level closer to the nominal working voltage, the correct output voltage will be reached (depending on the output load), and regulation will start working. This will result in increasing the frequency with increasing the input voltage until the nominal working voltage of V_{BOOST} is set.
4. When the basic functioning of the HBC is working well including SNSFB regulation, protection can be added one by one. Proper functioning or a need for change can be evaluated.
5. When a self-supplying application is used, the external supply voltage can be removed as soon as the system works well at nominal V_{BOOST} voltage. The system should now be able to start with the internal high voltage start-up supply and an auxiliary winding can take over the SUPIC supply.

Remark: If, during debugging or starting, a protection has been activated, it may be necessary to switch the SUPIC supply off and on to reset a latched protection state.

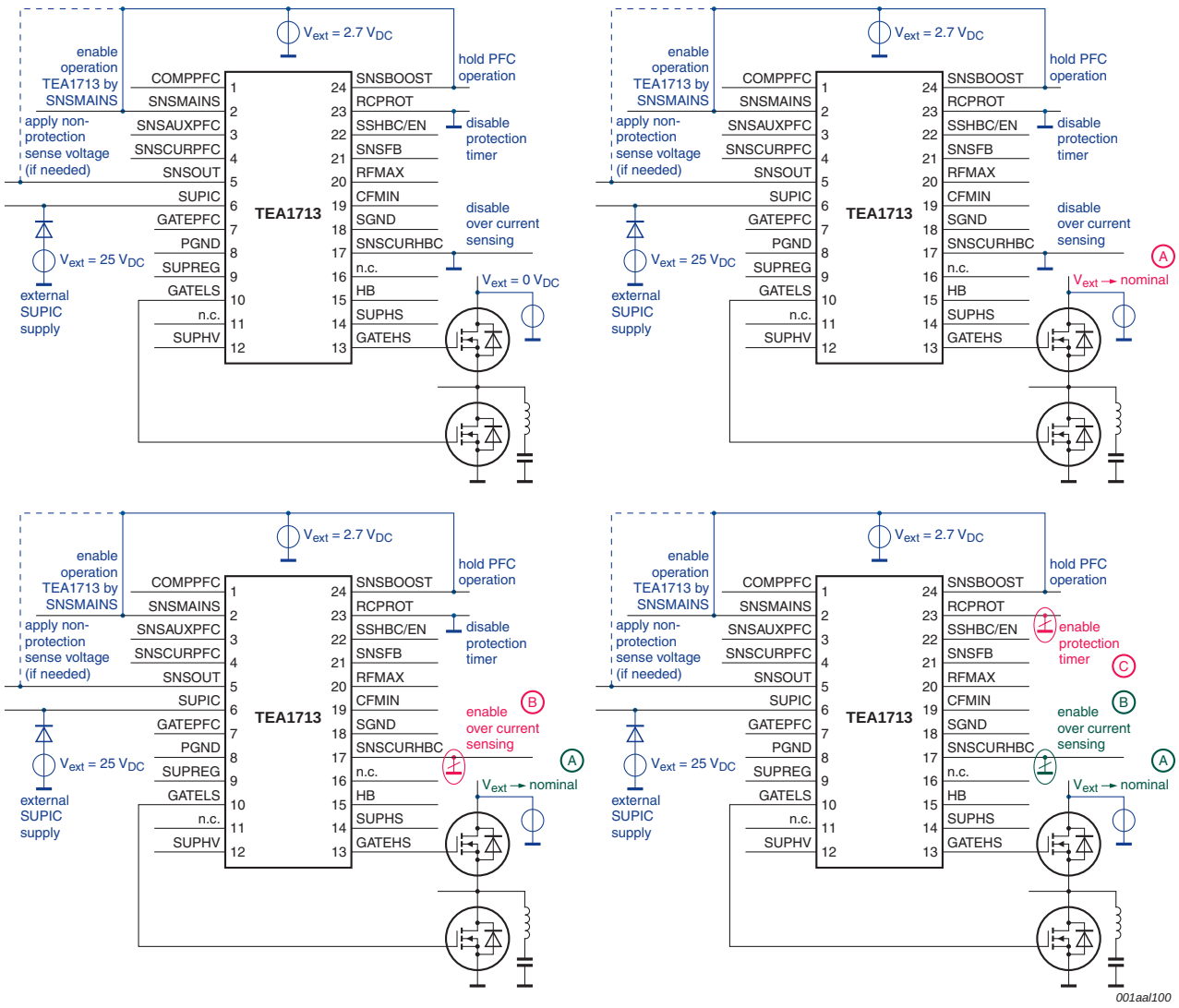


Fig 58. HBC only - start-up and debugging step-by-step

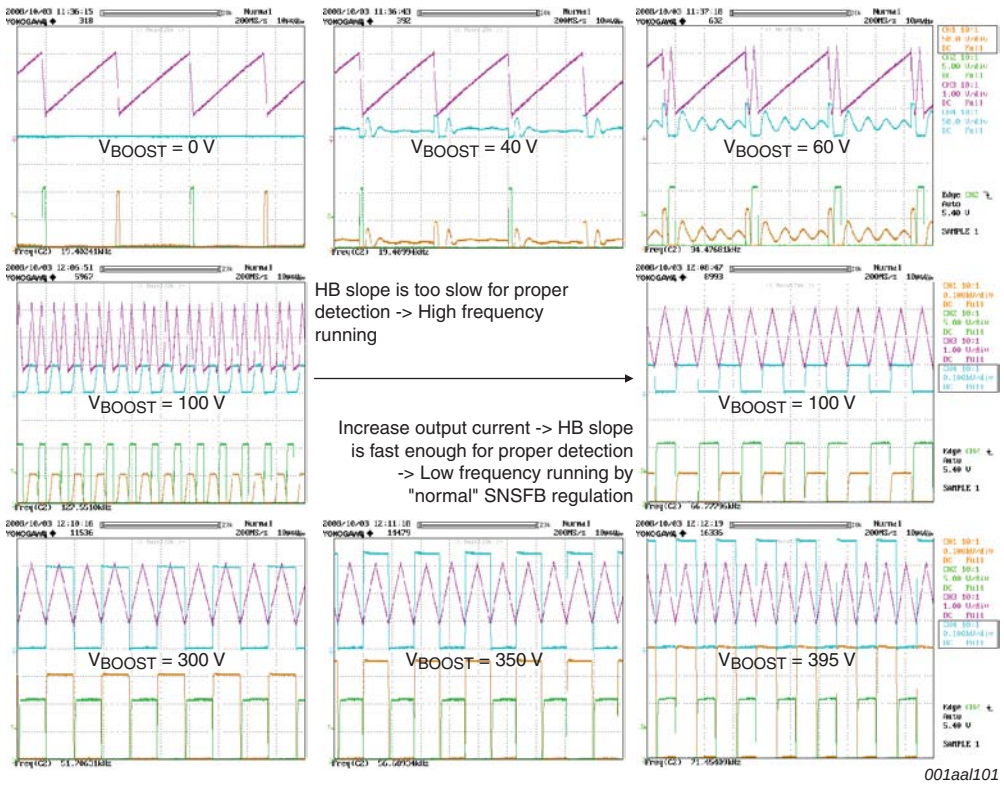


Fig 59. Typical signals during a separate HBC start-up for an increase in V_{BOOST}

The following list provides an association between pins and the protection states for which they are being monitored:

- **SSHBC/EN:** When the TEA1713 lowers the voltage to this pin, it indicates a protection with correction to high frequency.
- **RFMAX:** The voltage level on RFMAX indicates the oscillator frequency, which may cause a high frequency protection.
- **CFMIN:** No proper detection of HB slope or a possible capacitive mode detection can be observed by a (partially) slow oscillator signal.
- **PGND and SGND:** If the TEA1713 detects HB operation while there is zero input voltage, it indicates that the connection between these pins at the IC is not present. Gate currents lead to false HB-slope detection.
- **SNSCURHBC:** Any disturbances on this pin (voltage spikes) can lead to an increase of frequency while the original measurement voltage/signal is OK.
- **SNSOUT:** The voltage on this pin should be between 2.35 V and 3.5 V for normal operation. To avoid protection, a voltage can be forced on it. But it is often related (by a resistive divider) to the SUPIC and will be correct when SUPIC is supplied externally.
- **RCPROT:** Several protection functions will charge the timer.

12.2.2 PFC only

The HBC function can be disabled by keeping/forcing SSHBC/EN below 2.2 V. A voltage higher than 1.2 V can enable the PFC function. Applying an additional voltage (from an external supply) of approximately 1.5 V on SSHBC/EN will enable PFC only operation.

The setup is similar to that for HBC only operation, but for extra safety, the V_{BOOST} connection to the high side switch of the HBC can be disconnected. In addition, a small load can be connected on V_{BOOST} to prevent voltage overshoot and control the output power capability.

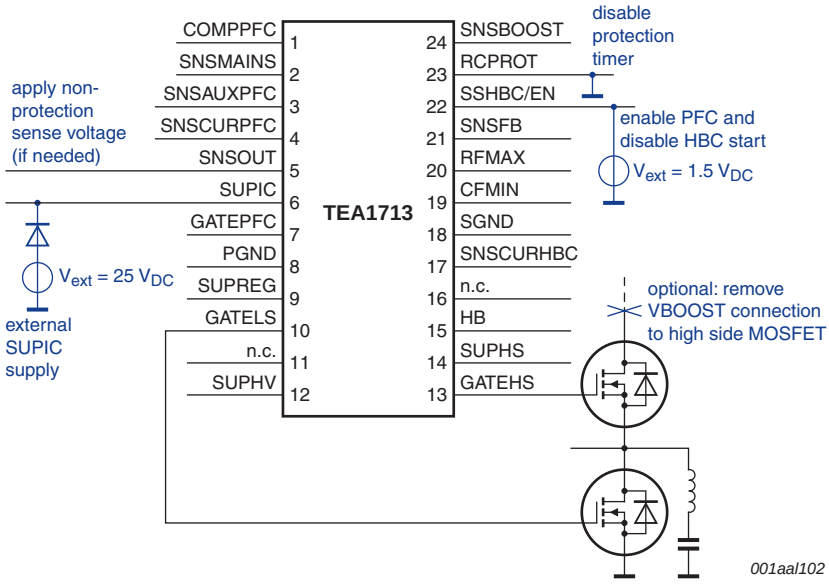


Fig 60. Start-up/debugging for PFC only

12.2.2.1 Operational check without mains voltage

Without mains input voltage, by lowering the (external) voltage on SNSMAINS and SNSBOOST to below 2.5 V, drive pulses can be observed on GATEPFC. Lower voltages lead to a longer on-time. Below 0.89 V, pulses stop because of SNSMAINS undervoltage protection and will restart when the level increases above 1.15 V.

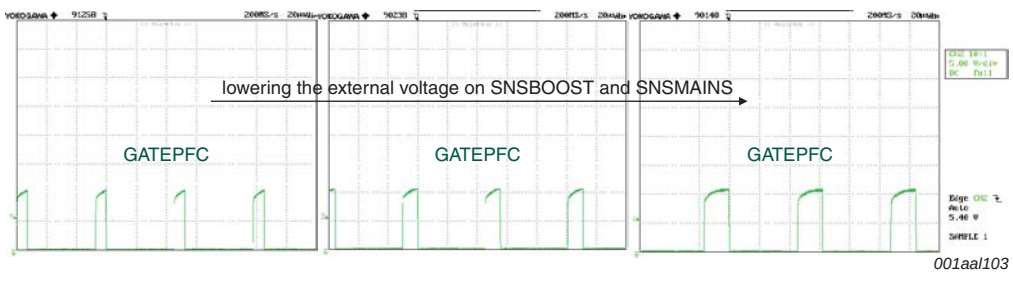


Fig 61. Typical GATEPFC signals without mains voltage

12.2.2.2 Operational check with mains voltage

There is no simple step by step method of gradually increasing the mains voltage to start PFC operation. So full mains voltage is applied to check PFC functionality. While doing this, any external voltage source on SNSMAINS and SNSBOOST must be removed.

If a problem is expected of an output voltage that may too high, the output measurement resistor from SNSBOOST to ground can be (temporarily) increased in value. This will lead to a lower output voltage regulation setting.

To be able to observe proper PFC operation more easily with an oscilloscope, a DC voltage should be supplied to the mains input instead of the usual AC voltage. This results in more stable signals for evaluation.

12.2.3 HBC and PFC operation

When both converters work properly independently, they can be checked working simultaneously. The additions used for start-up and debugging should be removed.

Be aware that a (normal) ripple voltage on V_{BOOST} will result in some continuous frequency variations in the HBC for compensation. At high output power, the voltage ripple on V_{BOOST} will be larger.

13. Application examples and topologies

13.1 Examples of IC evaluation and test setup

Examples of a test/evaluation setup are provided in Figure 62 and Figure 63. This setup can be used for:

- Checking if an IC is still functional (not defect).
- Evaluation of specific IC function(s) or pin properties with limited interference from the total system.

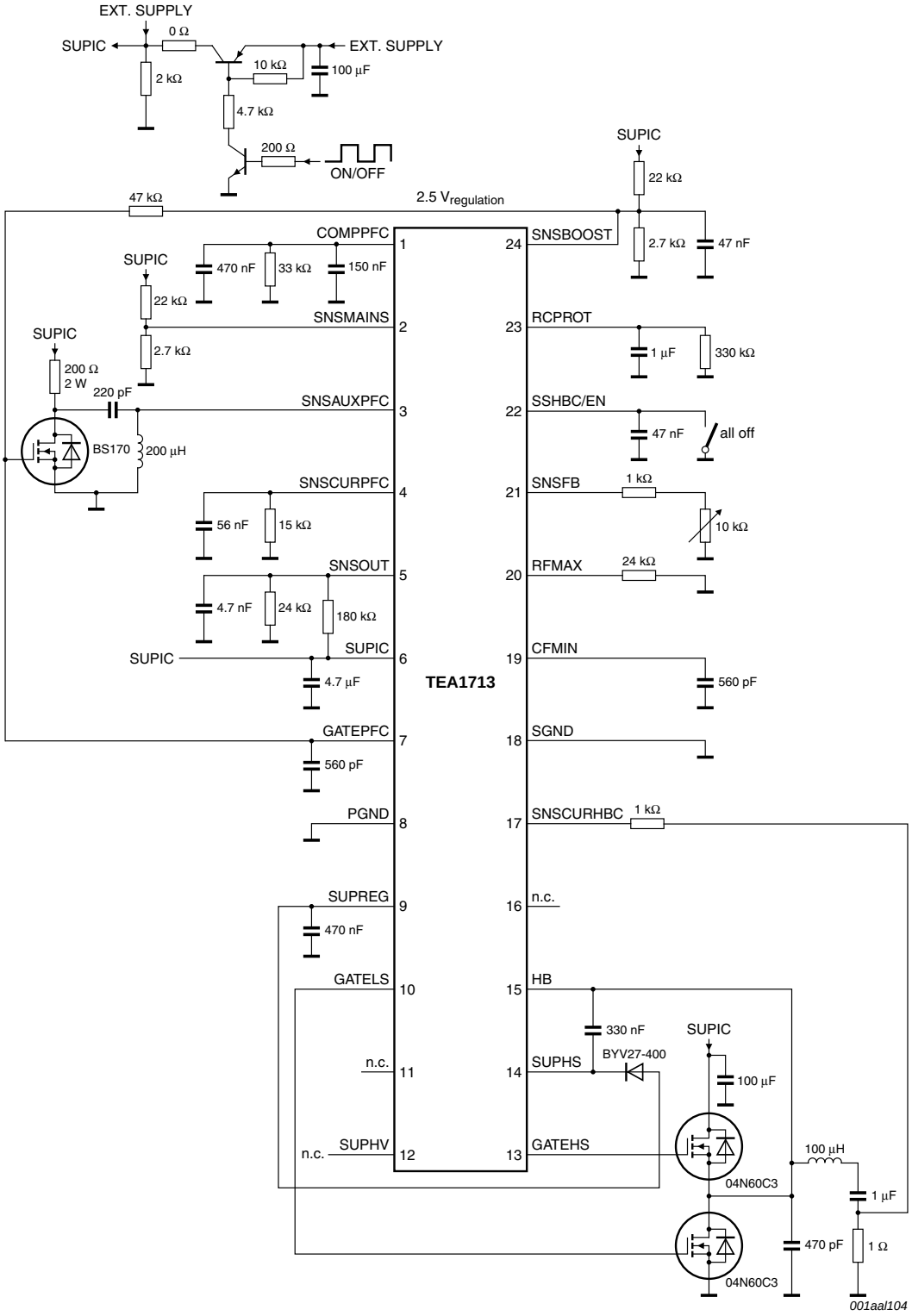


Fig 62. Example of a basic IC test setup on a single low voltage supply (24 V)

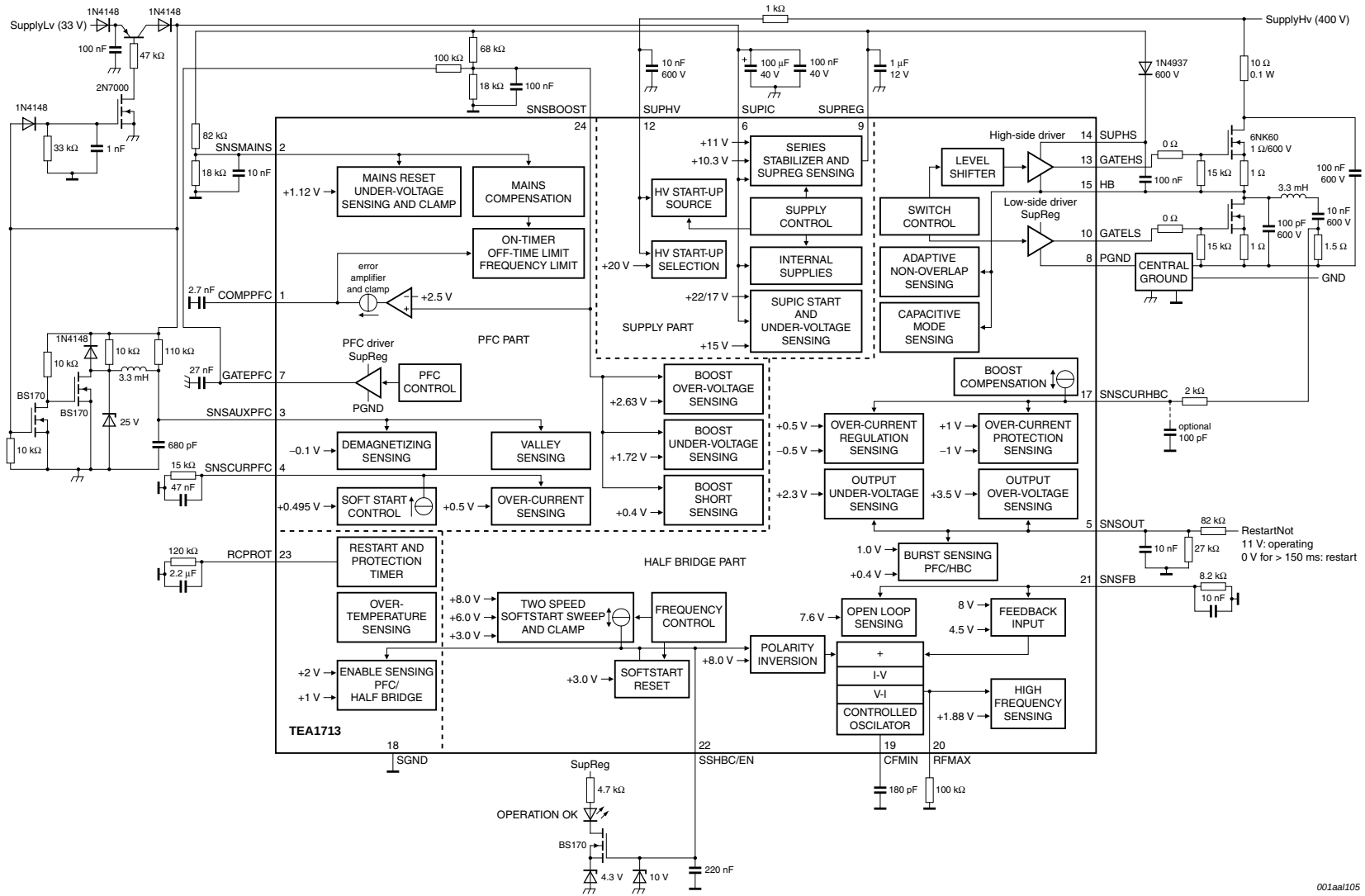


Fig 63. Example of a basic IC evaluation and test setup with a high bus voltage

13.2 Example of a 250 W LCD TV application

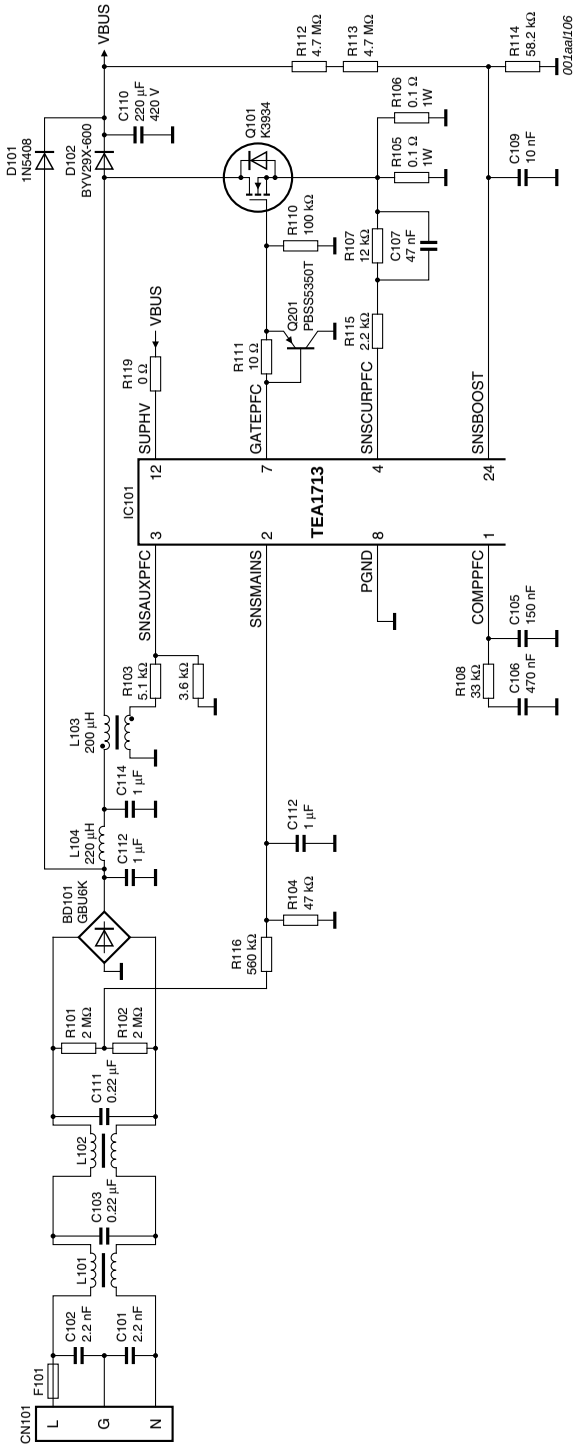
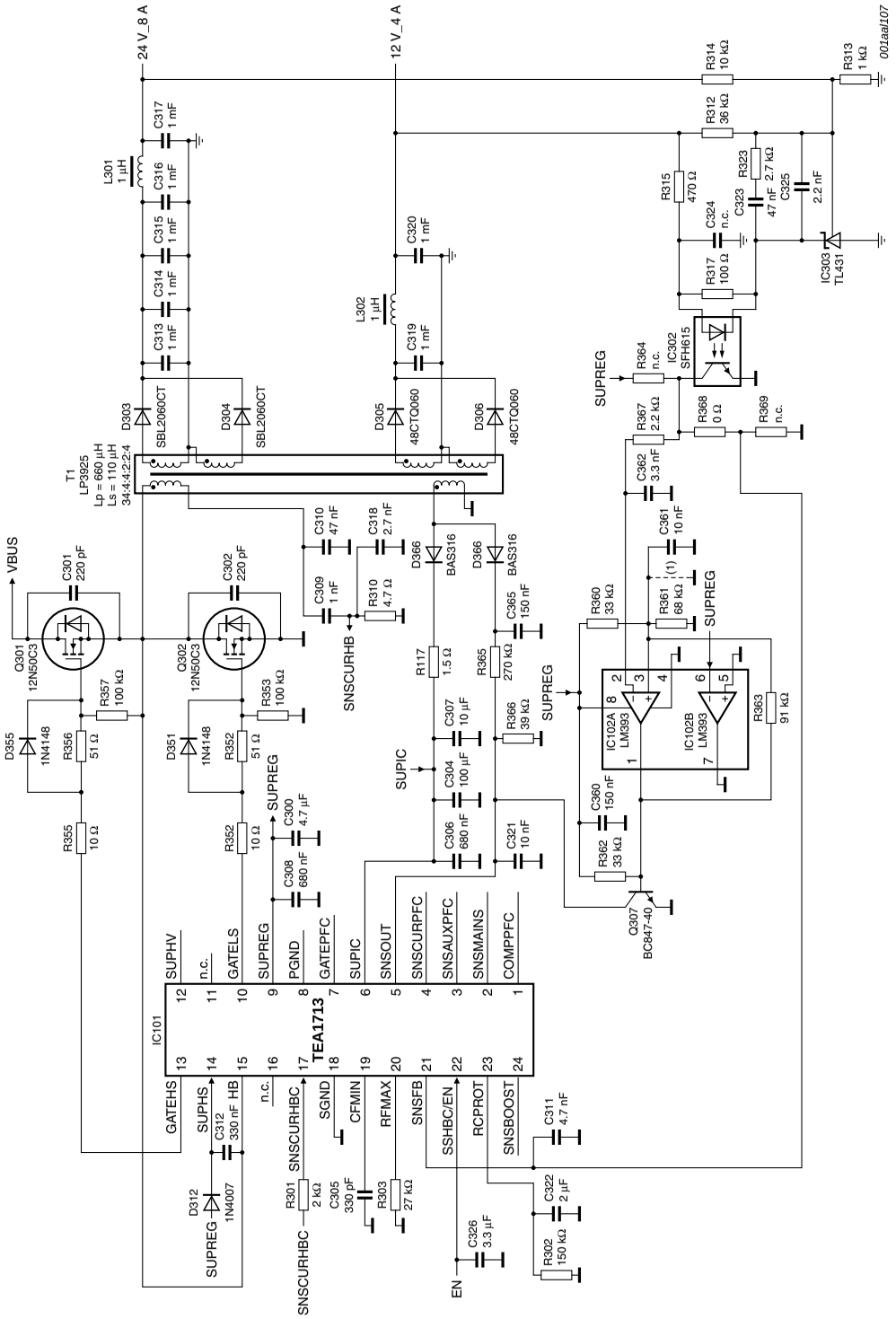


Fig 64. Example of a 250 W LCD TV application (part 1 of 3)



(1) Remove to enable burst mode operation

Fig 65. Example of a 250 W LCD TV application (part 2 of 3)

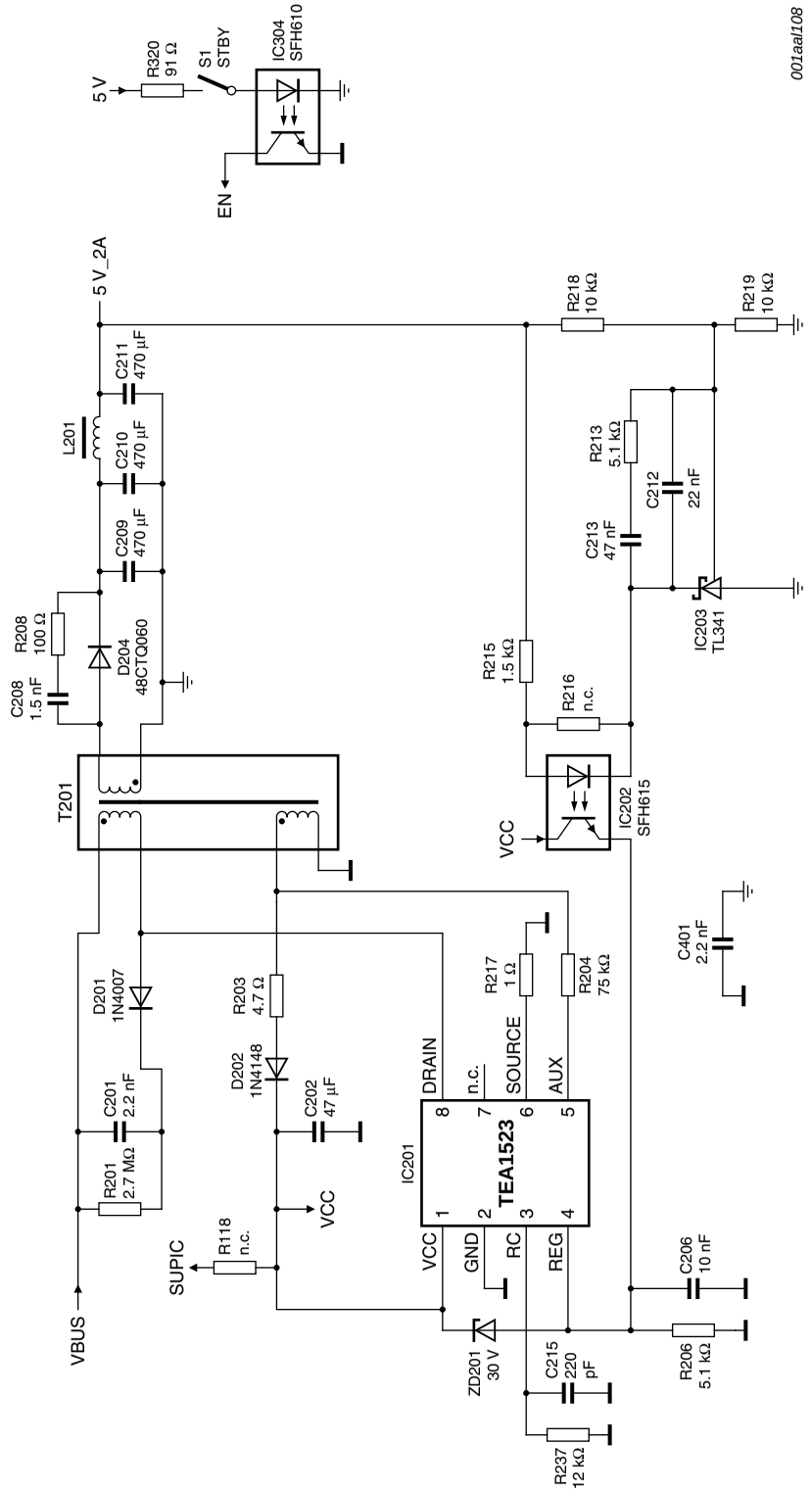


Fig 66. Example of a 250 W LCD TV application (part 3 of 3)

13.3 Example of a 90 W note book adapter application

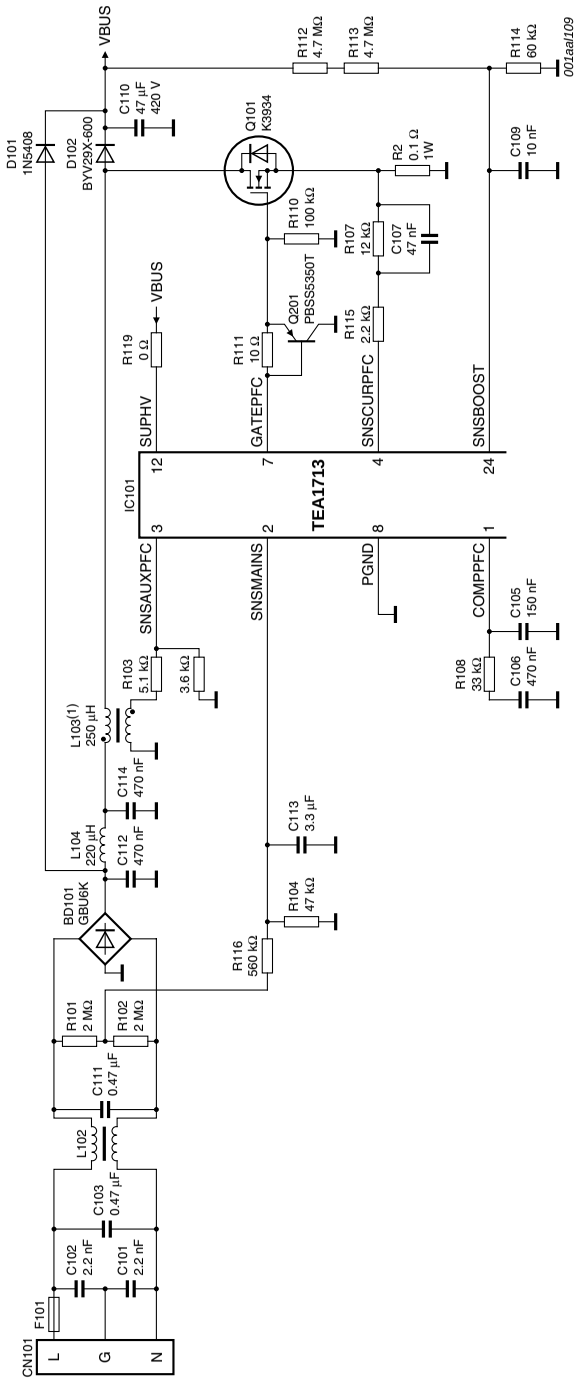


Fig 67. Example of a 90 W note book adapter application (PART 1 of 2)

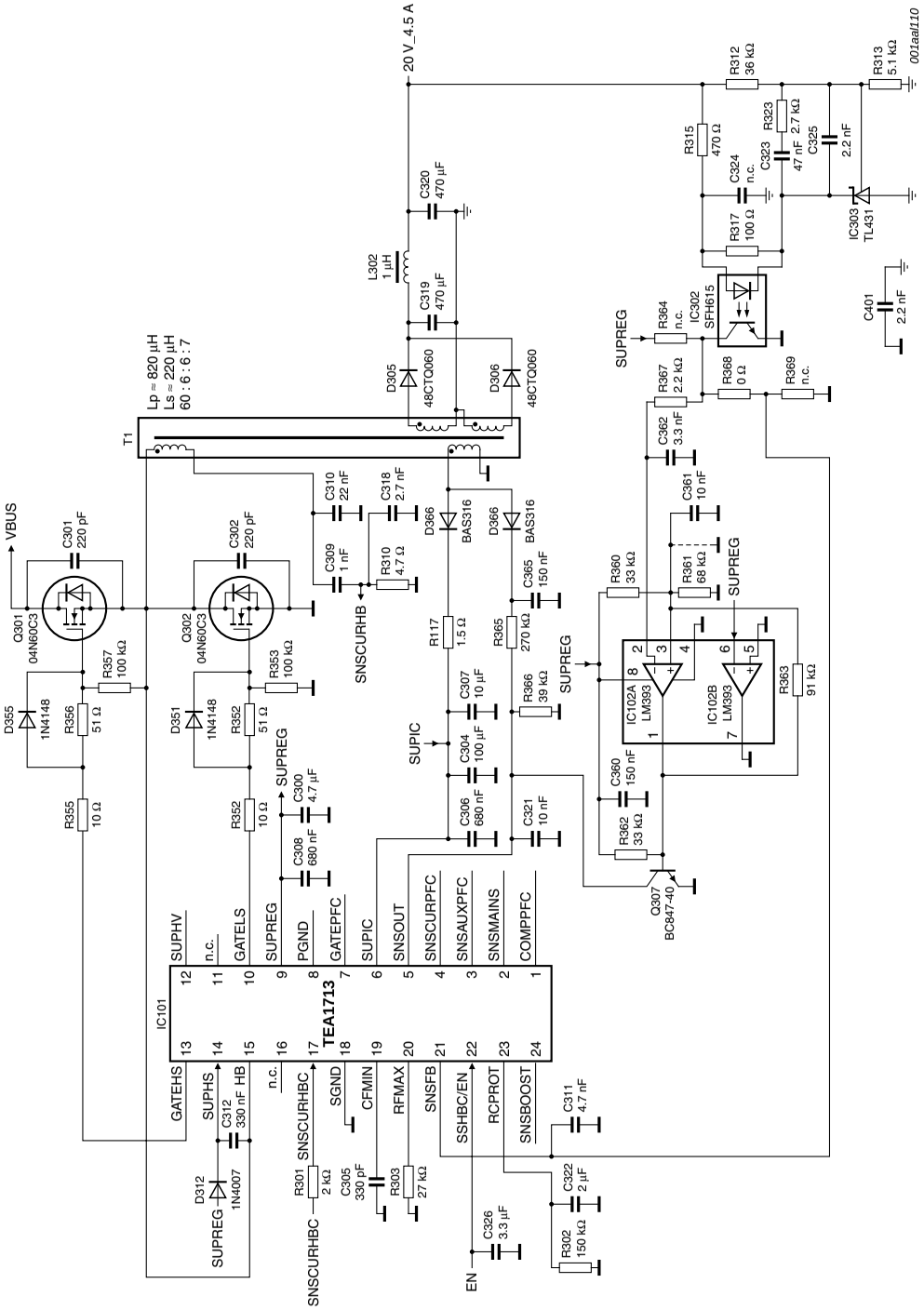


Fig 68. Example of a 90 W note book adapter application (PART 2 of 2)

14. Abbreviations

Table 5. Abbreviations

Acronym	Description
ADT	Adaptive Dead Time
BCD	Bipolar CMOS DMOS
CMR	Common Mode Rejection
EMC	ElectroMagnetic Compatibility
EMI	ElectroMagnetic Interference (or Immunity)
HB	Half Bridge
HBC	Half Bridge Converter (or Controller)
HFP	High-Frequency Protection
HV	High-Voltage
IC	Integrated Circuit
LCD	Liquid Crystal Display
LLC	Resonant tank or Converter (Lm + Lr + Cr in series)
OCP	OverCurrent Protection
OCR	OverCurrent Regulation
OLP	Open Loop Protection
OPTO	Opto-coupler
OTP	Over Temperature Protection
OVP	OverVoltage Protection
PCB	Printed Circuit Board
PFC	Power Factor Converter/Controller/Correction
PWM	Pulse Width Modulation
SCP	Short-Circuit Protection
SOI	Silicon-On-Insulator
UVP	Under Voltage Protection

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