Datasheet

DB_START_3C10

Cyclone III Development Board

www.devboards.de

Contents

Revisions

Revision	Remark	Date
1.00	Initial Version	28.09.2009
1.01	Changes in the documentation, new Quartus Version 9.1	02.12.2009

Package contents

DB_START_3C10

- DB_START_3C10 Development Board
- Mini USB to USB Cable
- Reference Designs can be downloaded from www.devboards.de

Introduction

The DB_START_3C10 is a Cyclone III Development Board with embedded USB-Blaster, Memory and IO Pins

The following features are integrated:

- EP3C10E144C8N
- EPCS16 configuration device
- 16Mbyte SDRAM
- 19 I/O Pins
- 6x Input Pins
- 8x User LEDs
- 2x user buttons
- JTAG interface
- Crystal Oscillator

- Embedded USB Blaster on Board

- Power Supply via USB or external 5V Power supply

- on board 3.3V, 2.5V and 1.2V power supply

- dimension : 70x60mm²

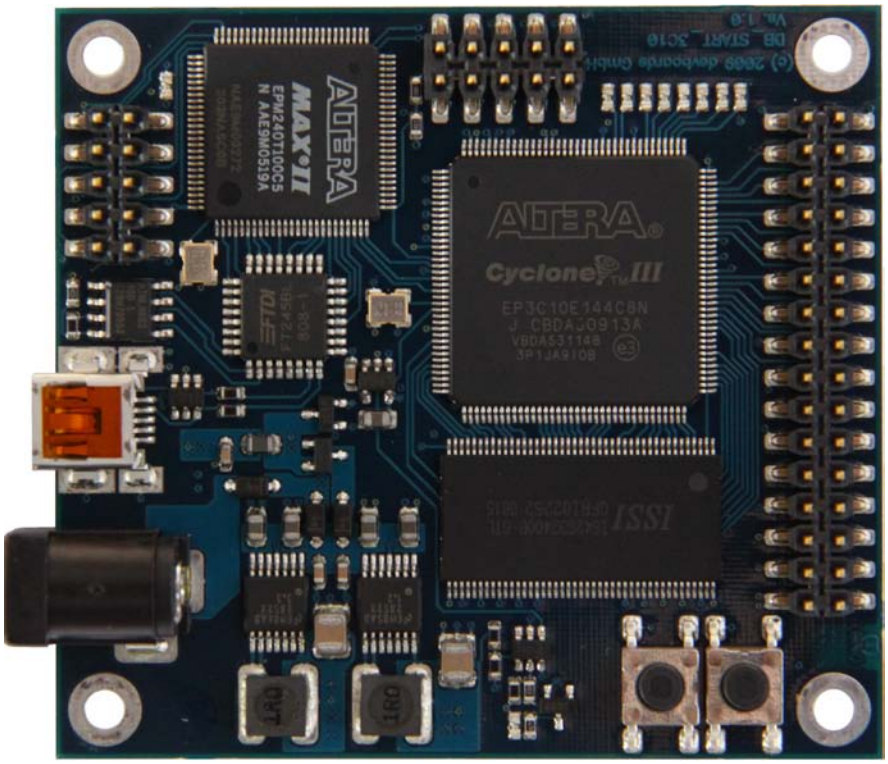


Figure 1

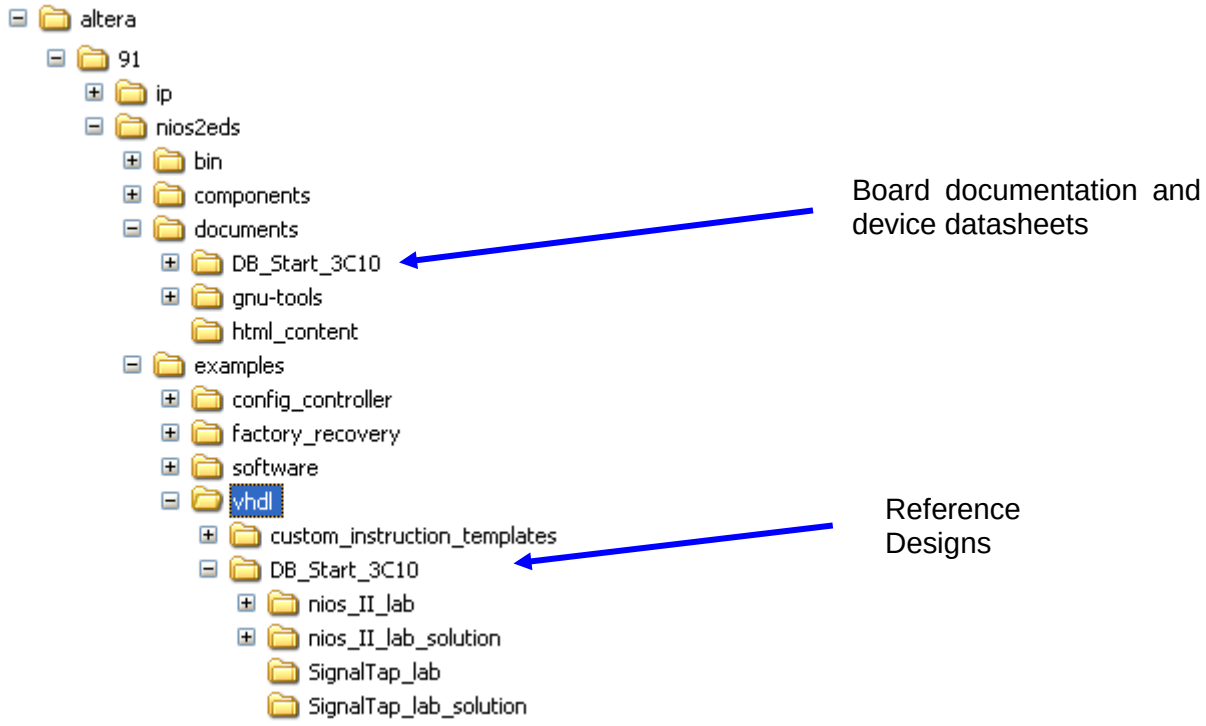
Installation

Download and execute the DB_Start_3C10_Setup.Exe file from www.devboards.de to install the Reference Designs and documentation. The Free Quartus Software and NIOS IDE can be downloaded from www.altera.com/download

Please install the applications in the following sequence:

- install the Quartus® 9.1 Web Edition
- install Nios®II 9.1 Version
- install the reference designs.

When you have finished the installation of the reference designs you can find the following folders on your hard disk:



Getting started

Documentation

The complete documentation of the board, the reference designs, IP functions and the on-board devices are stored in the documentation directory of the Altera® Nios®II directory e.g. C:\Altera\90SP2\nios2eds\documents\DB_START_3C10.

Setting up the board

Connect the DB_Start_3C10 Board via the USB Cable to the PC. The Power LED should lit and the board should be registered as an Altera USB-Blaster on your PC. After that you can work with the board.

IF you like to use the board with an external Power Supply, please make sure that the supply delivers 5V +/-10%. If you use an external Power supply, only the USB Blaster part of the Board will be supplied via USB, the rest is powered via the external power supply.

Flashing the board

Programming the configuration device

To program the EPCS16 configuration device on the DB_START_3C10 Development Board, a JTAG indirect programming file (.jic) is used. In the file / convert programming file menu in Quartus®II a .SOF file can be converted into a .jic file. The .jic file can be selected in the Quartus®II programmer (in JTAG mode). Make sure that both configure / program lines are selected to download the loader into the FPGA and the SOF file into the configuration device.
The Nios®II IDE flash programmer can also be used to program a SOF file into the configuration device.

Reference designs

Documentation for the Reference Designs is located in the \Altera\91\nios2eds\examples\vhdl\DB_Start_3C10 folder.

NIOS II Getting Started Tutorial

AS a NIOS II Starting point, a Step by Step Tutorial is available. This lab shows how to setup a NIOS II Processor, how to write C Code and debug it and how to add a custom peripheral to the NIOS II.

Signal Tap Tutorial

The Signal Tap Tutorial shows how to use the Signal Tap Logic Analyser inside the FPGA. Setup a small design, setup the SignalTap Logic Analyser and uses the In System Memory Content Editor to change parameters on the fly.

Board Description

FPGA Configuration

The DB_START_3C10 Development Board includes an on-board USB Blaster that can be used to configure the FPGA, program the EPCS Configuration device, use the Signal-Tap Logic Analyser and together with the NIOS IDE to download and debug software.

Clocking

The DB_START_3C10 Development Board includes a free running 50MHz Crystal Quartz Oscillator. The Crystal Quartz Oscillator drives the FPGA directly. Table 2 shows the clock distribution on the DB_START_3C10 board. The Crystal Quartz Oscillator is a ±50ppm Clock source. One PLL is used to generate an external clock for the SDRAM.

Clock Distribution

Function	FPGA Pin	Signal Name
50MHz	22	Clk50
SDRAM Clock	129	SCLK

Table 1

SDRAM Clock Setting

The SDRAM Clock is generated from the FPGA PLL Output. The phase of the PLL should be set that

Offset delay of the PLL – tco of the Clock Signal is between –1.0ns and –2.0ns.

The Offset delay value can be found in the Quartus® II compilation report, Timing Analysis, Clock Setting Summery. The tco can be found in the tco-section.

Power Supply

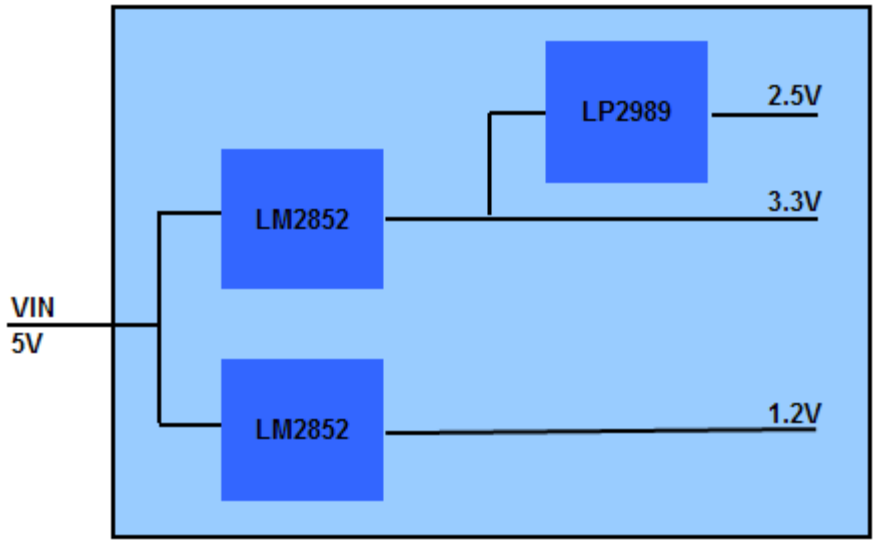
The DB_START_3C10 Development Board allows supplying the board either via the USB Connection to the PC or with a 5V regulated center-positive input power supply (P12). If both supplies are connected, the USB Supply is internally disconnected and the external 5V is used.

Figure 4 shows the Power distribution on the DBC3C40 board.
For details of the power supply refer to the schematic on the end of the document.

- 1.2V Core Voltage
- 2.5V Analog Supply for FPGA
- 3.3V I/O Voltage and supply for the other components

A Power Good signal is generated monitoring the 1.2V and 3.3V.

Figure 2



Reset Signal

Function	Pin	Signal Name
Power Good	23	RSTn

Table 2

I/O Connections

SDRAM

An ISSI 128Mbit SDRAM is used on the DB_START_3C10 development Board. The IS42S32400A Device is a 4Mx32bit SDRAM. Table 7 shows the wiring between the FPGA and the SDRAM. The Clock of the SDRAM comes directly from the FPGA. Figure 3 shows the settings of the SOPC-Builder Component.

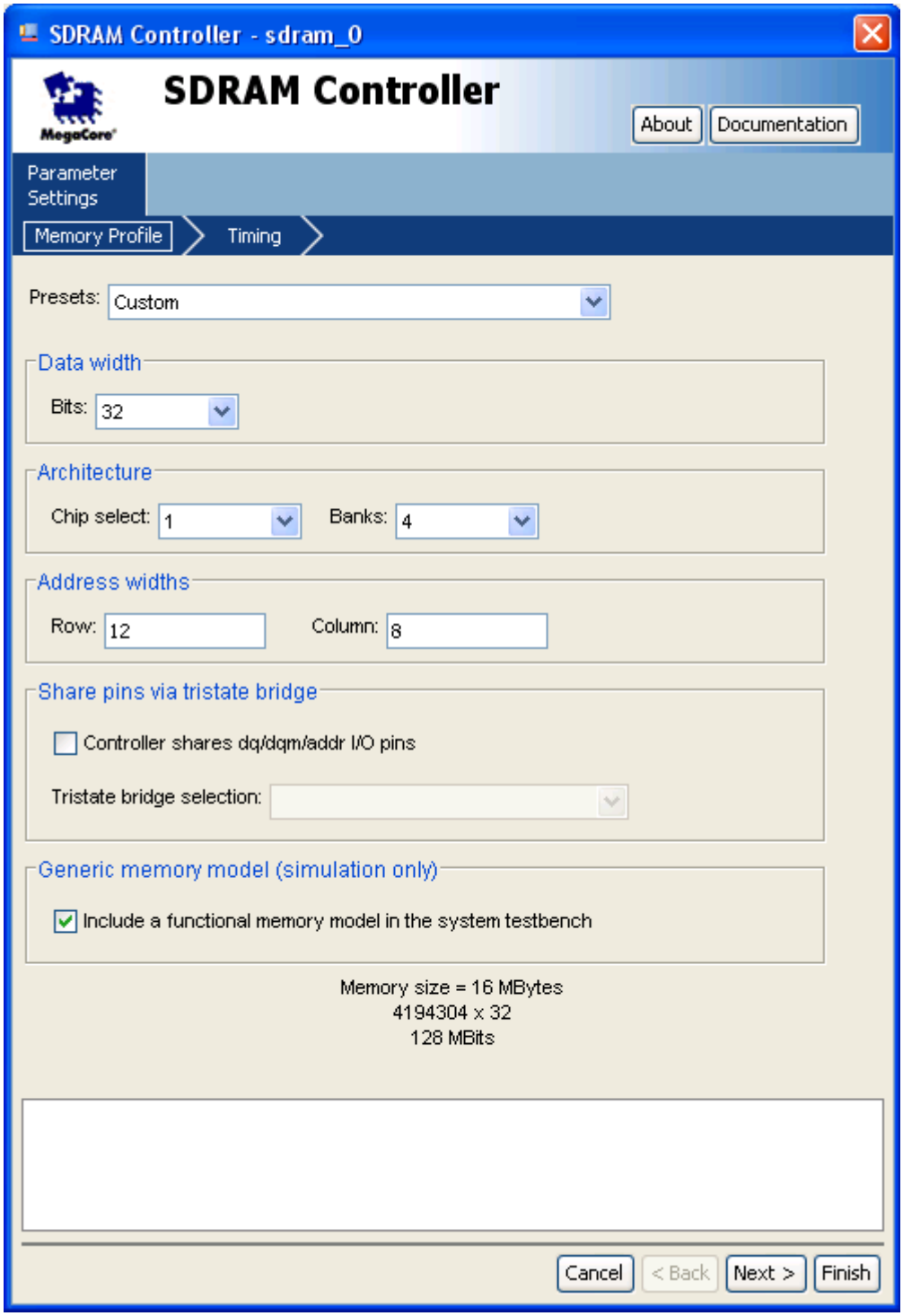


Figure 3

Figure 4 shows the SDRAM Timing Settings up to 66MHz Design. For more than 66MHz set the CAS latency cycles to 3!

The clock phase for the SDRAM must be set that the sum of PLL Offset and tco for the SDRAM clock signal is about –1.2ns. The PLL Offset value can be found in the Quartus compilation report, Timing Analysis, Clock Setting Summery. The tco can be found in the tco-section.

Figure 4

FPGA Connection

Function	Pin	FPGA Pin
SCLK	68	129
CKE	67	132
NCS	20	59
NRAS	19	60
NCAS	18	128
NSWE	17	127
DQM0	16	64
DQM1	71	126
DQM2	28	49
DQM3	59	144
A0	25	52

Function	Pin	FPGA Pin
A1	26	51
A2	27	50
A3	60	143
A4	61	142
A5	62	141
A6	63	138
A7	64	137
A8	65	135
A9	66	133
A10	24	53
A11	21	58
BA0	22	55
BA1	23	54
DQ0	2	73
DQ1	4	72
DQ2	5	71
DQ3	7	70
DQ4	8	69
DQ5	10	68
DQ6	11	67
DQ7	13	66
DQ8	74	74
DQ9	76	75
DQ10	77	76
DQ11	79	77
DQ12	80	79
DQ13	82	83
DQ14	83	84
DQ15	85	85
DQ16	31	44
DQ17	33	43
DQ18	34	42
DQ19	36	39
DQ20	37	38
DQ21	39	34
DQ22	40	33
DQ23	42	32
DQ24	45	28
DQ25	47	30
DQ26	48	11
DQ27	50	10
DQ28	51	4
DQ29	53	3
DQ30	54	2
DQ31	56	1

Table 3

Pin Header

A Pin header with 32 signals is directly connected to the FPGA. Table 4 shows the pinning and the FPGA connection for Pin Header P6.

Make sure that only 3.3V signals are connected to the Pin Headers P6.

I/O Connector P6

Function	FPGA	Pin	Pin	FPGA	Function
GND		1	2		VCC33
GIO0	106	3	4	105	GIO1
GIO2	104	5	6	103	GIO3
GIO4	101	7	8	100	GIO5
GIO6	99	9	10	98	GIO7
GIN0	91	11	12	90	GIN1
GIN2	89	13	14	88	GIN3
GIN4	24	15	16	25	GIN5
GND		17	18		GND
GIO8	86	19	20	87	GIO9
GIO10	80	21	22	7	GIO11
GIO12	136	23	24	125	GIO13
GIO14	31	25	26	124	GIO15
GIO16	46	27	28	121	GIO17
GIO18	65	29	30		GND
GND		31	31		GND

Table 4

Attention : Signals GIN4 and GIN5 are shared with the buttons!

Buttons & LEDs

2 Buttons and 8 LEDs are available on the DB-START-3C10 Development Board. The buttons are equipped with a 10K Pull-down resistor and are shared with the respective Input pins on connector P6. The LEDs are connected to 3.3V. To light the LED the FPGA must drive a Low signal.. Table 5 shows the FPGA connection of the Buttons and LEDs.

FPGA Connection

Function	Device	Pin	FPGA Pin
Button0	P3	1	24
Button1	P4	1	25
LED0	D2	1	110
LED1	D3	1	111
LED2	D9	1	112
LED3	D10	1	113
LED4	D11	1	114
LED5	D12	1	115
LED6	D13	1	119
LED7	D14	1	120

Table 5

Bill of Material

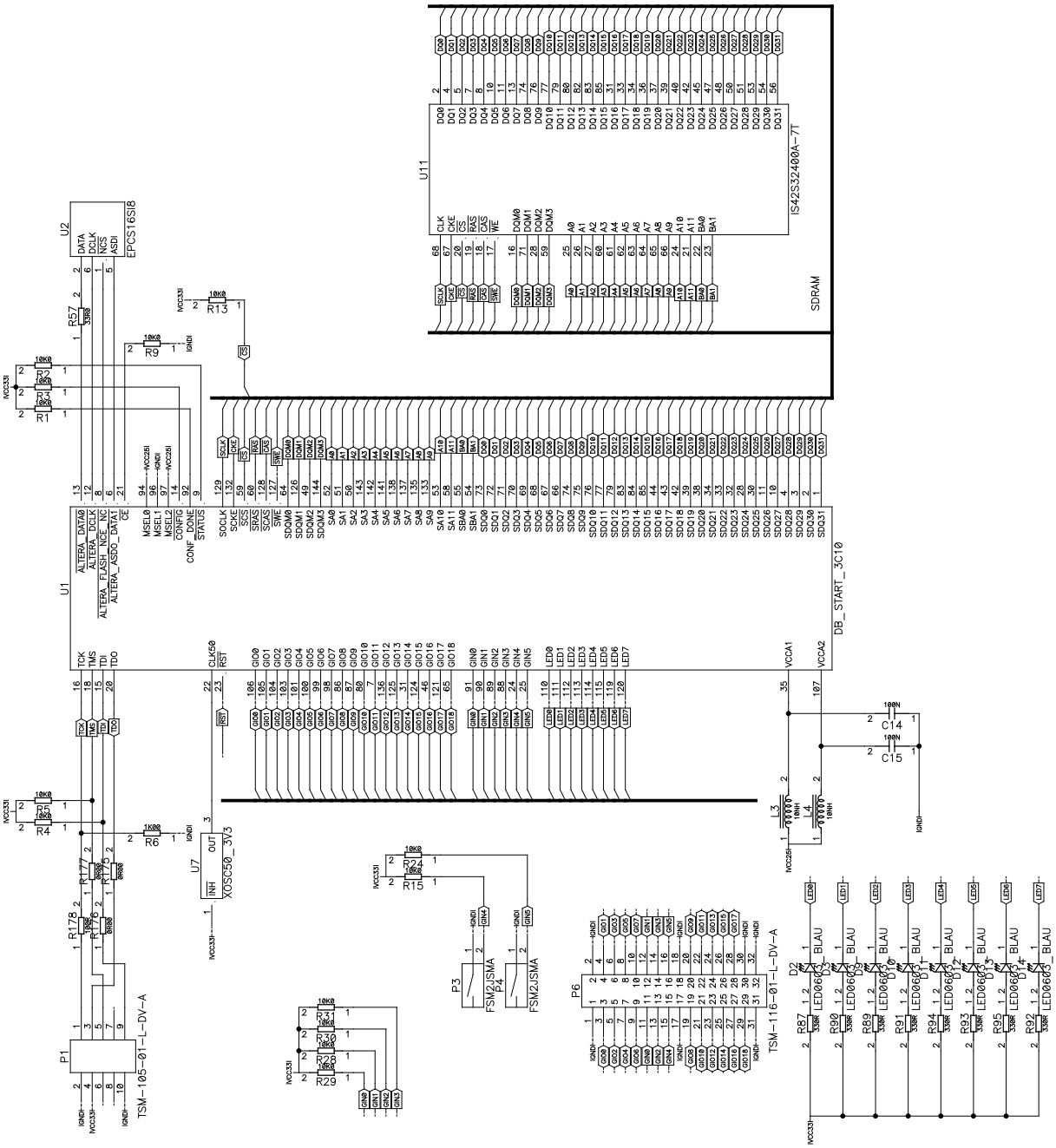
Description	Count	SMD	Package	Reference Designator
AT93C46-DN-SH-B	1	Ja	SO8	U4
BC850B	2	ja	SOT23	U13 U16
C0603_100NA50V	35	ja	C0603	C14 C15 C17 C57 C110 C111 C112 C117 C119 C13 C16 C19 C22 C34 C35 C36 C37 C38 C39 C40 C41 C42 C91 C92 C93 C94 C95 C96 C173 C1 C3 C4 C5 C30 C32
C0603_10N0A50V	2	ja	C0603	C6 174
C0603_2N20A50V	2	Ja	C0603	C29 C31
C0805_10UFA10V	7	ja	C0805	C2 C8 C9 C45 C46 C47 C48
C1206_1N00A2KV	1	Ja	C1206	C7
C1210_100UA6V3	2	ja	C1210	C33 C43
DC10A	1	nein		P12
EP3C10E144C8N	1	Ja	TQ144	U1
EPCS16SI8N	1	ja	SO8	U2
EPM240T100C5N	1	ja	TQ100	U5
FDN304P	1	ja	SOT23	U8
FSM6JSMA	2	ja		P3 P4
FT245BL	1	Ja		U10
IS42S32400B-6TL	1	ja	TSSOP68	U11
L0603_10NHA0A4 EPCOS B82496C3100J	2	ja	S0603BR	L3 L4
L0805_330RA2A0 Würth 742792037	1	Ja	L0805	L1
LED 0603_Blau	10	Ja	R0603	D1 D2 D3 D9 D10 D11 D12 D13 D14 D15
LM2852XMXA-1.2	1	ja	TSSOP14	U9
LM2852XMXA-3.3	1	ja	TSSOP14	U14
LP2992AIM5-2.5	1	ja	SOT23-5	U12
LWE-T_1U0A2A7 Würth 744042001	2	ja	WE-TPC-M	L7 L8
MBR0530T3	3	ja	SOD-123R	D4 D5 D7

Description	Count	SMD	Package	Reference Designator
R0603_0R00A1%	3	ja	R0603	R175 R176 R177
R0603_100KA1%0	1	ja	R0603	R22
R0603_100RA1%0	1	ja	R0603	R178
R0603_10K0A1%0	18	ja	R0603	R1 R2 R3 R4 R5 R9 R11 R13 R15 R17 R18 R19 R24 R25 R28 R29 R30 R31
R0603_10RA1%0	1	ja	R0603	R139
R0603_1K00A1%0	7	ja	R0603	R6 R16 R20 R26 R27 R32 R33
R0603_1K50A1%0	1	ja	R0603	R12
R0603_22R0A1%0	2	ja	R0603	R7 R8
R0603_2K20A1%0	1	ja	R0603	R10
R0603_330RA1%0	9	ja	R0603	R21 R87 R89 R90 R91 R92 R93 R94 R95
R0603_33R0A1%0	1	ja	R0603	R57
R0603_470RA1%0	2	ja	R0603	R14 R23
SN65220DBVT	1	Ja	SO8	U3
TPS3103K33DVBR	1	Ja	SOT23-5	U17
TSM-105-01-L-DV-A	2	ja		P1 P5
TSM-116-01-L-DV-A	1	ja		P6
USB_MINI_AB	1	ja	MOLEX	P2
O 24-JO32-B-3,3-1-L	1	Ja	JO32	U6
O 50-JO32-B-3,3-1-L	1	Ja	JO32	U7

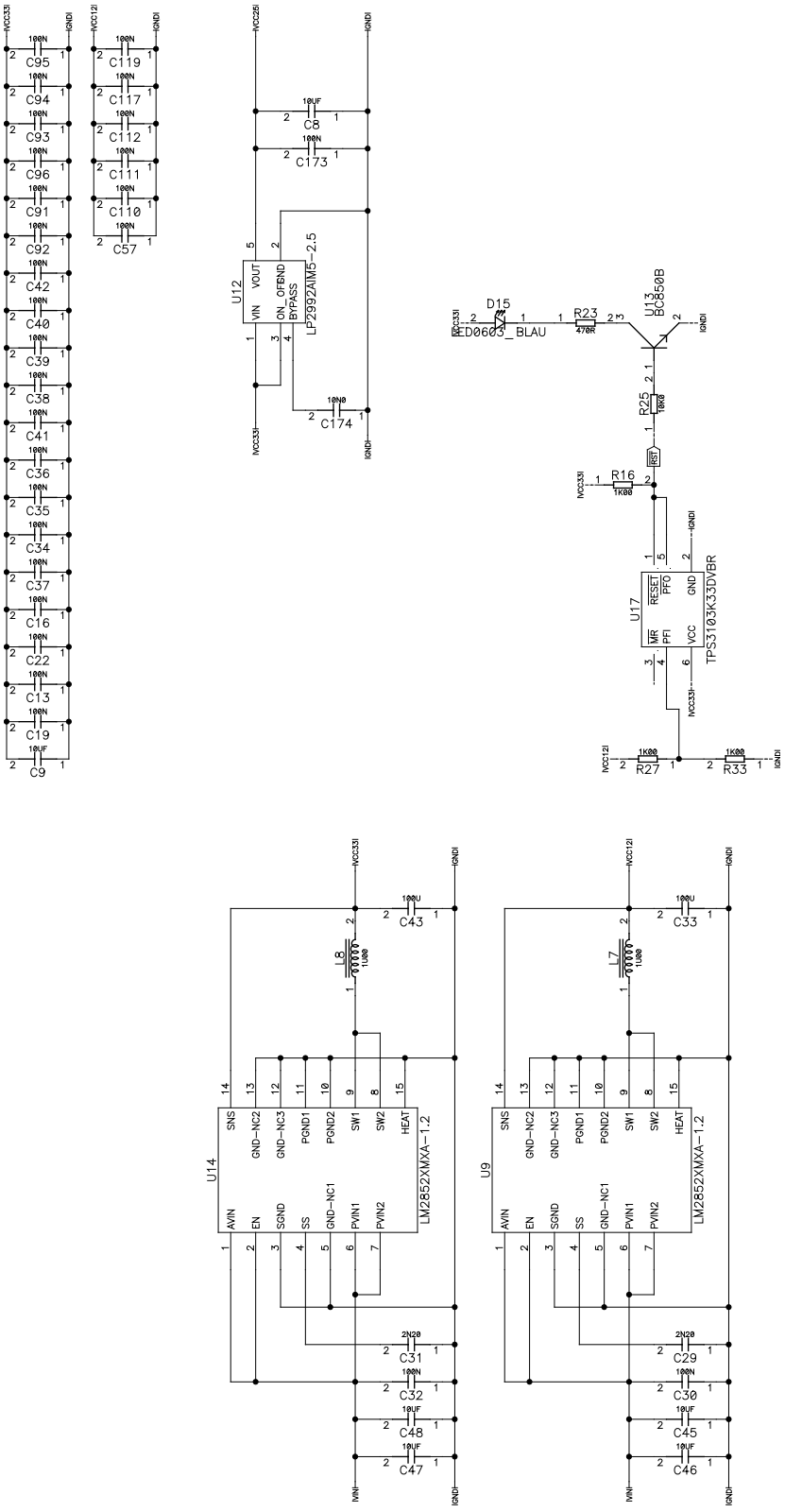
Table 6

Schematics

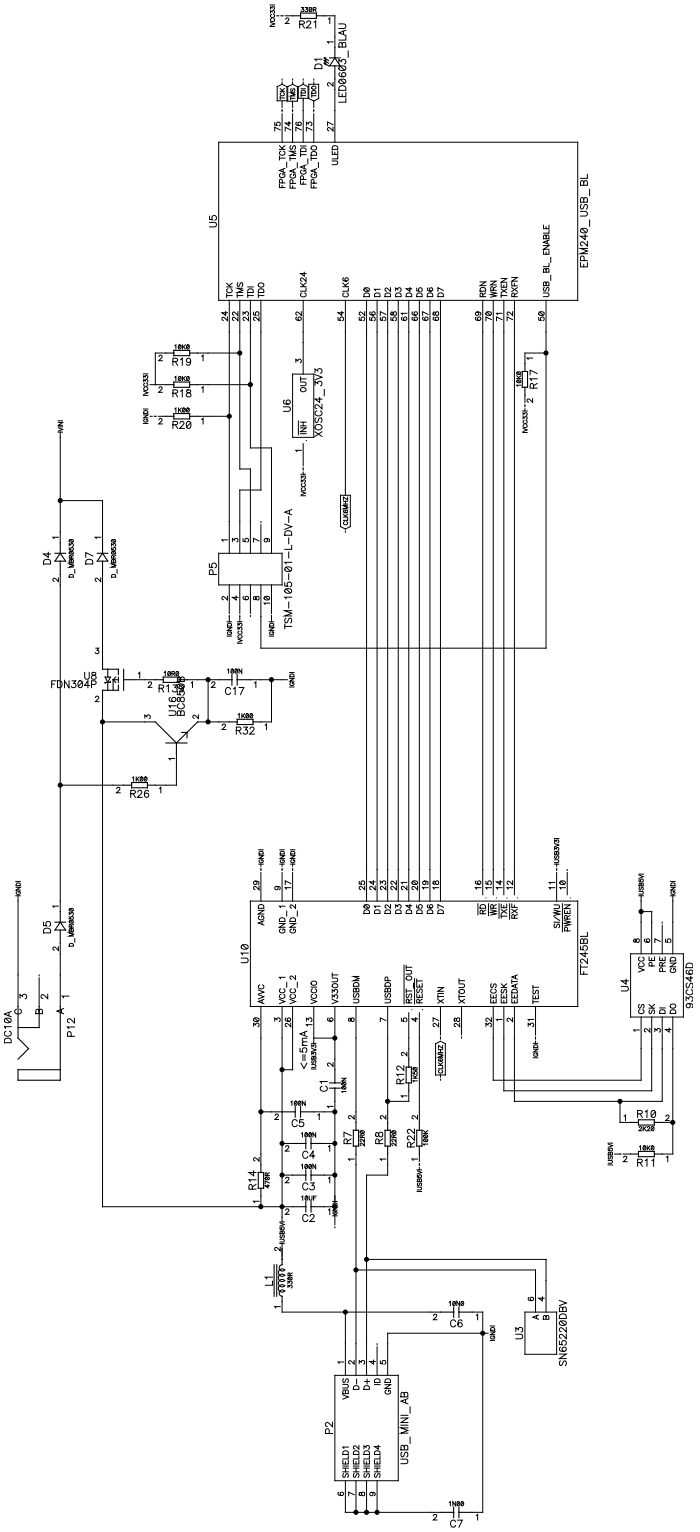
FPGA, Memory, IO



Power Supply



Embedded USB Blaster



Board Top View

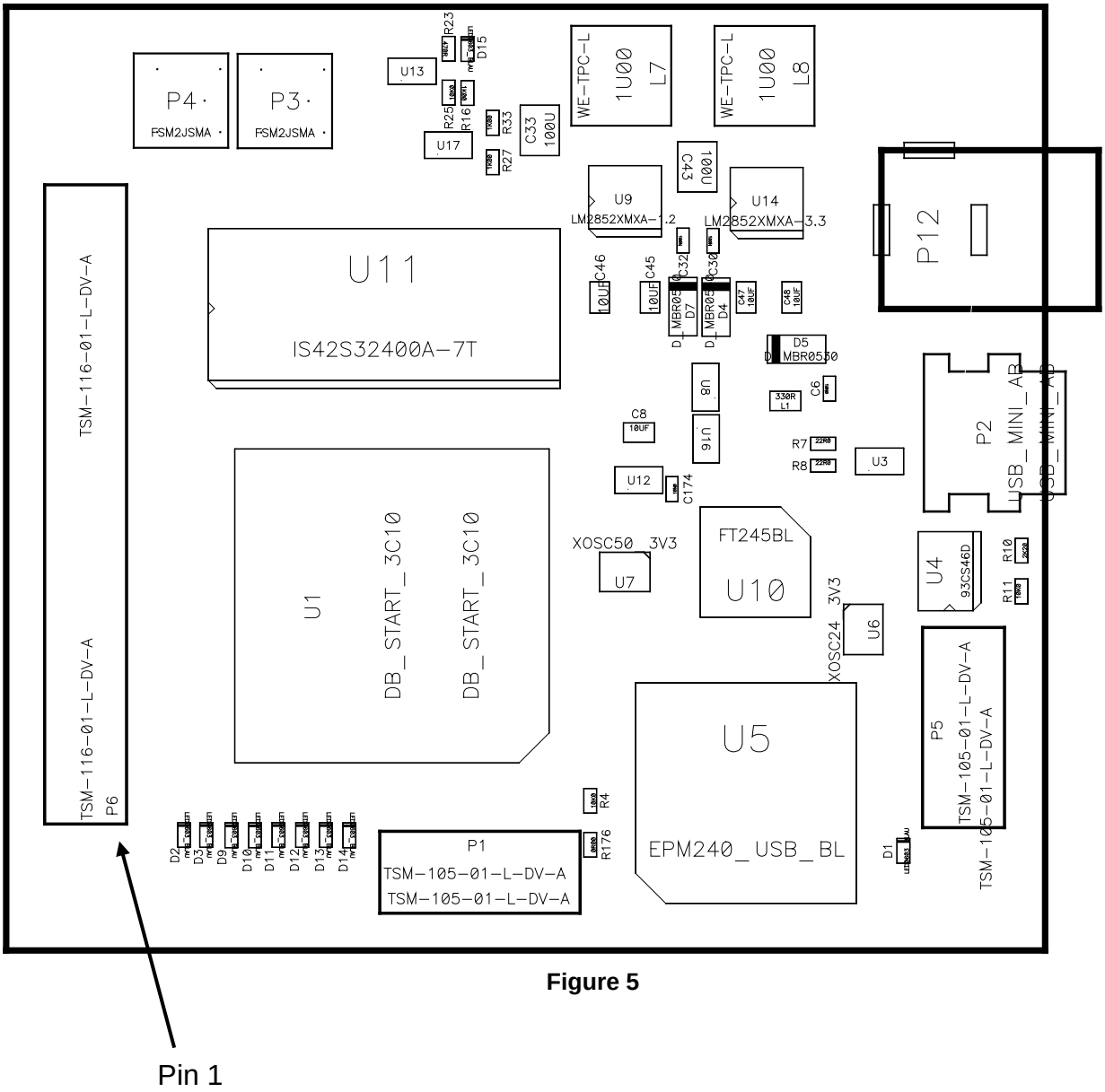


Figure 5

Pin 1

Board Bottom View

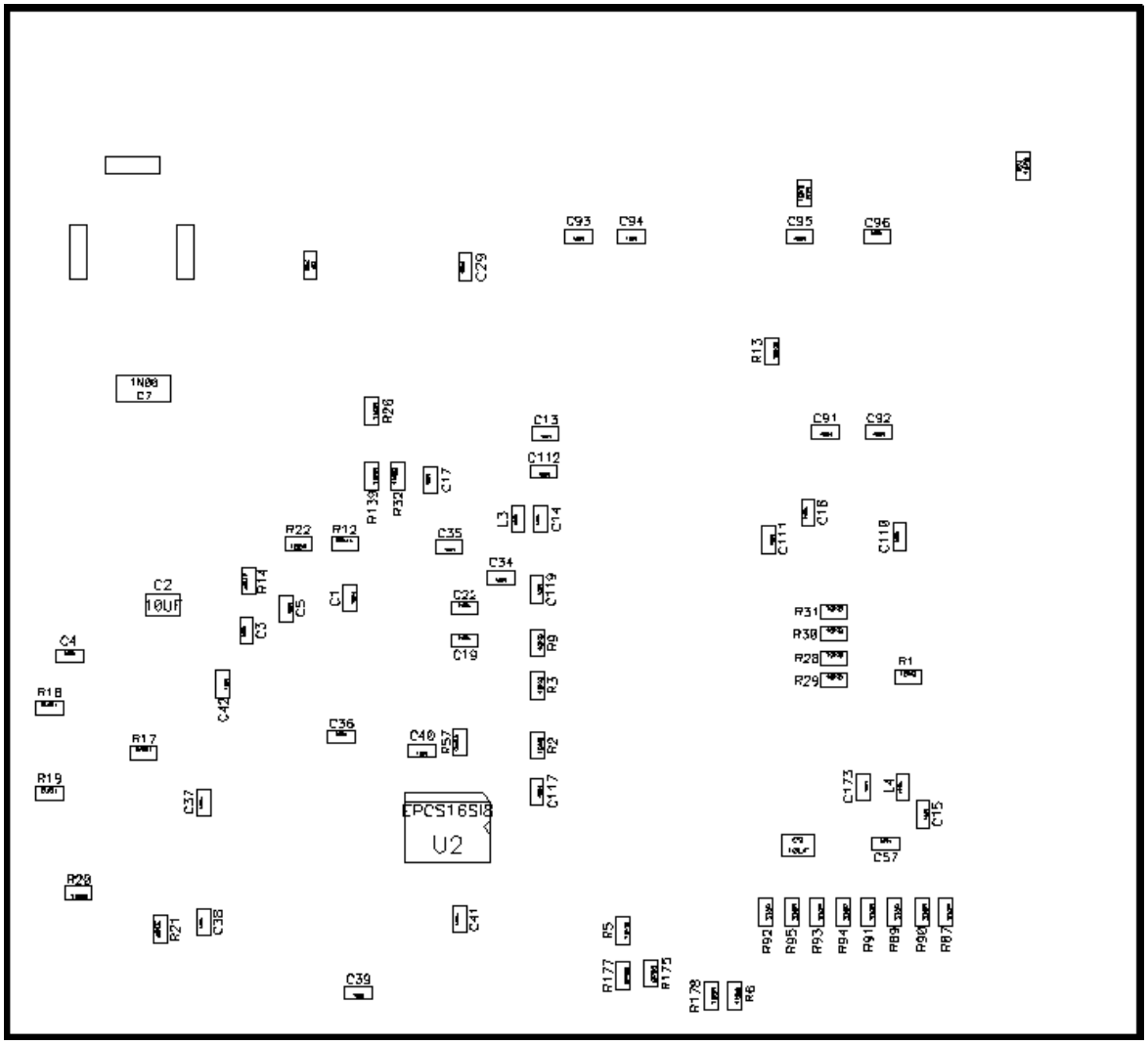


Figure 6