FAIRCHILD SEMICONDUCTOR®

December 2009

FODM8071
3.3V/5V Logic Gate Output Optocoupler with High Noise Immunity

Features

- High noise immunity characterized by common mode rejection
  - 20kV/μs minimum common mode rejection
- High speed
  - 20Mbit/sec date rate (NRZ)
  - 55ns max. propagation delay
  - 20ns max. pulse width distortion
  - 30ns max. propagation delay skew
- 3.3V and 5V CMOS compatibility
- Specifications guaranteed over 3V to 5.5V supply voltage and -40°C to +110°C temperature range
- Safety and regulatory approvals
  - UL1577, 3750 VAC_{RMS} for 1 min.
  - IEC60747-5-2 (pending)

Applications

- Microprocessor system interface
  - SPI, I^2C
- Industrial fieldbus communications
  - DeviceNet, CAN, RS485
- Programmable logic control
- Isolated data acquisition system
- Voltage level translator

Description

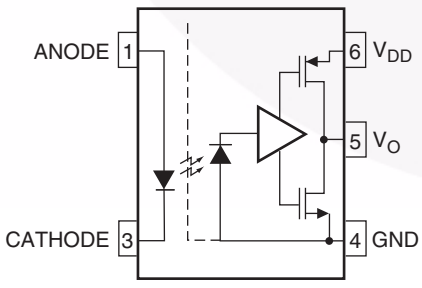
The FODM8071 is a 3.3V/5V high-speed logic gate output Optocoupler, which supports isolated communications allowing digital signals to communicate between systems without conducting ground loops or hazardous voltages. It utilizes Fairchild's patented coplanar packaging technology, Optoplanar®, and optimized IC design to achieve high noise immunity, characterized by high common mode rejection specifications.

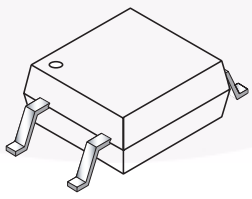
This high-speed logic gate output optocoupler, housed in a compact 5-Pin Mini-Flat package, consists of a high-speed AlGaAs LED at the input coupled to a CMOS detector IC at the output. The detector IC comprises an integrated photodiode, a high-speed transimpedance amplifier and a voltage comparator with an output driver. The CMOS technology coupled with a high efficiency LED achieves low power consumption as well as very high speed (55ns propagation delay, 20ns pulse width distortion).

Related Resources

- www.fairchildsemi.com/products/opto/
- www.fairchildsemi.com/pf/FO/FOD8001.html
- www.fairchildsemi.com/pf/FO/FOD0721.html

Functional Schematic





Truth Table

LED	Output
Off	High
On	Low

©2008 Fairchild Semiconductor Corporation

Pin Definitions

Number	Name	Function Description
1	ANODE	Anode
3	CATHODE	Cathode
4	GND	Output Ground
5	V_O	Output Voltage
6	V_{DD}	Output Supply Voltage

Safety and Insulation Ratings for Mini-Flat Package (SO5 Pin)

As per IEC60747-5-2 (Pending Certification). This optocoupler is suitable for “safe electrical insulation” only within the safety limit data. Compliance with the safety ratings shall be ensured by means of protective circuits.

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Installation Classifications per DIN VDE 0110/1.89 Table 1				
	For rated main voltage < 150Vrms		I-IV		
	For rated main voltage < 300Vrms		I-III		
	Climatic Classification		40/110/21		
	Pollution Degree (DIN VDE 0110/1.89)		2		
CTI	Comparative Tracking Index	175			
V_{PR}	Input to Output Test Voltage, Method b, VIORM x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial Discharge < 5 pC	1060			V
V_{PR}	Input to Output Test Voltage, Method a, VIORM x 1.5 = V_{PR}, Type and Sample Test with t_m = 60 sec, Partial Discharge < 5 pC	848			V
V_{IORM}	Max Working Insulation Voltage	565			V_{peak}
V_{IOTM}	Highest Allowable Over Voltage	4000			V_{peak}
	External Creepage	5.0			mm
	External Clearance	5.0			mm
	Insulation Thickness	0.5			mm
T_{Case}	Safety Limit Values, Maximum Values allowed in the event of a failure, Case Temperature	150			°C
R_{IO}	Insulation Resistance at T_{STG}, V_{IO} = 500V	10^9			Ω

Absolute Maximum Ratings (T_A = 25ºC unless otherwise specified)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. .

Symbol	Parameter	Value	Units
T_{STG}	Storage Temperature	-40 to +125	ºC
T_{OPR}	Operating Temperature	-40 to +110	ºC
T_J	Junction Temperature	-40 to +125	ºC
T_{SOL}	Lead Solder Temperature (Refer to Reflow Temperature Profile)	260 for 10sec	ºC
I_F	Forward Current	20	mA
V_R	Reverse Voltage	5	V
V_{DD}	Supply Voltage	0 to 6.0	V
V_O	Output Voltage	-0.5 to V_{DD}+0.5	V
I_O	Average Output Current	10	mA
PD_I	Input Power Dissipation(1)(3)	40	mW
PD_O	Output Power Dissipation(2)(3)	70	mW

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
T_A	Ambient Operating Temperature	-40	+110	ºC
V_{DD}	Supply Voltages(4)	3.0	5.5	V
V_{FL}	Logic Low Input Voltage	0	0.8	V
I_{FH}	Logic High Input Current	5	16	mA
I_{OL}	Logic Low Output Current	0	7	mA

Isolation Characteristics

(Apply over all recommended conditions, typical value is measured at T_A = 25ºC)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{ISO}	Input-Output Isolation Voltage	freq = 60Hz, t = 1.0min, $I_{I-O} \le 10\mu A$(5)(6)	3750			Vac_{RMS}
R_{ISO}	Isolation Resistance	V_{I-O} = 500V(5)	10^{11}			Ω
C_{ISO}	Isolation Capacitance	V_{I-O} = 0V, freq = 1.0MHz(5)		0.2		pF

Notes:

1. Derate linearly from 95˚C at a rate of -1.4mW/˚C
2. Derate linearly from 100˚C at a rate of -3.47mW/˚C.
3. Functional operation under these conditions is not implied. Permanent damage may occur if the device is subjected to conditions outside these ratings.
4. 0.1µF bypass capacitor must be connected between 4 and 6.
5. Device is considered a two terminal device: Pins 1, and 3 are shorted together and Pins 4, 5, and 6 are shorted together.
6. 3,750 VAC_{RMS} for 1 minute duration is equivalent to 4,500 VAC_{RMS} for 1 second duration.

Electrical Characteristics (Apply over all recommended conditions)

(T_A = -40ºC to +110ºC, 3.0V ≤ V_{DD} ≤ 5.5V), unless otherwise specified.
Typical value is measured at T_A = 25ºC and V_{DD} = 3.3V.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
INPUT CHARACTERISTICS						
V_F	Forward Voltage	I_F = 10mA, Fig. 1	1.05	1.35	1.8	V
BV_R	Input Reverse Breakdown Voltage	I_R = 10µA	5	15		V
I_{FHL}	Threshold Input Current	Fig. 2		2.8	5	mA
OUTPUT CHARACTERISTICS						
I_{DDL}	Logic Low Output Supply Current	V_{DD} = 3.3V, I_F = 10mA, Fig. 3, 5		3.3	4.8	mA
		V_{DD} = 5.0V, I_F = 10mA, Fig. 3, 6		4.0	5.0	mA
I_{DDH}	Logic High Output Supply Current	V_{DD} = 3.3V, I_F = 0mA, Fig. 4		3.3	4.8	mA
		V_{DD} = 5.0V, I_F = 0mA, Fig. 4		4.0	5.0	mA
V_{OH}	Logic High Output Voltage	V_{DD} = 3.3V, I_O = -20µA, I_F = 0mA	V_{DD} – 0.1V	3.3		V
		V_{DD} = 3.3V, I_O = -4mA, I_F = 0mA	V_{DD} – 0.5V	3.1		V
		V_{DD} = 5.0V, I_O = -20µA, I_F = 0mA	V_{DD} – 0.1V	5.0		V
		V_{DD} = 5.0V, I_O = -4mA, I_F = 0mA	V_{DD} – 0.5V	4.9		V
V_{OL}	Logic Low Output Voltage	I_O = 20µA, I_F = 10mA		0.0027	0.01	V
		I_O = 4mA, I_F = 10mA		0.27	0.8	V

Switching Characteristics (Apply over all recommended conditions)

(T_A = -40ºC to +110ºC, 3.0V ≤ V_{DD} ≤ 5.5V, I_F = 5mA), unless otherwise specified.
Typical value is measured at T_A = 25ºC and V_{DD} = 3.3V

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
Date Rate(7)					20	Mbps
t_{PW}	Pulse Width		50			ns
t_{PHL}	Propagation Delay Time to Logic Low Output	C_L = 15pF, Fig. 7, 8, 12		31	55	ns
t_{PLH}	Propagation Delay Time to Logic High Output	C_L = 15pF, Fig. 7, 8, 12		25	55	ns
PWD	Pulse Width Distortion, $\lvert t_{PHL} - t_{PLH} \rvert$	C_L = 15pF, Fig. 9, 10		5.5	20	ns
t_{PSK}	Propagation Delay Skew	C_L = 15pF(8)			30	ns
t_R	Output Rise Time (10% to 90%)	Fig. 11, 12		5.8		ns
t_F	Output Fall Time (90% to 10%)	Fig. 11, 12		5.3		ns
$\lvert CM_H \rvert$	Common Mode Transient Immunity at Output High	I_F = 0mA, V_O > 0.8V_{DD}, V_{CM} = 1000V, T_A = 25ºC, Fig. 13(9)	20	40		kV/µs
$\lvert CM_L \rvert$	Common Mode Transient Immunity at Output Low	I_F = 5mA, V_O < 0.8V, V_{CM} = 1000V, T_A = 25ºC, Fig. 13(9)	20	40		kV/µs
C_{PDO}	Output Dynamic Power Dissipation Capacitance(10)			4		pF

Notes:

7. Data rate is based on 10MHz, 50% NRZ pattern with a 50nsec minimum bit time.
8. t_{PSK} is equal to the magnitude of the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between any two units from the same manufacturing date code that are operated at same case temperature (±5°C), at same operating conditions, with equal loads (R_L = 350Ω and C_L = 15pF), and with an input rise time less than 5ns.
9. Common mode transient immunity at output high is the maximum tolerable positive dVcm/dt on the leading edge of the common mode impulse signal, Vcm, to assure that the output will remain high. Common mode transient immunity at output low is the maximum tolerable negative dVcm/dt on the trailing edge of the common pulse signal, Vcm, to assure that the output will remain low.
10. Unloaded dynamic power dissipation is calculated as follows: C_{PD} x V_{DD} x *f* + I_{DD} + V_{PD} where *f* is switched time in MHz.

©2008 Fairchild Semiconductor Corporation

Typical Performance Curves (Continued)

Fig. 1 Input Forward Current vs. Forward Voltage

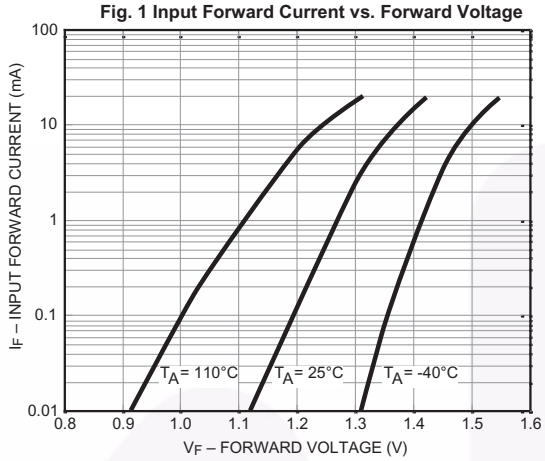


Fig. 2 Input Threshold Current vs. Ambient Temperature

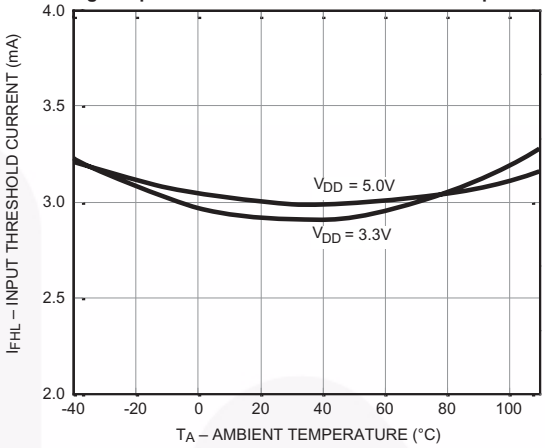


Fig 3. Logic Low Output Supply Current vs. Ambient Temperature

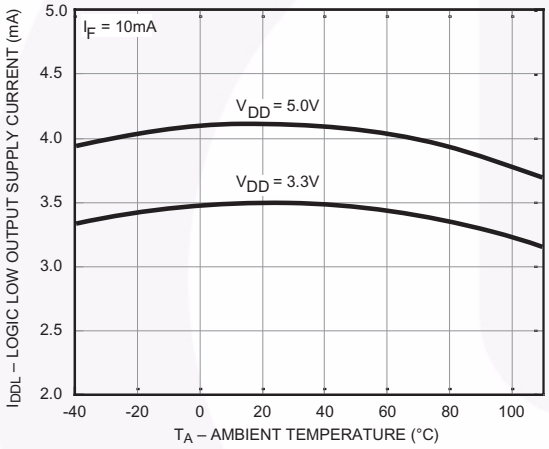


Fig 4. Logic High Output Supply Current vs. Ambient Temperature

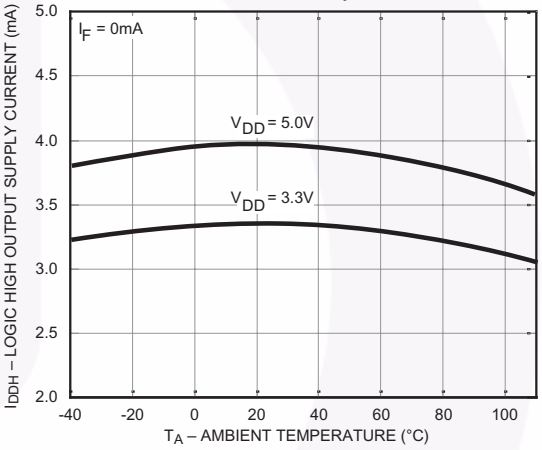


Fig. 5 Dynamic Logic Low Output Supply Current vs. Input Frequency (V_{DD} = 3.3V)

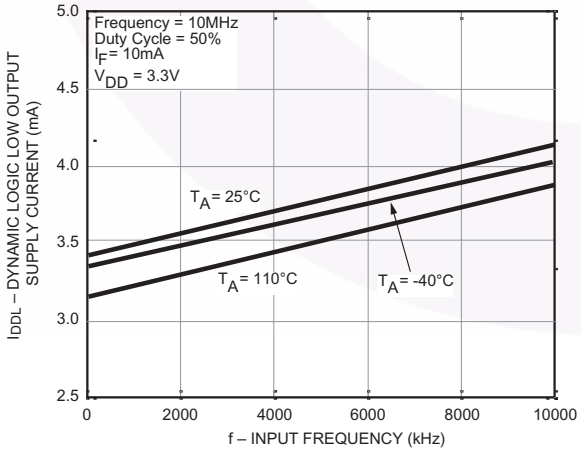
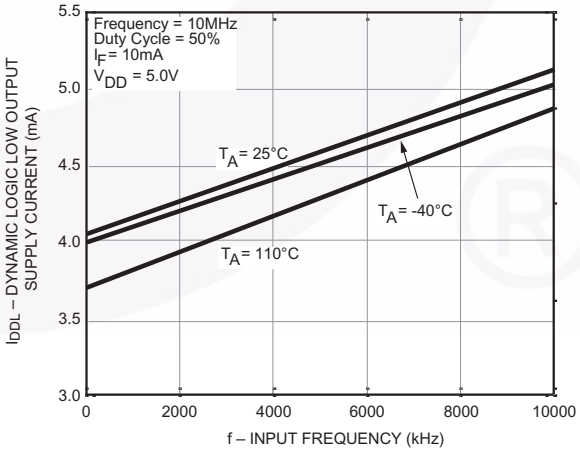


Fig. 6 Dynamic Logic Low Output Supply Current vs. Input Frequency (V_{DD} = 5.0V)



Typical Performance Curves (Continued)

Fig 7. Propagation Delay vs. Ambient Temperature

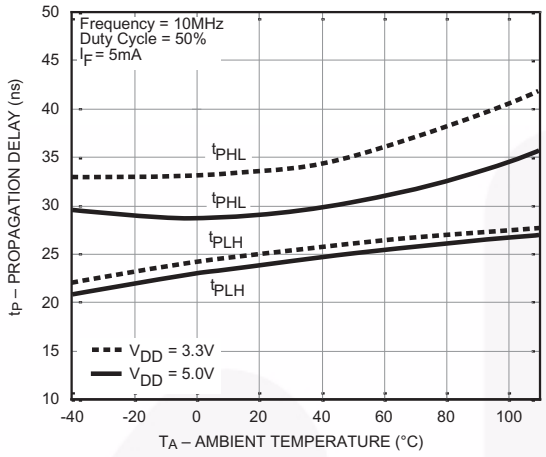


Fig 8. Propagation Delay vs. Pulse Input Current

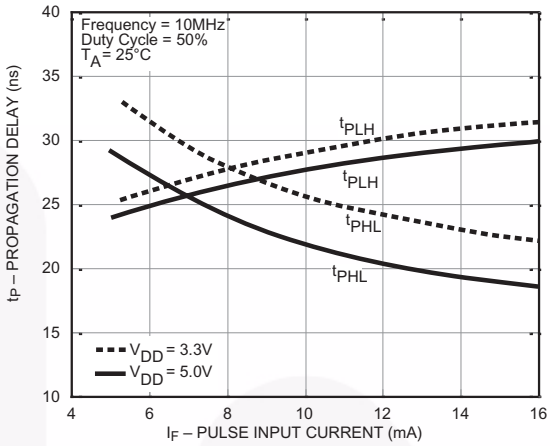


Fig 9. Pulse Width Distortion vs. Ambient Temperature

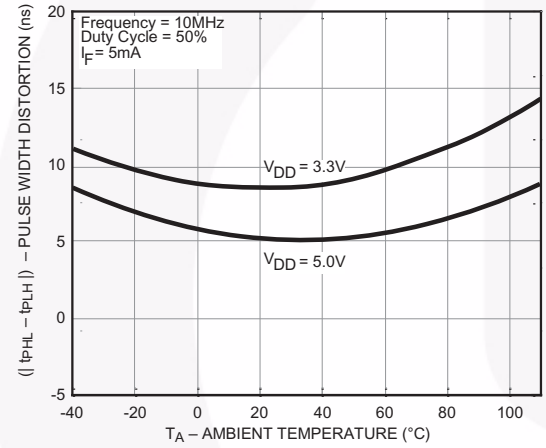


Fig 10. Pulse Width Distortion vs Pulse Input Current

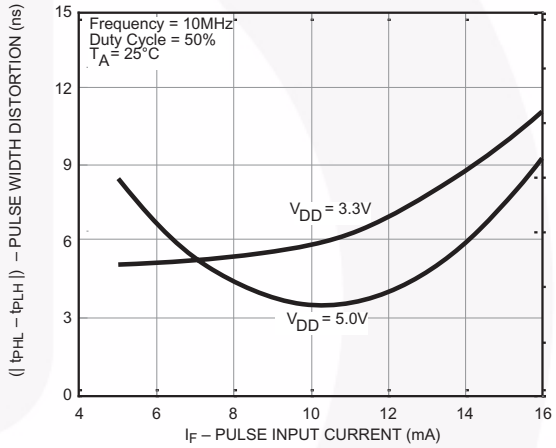
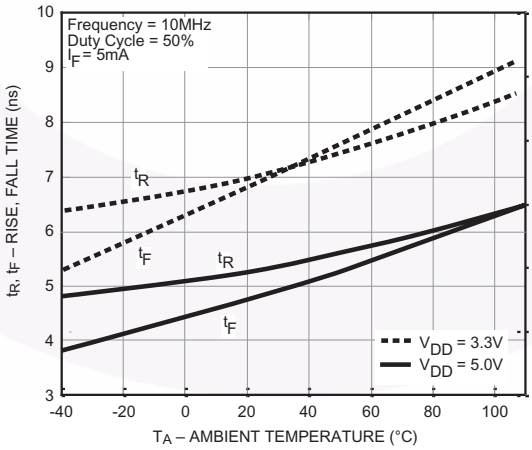


Fig 11. Rise and Fall Time vs. Ambient Temperature



Schematics

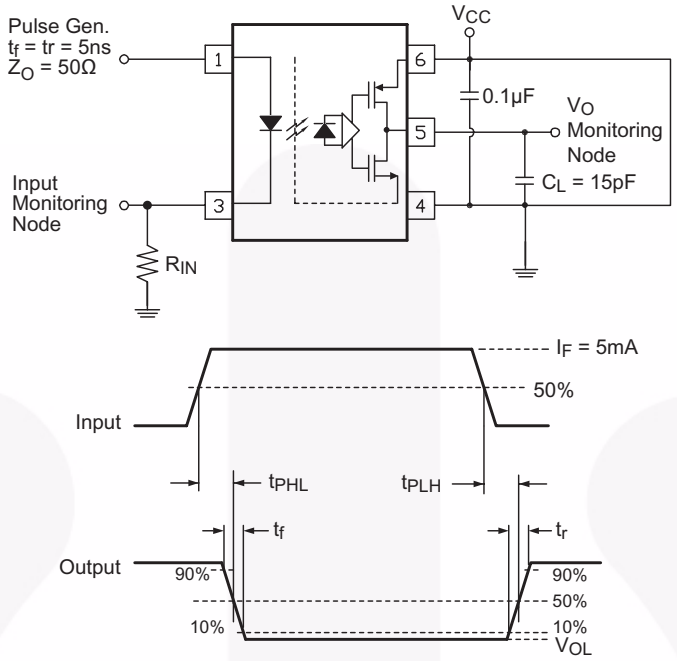


Figure 12. Test Circuit for Propagation Delay Time, Rise Time and Fall Time

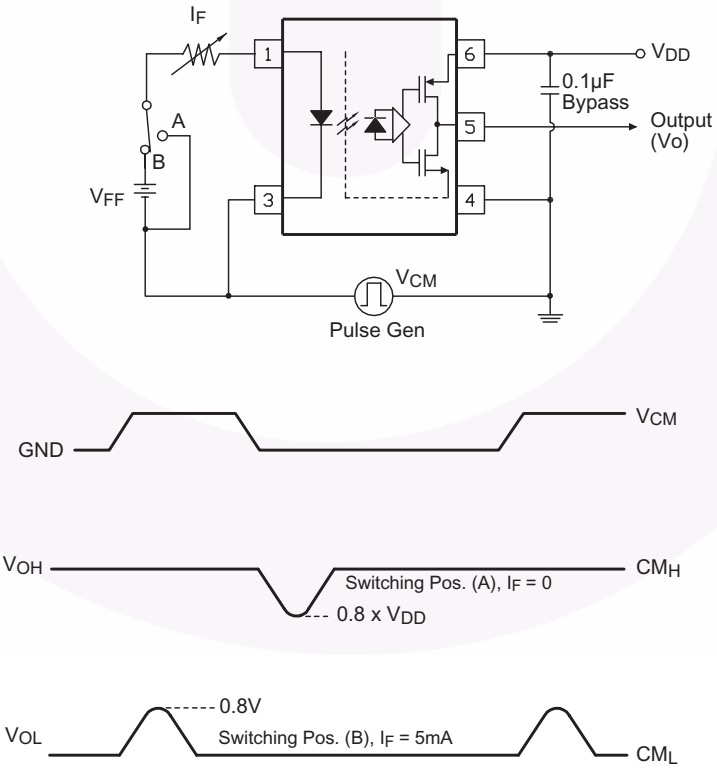
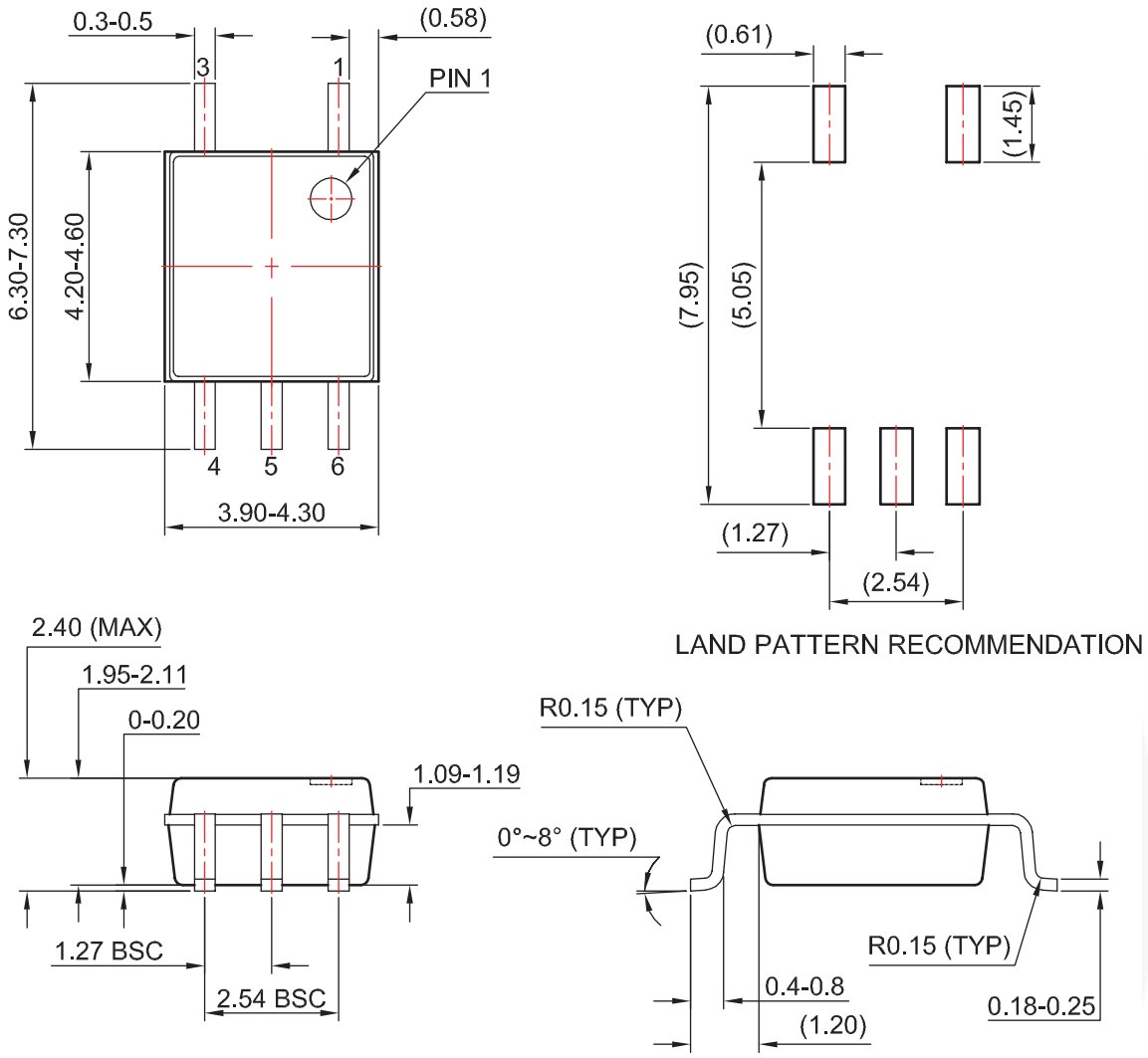


Figure 13. Test Circuit for Instantaneous Common Mode Rejection Voltage

Package Dimensions



Notes:

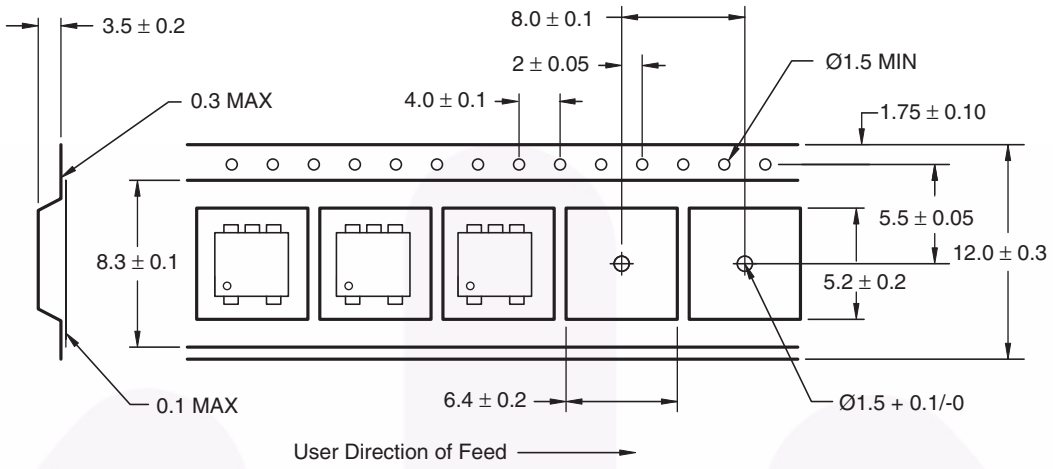
1. No standard applies to this package.
2. All dimensions are in millimeters.
3. Dimensions are exclusive of burrs, mold flash, and tie bar extrusion.
4. Drawings filesname and revision: MKT-MFP05A.

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

http://www.fairchildsemi.com/packaging/

Carrier Tape Specification



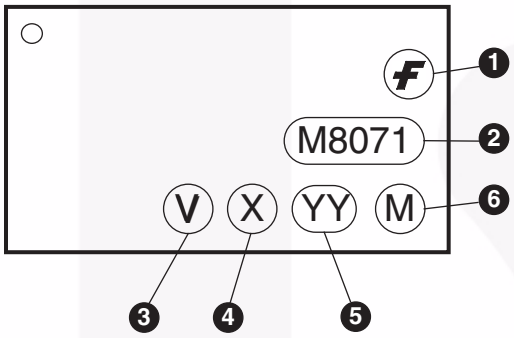
Note:
All dimensions are in millimeters.

Ordering Information

Option	Order Entry Identifier	Description
No Suffix	FODM8071	Mini-Flat 5-pin, shipped in tubes (100 units per tube)
R2	FODM8071R2	Mini-Flat 5-pin, tape and reel (2,500 units per reel)

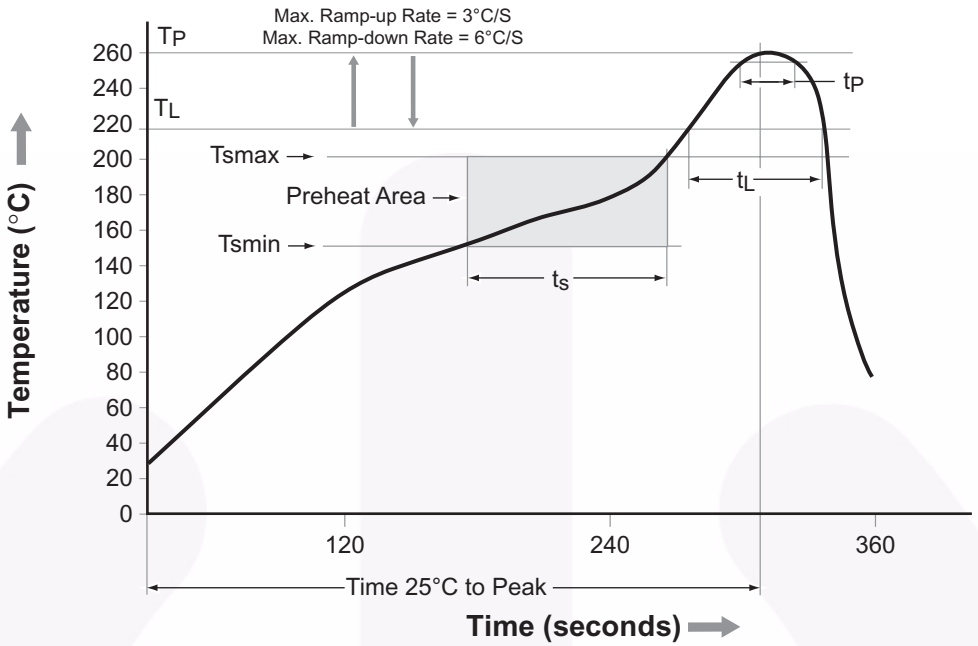
All packages are lead free per JEDEC: J-STD-020B standard.

Marking Information



Definitions	
1	Fairchild logo
2	Device number
3	IEC60747-5-2 (VDE marking)
4	One digit year code, e.g., ‘9’
5	Two digit work week ranging from ‘01’ to ‘53’
6	Assembly package code

Reflow Profile



Profile Feature	Pb-Free Assembly Profile
Temperature Min. (Tsmin)	150°C
Temperature Max. (Tsmax)	200°C
Time (t_S) from (Tsmin to Tsmax)	60–120 seconds
Ramp-up Rate (t_L to t_P)	3°C/second max.
Liquidous Temperature (T_L)	217°C
Time (t_L) Maintained Above (T_L)	60–150 seconds
Peak Body Package Temperature	260°C +0°C / –5°C
Time (t_P) within 5°C of 260°C	30 seconds
Ramp-down Rate (T_P to T_L)	6°C/second max.
Time 25°C to Peak Temperature	8 minutes max.

FAIRCHILD SEMICONDUCTOR®

TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

AccuPower™
Auto-SPM™
Build it Now™
CorePLUS™
CorePOWER™
CROSSVOLT™
CTL™
Current Transfer Logic™
DEUXPEED®
Dual Cool™
EcoSPARK®
EfficientMax™
EZSWITCH™*
EZ™*
F®
Fairchild®
Fairchild Semiconductor®
FACT Quiet Series™
FACT®
FAST®
FastvCore™
FETBench™
FlashWriter®*
FPS™
F-PFS™
FRFET®
Global Power Resource SM
Green FPS™
Green FPS™ e-Series™
G*max*™
GTO™
IntelliMAX™
ISOPLANAR™
MegaBuck™
MICROCOUPLER™
MicroFET™
MicroPak™
MillerDrive™
MotionMax™
Motion-SPM™
OPTOLOGIC®
OPTOPLANAR®
®
PDP SPM™
Power-SPM™
PowerTrench®
PowerXS™
Programmable Active Droop™
QFET®
QS™
Quiet Series™
RapidConfigure™
™
Saving our world, 1mW/W/kW at a time™
SignalWise™
SmartMax™
SMART START™
SPM®
STEALTH™
SuperFET™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SupreMOS™
SyncFET™
Sync-Lock™
SYSTEM GENERAL ®*
The Power Franchise®
the power franchise
TinyBoost™
TinyBuck™
TinyCalc™
TinyLogic®
TINYOPTO™
TinyPower™
TinyPWM™
TinyWire™
TriFault Detect™
TRUECURRENT™*
µSerDes™
SerDes™
UHC®
Ultra FRFET™
UniFET™
VCX™
VisualMax™
XS™

* Trademarks of System General Corporation, used under license by Fairchild Semiconductor.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, www.fairchildsemi.com, under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I45