FT 5000 Smart Transceiver
Model 14235R

- 3.3V operation
- Higher Performance Neuron Core – Internal system clock scales up to 40 MHz
- Significant node cost reduction
- Serial interface for inexpensive external EEPROM and flash non-volatile memories
- Supports up to 254 Network Variables (NVs)
- Low-cost surface mount FT-X3 Communications Transformer
- User programmable interrupts provide faster response time to external events
- 7 mm by 7 mm 48-pin QFN package
- Supports polarity insensitive free topology star, daisy chain, bus, loop, or mixed topology wiring
- Compliant with TP/FT-10 channels using FT 3120®/ FT 3150® Smart Transceivers and FTT-10 / FTT-10A / LPT-10 / LPT-11 Transceivers
- 12 I/O pins with 35 programmable standard I/O modes
- Supports up to 42 KB of application code space
- 64 KB RAM (44 KB user accessible) and 16KB ROM on-chip memories
- Unique 48-bit Neuron ID in every device for network installation and management
- Very high common-mode noise immunity
- -40°C to +85°C operating temperature range

Description

The FT 5000 Smart Transceiver is the next generation Echelon Free Topology Smart Transceiver integrating a high performance Neuron® Core with a free topology twisted-pair transceiver. Combined with a new low-cost FT-X3 Communications Transformer and inexpensive serial memories, the FT 5000 Smart Transceiver provides a lower cost, higher performance LonWorks® solution compared to those based on previous generation FT Smart Transceivers.

LonWorks networks are ideal as control networks for building, industrial, transportation, home, utility, and other automation applications.

The FT 5000 Smart Transceiver includes three independent 8-bit logical processors to manage the physical MAC layer, the network, and the user application. These are called the Media-Access Control (MAC) processor, the network (NET) processor and the application (APP) processor respectively (see Figure 1). At higher system clock rates, there is also a fourth processor to handle interrupts.

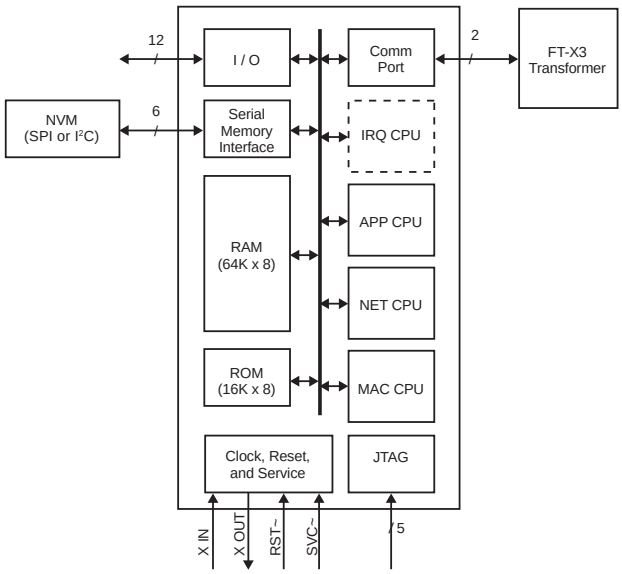

Figure 1: FT 5000 Smart Transceiver Chip Block Diagram

The FT 5000 Smart Transceiver supports polarity insensitive cabling using a star, bus, daisy-chain, loop, or combination topology (see Figure 2). This frees the installer from the need to adhere to a strict set of wiring rules as imposed by other networking technologies. Free topology wiring reduces the time and expense of device installation by allowing the wiring to be installed in the most expeditious and cost-effective manner. It also simplifies network expansion by eliminating restrictions on wire routing, splicing, and device placement.

The FT-X3 Communications Transformer is a surface mount communication transformer that is compatible both with the new FT 5000 Smart Transceiver and the previous generation FT 3120/ FT 3150 Smart Transceivers. The FT-X3 Communications Transformer provides equivalent noise immunity to both the FT-X1 and FT-X2 Communication Transformers, the previous generation communication transformers. However, the FT-X3 Communications Transformer is not pin compatible with the FT-X2 Communication Transformer, which is also a surface mount transformer. The FT 5000 Smart Transceiver can also be used with the FT-X1 and FT-X2 Communication Transformers.

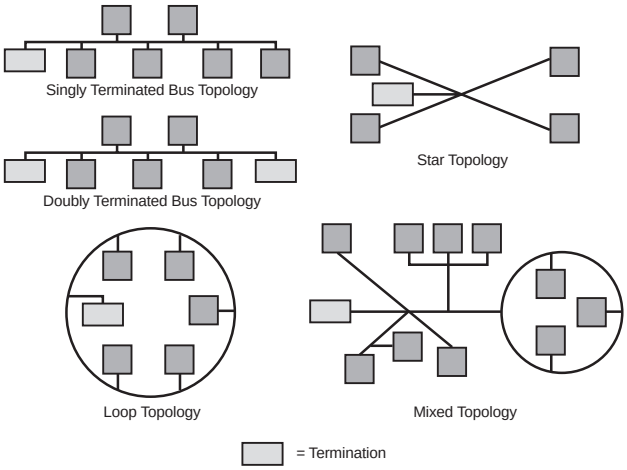

Figure 2: Free Topology Network Configurations

Backward Compatibility

The FT 5000 Smart Transceiver is fully compliant with the TP/FT-10 channel and can communicate with devices that use Echelon's FTT-10/FTT-10A Transceivers, FT 3120/FT 3150 Smart Transceivers, or LPT-10/LPT-11 Link Power Transceiver.

The Neuron Core in the FT 5000 Smart Transceiver uses the same instruction set architecture as the previous generation Neuron Core, but with two new additional instructions for hardware multiplication and division. It is backward compatible with applications written for previous-generation Neuron Chips and Smart Transceivers. However, the old applications need to be recompiled with the latest versions of the NodeBuilder® Development Tool or Mini EVK Evaluation Kit before they can be used with the FT 5000 Smart Transceiver.

The FT 5000 Smart Transceiver uses new firmware, version 18. Older firmware versions are not compatible with the FT 5000 Smart Transceiver. The Neuron firmware is pre-programmed into the on-chip ROM. The FT 5000 Smart Transceiver can also be configured to read newer firmware from external memories, allowing the firmware to be upgraded over time.

Enhanced Performance

Faster System Clock

The internal system clock for the FT 5000 Smart Transceiver can be user configured to run from 10 MHz to 40 MHz. The required external crystal provides a 10 MHz clock frequency, and an internal PLL boosts the frequency to a maximum of 40 MHz as the internal system clock speed. The previous generation Neuron 3120/3150 Core divided the external oscillator frequency by two to create the internal system clock. An FT 5000 Smart Transceiver running with a 40 MHz internal clock is thus 8 times faster than a 10 MHz Neuron 3120/3150 Core.

The Neuron Core inside the FT 5000 Smart Transceiver includes a hardware multiplier and divider built in to increase performance of arithmetic operations.

Support for More Network Variables

The FT 5000 Smart Transceiver supports up to 254 Network Variables (NVs), substantially more than the 62 NVs supported by the Neuron 3120/3150 Core. The use of a ShortStack® Micro Server with a host microcontroller is not required to define 254 NVs with the FT 5000 Smart Transceiver. However, the FT 5000 Smart Transceiver can run new or existing ShortStack applications.

Interrupts

The FT 5000 Smart Transceiver allows a developer to define user interrupts to handle asynchronous events related to I/O objects. There are also system-level exceptions and internal traps, which have higher priority than user-defined interrupts.

JTAG

The FT 5000 Smart Transceiver provides an interface for the Institute of Electrical and Electronics Engineers (IEEE) Standard Test Access Port and Boundary-Scan Architecture (IEEE 1149.1-1990) of the Joint Test Action Group (JTAG). A Boundary Scan Description Language (BSDL) file for the FT 5000 Smart Transceiver will be available for download from the Echelon Web site.

I/O Pins and Counters

The FT 5000 Smart Transceiver provides 12 bidirectional I/O pins that are 5V tolerant and can be configured to operate in one or more of 35 predefined standard input/output modes. The chip also has two 16-bit timer/counters that reduce the need for external logic and software development.

Memory Architecture

The FT 5000 Smart Transceiver memory architecture is very different from that in the previous generation FT Smart Transceivers and Neuron Chips. It has 16 KB of read-only memory (ROM) and 64 KB (44 KB user accessible) of random access memory (RAM) on the chip. It has no on-chip non-volatile memory (EEPROM or flash) for application use. Each chip however contains its unique Neuron identifier (Neuron ID) in an on-chip non-volatile read-only memory.

The FT 5000 Smart Transceiver uses a serial memory interface for external non-volatile memories (EEPROM or flash). The application code and configuration data are stored in the external non-volatile memory (NVM) and copied into the internal RAM during device reset; the instructions then execute from internal RAM. Writes to NVM are shadowed in the internal RAM and pushed out to external NVM by the system firmware (see Figure 2). The application does not need to manage NVM directly.

External Memories Supported

The FT 5000 Smart Transceiver supports two serial interfaces for accessing off-chip non-volatile memories: serial Inter-

Integrated Circuit (I^2C) and serial peripheral interface (SPI). EEPROM devices can use either the I^2C interface or the SPI interface; flash memory devices must use the SPI interface.

External serial EEPROMs and flash devices are low-cost and available from multiple vendors in very small form factors.

The FT 5000 Smart Transceiver requires at least 2 KB of off-chip memory available in an EEPROM device to store the configuration data. The application code can be stored either in the EEPROM (by using a larger capacity EEPROM device) or in a flash memory device used in addition to the EEPROM. Thus, the external memory for FT 5000 Smart Transceiver has one of the following configurations listed in Table 1:

Configuration	EEPROM		Flash	Notes
	I^2C	SPI	SPI	
1	☑			A single I^2C EEPROM memory device, from 2 KB to 64 KB in size
2	☑		☑	One I^2C EEPROM (at least 2 KB in size, up to 64 KB in size, but the system uses only the first 2 KB of the EEPROM memory) One SPI flash memory device
3		☑		A single SPI EEPROM memory device, from 2 KB to 64 KB in size
4		☑	☑	One SPI EEPROM (at least 2 KB in size, up to 64 KB in size, but the system uses only the first 2 KB of the EEPROM memory) One SPI flash memory device

Table 1: Allowed External Memory Device Configurations

As Table 1 shows, the FT 5000 Smart Transceiver supports using a single EEPROM memory device, or a single EEPROM memory device plus a single flash memory device.

If the FT 5000 Smart Transceiver includes flash memory, the flash memory represents the entire user non-volatile memory for the device. That is, any additional EEPROM memory beyond the mandatory 2 KB is not used.

Using the I^2C Interface

When using the I^2C interface for external EEPROM, the FT 5000 Smart Transceiver is always the master I^2C device (see Figure 3). The clock speed supported for the I^2C serial memory interface is 400 kHz (fast I^2C mode). The I^2C memory device must specify I^2C address 0. Both 1-byte and 2-byte address modes are supported, but 3-byte addressing mode is not supported.

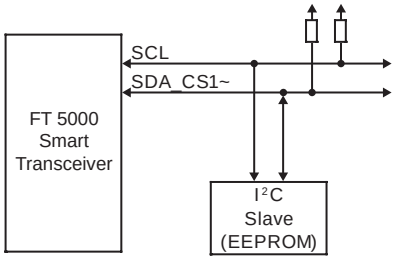

Figure 3: Using the I^2C Interface for External NVM EEPROM Memory

Using the SPI Interface

The FT 5000 Smart Transceiver is always the master SPI device; any external NVM devices are always slave devices. The FT 5000 Smart Transceiver can support up to two SPI slave devices from the serial memory interface: one EEPROM device at CS0~ and one flash device at CS1~ (see Figure 4). The FT 5000 Smart Transceiver supports 2-byte addressing mode for SPI EEPROM devices, but does not support 3-byte addressing. The FT 5000 Smart Transceiver runs the SPI protocol from the serial memory interface at 2.5 MHz and supports SPI Mode 0. In Mode 0, the base value of the clock is zero; the data is read on the clock's rising edge and changed on the clock's falling edge. Most external NVMs support SPI Mode 0 and 3.

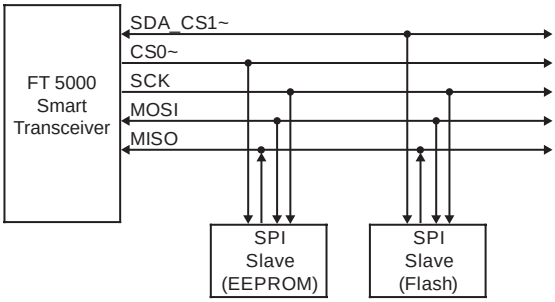

Figure 4: Using the SPI Interface for External NVM Memories

Using Both I^2C and SPI Interfaces

Figure 5 shows an FT 5000 Smart Transceiver that includes both an I^2C memory device (a 2 KB EERPOM device) and a SPI memory device (a flash memory device). Although both EEPROM and flash memory share the SDA_CS1~ pin, there is no conflict because only one of them can be active at a time. SDA is an active high signal and CS1~ is an active low signal. While small applications could use EEPROM both for application code and configuration data, larger applications might find it economical to use a small EEPROM for configuration data and a flash device for application code. The choice between EEPROM and flash can be affected by multiple factors, including:

- Use of single external memory versus two memories
- Cost comparison between a large EEPROM device and a combination of a small EEPROM and large flash devices
- Use of non-volatile variables by the application, which can require a large number of writes to the device

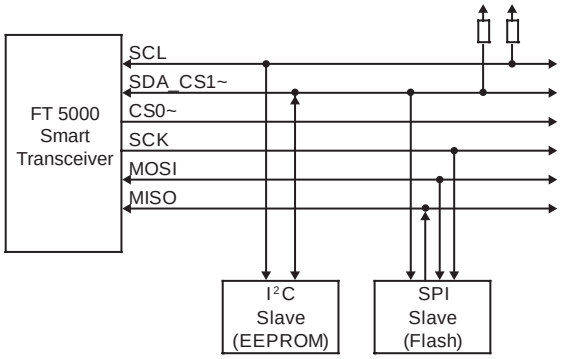

Figure 5: Using Both I^2C and SPI Interfaces for External NVM Memories

Memory Devices Supported

The FT 5000 Smart Transceiver supports any EEPROM device that uses the SPI or I^2C protocol, and meets the clock speed and addressing requirements described above.

While all EEPROM devices have a uniform write procedure, flash devices from various manufacturers differ slightly in their write procedure. Thus, a small library routine is stored in the external EEPROM device that helps the system write successfully to the external flash device. Echelon has qualified the following SPI flash memory devices for use with the FT 5000 Smart Transceiver:

- Atmel® AT25F512B 512-Kilobit 2.7-volt Minimum SPI Serial Flash Memory
- Numonyx™ M25P05-A 512-Kbit, serial flash memory, 50 MHz SPI bus interface
- Silicon Storage Technology SST25VF512A 512 Kbit SPI Serial Flash

Additional devices may be qualified in the future.

Memory Map

A Neuron C device has a memory map of 64 KB. A Neuron C application program uses this memory map to organize its memory and data access. The memory map is a logical view of device memory, rather than a physical view, because the chip's processors only directly access RAM. The memory map divides the FT 5000 Smart Transceiver's physical 64 KB RAM into the following types of logical memory, as shown in Figure 6:

- System firmware image (stored in on-chip ROM or external NVM).
- On-chip RAM or NVM. Memory ranges for each are configurable within the device hardware template. The non-volatile memory represents the area shadowed from external NVM into the RAM.
- On-chip RAM for stack segments and RAMNEAR data.
- Mandatory external EEPROM that holds configuration data and non-volatile application variables.
- Reserved space for system use.

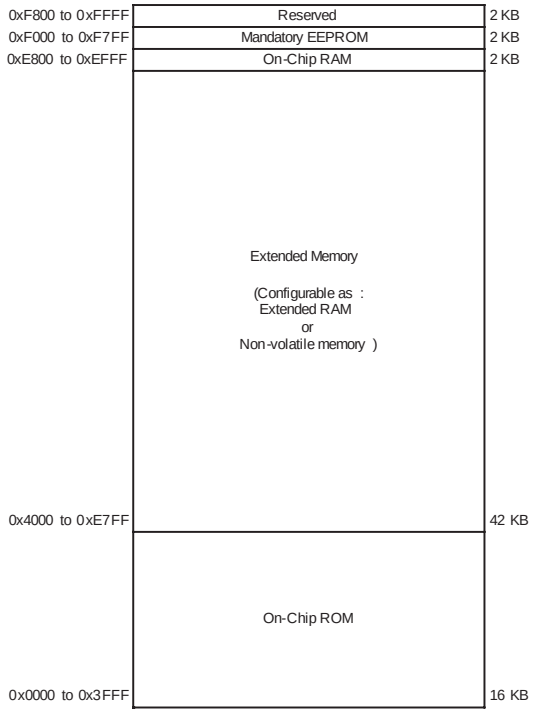

Figure 6: FT 5000 Smart Transceiver Memory Map

If a 64 KB external serial EEPROM or flash device is used, the maximum allowed size of application code is 42 KB as defined by extended NVM area in the memory map. Additional 16 KB of the remaining space can hold an external system firmware image in case firmware upgrade is required.

Programming Memory Devices

Because the FT 5000 Smart Transceiver does not have any on-chip user-accessible NVM, only the external serial EEPROM or flash devices need to be programmed with the application and configuration data. The memory devices can be programmed in any of the following three ways:

- In-circuit programming on the board
- Over the network
- Pre-programming before soldering on the board

Easy interface to Any Host MCU

The FT 5000 Smart Transceiver can easily interface with other host MCUs via Echelon's ShortStack Micro Server. When used with ShortStack, the FT 5000 Smart Transceiver enables any OEM product with a host microcontroller to quickly and inexpensively become a networked, Internet accessible device. The ShortStack firmware uses a serial interface (using GPIO SCI or SPI pins) to communicate between the host and the Smart Transceiver. ShortStack Micro Server is a royalty-free download from Echelon web site. Visit www.echelon.com/shortstack for more information.

For a very high-performance hosted LonWorks solution, visit www.echelon.com/ftxl and read about the FTXL™ 3190 Free Topology Transceiver.

Noise Immunity

A LonWorks device based on the FT 5000 Smart Transceiver is composed of two components—the FT 5000 IC and an external communications transformer (the FT-X3). The transformer enables operation in the presence of high frequency common-mode noise on unshielded twisted-pair networks. Properly designed devices can meet the rigorous Level 3 requirements of EN 61000-4-6 without the need for a network isolation choke. The transformer also offers outstanding immunity from magnetic noise, eliminating the need for protective magnetic shields in most applications.

The FT 5000 Smart Transceiver and the FT-X3 Communications Transformer are designed to be used as a pair, and therefore must be implemented together in all designs. No transformer other than the FT-X3 (or FT-X1 or FT-X2) communications transformer may be used with the FT 5000 Smart Transceiver, or the smart transceiver warranty will be void.

Migration Considerations

Most device designs that use the previous generation FT 3120 / 3150 Smart Transceiver can transition to using the FT 5000 Smart Transceiver. However, because the supply voltage and memory architecture between FT 3120 / 3150 Smart Transceivers and FT 5000 Smart Transceivers are different, hardware redesign of the boards is required to transition to the FT 5000 Smart Transceiver.

See the *5000 Series Chip Data Book* for more information about migrating device designs for FT 3120 / 3150 Smart Transceivers to FT 5000 Smart Transceivers.

End-to-End Solutions

A typical FT 5000 Smart Transceiver based device requires a power source, crystal, external memory and an I/O interface to the device being controlled (see Figure 7 for a typical FT 5000 Smart Transceiver based device).

Echelon provides all of the building blocks required to successfully design and field cost-effective, robust products based on the FT 5000 Smart Transceivers. Our end-to-end solutions include a comprehensive set of development tools, network interfaces, routers, and network tools. Pre-production design review services, training, and worldwide technical support—including on-site support—are available through Echelon's LonSupport™ technical assistance program.

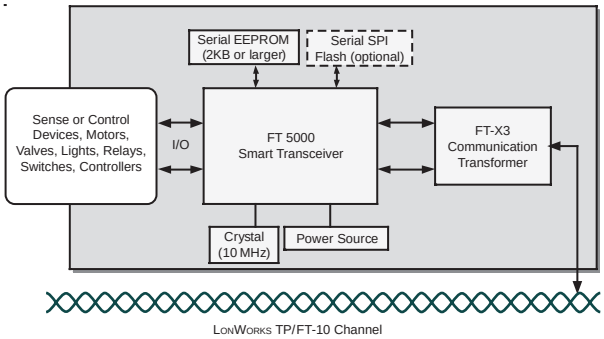

Figure 7: Typical LonWorks Based Device Block Diagram

FT 5000 Smart Transceiver IC Pin Configuration

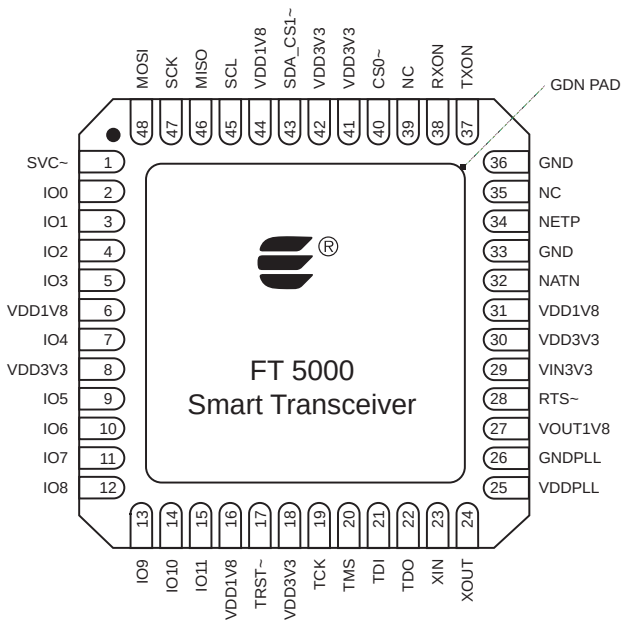

Figure 8: FT 5000 Smart Transceiver Pinout

FT 5000 Smart Transceiver IC Pin Descriptions

All digital inputs are low-voltage transistor-transistor logic (LVTTL) compatible, low leakage, 5V tolerant, with hysteresis. All digital outputs are slew-rate limited to reduce Electromagnetic Interference (EMI) concerns.

Pin Name	Pin Number	Type	Description
SVC~	1	Digital I/O	Service (active low)
IO0	2	Digital I/O	IO0 for I/O Objects
IO1	3	Digital I/O	IO1 for I/O Objects
IO2	4	Digital I/O	IO2 for I/O Objects
IO3	5	Digital I/O	IO3 for I/O Objects
VDD1V8	6	Power	1.8 V input from internal voltage regulator
IO4	7	Digital I/O	IO4 for I/O Objects
VDD3V3	8	Power	3.3 V Power
IO5	9	Digital I/O	IO5 for I/O Objects
IO6	10	Digital I/O	IO6 for I/O Objects
IO7	11	Digital I/O	IO7 for I/O Objects
IO8	12	Digital I/O	IO8 for I/O Objects
IO9	13	Digital I/O	IO9 for I/O Objects
IO10	14	Digital I/O	IO10 for I/O Objects
IO11	15	Digital I/O	IO11 for I/O Objects
VDD1V8	16	Power	1.8 V input from internal voltage regulator
TRST~	17	Digital Input	JTAG Test Reset (active low)
VDD3V3	18	Power	3.3 V Power

Pin Name	Pin Number	Type	Description
TCK	19	Digital Input	JTAG Test Clock
TMS	20	Digital Input	JTAG Test Mode Select
TDI	21	Digital Input	JTAG Test Data In
TDO	22	Digital Output	JTAG Test Data Out
XIN	23	Oscillator In	Crystal oscillator input
XOUT	24	Oscillator Out	Crystal oscillator Output
VDDPLL	25	Power	1.8 V input from internal voltage regulator
GNDPLL	26	Power	Ground
VOUT1V8	27	Power	1.8 V output from internal voltage regulator
RST~	28	Digital I/O	Reset (active low)
VIN3V3	29	Power	3.3 V input to internal voltage regulator
VDD3V3	30	Power	3.3 V Power
VDD1V8	31	Power	3.3 V Power
NETN	32	Communications	Network Port (polarity insensitive)
VSSFT	33		Ground
NETP	34	Communications	Network Port (polarity insensitive)
NC	35	N/A	No Connect
GND	36	Ground	Ground
TXON	37	Digital I/O	TxActive for optional network activity LED
RXON	38	Digital I/O	RxActive for optional network activity LED
NC	39	N/A	No Connect
CS0~	40	Digital I/O	SPI slave select 0 (active low)
VDD3V3	41	Power	3.3 V Power
VDD3V3	42	Power	3.3 V Power
SDA_CS1~	43	Digital I/O	I^2C: serial data (SDA) SPI: slave select 1 (CS1~, active low)
VDD1V8	44	Power	1.8 V input from internal voltage regulator
SCL	45	Digital I/O	I^2C: serial clock (SCL)
MISO	46	Digital I/O	SPI master input, slave output
SCK	47	Digital I/O	SPI serial clock
MOSI	48	Digital I/O	SPI master output, slave input
PAD	49	Ground Pad	Ground

Table 2: FT 5000 Smart Transceiver Pin Description

Electrical Characteristics

FT 5000 Smart Transceiver Operating Conditions

Parameter	Description	Minimum	Typical	Maximum
V_{DD3V3}	Supply voltage	3.00 V	3.3 V	3.60 V
V_{IO}	Digital input pins voltage range	-0.3 V		5.5 V
TA	Ambient temperature	-40° C		+85° C
f_{XIN}	XIN clock frequency	-	10.0000 MHz	-
I_{DD3-RX}	Current consumption in receive mode		TBD	TBD
I_{DD3-TX}	Current consumption in transmit mode		TBD	TBD

Table 3: FT 5000 Smart Transceiver Operating Conditions

Input/Output Pin Characteristics

TBD

Recommended FT 5000 Smart Transceiver Pad Layout

TBD

Recommended FT-X3 Communications Transformer Pad Layout

TBD

Chip Package Diagrams

TBD

Specifications

Function	Description
Data Communications Type	Differential Manchester encoding
Network Polarity	Polarity insensitive
Isolation between Network and:	
0-60Hz, 60 seconds	1000Vrms
0-60Hz, continuous	277Vrms[1]
EMI	Designed to comply with FCC Part 15 Level B and EN55022 Level B
ESD	Designed to comply with EN 61000-4-2, Level 4

Specifications (continued)

Function	Description
Radiated Electromagnetic Susceptibility	Designed to comply with EN 61000-4-3, Level 3
Fast Transient/Burst Immunity	Designed to comply with EN 61000-4-4, Level 4
Surge Immunity	Designed to comply with EN 61000-4-5, Level 3
Conducted RF Immunity	Designed to comply with EN 61000-4-6, Level 3
Safety Approvals (FT-X3 Communication Transformer)	TBD
Transmission Speed	78 kilobits per second
Number of Transceivers Per Segment	Up to 64
Network Wiring	24 to 16AWG twisted pair; see User's Guide or *Junction Box and Wiring Guidelines* application note for qualified cable types
Network Length in Free Topology2	1000m (3,280 feet) maximum total wire with one repeater 500m (1,640 feet) maximum total wire with no repeaters 500m (1,640 feet) maximum device-to-device distance
Network Length in Doubly Terminated Bus Topology[2]	5400m (17,710 feet) with one repeater 2700m (8,850 feet) with no repeaters
Maximum Stub Length in Doubly-Terminated Bus Topology	3m (9.8 feet)
Network Termination	One terminator in free topology; two terminators in bus topology (more details TBD in FT 5000 Data Book)
Power-down Network Protection	High impedance when unpowered
Physical Layer Repeater	TBD
Operating Temperature	-40 to 85 °C
Operating Humidity	25-90% RH @50 °C, non-condensing
Non-operating Humidity	95% RH @ 50 °C, non-condensing
Vibration	1.5g peak-to-peak, 8Hz-2kHz
Mechanical Shock	100g (peak)
Reflow Soldering Temperature Profile	Refer to Joint Industry Standard document *IPC/JEDEC J-STD-020D.1* (March 2008)
Peak Reflow Soldering Temperature	260°C

NOTES:

1. Safety agency hazardous voltage barrier requirements are not supported.
2. Network segment length varies depending on wire type. See *Junction Box and Wiring Guidelines* application note for detailed specifications.

Ordering Information

The FT 5000 Smart Transceiver can be purchased from Echelon directly or from any of the distributors carrying Echelon products. For more information on sales, visit www.echelon.com/sales

Product	Echelon Model Number	Where to Buy?
FT 5000 Smart Transceiver	14235R	Echelon Direct or Distributors www.echelon.com/sales
FT-X3 Communications Transformer	TBD	TBD