

High-voltage high and low side driver

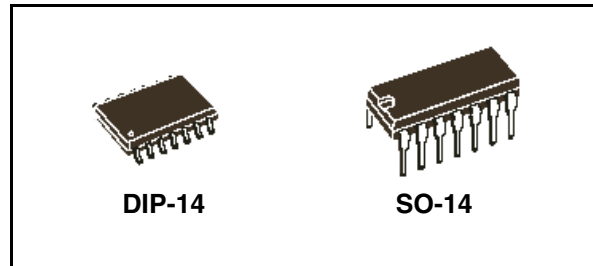
Features

- High voltage rail up to 600 V
- dV/dt immunity ± 50 V/nsec in full temperature range
- Driver current capability:
 - 290 mA source
 - 430 mA sink
- Switching times 75/35 nsec rise/fall with 1 nF load
- 3.3 V, 5 V TTL/CMOS inputs with hysteresis
- Integrated bootstrap diode
- Operational amplifier for advanced current sensing
- Adjustable dead-time
- Interlocking function
- Compact and simplified layout
- Bill of material reduction
- Flexible, easy and fast design

Application

Motor driver for home appliances, factory automation, industrial drives.

HID ballasts, power supply units.



Description

The L6392 is a high-voltage device, manufactured with the BCD "OFF-LINE" technology. It is a single chip half-bridge gate driver for N-channel Power MOSFET or IGBT.

The high side (floating) section is designed to stand a voltage rail up to 600 V. The logic inputs are CMOS/TTL compatible down to 3.3 V for easy of interfacing microcontroller/DSP

The IC embeds an operational amplifier suitable for advanced current sensing in applications such as field oriented motor control.

Table 1. Device summary

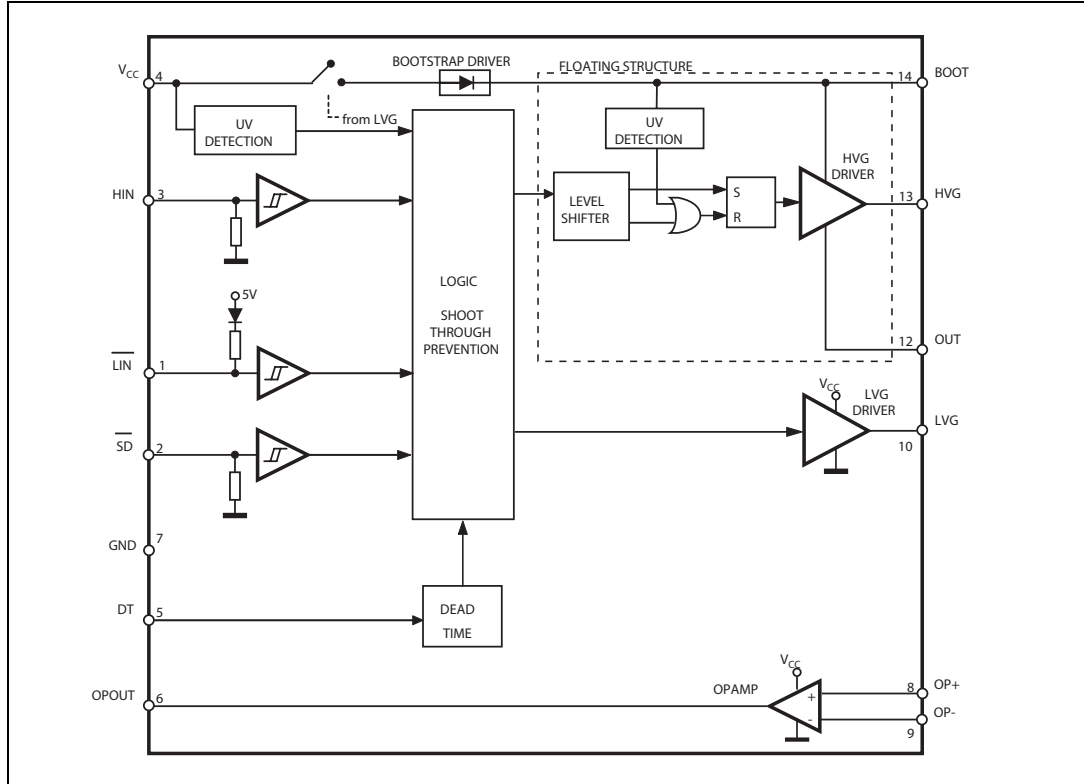
Order codes	Package	Packaging
L6392	DIP-14	Tube
L6392D	SO-14	Tube
L6392D013TR	SO-14	Tape and reel

Contents

1	Block diagram	3
2	Pin connection	4
3	Truth table	5
4	Electrical data	6
	4.1 Absolute maximum ratings	6
	4.2 Thermal data	6
	4.3 Recommended operating conditions	7
5	Electrical characteristics	8
	5.1 AC operation	8
	5.2 DC operation	9
6	Waveforms definitions	12
7	Typical application diagram	13
8	Bootstrap driver	14
	8.1 CBOOT selection and charging	14
9	Package mechanical data	16
10	Revision history	19

1 Block diagram

Figure 1. Block diagram



2 Pin connection

Figure 2. Pins connection (top view)

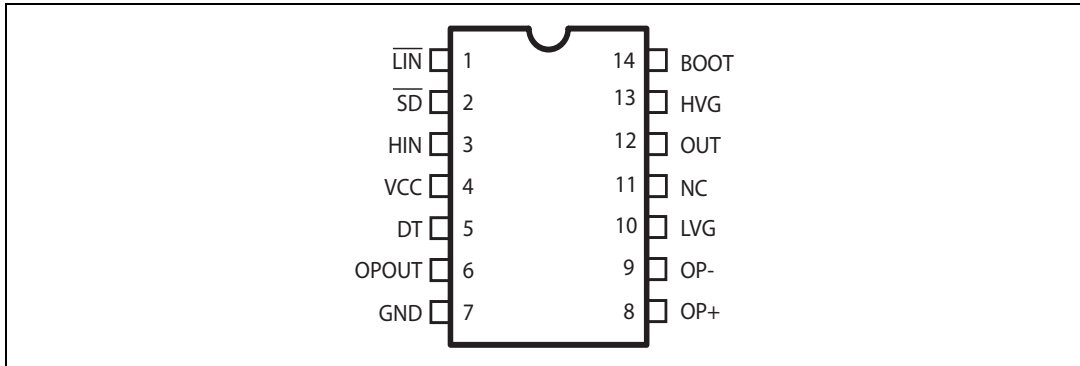


Table 2. Pin description

Pin N#	Pin name	Type	Function
1	$\overline{\text{LIN}}$	I	Low side driver logic input (active low)
2	$\overline{\text{SD}}^{(1)}$	I	Shut down logic input (active low)
3	HIN	I	High side driver logic input (active high)
4	VCC	P	Lower section supply voltage
5	DT	I	Dead time setting
6	OPOUT	O	Opamp output
7	GND	P	Ground
8	OP+	I	Opamp non inverting input
9	OP-	I	Opamp inverting input
10	LVG ⁽¹⁾	O	Low side driver output
11	NC		Not connected
12	OUT	P	High side (floating) common voltage
13	HVG ⁽¹⁾	O	High side driver output
14	BOOT	P	Bootstrapped supply voltage

1. The circuit provides less than 1 V on the LVG and HVG pins (@ Isink = 10 mA), with V_{CC} > 3 V. This allows to omitting the "bleeder" resistor connected between the gate and the source of the external MOSFET normally used to hold the pin low; the gate driver assures low impedance also in SD condition.

3 Truth table

Table 3. Truth table

Inputs			Outputs	
\overline{SD}	\overline{LIN}	HIN	LVG	HVG
L	X	X	L	L
H	L	L	H	L
H	L	H	L	L
H	H	L	L	L
H	H	H	L	H

Note: X: don't care

4 Electrical data

4.1 Absolute maximum ratings

Table 4. Absolute maximum rating

Symbol	Parameter	Value		Unit
		Min	Max	
V_{CC}	Supply voltage	- 0.3	+ 21	V
V_{out}	Output voltage	$V_{boot} - 21$	$V_{boot} + 0.3$	V
V_{boot}	Bootstrap voltage	- 0.3	620	V
V_{hvg}	High side gate output voltage	$V_{out} - 0.3$	$V_{boot} + 0.3$	V
V_{lvg}	Low side gate output voltage	-0.3	$V_{CC} + 0.3$	V
V_{op+}	Opamp non-inverting input	-0.3	$V_{CC} + 0.3$	V
V_{op-}	Opamp inverting input	-0.3	$V_{CC} + 0.3$	V
V_i	Logic input voltage	-0.3	15	V
dV_{out}/dt	Allowed output slew rate		50	V/ns
P_{tot}	Total power dissipation ($T_A = 25\text{ °C}$)		800	mW
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	-50	150	°C

Note: ESD immunity for pins 12, 13 and 14 is guaranteed up to 1 kV (Human body model)

4.2 Thermal data

Table 5. Thermal data

Symbol	Parameter	SO-14	DIP-14	Unit
$R_{th(JA)}$	Thermal resistance junction to ambient	165	100	°C/W

4.3 Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Pin	Parameter	Test condition	Min	Max	Unit
V_{CC}	4	Supply voltage		12.5	20	V
$V_{BO}^{(1)}$	14-12	Floating supply voltage		12.4	20	V
V_{out}	12	DC output voltage		-9 ⁽²⁾	580	V
f_{sw}		Switching frequency	HVG, LVG load $C_L = 1\text{nF}$		800	kHz
T_J		Junction temperature		-40	125	°C

- $V_{BO} = V_{boot} - V_{out}$
- LVG off. $V_{CC} = 12.5\text{ V}$.
Logic is operational if $V_{boot} > 5\text{ V}$.

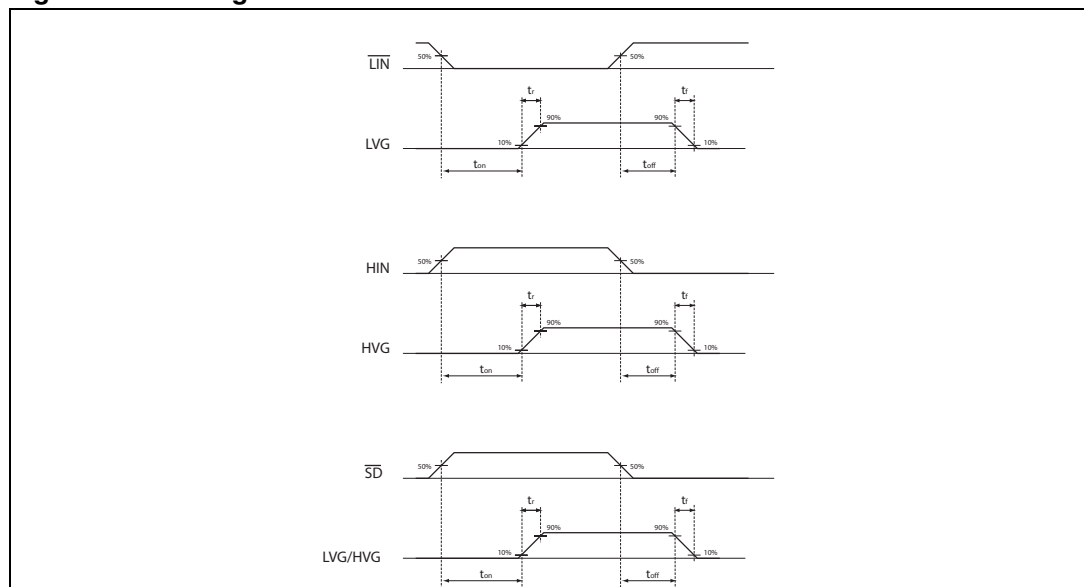
5 Electrical characteristics

5.1 AC operation

Table 7. AC operation electrical characteristics ($V_{CC} = 15\text{ V}$; $T_J = +25\text{ }^\circ\text{C}$)

Symbol	Pin	Parameter	Test condition	Min	Typ	Max	Unit
t_{on}	1 vs 10	High/low side driver turn-on propagation delay	$V_{out} = 0\text{ V}$ $V_{boot} = V_{CC}$ $C_L = 1\text{ nF}$ $V_i = 0\text{ to }3.3\text{ V}$ See Figure 3		125	200	ns
t_{off}	3 vs 13	High/low side driver turn-off propagation delay			125	200	ns
t_{sd}	2 vs 10, 13	Shut down to high/low side propagation delay			125	200	ns
MT		Delay matching, HS and LS turn-on/off				40	ns
dt	5	Dead time setting range	$R_{dt} = 0\text{ }\Omega$; $C_L = 1\text{ nF}$; $C_{DT} = 100\text{ nF}$	0.1	0.18	0.25	μs
			$R_{dt} = 37\text{ k}\Omega$; $C_L = 1\text{ nF}$; $C_{DT} = 100\text{ nF}$	0.48	0.6	0.72	
			$R_{dt} = 136\text{ k}\Omega$; $C_L = 1\text{ nF}$; $C_{DT} = 100\text{ nF}$	1.35	1.6	1.85	
			$R_{dt} = 260\text{ k}\Omega$; $C_L = 1\text{ nF}$; $C_{DT} = 100\text{ nF}$	2.6	3.0	3.4	
MDT		Matching dead time	$R_{dt} = 0\text{ }\Omega$; $C_L = 1\text{ nF}$; $C_{DT} = 100\text{ nF}$			60	ns
			$R_{dt} = 37\text{ k}\Omega$; $C_L = 1\text{ nF}$; $C_{DT} = 100\text{ nF}$			100	
			$R_{dt} = 136\text{ k}\Omega$; $C_L = 1\text{ nF}$; $C_{DT} = 100\text{ nF}$			240	
			$R_{dt} = 260\text{ k}\Omega$; $C_L = 1\text{ nF}$; $C_{DT} = 100\text{ nF}$			350	
t_r	10, 13	Rise time	$C_L = 1\text{ nF}$		75	120	ns
t_f		Fall time	$C_L = 1\text{ nF}$		35	70	ns

Figure 3. Timing characteristics



5.2 DC operation

Table 8. DC operation electrical characteristics ($V_{CC} = 15\text{ V}; T_J = +25\text{ }^\circ\text{C}$)

Symbol	Pin	Parameter	Test condition	Min	Typ	Max	Unit
Low supply voltage section							
V_{CC_hys}	4	V_{CC} UV hysteresis		1200	1500	1800	mV
V_{CC_thON}		V_{CC} UV turn ON threshold		11.5	12	12.5	V
V_{CC_thOFF}		V_{CC} UV turn OFF threshold		10	10.5	11	V
I_{qccu}		Undervoltage quiescent supply current	$V_{CC} = 10\text{ V}$ $\overline{SD} = 5\text{ V}; \overline{LIN} = 5\text{ V};$ $HIN = GND;$ $R_{DT} = 0\ \Omega;$ $OP + = GND; OP - = 5\text{ V}$		120	150	μA
I_{qcc}		Quiescent current	$V_{CC} = 15\text{ V}$ $\overline{SD} = 5\text{ V}; \overline{LIN} = 5\text{ V};$ $HIN = GND;$ $R_{DT} = 0\ \Omega;$ $OP + = GND; OP - = 5\text{ V}$		680	1000	μA
Bootstrapped supply voltage section ⁽¹⁾							
V_{BO_hys}	14	V_{BO} UV hysteresis		1200	1500	1800	mV
V_{BO_thON}		V_{BO} UV turn ON threshold		10.6	11.5	12.4	V
V_{BO_thOFF}		V_{BO} UV turn OFF threshold		9.1	10	10.9	V
I_{QBOU}		Undervoltage V_{BO} quiescent current	$V_{BO} = 9\text{ V}$ $\overline{SD} = 5\text{ V}; \overline{LIN}$ and $HIN = 5\text{ V};$ $R_{DT} = 0\ \Omega;$ $OP + = GND; OP - = 5\text{ V}$		70	110	μA
I_{QBO}		V_{BO} quiescent current	$V_{BO} = 15\text{ V}$ $\overline{SD} = 5\text{ V}; \overline{LIN}$ and $HIN = 5\text{ V};$ $R_{DT} = 0\ \Omega;$ $OP + = GND; OP - = 5\text{ V}$		150	210	μA
I_{LK}		High voltage leakage current	$V_{hvg} = V_{out} = V_{boot} = 600\text{ V}$			10	μA
$R_{DS(on)}$		Bootstrap driver on resistance ⁽²⁾	LVG ON		120		Ω

Table 8. DC operation electrical characteristics ($V_{CC} = 15\text{ V}; T_J = +25\text{ }^\circ\text{C}$)

Symbol	Pin	Parameter	Test condition	Min	Typ	Max	Unit
Driving buffers section							
I_{so}	10, 13	High/low side source short circuit current	$V_i = V_{ih} (t_p < 10\text{ ms})$	200	290		mA
I_{si}		High/low side sink short circuit current	$V_i = V_{il} (t_p < 10\text{ ms})$	250	430		mA
Logic inputs							
V_{il}	1, 2, 3	Low logic level voltage				0.8	V
V_{ih}		High logic level voltage		2.25			V
I_{HINh}	3	HIN logic "1" input bias current	$HIN = 15\text{ V}$		175	260	μA
I_{HINl}		HIN logic "0" input bias current	$HIN = 0\text{ V}$			1	μA
I_{LINl}	1	\overline{LIN} logic "0" input bias current	$\overline{LIN} = 0\text{ V}$		6	20	μA
I_{LINh}		\overline{LIN} logic "1" input bias current	$\overline{LIN} = 15\text{ V}$			1	μA
I_{SDh}	2	\overline{SD} logic "1" input bias current	$\overline{SD} = 15\text{ V}$		30	100	μA
I_{SDl}		\overline{SD} logic "0" input bias current	$\overline{SD} = 0\text{ V}$			1	μA

1. $V_{BO} = V_{boot} - V_{out}$

2. R_{DSon} is tested in the following way:

$$R_{DSon} = [(V_{CC} - V_{CBOOT1}) - (V_{CC} - V_{CBOOT2})] / [I_1(V_{CC}, V_{CBOOT1}) - I_2(V_{CC}, V_{CBOOT2})]$$

where I_1 is pin 14 current when $V_{CBOOT} = V_{CBOOT1}$, I_2 when $V_{CBOOT} = V_{CBOOT2}$

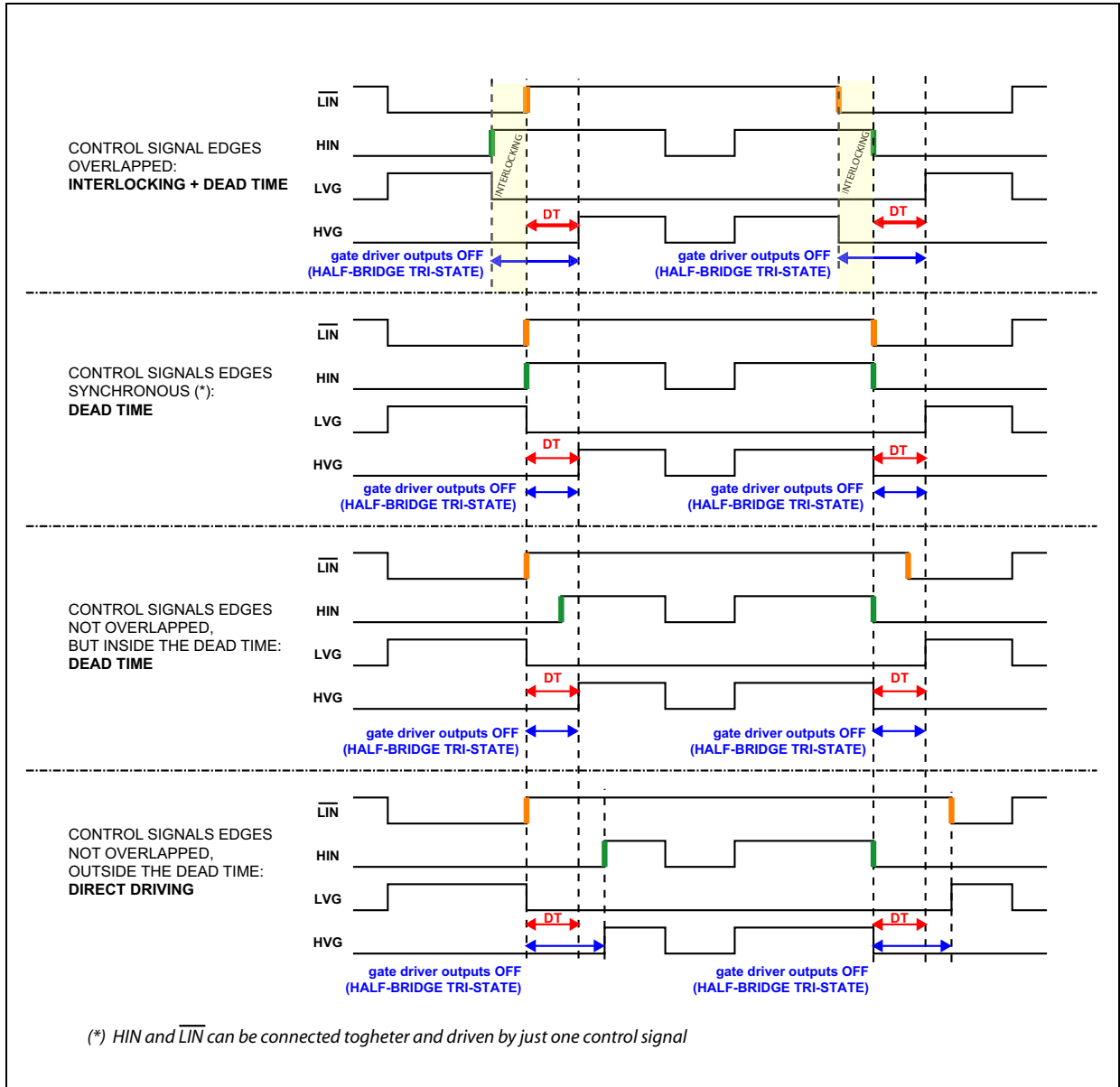
Table 9. OPAMP characteristics ($V_{CC} = 15\text{ V}$, $T_J = +25\text{ °C}$)

Symbol	Pin	Parameter	Test condition	Min	Typ	Max	Unit
I_{io}	8, 9	Input offset current			4	40	nA
I_{ib}		Input bias current ⁽¹⁾			100	200	nA
V_{icm}		Input common mode voltage range		0			V
V_{OL}	6	Low level output voltage	$R_L = 10\text{ k}\Omega$ to V_{CC}		75	150	mV
V_{OH}		High level output voltage	$R_L = 10\text{ k}\Omega$ to GND	14	14.7		V
I_o		Output short circuit current	Source, $V_{id} = +1\text{ V}$; $V_o = 0\text{ V}$	16	30		mA
		Sink $V_{id} = -1\text{ V}$; $V_o = V_{CC}$	50	80		mA	
SR		Slew rate	$V_i = 1\div 4$; $C_L = 100\text{ pF}$; unity gain	2.5	3.8		V/ μ s
GBWP		Gain bandwidth product	$V_o = 7.5$; $R_L = 2\text{ k}\Omega$	8	12		MHz
A_{vd}		Large signal voltage gain		75	85		dB
SRV		Power supply rejection ratio	vs V_{CC}	60	70		dB
CMRR		Common mode rejection ratio		60	70		dB

1. The direction of input current is out of the IC.

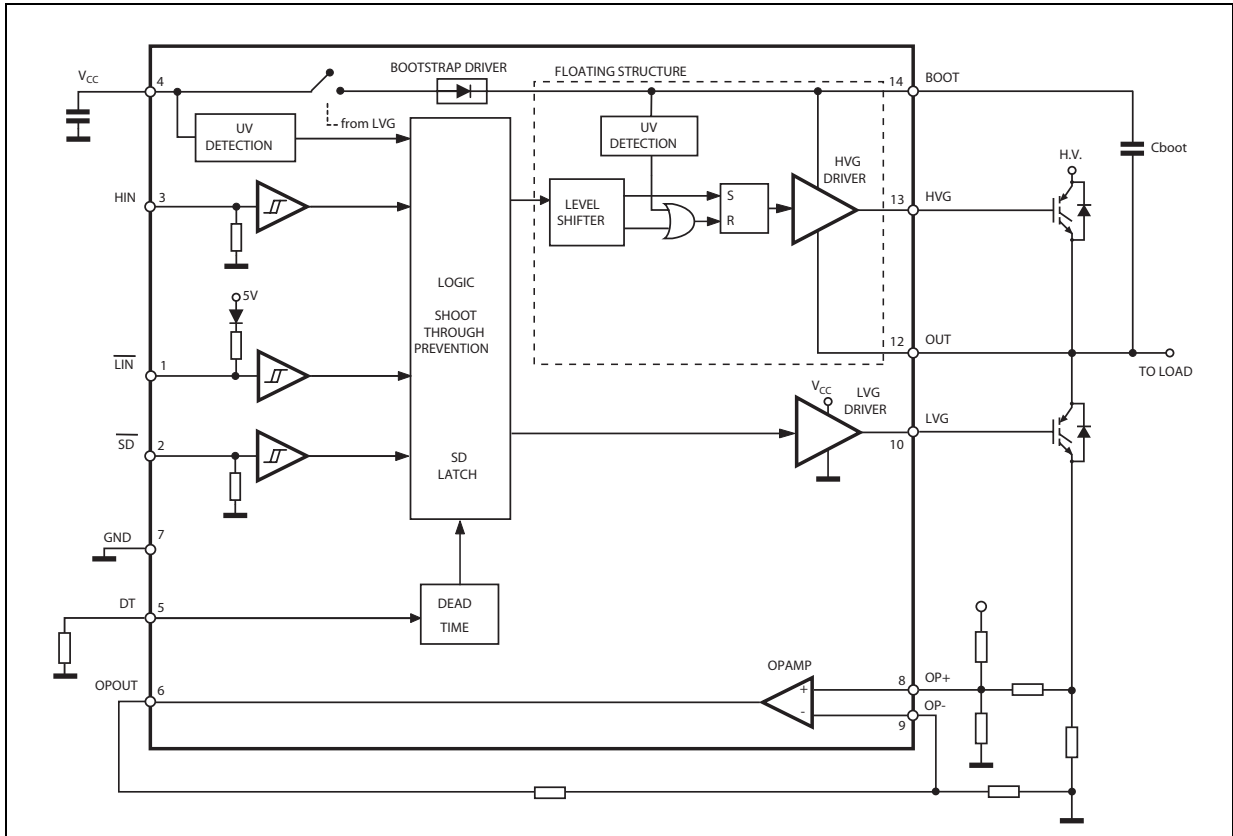
6 Waveforms definitions

Figure 4. Dead time - timing waveforms



7 Typical application diagram

Figure 5. Application diagram



8 Bootstrap driver

A bootstrap circuitry is needed to supply the high voltage section. This function is normally accomplished by a high voltage fast recovery diode (*Figure 6 a*). In the L6392 a patented integrated structure replaces the external diode. It is realized by a high voltage DMOS, driven synchronously with the low side driver (LVG), with diode in series, as shown in *Figure 6 b*.

An internal charge pump (*Figure 6 b*) provides the DMOS driving voltage.

8.1 C_{BOOT} selection and charging

To choose the proper C_{BOOT} value the external MOS can be seen as an equivalent capacitor. This capacitor C_{EXT} is related to the MOS total gate charge:

$$C_{EXT} = \frac{Q_{gate}}{V_{gate}}$$

The ratio between the capacitors C_{EXT} and C_{BOOT} is proportional to the cyclical voltage loss. It has to be:

$$C_{BOOT} \gg \gg C_{EXT}$$

e.g.: if Q_{gate} is 30 nC and V_{gate} is 10 V, C_{EXT} is 3 nF. With C_{BOOT} = 100 nF the drop would be 300 mV.

If HVG has to be supplied for a long time, the C_{BOOT} selection has to take into account also the leakage and quiescent losses.

e.g.: HVG steady state consumption is lower than 200 μA, so if HVG T_{ON} is 5 ms, C_{BOOT} has to supply 1 μC to C_{EXT}. This charge on a 1 μF capacitor means a voltage drop of 1 V.

The internal bootstrap driver gives a great advantage: the external fast recovery diode can be avoided (it usually has great leakage current).

This structure can work only if V_{OUT} is close to GND (or lower) and in the meanwhile the LVG is on. The charging time (T_{charge}) of the C_{BOOT} is the time in which both conditions are fulfilled and it has to be long enough to charge the capacitor.

The bootstrap driver introduces a voltage drop due to the DMOS R_{DSON} (typical value: 120 Ω). At low frequency this drop can be neglected. Anyway increasing the frequency it must be taken in to account.

The following equation is useful to compute the drop on the bootstrap DMOS:

$$V_{drop} = I_{charge} R_{dson} \rightarrow V_{drop} = \frac{Q_{gate}}{T_{charge}} R_{dson}$$

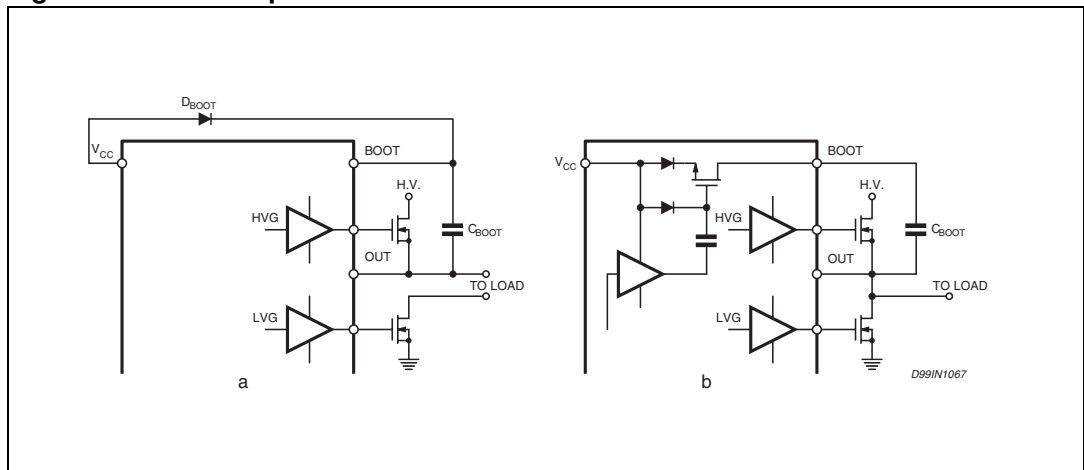
where Q_{gate} is the gate charge of the external power MOS, R_{dson} is the on resistance of the bootstrap DMOS, and T_{charge} is the charging time of the bootstrap capacitor.

For example: using a power MOS with a total gate charge of 30 nC the drop on the bootstrap DMOS is about 1 V, if the T_{charge} is 5 μs . In fact:

$$V_{\text{drop}} = \frac{30\text{nC}}{5\mu\text{s}} \cdot 120\Omega \sim 0.7\text{V}$$

V_{drop} has to be taken into account when the voltage drop on C_{BOOT} is calculated: if this drop is too high, or the circuit topology doesn't allow a sufficient charging time, an external diode can be used.

Figure 6. Bootstrap driver



9 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

Figure 7. DIP-14 mechanical data and package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100

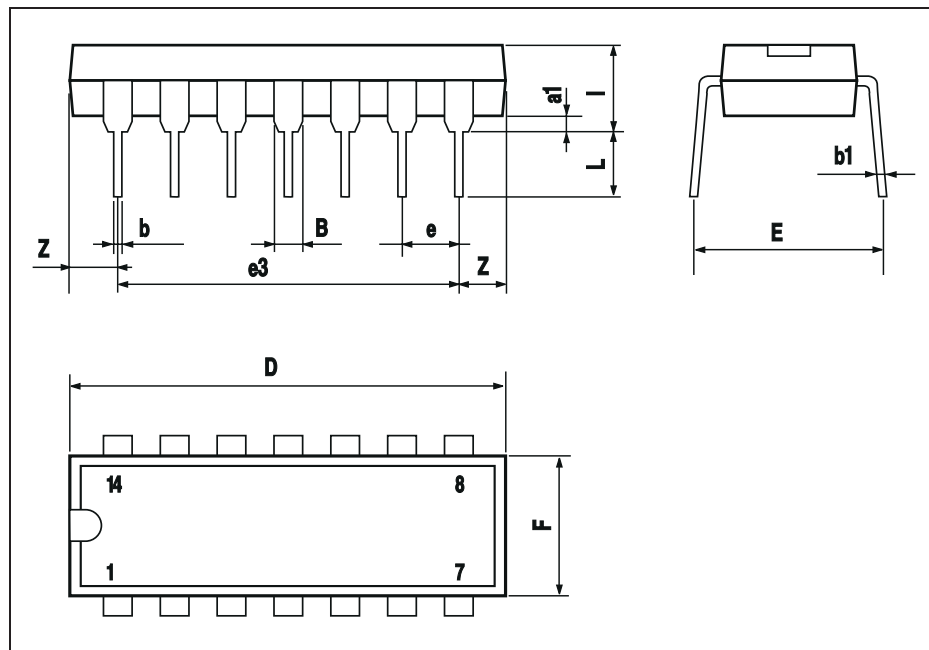
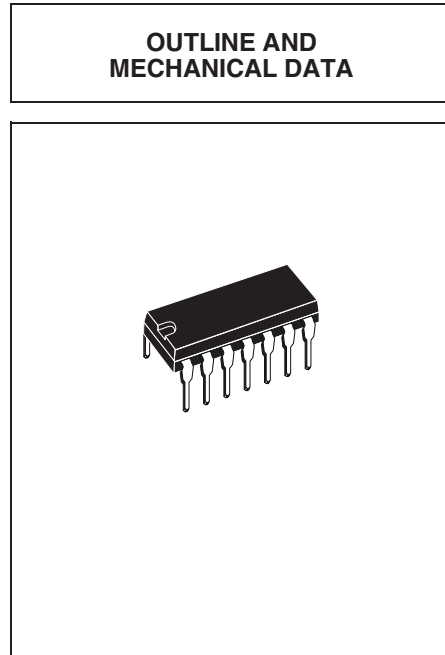
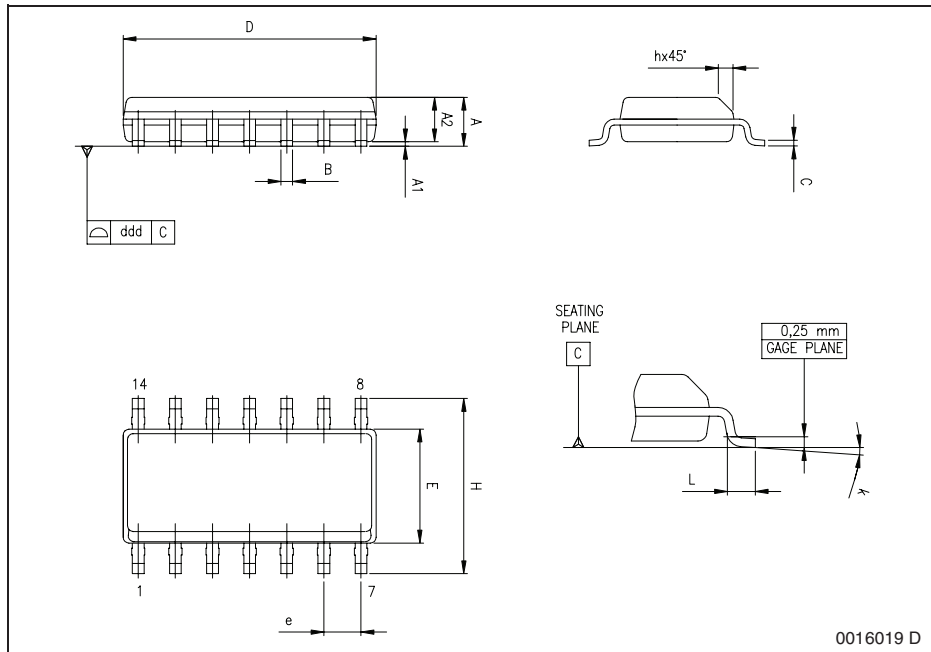
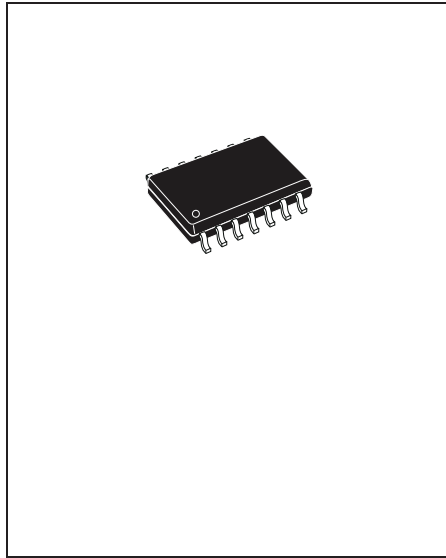


Figure 8. SO-14 mechanical data and package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	1.35		1.75	0.053		0.069
A1	0.10		0.30	0.004		0.012
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.01
D (1)	8.55		8.75	0.337		0.344
E	3.80		4.0	0.150		0.157
e		1.27			0.050	
H	5.8		6.20	0.228		0.244
h	0.25		0.50	0.01		0.02
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

(1) "D" dimension does not include mold flash, protusions or gate burrs. Mold flash, protusions or gate burrs shall not exceed 0.15mm per side.

OUTLINE AND MECHANICAL DATA



0016019 D

10 Revision history

Table 10. Document revision history

Date	Revision	Changes
29-Feb-2008	1	Initial release
18-Mar-2008	2	Cover page updated
17-Sep-2008	3	Updated Table 4 on page 6 , Table 4 on page 6 , Table 9 on page 11

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER'S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2008 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com