Neuron® 5000 Processor
Model 14305R

- 3.3V operation
- Higher Performance Neuron Core – Internal system clock scales up to 40 MHz
- Enables lower cost device designs
- Serial interface for inexpensive external EEPROM and flash non-volatile memories
- Supports up to 254 Network Variables (NVs)
- User programmable interrupts provide faster response time to external events
- 7 mm by 7 mm 48-pin QFN package
- 5-pin network communications port with 3.3 V drive and 5V tolerant pins
- 12 I/O pins with 35 programmable standard I/O modes
- Supports up to 42 KB of application code space
- 64 KB RAM (44 KB user accessible) and 16 KB ROM on-chip memories
- Unique 48-bit Neuron ID in every device for network installation and management
- -40°C to +85°C operating temperature range

Description

The Echelon Neuron 5000 Processor is the next generation Neuron Chip for LonWorks® distributed intelligent control networks. Combined with inexpensive serial memories, the Neuron 5000 Processor provides a lower cost, higher performance LonWorks solution compared to those based on previous generation Neuron 3120 and Neuron 3150 Chips.

The Neuron 5000 Processor incorporates the necessary communication and control functions, on a single chip, both in hardware and firmware, to facilitate the design of a LonWorks device. LonWorks networks are ideal as control networks for building, industrial, transportation, home, utility, and many other automation applications.

The Neuron 5000 Processor contains a very flexible 5-pin communications port that can be configured to interface with a wide variety of media transceivers at a wide range of data rates. The most common transceiver types are twisted-pair, RF, IR, fiber-optics, and coaxial.

The Neuron 5000 Processor includes three independent 8-bit logical processors to manage the physical MAC layer, the network, and the user application. These are called the Media-Access Control (MAC) processor, the network (NET) processor, and the application (APP) processor respectively (see Figure 1). At higher system clock rates, there is also a fourth processor to handle interrupts.

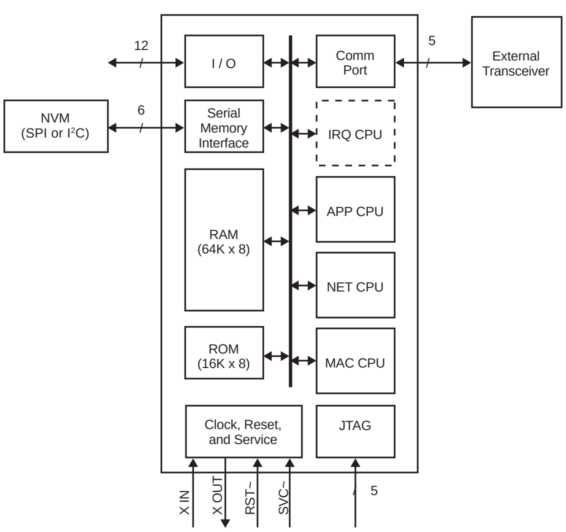

Figure 1: Neuron 5000 Processor Block Diagram

Backward Compatibility

The pins for the Neuron 5000 Processor's communications port drive a 3.3V signal and are 5V input tolerant. Thus, the Neuron 5000 Processor is compatible with 3.3V transceivers and with 5V transceivers that have TTL-compatible input.

The Neuron 5000 Processor is compatible with TP/XF-1250 and EIA-485 channels. It can also support a variety of other channels used with previous generation Neuron Chips, such as RF, IR, fiber-optic, and coaxial. Echelon does not support use of a TP/XF-78 channel with the Neuron 5000 Processor.

To support a TP/FT-10 channel, use an Echelon Free Topology Smart Transceiver (FT 3120 / 3150 Smart Transceiver or FT 5000 Smart Transceiver); to support a PL-20 power line channel, use an Echelon Power Line Smart Transceiver (PL 3120 / 3150 / 3170 Smart Transceiver). The Echelon Smart Transceivers integrate the transceiver for the channel type and the Neuron Core into a single chip, which enables smaller designs and provides cost savings.

The Neuron Core in the Neuron 5000 Processor uses the same instruction set architecture as the previous generation Neuron Core, but with two new additional instructions for hardware multiplication and division. It is backward compatible with applications written for previous generation Neuron Chips and Smart Transceivers. However, the old applications need to be recompiled with the latest versions of the NodeBuilder® Development Tool or the Mini EVK Evaluation Kit before they can be used with the Neuron 5000 Processor.

The Neuron 5000 Processor uses new system firmware, version 18. Older firmware versions are not compatible with the Neuron 5000 Processor. The Neuron firmware is pre-programmed into the on-chip ROM. The Neuron 5000 Processor can also be configured to read newer firmware from external memories, allowing the firmware to be upgraded over time.

Enhanced Performance

Faster System Clock

The internal system clock for the Neuron 5000 Processor can be user configured to run from 10 MHz to 40 MHz. The required external crystal provides a 10 MHz clock frequency, and an internal PLL boosts the frequency to a maximum of 40 MHz as the internal system clock speed. The previous generation Neuron 3120/3150 Core divided the external oscillator frequency by two to create the internal system clock. Hence, a Neuron 3120/3150 Core running with a 10 MHz external crystal had a 5 MHz internal system clock. A Neuron 5000 Processor running with a 40 MHz internal clock is thus 8 times faster than a 10 MHz Neuron 3120/3150 Core.

The Neuron Core inside the Neuron 5000 Processor includes a hardware multiplier and divider built in to increase performance of arithmetic operations.

Support for More Network Variables

The Neuron 5000 Processor supports up to 254 Network Variables (NVs), substantially more than the 62 NVs supported by the Neuron 3120/3150 Core.

Interrupts

The Neuron 5000 Processor allows a developer to define user interrupts to handle asynchronous events related to I/O objects. There are also system-level exceptions and internal traps, which have higher priority than user-defined interrupts.

JTAG

The Neuron 5000 Processor provides an interface for the Institute of Electrical and Electronics Engineers (IEEE) Standard Test Access Port and Boundary-Scan Architecture (IEEE 1149.1-1990) of the Joint Test Action Group (JTAG). A Boundary Scan Description Language (BSDL) file for the Neuron 5000 Processor will be available for download from the Echelon Web site.

Communications Port

The Neuron 5000 Processor includes a versatile 5-pin communications port that can be configured in two different ways: 3.3 V Single-Ended Mode and 3.3 V Special-Purpose Mode.

In Single-Ended Mode, pin CP0 is used for receiving serial data, pin CP1 for transmitting serial data, and pin CP2 enables an external transmitter. Data is communicated using Differential Manchester encoding.

In Special-Purpose Mode, pin CP0 is used for receiving serial data, pin CP1 for transmitting serial data, pin CP2 transmits a bit clock, and pin CP4 transmits a frame clock for use by an external intelligent transceiver. In this mode, the external transceiver is responsible for encoding and decoding the data stream.

Unlike the Neuron 3120 / 3150 Chips, the Neuron 5000 Processor does not support the Differential Mode configuration for the communications port. Thus, devices that require Differential Mode transceiver types must be redesigned for a Neuron 5000 Processor to use Single-Ended Mode with external circuitry to provide Single-Ended to Differential Mode conversions. See the *5000 Series Chip Data Book* for more information.

Any 3.3V transceiver or a 5V transceiver with TTL-compatible inputs can be used with the Neuron 5000 Processor because the communications port has pins that are 5V tolerant and drive a 3.3V signal. Common transceiver types that can be used with a Neuron 5000 Processor include twisted-pair, RF, IR, fiber-optics, and coaxial.

I/O Pins and Counters

The Neuron 5000 Processor provides 12 bidirectional I/O pins that are 5V tolerant and can be configured to operate in one or more of 35 predefined standard input/output modes. The chip also has two 16-bit timer/counters that reduce the need for external logic and software development.

Memory Architecture

The Neuron 5000 Processor memory architecture is very different from that in the previous generation FT Smart Transceivers and Neuron Chips. It has 16 KB of read-only memory (ROM) and 64 KB (44 KB user accessible) of random access memory (RAM) on the chip. It has no on-chip non-volatile memory (EEPROM or flash) for application use. Each chip however contains its unique Neuron identifier (Neuron ID) in an on-chip non-volatile read-only memory.

The Neuron 5000 Processor uses a serial memory interface for external non-volatile memories (EEPROM or flash). The application code and configuration data are stored in the external non-volatile memory (NVM) and copied into the internal RAM during device reset; the instructions then execute from internal RAM. Writes to NVM are shadowed in the internal RAM and pushed out to external NVM by the system firmware (see Figure 1). The application does not need to manage NVM directly.

External Memories Supported

The Neuron 5000 Processor supports two serial interfaces for accessing off-chip non-volatile memories: serial Inter-Integrated Circuit (I^2C) and serial peripheral interface (SPI). EEPROM devices can use either the I^2C interface or the SPI interface; flash memory devices must use the SPI interface.

External serial EEPROMs and flash devices are low-cost and available from multiple vendors in very small form factors.

The Neuron 5000 Processor requires at least 2 KB of off-chip memory available in an EEPROM device to store the configuration data. The application code can be stored either in the EEPROM (by using a larger capacity EEPROM device) or in a flash memory device used in addition to the EEPROM. Thus, the external memory for a Neuron 5000 Processor has one of the configurations listed in Table 1:

Configuration	EEPROM		Flash	Description
	I^{2}C	SPI	SPI	
1	☑			A single I^{2}C EEPROM memory device, from 2 KB to 64 KB in size
2	☑		☑	One I^{2}C EEPROM (at least 2 KB in size, up to 64 KB in size, but the system uses only the first 2 KB of the EEPROM memory) One SPI flash memory device
3		☑		A single SPI EEPROM memory device, from 2 KB to 64 KB in size
4		☑	☑	One SPI EEPROM (at least 2 KB in size, up to 64 KB in size, but the system uses only the first 2 KB of the EEPROM memory) One SPI flash memory device

Table 1: Allowed External Memory Device Configurations

As Table 1 shows, the Neuron 5000 Processor supports using a single EEPROM memory device, or a single EEPROM memory device plus a single flash memory device.

If the Neuron 5000 Processor uses flash memory, the flash memory represents the entire user non-volatile memory for the device. That is, any additional EEPROM memory beyond the mandatory 2 KB is not used.

Using the I^{2}C Interface

When using the I^{2}C interface for external EEPROM, the Neuron 5000 Processor is always the master I^{2}C device (see Figure 2). The clock speed supported for the I^{2}C serial memory interface is 400 kHz (fast I^{2}C mode). The I^{2}C memory device must specify I^{2}C address 0. Both 1-byte and 2-byte address modes are supported, but 3-byte addressing mode is not supported.

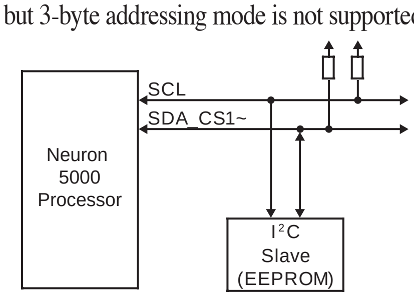

Figure 2: Using the I^{2}C Interface for External NVM EEPROM Memory

Using the SPI Interface

The Neuron 5000 Processor is always the master SPI device; any external NVM devices are always slave devices. The Neuron 5000 Processor can support up to two SPI slave devices from the serial memory interface: one EEPROM device at CS0~ and one flash device at CS1~ (see Figure 3). The Neuron 5000 Processor supports 2-byte addressing mode for SPI EEPROM devices, but does not support 3-byte addressing. The Neuron 5000 Processor runs the SPI protocol from the serial memory interface at 2.5 MHz and supports SPI Mode 0. In Mode 0, the base value of the clock is zero; the data is read on the clock's rising edge and changed on the clock's falling edge. Most external NVMs support SPI Mode 0 and 3.

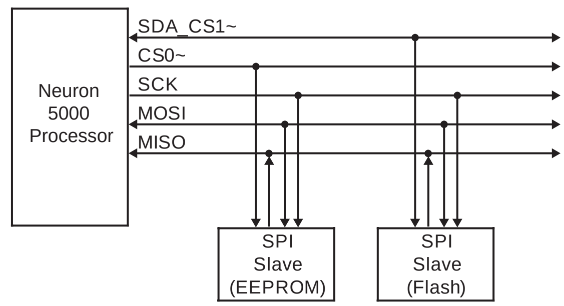

Figure 3: Using the SPI Interface for External NVM Memories

Using Both I^{2}C and SPI Interfaces

Figure 4 shows a Neuron 5000 Processor that includes both an I^{2}C memory device (a 2 KB EERPOM device) and a SPI memory device (a flash memory device). Although both EEPROM and flash memory share the SDA_CS1~ pin, there is no conflict because only one of them can be active at a time. SDA is an active high signal and CS1~ is an active low signal. While small applications could use EEPROM both for application code and configuration data, larger applications might find it economical to use a small EEPROM for configuration data and a flash device for application code. The choice between EEPROM and flash can be affected by multiple factors, including:

- Use of single external memory versus two memories
- Cost comparison between a large EEPROM device and a combination of a small EEPROM and large flash devices
- Use of non-volatile variables by the application, which can require a large number of writes to the device

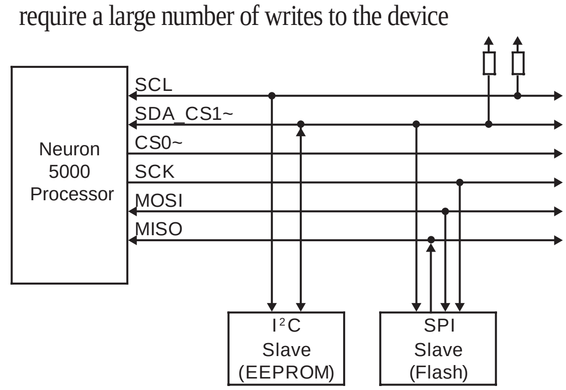

Figure 4: Using Both I^{2}C and SPI Interfaces for External NVM Memories

Memory Devices Supported

The Neuron 5000 Processor supports any EEPROM device that uses the SPI or I^2C protocol, and meets the clock speed and addressing requirements described above.

While all EEPROM devices have a uniform write procedure, flash devices from various manufacturers differ slightly in their write procedure. Thus, a small library routine is stored in the external EEPROM device that helps the system write successfully to the external flash device. Echelon has qualified the following SPI flash memory devices for use with the Neuron 5000 Processor:

- Atmel® AT25F512B 512-Kilobit 2.7-volt Minimum SPI Serial Flash Memory
- Numonyx™ M25P05-A 512-Kbit, serial flash memory, 50 MHz SPI bus interface
- Silicon Storage Technology SST25VF512A 512 Kbit SPI Serial Flash

Additional devices may be qualified in the future.

Memory Map

A Neuron C device has a memory map of 64 KB. A Neuron C application program uses this memory map to organize its memory and data access. The memory map is a logical view of device memory, rather than a physical view, because the chip's processors only directly access RAM. The memory map divides the Neuron 5000 Processor's physical 64 KB RAM into the following types of logical memory, as shown in Figure 5:

- System firmware image (stored in on-chip ROM or external NVM)
- On-chip RAM or NVM. Memory ranges for each are configurable within the device hardware template. The non-volatile memory represents the area shadowed from external NVM into the RAM.
- On-chip RAM for stack segments and RAMNEAR data
- Mandatory external EEPROM that holds configuration data and non-volatile application variables
- Reserved space for system use

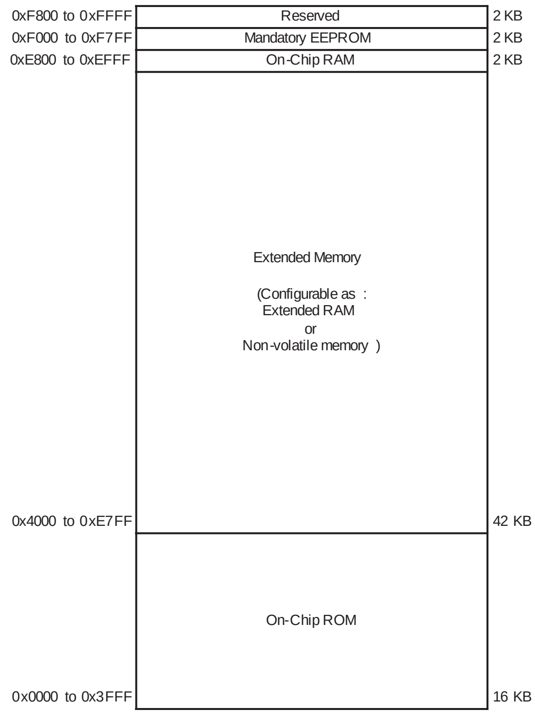

Figure 5: Neuron 5000 Processor Memory Map

If a 64 KB external serial EEPROM or flash device is used, the maximum allowed size of application code is 42 KB as defined by extended NVM area in the memory map. Additional 16 KB of the remaining space can hold an external system firmware image in case firmware upgrade is required.

Programming Memory Devices

Because the Neuron 5000 Processor does not have any on-chip user-accessible NVM, only the external serial EEPROM or flash devices need to be programmed with the application and configuration data. The memory devices can be programmed in any of the following three ways:

- In-circuit programming on the board
- Over the network
- Pre-programming before soldering on the board

Migration Considerations

Most device designs that use the previous generation Neuron 3120 or Neuron 3150 Chip can transition to using the Neuron 5000 Processor. However, because the supply voltage and memory architecture between Neuron 3120 / 3150 Chips and Neuron 5000 Processors are different, hardware redesign of the boards is required to transition to the Neuron 5000 Processor.

The recommended migration path for devices that are based on a Neuron Chip depends on the transceiver type used with the Neuron Chip, as shown in Table 2.

See the *5000 Series Chip Data Book* for more information about migrating device designs for Neuron 3120 / 3150 Chips to Neuron 5000 Processors.

Current Transceiver Type Used	Equivalent 5000 Family Design	Comments
FTT-10A transceiver	FT 5000 Smart Transceiver plus: FT-X3 Communications Transformer	Echelon recommends using an FT 5000 Smart Transceiver for TP/FT-10 channels
EIA-485 Transceiver	Neuron 5000 Processor plus: EIA-485 Transceiver OR (if possible) FT 5000 Smart Transceiver plus: FT-X3 Communications Transformer	If your design is flexible enough to allow either an EIA-485 channel or a TP/FT-10 channel, Echelon recommends using the FT 5000 Smart Transceiver with the TP/FT-10 channel
TPT Twisted Pair Transceiver Module (for a TP/XF-1250 channel type)	Neuron 5000 Processor plus: TPT Twisted Pair Transceiver Module (for a TP/XF-1250 channel type)	The Neuron 5000 Processor must be configured to operate in 3.3V Single-Ended Mode with the TPT Twisted Pair Transceiver Module and external circuitry for Single Ended to Differential Mode conversion
Other transceiver type	Neuron 5000 Processor plus: Other transceiver type	The Neuron 5000 Processor can connect to other transceiver types for the supported channel types, although additional hardware design work might be required

Table 2: Migration for Devices with Neuron Chips

End-to-End Solutions

A typical Neuron 5000 Processor based device requires a power source, crystal, external memory, and an I/O interface to the device being controlled (see Figure 6 for a typical Neuron 5000 Processor based device).

Echelon provides all of the building blocks required to successfully design and field cost-effective, robust products based on the Neuron 5000 Processor. Our end-to-end solutions include a comprehensive set of development tools, network interfaces, routers, and network tools. Pre-production design review services, training, and worldwide technical support—including on-site support—are available through Echelon's LonSupport™ technical assistance program.

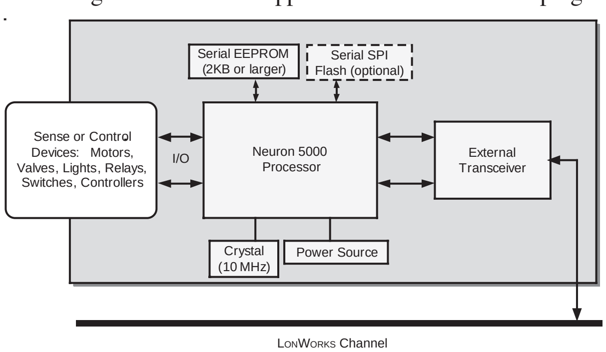

Figure 6: Typical LonWorks Based Device Block Diagram

Neuron 5000 Processor Pin Configuration

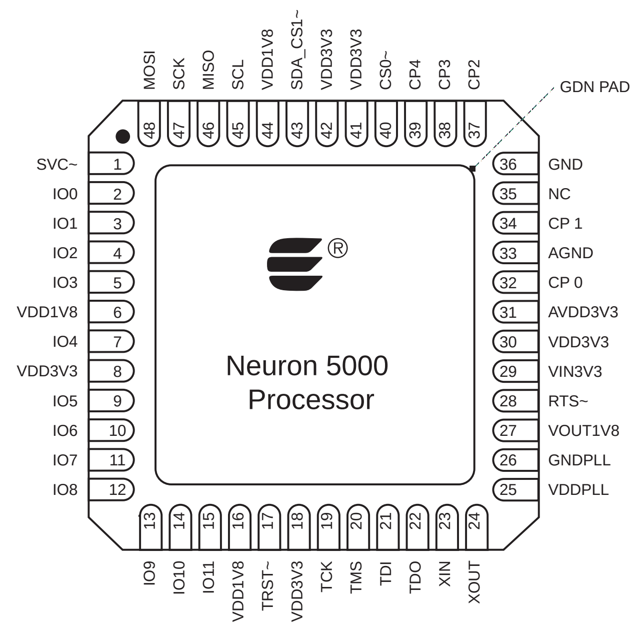

Figure 7: Neuron 5000 Processor Pinout

Neuron 5000 Processor Pin Descriptions

All digital inputs are low-voltage transistor-transistor logic (LVTTL) compatible, low leakage, 5V tolerant, with hysteresis. All digital outputs are slew-rate limited to reduce Electromagnetic Interference (EMI) concerns.

Pin Name	Pin Number	Type	Description
SVC~	1	Digital I/O	Service (active low)
IO0	2	Digital I/O	IO0 for I/O Objects
IO1	3	Digital I/O	IO1 for I/O Objects
IO2	4	Digital I/O	IO2 for I/O Objects
IO3	5	Digital I/O	IO3 for I/O Objects
VDD1V8	6	Power	1.8 V input from internal voltage regulator
IO4	7	Digital I/O	IO4 for I/O Objects
VDD3V3	8	Power	3.3 V Power
IO5	9	Digital I/O	IO5 for I/O Objects
IO6	10	Digital I/O	IO6 for I/O Objects
IO7	11	Digital I/O	IO7 for I/O Objects
IO8	12	Digital I/O	IO8 for I/O Objects
IO9	13	Digital I/O	IO9 for I/O Objects
IO10	14	Digital I/O	IO10 for I/O Objects
IO11	15	Digital I/O	IO11 for I/O Objects
VDD1V8	16	Power	1.8 V input from internal voltage regulator
TRST~	17	Digital Input	JTAG Test Reset (active low)
VDD3V3	18	Power	3.3 V Power

Pin Name	Pin Number	Type	Description
TCK	19	Digital Input	JTAG Test Clock
TMS	20	Digital Input	JTAG Test Mode Select
TDI	21	Digital Input	JTAG Test Data In
TDO	22	Digital Output	JTAG Test Data Out
XIN	23	Oscillator In	Crystal oscillator input
XOUT	24	Oscillator Out	Crystal oscillator Output
VDDPLL	25	Power	1.8 V input from internal voltage regulator
GNDPLL	26	Power	Ground
VOUT1V8	27	Power	1.8 V output from internal voltage regulator
RST~	28	Digital I/O	Reset (active low)
VIN3V3	29	Power	3.3 V input to internal voltage regulator
VDD3V3	30	Power	3.3 V Power
AVDD3V3	31	Power	3.3 V Power
CP0	32	Communications	Single-Ended Mode: Receive serial data Special Purpose Mode: Receive serial data
AGND	33		Ground
CP1	34	Communications	Single-Ended Mode: Transmit serial data Special Purpose Mode: Transmit serial data
NC	35	N/A	No Connect
GND	36	Ground	Ground
CP2	37	Communications	Single-Ended Mode: External transceiver enable Special Purpose Mode: Bit clock
CP3	38	Communications	Single-Ended Mode: Sleep Special Purpose Mode: Wake up
CP4	39	Communications	Single-Ended Mode: Collision detect Special Purpose Mode: Frame clock
CS0~	40	Digital I/O	SPI slave select 0 (active low)
VDD3V3	41	Power	3.3 V Power
VDD3V3	42	Power	3.3 V Power
SDA_CS1~	43	Digital I/O	I^2C: serial data (SDA) SPI: slave select 1 (CS1~, active low)
VDD1V8	44	Power	1.8 V input from internal voltage regulator
SCL	45	Digital I/O	I^2C: serial clock (SCL)
MISO	46	Digital I/O	SPI master input, slave output
SCK	47	Digital I/O	SPI serial clock
MOSI	48	Digital I/O	SPI master output, slave input
PAD	49	Ground Pad	Ground

Table 3: Neuron 5000 Processor Pin Description

Electrical Characteristics

Neuron 5000 Processor Operating Conditions

Parameter	Description	Minimum	Typical	Maximum
V_{DD3V3}	Supply voltage	3.00 V	3.3 V	3.60 V
V_{IO}	Digital input pins voltage range	-0.3 V		5.5 V
TA	Ambient temperature	-40° C		+85° C
f_{XIN}	XIN clock frequency	-	10.0000 MHz	-
I_{DD3-RX}	Current consumption in receive mode		TBD	TBD
I_{DD3-TX}	Current consumption in transmit mode		TBD	TBD

Table 4: Neuron 5000 Processor Operating Conditions

Input/Output Pin Characteristics

TBD

Recommended Neuron 5000 Processor Pad Layout

TBD

Chip Package Diagrams

TBD

Specifications

Function	Description
RoHS Compliant	The Neuron 5000 Processor is compliant with the European Directive 2002/95/EC on the restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment.
EMI	Designed to comply with FCC Part 15 Level B and EN55022 Level B
ESD	Designed to comply with EN 61000-4-2, Level 4
Radiated Electromagnetic Susceptibility	Designed to comply with EN 61000-4-3, Level 3
Fast Transient/Burst Immunity	Designed to comply with EN 61000-4-4, Level 4
Surge Immunity	Designed to comply with EN 61000-4-5, Level 3
Conducted RF Immunity	Designed to comply with EN 61000-4-6, Level 3
Transmission Speed	Depends on network transceiver: • 78 kbit/s for TP/FT-10 channel • 1250 kbit/s for TP/XF-1250 channel • See EIA-485 channel specification for transmission speed characteristics
Operating Temperature	-40 to 85°C
Operating Humidity	25-90% RH @50°C, non-condensing
Non-operating Humidity	95% RH @ 50°C, non-condensing
Reflow Soldering Temperature Profile	Refer to Joint Industry Standard document IPC/JEDEC J-STD-020D.1 (March 2008)
Peak Reflow Soldering Temperature	260°C

Ordering Information

The Neuron 5000 Processor can be purchased from Echelon directly or from any of the distributors carrying Echelon products. For more information on sales, visit www.echelon.com/sales

Product	Echelon Model Number	Where to Buy?
Neuron 5000 Processor	14305R	Echelon Direct or Distributors www.echelon.com/sales