NCP1529

1.7MHz, 1A, High Efficiency, Low Ripple, Adjustable Output Voltage Step-down Converter

ON Semiconductor®

http://onsemi.com

The NCP1529 step−down DC−DC converter is a monolithic integrated circuit for portable applications powered from one cell Li−ion or three cell Alkaline/NiCd/NiMH batteries. The device − available in an adjustable output voltage from 0.9 V to 3.9 V − is able to deliver up to 1 A. It uses synchronous rectification to increase efficiency and reduce external part count. The device also has a built−in 1.7 MHz (nominal) oscillator which reduces component size by allowing a small inductor and capacitors. Automatic switching PWM/PFM mode offers improved system efficiency.

Additional features include integrated soft−start, cycle−by−cycle current limiting and thermal shutdown protection.

The NCP1529 is available in a space saving, low profile 2x2x0.5 mm UDFN6 package and TSOP−5 package.

Features

- Up to 96% Efficiency
- Best In Class Ripple, including PFM mode
- Source up 1 A
- 1.7 MHz Switching Frequency
- Adjustable Output Voltage from 0.9 V to 3.9 V
- Synchronous rectification for higher efficiency
- 2.7 V to 5.5 V Input Voltage Range
- Low Quiescent Current 28 μA
- Shutdown Current Consumption of 0.3 μA
- Thermal Limit Protection
- Short Circuit Protection
- All pins are fully ESD protected
- These are Pb−Free Devices

Typical Applications

- Cellular Phones, Smart Phones and PDAs
- Digital Still Cameras
- MP3 Players and Portable Audio Systems
- Wireless and DSL Modems
- USB powered devices
- Portable Equipment

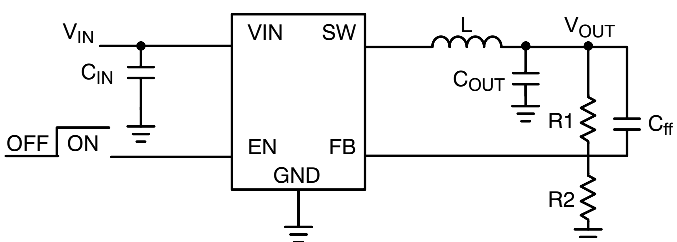
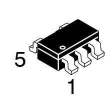
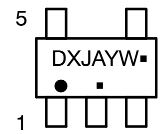


Figure 1. Typical Application

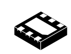
MARKING DIAGRAM



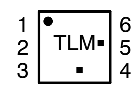
TSOP−5
SN SUFFIX
CASE 483



DXJ = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)



UDFN6
MU SUFFIX
CASE 517AB



TL = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NCP1529ASNT1G	TSOP−5 (Pb−Free)	3000/Tape & Reel
NCP1529MUTBG	UDFN6 (Pb−Free)	3000/Tape & Reel

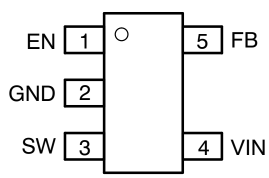
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

PIN FUNCTION DESCRIPTION

Pin TSOP−5	Pin UDFN6	Pin Name	Type	Description
1	6	EN	Analog Input	Enable for switching regulators. This pin is active HIGH and is turned off by logic LOW on this pin.
2	2,4,7 (Note 1)	GND	Analog / Power Ground	This pin is the GND reference for the NFET power stage and the analog section of the IC. The pin must be connected to the system ground.
3	5	SW	Analog Output	Connection from power MOSFETs to the Inductor.
4	3	VIN	Analog / Power Input	Power supply input for the PFET power stage, analog and digital blocks. The pin must be decoupled to ground by a 4.7 μF ceramic capacitor.
5	1	FB	Analog Input	Feedback voltage from the output of the power supply. This is the input to the error amplifier.

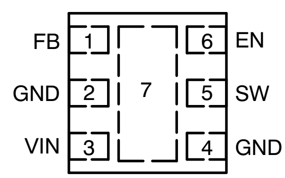
1. Exposed pad for UDFN6 package, named Pin 7, must be connected to system ground.

PIN CONNECTIONS



(Top View)

Figure 2. Pin Connections − TSOP−5



(Top View)

Figure 3. Pin Connections − UDFN6

PERFORMANCES

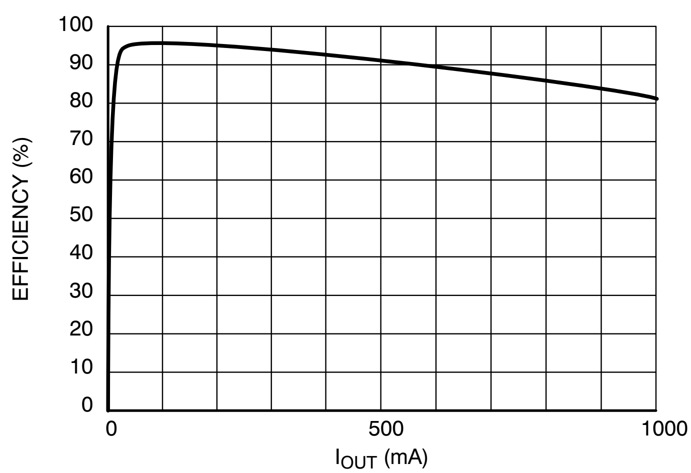


Figure 4. Efficiency vs Output Current
V_{IN} = 3.6 V, V_{OUT} = 3.3 V

FUNCTIONAL BLOC DIAGRAM

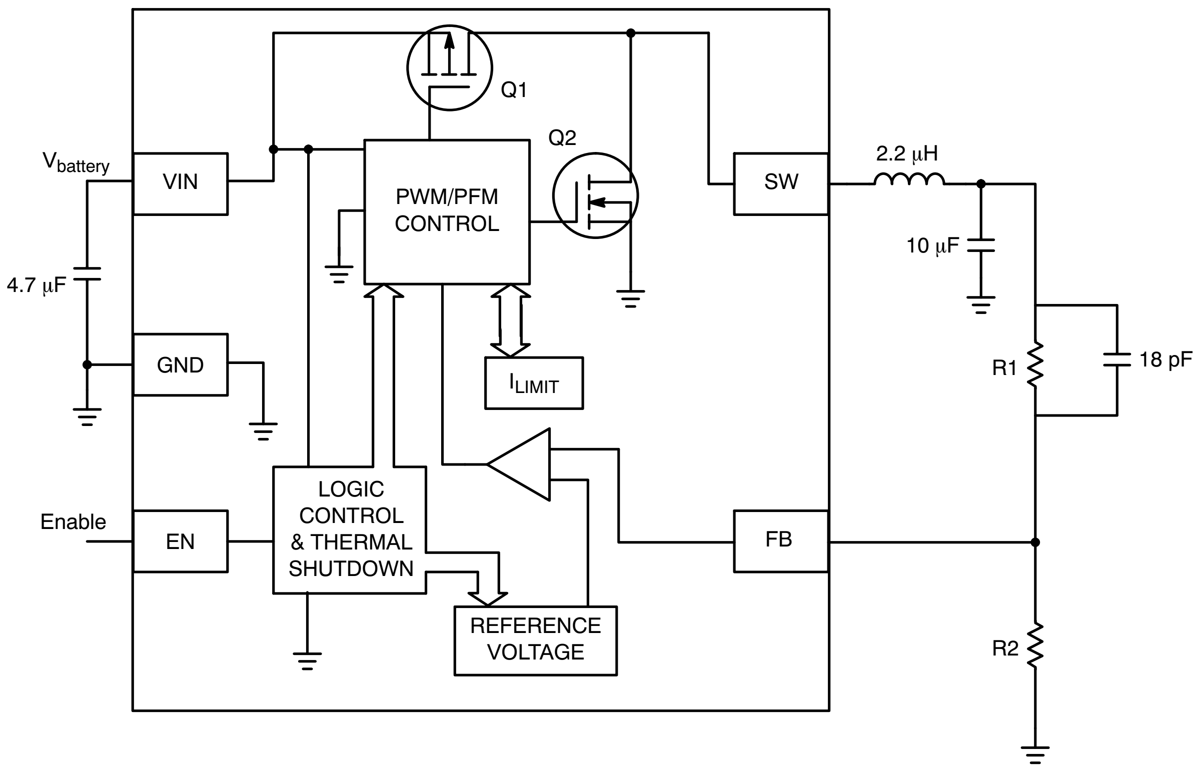


Figure 5. Simplified Block Diagram

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Minimum Voltage All Pins	V_{min}	−0.3	V
Maximum Voltage All Pins (Note 2)	V_{max}	7.0	V
Maximum Voltage EN, ENI2C, SDA, SCL	V_{max}	V_{IN} + 0.3	V
Thermal Resistance, Junction−to−Air (TSOP−5 Package) Thermal Resistance using TSOP−5 Recommended Board Layout (Note 9)	$R_{\theta JA}$	300 110	°C/W
Thermal Resistance, Junction−to−Air (UDFN6 Package) Thermal Resistance using UDFN6 Recommended Board Layout (Note 9)	$R_{\theta JA}$	220 40	°C/W
Operating Ambient Temperature Range (Notes 7 and 8)	T_A	−40 to 85	°C
Storage Temperature Range	T_{stg}	−55 to 150	°C
Junction Operating Temperature (Notes 7 and 8)	T_j	−40 to 150	°C
Latchup Current Maximum Rating (T_A = 85°C) (Note 5) Other Pins	Lu	±100	mA
ESD Withstand Voltage (Note 4) Human Body Model Machine Model	V_{esd}	 2.0 200	 kV V
Moisture Sensitivity Level (Note 6)	MSL	1	per IPC

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

2. Maximum electrical ratings are defined as those values beyond which damage to the device may occur at T_A = 25°C.
3. According to JEDEC standard JESD22−A108B.
4. This device series contains ESD protection and exceeds the following tests:
   Human Body Model (HBM) per JEDEC standard: JESD22−A114.
   Machine Model (MM) per JEDEC standard: JESD22−A115.
5. Latchup current maximum rating per JEDEC standard: JESD78.
6. JEDEC Standard: J−STD−020A.
7. In applications with high power dissipation (low V_{IN}, high I_{OUT}), special care must be paid to thermal dissipation issues. Board design considerations − thermal dissipation vias, traces or planes and PCB material − can significantly improve junction to air thermal resistance $R_{\theta JA}$ (for more information, see design and layout consideration section). Environmental conditions such as ambient temperature T_A brings thermal limitation on maximum power dissipation allowed.
   The following formula gives calculation of maximum ambient temperature allowed by the application:
   $T_{A\ MAX} = T_{J\ MAX} - (R_{\theta JA} \times P_d)$
   Where: T_J is the junction temperature,
   P_d is the maximum power dissipated by the device (worst case of the application),
   and $R_{\theta JA}$ is the junction−to−ambient thermal resistance.
8. To prevent permanent thermal damages, this device include a thermal shutdown which engages at 180°C (typ).
9. Board recommended TSOP−5 and UDFN6 layouts are described on Layout Considerations section.

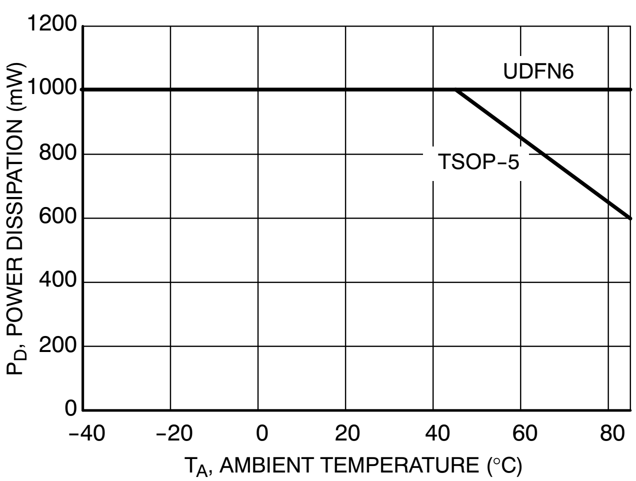


Figure 7. Power Derating

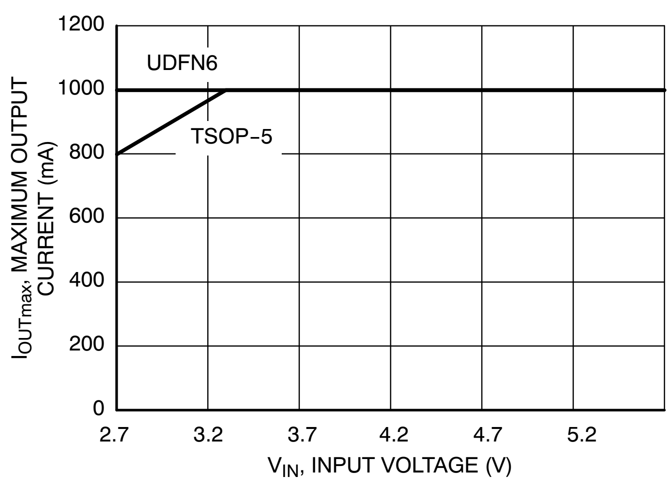


Figure 6. Maximum Output Current, T_A = 45°C

ELECTRICAL CHARACTERISTICS (Typical values are referenced to T_A = +25°C, Min and Max values are referenced −40°C to +85°C ambient temperature, unless otherwise noted, operating conditions V_{IN} = 3.6 V, V_{OUT} = 1.2 V, unless otherwise noted.)

Rating	Conditions	Symbol	Min	Typ	Max	Unit
INPUT VOLTAGE						
Input Voltage Range		V_{in}	2.7	–	5.5	V
Quiescent Current	No Switching, No load	I_Q	–	28	39	μA
Standby Current	EN Low	I_{STB}	–	0.3	1.0	μA
Under Voltage Lockout	V_{IN} Falling	V_{UVLO}	2.2	2.4	2.55	V
Under Voltage Hysteretis		V_{UVLOH}	–	100	–	mV
ANALOG AND DIGITAL PIN						
Positive going Input High Voltage Threshold		V_{IH}	1.2	–	–	V
Negative going Input High Voltage Threshold		V_{IL}	–	–	0.4	V
EN Threshold Hysteresis		V_{ENH}	–	100	–	mV
EN High Input Current	EN = 3.6 V	I_{ENH}	–	1.5	–	μA
OUTPUT						
Feedback Voltage Level		V_{FB}	–	0.6	–	V
Minimum Output Voltage		V_{OUT}	–	0.9	–	V
Maximum Output Voltage		V_{OUT}	–	3.3	–	V
Maximum Output Voltage for USB or 5 V Rail Powered Applications (Note 10)	V_{IN} from 4.3 V to 5.5 V	V_{OUT}	–	3.9	–	V
Output Voltage Accuracy (Note 11)	Room Temperature Overtemperature Range	ΔV_{OUT}	– −3	±1 ±2	– +3	%
Maximum Output Current		I_{OUTMAX}	1	–	–	A
Output Voltage Load Regulation Overtemperature	Load = 100 mA to 1000 mA (PWM Mode) Load = 0 mA to 100 mA (PFM Mode)	V_{LOADR}	– –	−0.9 1.1	– –	%
Load Transient Response Rise/Fall Time 1 μs	10 mA to 100 mA Load Step (PFM to PWM Mode) 200 mA to 600 mA Load Step (PWM to PWM Mode)	V_{LOADT}	– –	40 85	– –	mV
Output Voltage Line Regulation Load = 100 mA	V_{IN} = 2.7 V to 5.5 V	V_{LINER}	–	0.05	–	%
Line Transient Response Load = 100 mA	3.6 V to 3.2 V Line Step (Fall Time = 50 μs)	V_{LINET}	–	6.0	–	mV_{PP}
Output Voltage Ripple	I_{OUT} = 0 mA I_{OUT} = 300 mA	V_{RIPPLE}	– –	8.0 3.0	– –	mV_{PP}
Switching Frequency		F_{SW}	1.2	1.7	2.2	MHz
Duty Cycle		D	–	–	100	%
Soft−Start Time	Time from EN to 90% of Output Voltage	t_{START}	–	310	500	μs
POWER SWITCHES						
High−Side MOSFET On−Resistance		R_{ONHS}	–	400	–	mΩ
Low−Side MOSFET On−Resistance		R_{ONLS}	–	300	–	mΩ
High−Side MOSFET Leakage Current		I_{LEAKHS}	–	0.05	–	μA
Low−Side MOSFET Leakage Current		I_{LEAKLS}	–	0.01	–	μA
PROTECTION						
DC−DC Short Circuit Protection	Peak Inductor Current	I_{PK}	–	1.6	–	A
Thermal Shutdown Threshold		T_{SD}	–	180	–	°C
Thermal Shutdown Hysteresis		T_{SDH}	–	40	–	°C

10. Functionality guaranteed per design and characterization, see chapter ”USB or 5 V Rail Powered Applications”.
11. The overall output voltage tolerance depends upon the accuracy of the external resistor (R1 and R2).

TABLE OF GRAPHS

Typical Characteristics for Step−down Converter			Figure
η	Efficiency	vs. Output Current	10, 11, 12
$I_{q\ ON}$	Quiescent Current, PFM no load	vs. Input Voltage	9
$I_{q\ OFF}$	Standby Current, EN Low	vs. Input Voltage	8
F_{SW}	Switching Frequency	vs. Ambient Temperature	13
V_{LOADR}	Load Regulation	vs. Load Current	14
V_{LOADT}	Load Transient Response		16, 17
V_{LINER}	Line Regulation	vs. Output Current	15
V_{LINET}	Line Transient Response		18, 19
t_{START}	Soft Start		20
I_{PK}	Short Circuit Protection		21
V_{UVLO}	Under Voltage Lockout Threshold	vs. Ambient Temperature	22
V_{IL}, V_{IH}	Enable Threshold	vs. Ambient Temperature	23
P, G	Phase & Gain Performance		24

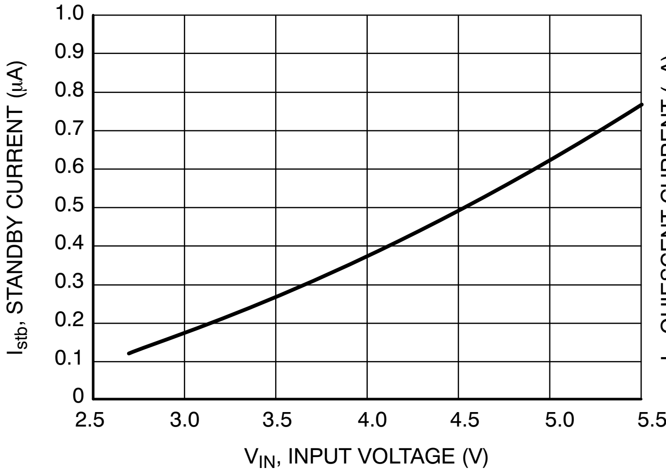


Figure 8. Standby Current vs. Input Voltage (Enable = 0, Temperature = 25°C)

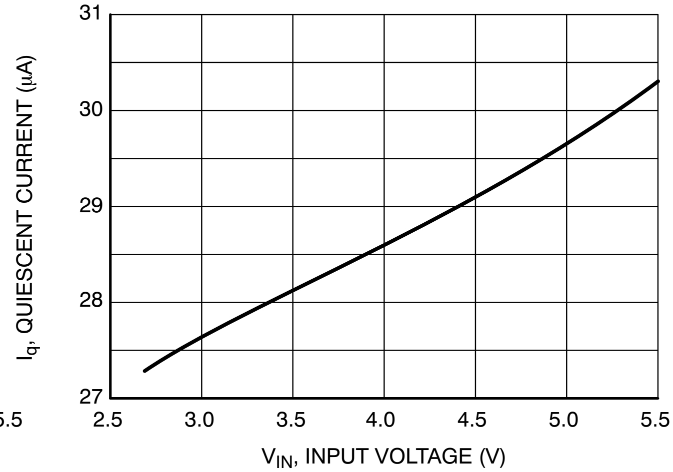


Figure 9. Quiescent Current vs. Input Voltage (Open Loop, Feedback = 1, Temperature = 25°C)

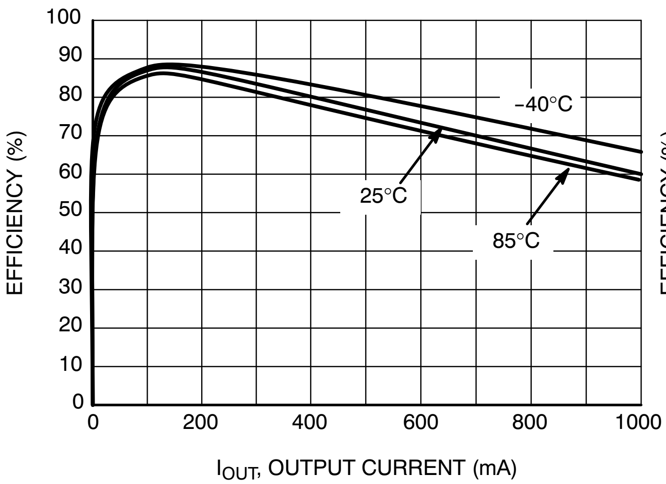


Figure 10. Efficiency vs. Output Current (V_{IN} = 3.3 V, V_{OUT} = 1.2 V)

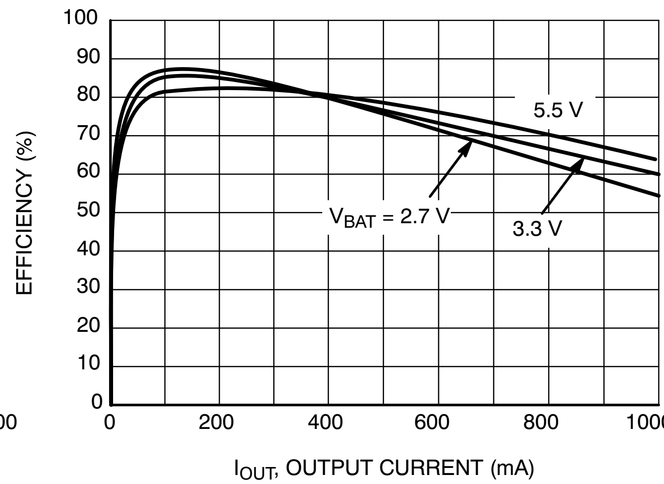


Figure 11. Efficiency vs. Output Current (V_{IN} = 1.2 V, Temperature = 25°C)

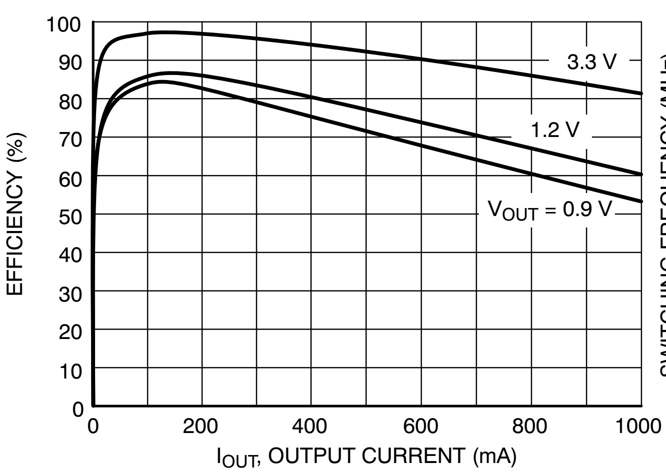


Figure 12. Efficiency vs. Output Current (V_{IN} = 3.6 V, Temperature = 25°C)

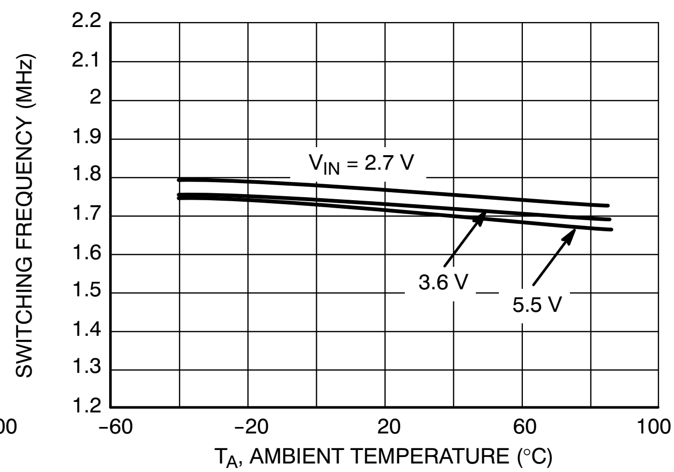


Figure 13. Switching Frequency vs. Ambient Temperature (V_{out} = 1.2 V, I_{out} = 200 mA)

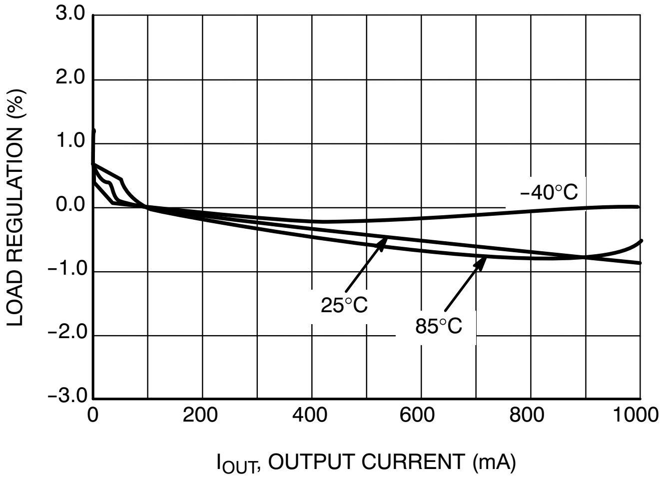


Figure 14. Load Regulation vs. Output Current (V_{IN} = 5.5 V, V_{OUT} = 1.2 V)

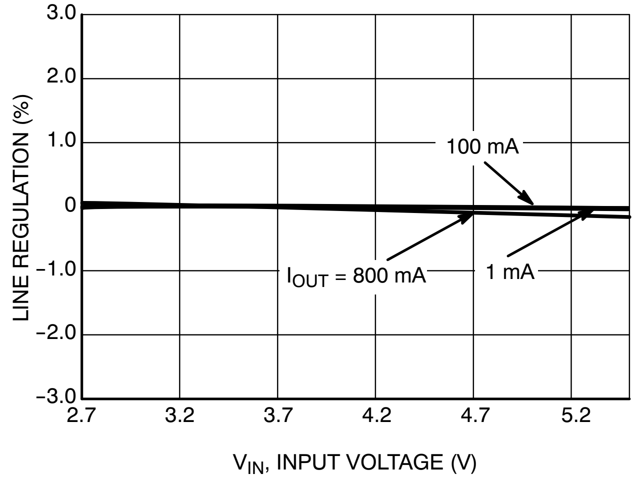


Figure 15. Line Regulation vs. Input Voltage (V_{OUT} = 1.2 V, Temperature = 25°C)

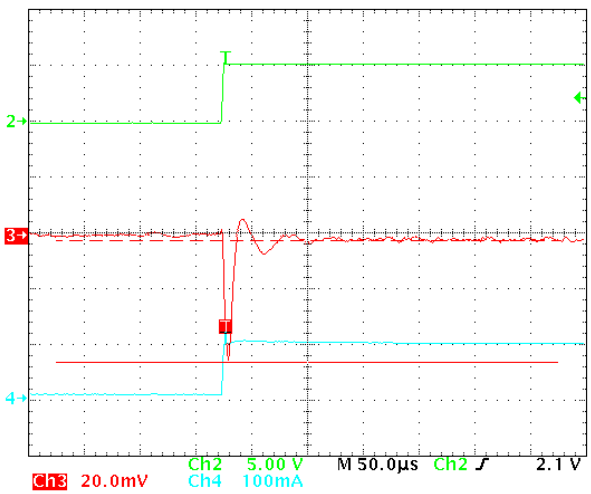


Figure 16. 10 mA to 100 mA Load Transient in 1 µs (V_{IN} = 3.6 V, V_{OUT} = 1.2 V, Temperature = 25°C)

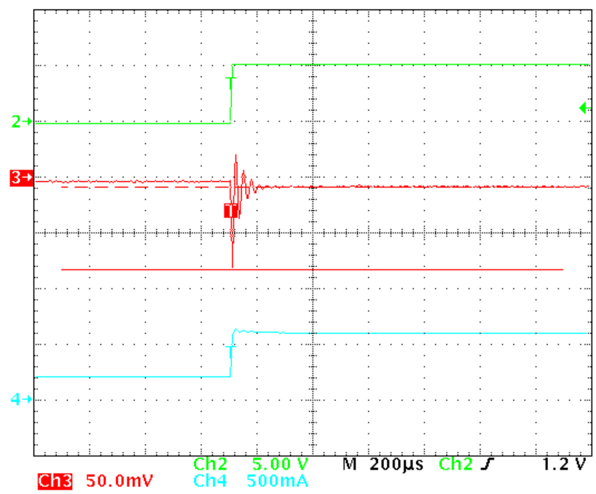


Figure 17. 200 mA to 600 mA Load Transient in 1 µs (V_{IN} = 3.6 V, V_{OUT} = 1.2 V, Temperature = 25°C)

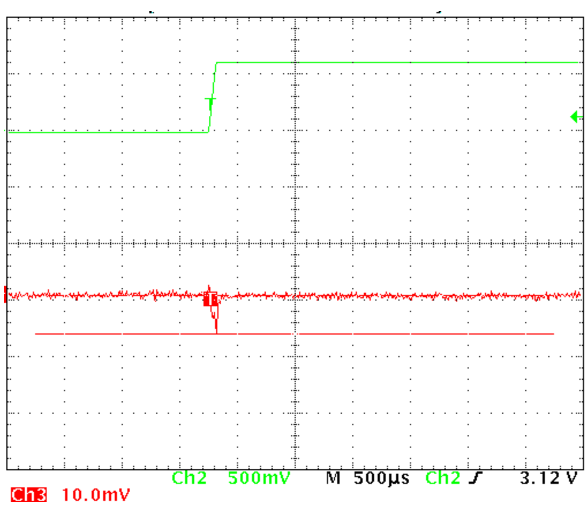


Figure 18. 3.0 V to 3.6 V Line Transient, Rise = 50 µs (V_{IN} = 1.2 V, I_{OUT} = 100 mA, Temperature = 25°C)

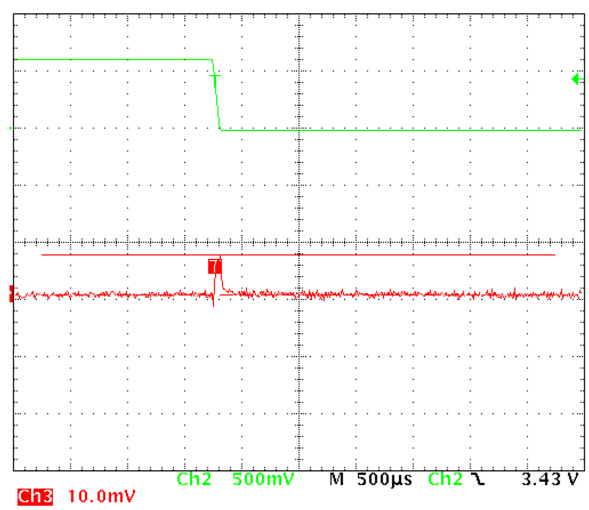


Figure 19. 3.6 V to 3.0 V Line Transient, Fall = 50 µs (V_{IN} = 1.2 V, I_{OUT} = 100 mA, Temperature = 25°C)

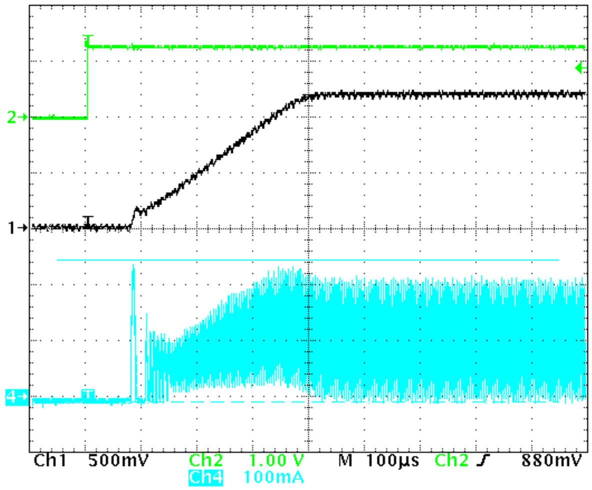


Figure 20. Typical Soft−Start (V_{IN} = 3.6 V, V_{OUT} = 1.2 V, I_{OUT} = 100 mA, Temperature = 25°C)

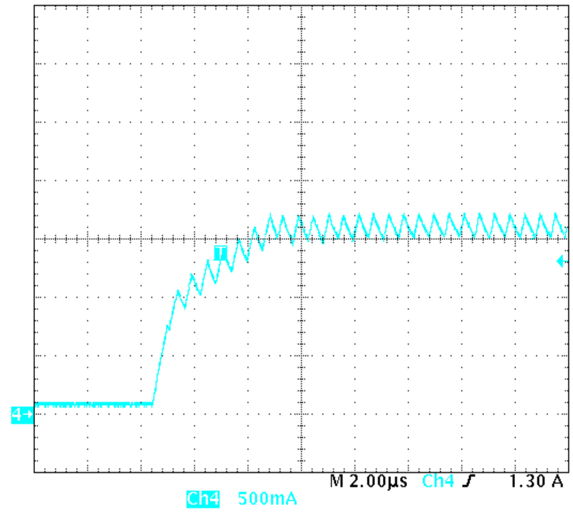


Figure 21. Short−Circuit Protection (V_{IN} = 3.6 V, V_{OUT} = 1.2 V, I_{OUT} = CC, Temperature = 25°C)

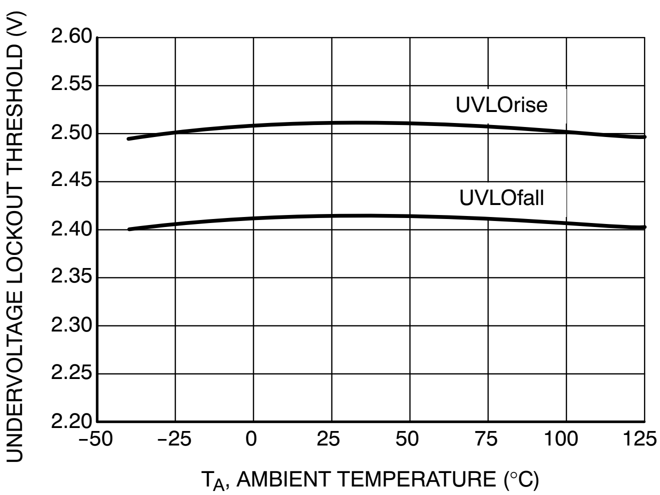


Figure 22. Undervoltage Lockout Threshold vs. Ambient Temperature

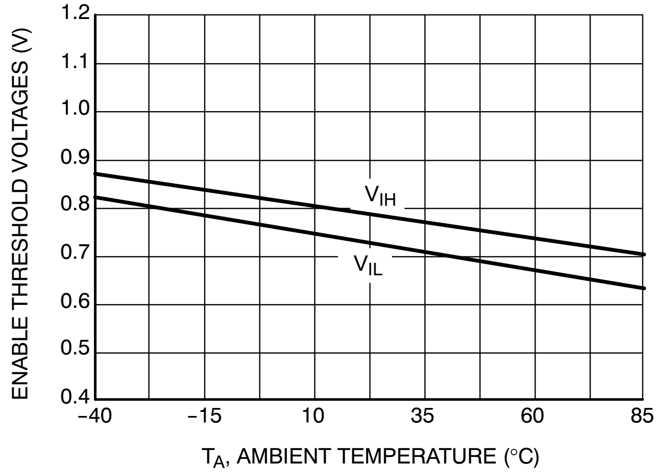


Figure 23. Enable Threshold Voltages vs. Ambient Temperature

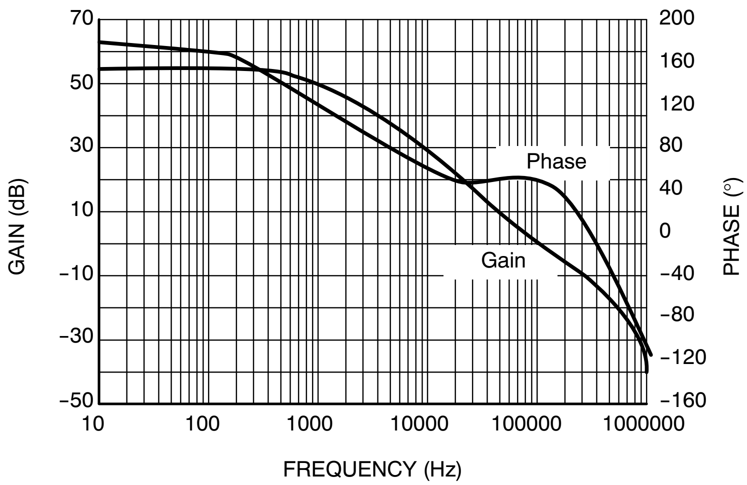


Figure 24. Phase and Gain Performance (V_{IN} = 3.6 V, V_{OUT} = 1.2 V, I_{OUT} = 200 mA, Temperature = 25°C)

DC/DC OPERATION DESCRIPTION

Detailed Description

The NCP1529 uses a constant frequency, current mode step−down architecture. Both the main (P−channel MOSFET) and synchronous (N−channel MOSFET) switches are internal.

The output voltage is set by an external resistor divider in the range of 0.9 V to 3.9 V and can source at least 1A.

The NCP1529 works with two modes of operation; PWM/PFM depending on the current required. In PWM mode, the device can supply voltage with a tolerance of ±3% and 90% efficiency or better. Lighter load currents cause the device to automatically switch into PFM mode to reduce current consumption and extended battery life.

Additional features include soft−start, undervoltage protection, current overload protection and thermal shutdown protection. As shown on Figure 1, only six external components are required. The part uses an internal reference voltage of 0.6 V. It is recommended to keep NCP1529 in shutdown mode until the input voltage is 2.7 V or higher.

PWM Operating Mode

In this mode, the output voltage of the device is regulated by modulating the on−time pulse width of the main switch Q1 at a fixed 1.7 MHz frequency.

The switching of the PMOS Q1 is controlled by a flip−flop driven by the internal oscillator and a comparator that compares the error signal from an error amplifier with the sum of the sensed current signal and compensation ramp.

The driver switches ON and OFF the upper side transistor (Q1) while the lower side transistor is switched OFF then ON.

At the beginning of each cycle, the main switch Q1 is turned ON by the rising edge of the internal oscillator clock. The inductor current ramps up until the sum of the current sense signal and compensation ramp becomes higher than the error amplifier's voltage. Once this has occurred, the PWM comparator resets the flip−flop, Q1 is turned OFF while the synchronous switch Q2 is turned ON. Q2 replaces the external Schottky diode to reduce the conduction loss and improve the efficiency. To avoid overall power loss, a certain amount of dead time is introduced to ensure Q1 is completely turned OFF before Q2 is being turned ON.

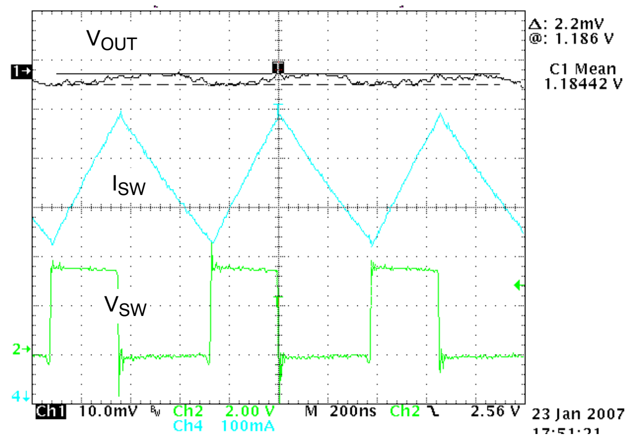


Figure 25. PWM Switching Waveforms (V_{IN} = 3.6 V, V_{OUT} = 1.2 V, I_{OUT} = 600 mA, Temperature = 25°C)

PFM Operating Mode

Under light load conditions, the NCP1529 enters in low current PFM mode of operation to reduce power consumption. The output regulation is implemented by pulse frequency modulation. If the output voltage drops below the threshold of PFM comparator a new cycle will be initiated by the PFM comparator to turn on the switch Q1. Q1 remains ON during the minimum on time of the structure while Q2 is in its current source mode. The peak inductor current depends upon the drop between input and output voltage. After a short dead time delay where Q1 is switched OFF, Q2 is turned in its ON state. The negative current detector will detect when the inductor current drops below zero and sends a signal to turn Q2 to current source mode to prevent a too large deregulation of the output voltage. When the output voltage falls below the threshold of the PFM comparator, a new cycle starts immediately.

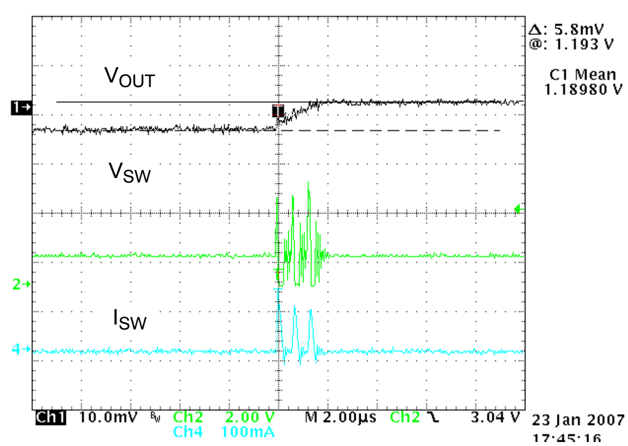


Figure 26. PFM Switching Waveforms (V_{IN} = 3.6 V, V_{OUT} = 1.2 V, I_{OUT} = 0 mA, Temperature = 25°C)

Soft−Start

The NCP1529 uses soft−start to limit the inrush current when the device is initially powered up or enabled. Soft start is implemented by gradually increasing the reference voltage until it reaches the full reference voltage. During startup, a pulsed current source charges the internal soft−start capacitor to provide gradually increasing reference voltage. When the voltage across the capacitor ramps up to the nominal reference voltage, the pulsed current source will be switched off and the reference voltage will switch to the regular reference voltage.

Cycle−by−cycle Current Limitation

From the block diagram, an I_{LIM} comparator is used to realize cycle−by−cycle current limit protection. The comparator compares the SW pin voltage with the reference voltage, which is biased by a constant current. If the inductor current reaches the limit, the I_{LIM} comparator detects the SW voltage falling below the reference voltage and releases the signal to turn off the switch Q1. The cycle−by−cycle current limit is set at 1200 mA (nom).

Low Dropout Operation

The NCP1529 offers a low input to output voltage difference. The NCP1529 can operate at 100% duty cycle.

In this mode the PMOS (Q1) remains completely ON. The minimum input voltage to maintain regulation can be calculated as:

$$V_{out} = V_{OUT(max)} + \left(I_{OUT}\left(R_{DS(on)} - R_{INDUCTOR}\right)\right) \quad \text{(eq. 1)}$$

- V_{OUT}: Output Voltage (V)
- I_{OUT}: Max Output Current
- $R_{DS(on)}$: P−Channel Switch $R_{DS(on)}$
- $R_{INDUCTOR}$: Inductor Resistance (DCR)

Undervoltage Lockout

The Input voltage V_{IN} must reach 2.4 V (typ) before the NCP1529 enables the DC/DC converter output to begin the start up sequence (see soft−start section). The UVLO threshold hysteresis is typically 100 mV.

Shutdown Mode

Forcing this pin to a voltage below 0.4 V will shut down the IC. In shutdown mode, the internal reference, oscillator and most of the control circuitries are turned off. Therefore, the typical current consumption will be 0.3 μA (typical value). Applying a voltage above 1.2 V to EN pin will enable the DC/DC converter for normal operation. The device will go through soft−start to normal operation.

Thermal Shutdown

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction Temperature is exceeded. If the junction temperature exceeds 180°C, the device shuts down. In this mode all power transistors and control circuits are turned off. The device restarts in soft−start after the temperature drops below 140°C. This feature is provided to prevent catastrophic failures from accidental device overheating.

Short Circuit Protection

When the output is shorted to ground, the device limits the inductor current. The duty−cycle is minimum and the consumption on the input line is 550 mA (typ). When the short circuit condition is removed, the device returns to the normal mode of operation.

USB or 5 V Rail Powered Applications

For USB or 5 V rail powered applications, NCP1529 is able to supply voltages up to 3.9 V, 600 mA, operating in PWM mode only, with high efficiency (Figure 27), low output voltage ripple and good load regulation results over all current range (Figure 28).

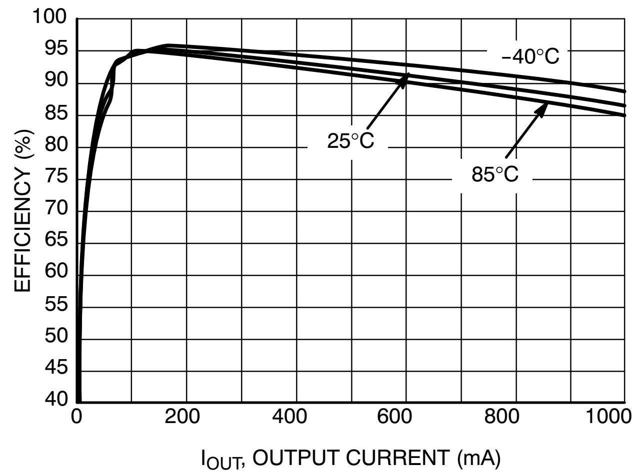


Figure 27. Efficiency vs. Output Current (V_{IN} = 5.0 V, V_{OUT} = 3.9 V)

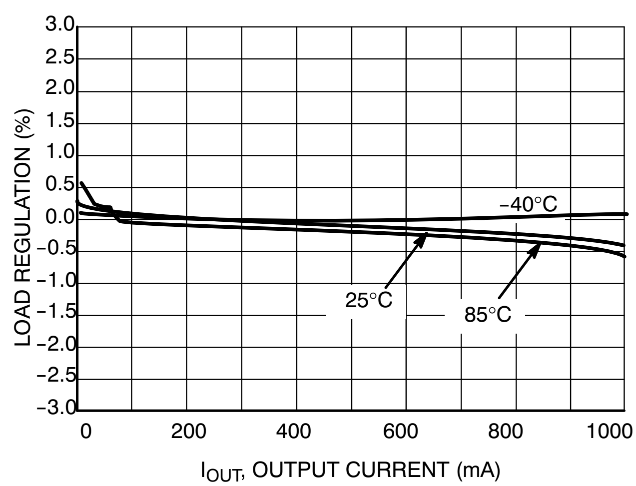


Figure 28. Load Regulation vs. Output Current (V_{IN} = 5.0 V, V_{OUT} = 3.9 V)

APPLICATION INFORMATION

Output Voltage Selection

The output voltage is programmed through an external resistor divider connected from V_{OUT} to FB then to GND.

For low power consumption and noise immunity, the resistor from FB to GND (R2) should be in the [100k–600k] range. If R2 is 200 k given the V_{FB} is 0.6 V, the current through the divider will be 3.0 μA.

The formula below gives the value of V_{OUT}, given the desired R1 and the R1 value:

$$V_{out} = V_{FB} \times (1 + R1/R2) \quad \text{(eq. 2)}$$

- V_{OUT}: Output Voltage (V)
- V_{FB}: Feedback Voltage = 0.6 V
- R1: Feedback Resistor from V_{OUT} to FB
- R2: Feedback Resistor from FB to GND

Input Capacitor Selection

In PWM operating mode, the input current is pulsating with large switching noise. Using an input bypass capacitor can reduce the peak current transients drawn from the input supply source, thereby reducing switching noise significantly. The capacitance needed for the input bypass capacitor depends on the source impedance of the input supply.

The maximum RMS current occurs at 50% duty cycle with maximum output current, which is IO, max/2.

For NCP1529, a low profile ceramic capacitor of 4.7 μF should be used for most of the cases. For effective bypass results, the input capacitor should be placed as close as possible to the VIN Pin

Table 1. LIST OF INPUT CAPACITOR

Murata	GRM188R60J475KE	4.7 μF
	GRM21BR71C475KA	
Taiyo Yuden	JMK212BY475MG	4.7 μF
TDK	C2012X5R0J475KT	4.7 μF
	C1608X5R0J475KT	

Output L–C Filter Design Considerations

The NCP1529 operates at 1.7 MHz frequency and uses current mode architecture. The correct selection of the output filter ensures good stability and fast transient response.

Due to the nature of the buck converter, the output L–C filter must be selected to work with internal compensation. For NCP1529, the internal compensation is internally fixed and it is optimized for an output filter of L = 2.2 μH and C_{OUT} = 10 μF.

The corner frequency is given by:

$$f = \frac{1}{2\pi\sqrt{L \times C_{OUT}}} = \frac{1}{2\pi\sqrt{2.2\ \mu H \times 10\ \mu F}} = 34\ \text{kHz} \quad \text{(eq. 3)}$$

The device operates with inductance value of 2.2 μH. If the corner frequency is moved, it is recommended to check the loop stability depending of the accepted output ripple voltage and the required output current. Take care to check the loop stability. The phase margin is usually higher than 45°.

Table 2. L–C FILTER EXAMPLE

Inductance (L)	Output Capacitor (C_{OUT})
2.2 μH	10 μF
4.7 μH	4.7 μF

Inductor Selection

The inductor parameters directly related to device performances are saturation current and DC resistance and inductance value. The inductor ripple current (ΔI_L) decreases with higher inductance:

$$\Delta I_L = \frac{V_{OUT}}{L \times f_{SW}}\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad \text{(eq. 4)}$$

- ΔI_L: Peak to peak inductor ripple current
- L: Inductor value
- f_{SW}: Switching frequency

The saturation current of the inductor should be rated higher than the maximum load current plus half the ripple current:

$$I_{L(max)} = I_{O(max)} + \frac{\Delta I_L}{2} \quad \text{(eq. 5)}$$

- $I_{L(max)}$: Maximum inductor current
- $I_{O(max)}$: Maximum Output current

The inductor's resistance will factor into the overall efficiency of the converter. For best performances, the DC resistance should be less than 0.3 Ω for good efficiency.

Table 3. LIST OF INDUCTOR

FDK	MIPW3226 Series
TDK	VLF3010AT Series
	TFC252005 Series
Taiyo Yuden	LQ CBL2012
Coil Craft	DO1605–T Series
	LPS3008

Output Capacitor Selection

Selecting the proper output capacitor is based on the desired output ripple voltage. Ceramic capacitors with low ESR values will have the lowest output ripple voltage and are strongly recommended. The output capacitor requires either an X7R or X5R dielectric.

The output ripple voltage in PWM mode is given by:

$$\Delta V_{OUT} = \Delta I_L \times \left(\frac{1}{4 \times f_{SW} \times C_{OUT}} + ESR \right) \qquad \text{(eq. 6)}$$

Table 4. LIST OF OUTPUT CAPACITOR

Murata	GRM188R60J475KE	4.7 µF
	GRM21BR71C475KA	
	GRM188R60OJ106ME	10 µF
Taiyo Yuden	JMK212BY475MG	4.7 µF
	JMK212BJ106MG	10 µF
TDK	C2012X5R0J475	4.7 µuF
	C1608X5R0J475	
	C2012X5R0J106	10 µF

Feed–Forward Capacitor Selection

The feed–forward capacitor sets the feedback loop response and is critical to obtain good loop stability. Given that the compensation is internally fixed, an 18 pF ceramic capacitor is needed. Choose a small ceramic capacitor X7R or X5R or COG dielectric.

LAYOUT CONSIDERATIONS

Electrical Layout Considerations

Implementing a high frequency DC–DC converter requires respect of some rules to get a powerful portable application. Good layout is key to prevent switching regulators to generate noise to application and to themselves.

Electrical layout guide lines are:

- Use short and large traces when large amount of current is flowing.
- Keep the same ground reference for input and output capacitors to minimize the loop formed by high current path from the battery to the ground plane.
- Isolate feedback pin from the switching pin and the current loop to protect against any external parasitic signal coupling. Add a feed–forward capacitor between V_{OUT} and FB which adds a zero to the loop and participates to the good loop stability. A 18 pF capacitor is recommended to meet compensation requirements.

A four layer PCB with a ground plane and a power plane will help NCP1529 noise immunity and loop stability.

Thermal Layout Considerations

High power dissipation in small package leads to thermal consideration such as:

- Enlarge V_{IN} trace and added several vias connected to power plane.
- Connect GND pin to top plane.
- Join top, bottom and each ground plane together using several free vias in order to increase radiator size.

For high ambient temperature and high power dissipation requirements, UDFN6 package using exposed pad connected to main radiator is recommended. Refer to Notes 7, 8, and 9.

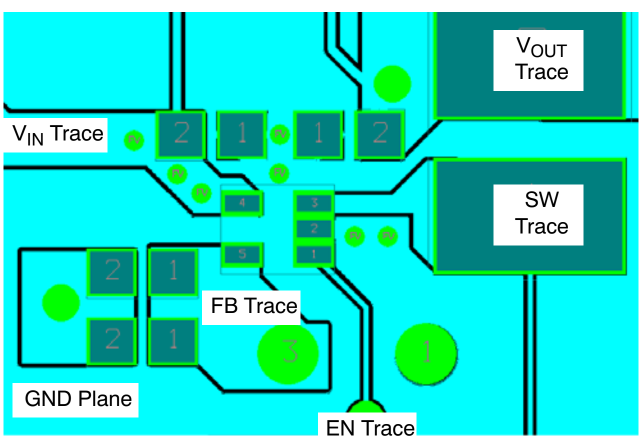


Figure 29. TSOP–5 Recommended Board Layout

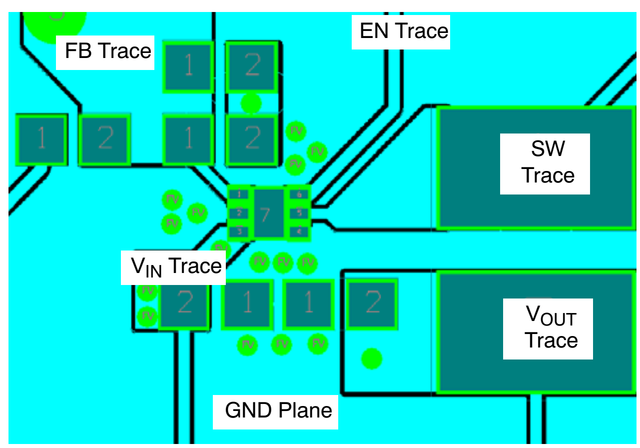
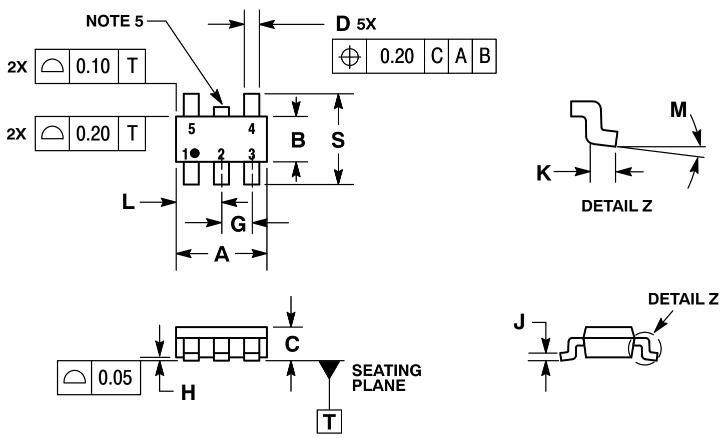


Figure 30. UDFN6 Recommended Board Layout

PACKAGE DIMENSIONS

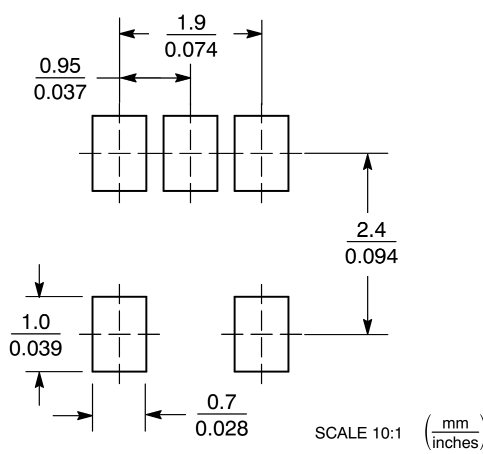
TSOP−5
CASE 483−02
ISSUE G



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

	MILLIMETERS	
DIM	MIN	MAX
A	3.00 BSC	
B	1.50 BSC	
C	0.90	1.10
D	0.25	0.50
G	0.95 BSC	
H	0.01	0.10
J	0.10	0.26
K	0.20	0.60
L	1.25	1.55
M	0 °	10 °
S	2.50	3.00

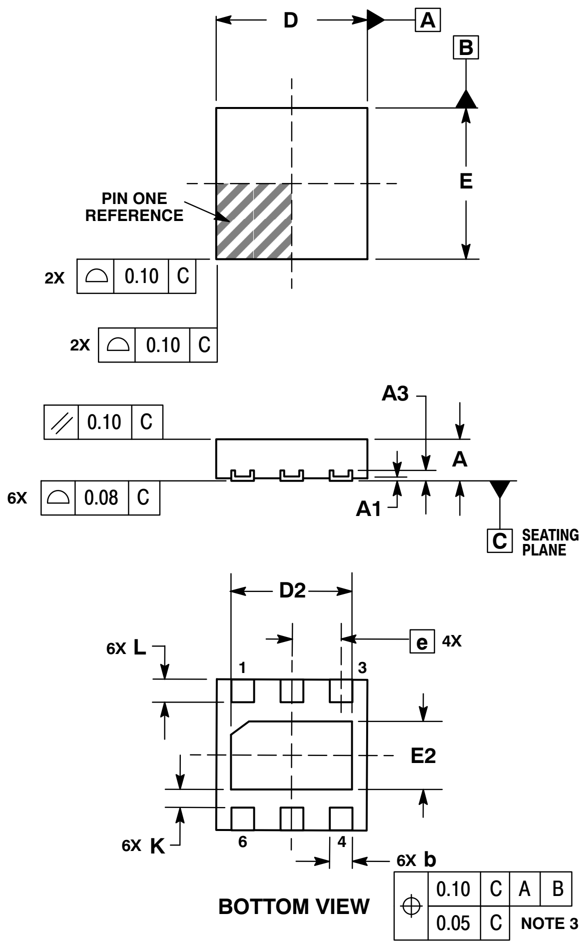
SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

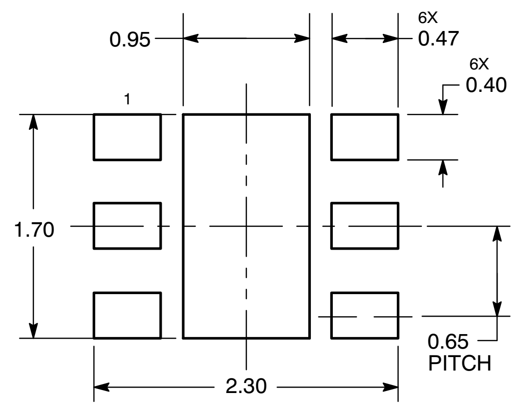
UDFN6 2x2, 0.65P
CASE 517AB−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.127 REF	
b	0.25	0.35
D	2.00 BSC	
D2	1.50	1.70
E	2.00 BSC	
E2	0.80	1.00
e	0.65 BSC	
K	0.20	---
L	0.25	0.35

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

The product described herein (NCP1529), may be covered by the following U.S. patents: TBD. There may be other patents pending.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5773−3850

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative