N-Channel Power MOSFET 0.65 Ω , 600 Volts

Features

- Low ON Resistance
- Low Gate Charge
- Zener Diode-protected Gate
- 100% Avalanche Tested
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Adapter (Notebook, Printer, Gaming)
- LCD Panel Power
- ATX Power Supplies
- Lighting Ballasts

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^{\circ}C$ unless otherwise noted)

Rating	Symbol	NDF10N60Z	NDP10N60Z	Unit
Drain-to-Source Voltage	V_{DSS}	600		V
Continuous Drain Current,	I _D	10 (Note 2)		Α
Continuous Drain Current $T_A = 100^{\circ}C, R_{\theta JC}$	I _D	5.7 (Note 2)		Α
Pulsed Drain Current, V _{GS} @ 10 V	I _{DM}	36 (Note 2)		Α
Power Dissipation, $R_{\theta JC}$ (Note 1)	P _D	36	125	W
Gate-to-Source Voltage	V _{GS}	±30		٧
Single Pulse Avalanche Energy, L = 6.0 mH, I _D = 10 A	E _{AS}	300		mJ
ESD (HBM) (JESD22-A114)	V _{esd}	3900		٧
RMS Isolation Voltage (t = 0.3 sec., R.H. \leq 30%, T _A = 25°C) (Figure 13)	V _{ISO}	4500		٧
Peak Diode Recovery	dv/dt	4.5 (Note 3)		V/ns
Continuous Source Current (Body Diode)	IS	10		Α
Maximum Temperature for Soldering Leads, 0.063" (1.6 mm) from Case for 10 s Package Body for 10 s	T _L T _{PKG}	300 260		°C
Operating Junction and Storage Temperature Range	T _J , T _{stg}	–55 to 150		°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

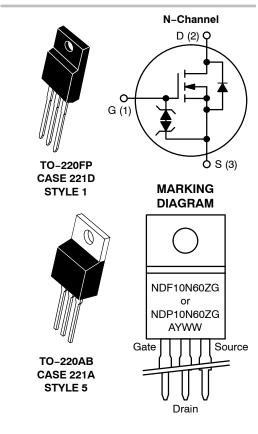
- 1. Surface mounted on FR4 board using 1" sq. pad size, 1 oz cu
- 2. Limited by maximum junction temperature
- 3. $I_S \le 10$ A, di/dt ≤ 200 A/ μs , $V_{DD} = 80\%$ BV $_{DSS}$



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V _{DSS}	R _{DS(ON)} (TYP) @ 5 A
600 V	0.65 Ω



A = Location Code
 Y = Year
 WW = Work Week
 G = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping
NDF10N60ZG	TO-220FP	50 Units/Rail
NDP10N60ZG	TO-220AB	In Development

THERMAL RESISTANCE

Parameter	Symbol	NDF10N60Z	NDP10N60Z	Unit
Junction-to-Case (Drain)	$R_{ heta JC}$	3.4	1.0	°C/W
Junction-to-Ambient Steady State (Note 4)	$R_{\theta JA}$	50	50	

Characteristic	Test Conditions		Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 1 \text{ mA}$	١	BV _{DSS}	600			V
Breakdown Voltage Temperature Coefficient	Reference to 25°C, $I_D = 1 \text{ mA}$		$\Delta BV_{DSS}/ \Delta T_{J}$		0.6		V/°C
Drain-to-Source Leakage Current		25°C	I _{DSS}			1	μΑ
	$V_{DS} = 600 \text{ V}, V_{GS} = 0 \text{ V}$	150°C				50	1
Gate-to-Source Forward Leakage	V _{GS} = ±20 V	1	I _{GSS}			±10	μΑ
ON CHARACTERISTICS (Note 5)							
Static Drain-to-Source On-Resistance	$V_{GS} = 10 \text{ V}, I_D = 5.0 \text{ A}$	A	R _{DS(on)}		0.65	0.75	Ω
Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 100 μ	ıA	V _{GS(th)}	3.0		4.5	V
Forward Transconductance	V _{DS} = 15 V, I _D = 10 A		9FS		7.9		S
YNAMIC CHARACTERISTICS							
Input Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1.0 MHz		C _{iss}		1425		pF
Output Capacitance			C _{oss}		150		
Reverse Transfer Capacitance			C _{rss}		35		
Total Gate Charge	V _{DD} = 300 V, I _D = 10 A, V _{GS} = 10 V		Qg		47		nC
Gate-to-Source Charge			Q _{gs}		9.0		1
Gate-to-Drain ("Miller") Charge	VGS = 10 V		Q _{gd}		26		
Gate Resistance			R_g		1.5		Ω
ESISTIVE SWITCHING CHARACTER	STICS				-		
Turn-On Delay Time			t _{d(on)}		15		ns
Rise Time	V _{DD} = 300 V, I _D = 10 /	V _{DD} = 300 V, I _D = 10 A.			31		
Turn-Off Delay Time	V_{GS} = 10 V, R_{G} = 5 Ω		t _{d(off)}		40		
Fall Time			t _f		23		
OURCE-DRAIN DIODE CHARACTER	ISTICS (T _C = 25°C unless oth	erwise not	ed)				
Diode Forward Voltage	I _S = 10 A, V _{GS} = 0 V	,	V_{SD}			1.6	V
Reverse Recovery Time	V _{GS} = 0 V, V _{DD} = 30 V I _S = 10 A, di/dt = 100 A/μs		t _{rr}		395		ns
Reverse Recovery Charge			Q _{rr}		3.0		μС

Insertion mounted
 Pulse Width ≤ 380 μs, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

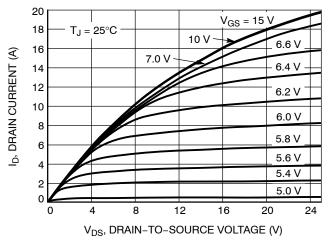


Figure 1. On-Region Characteristics

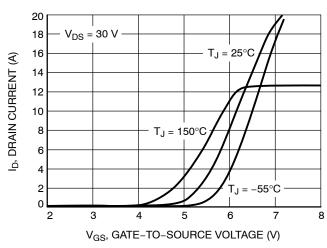


Figure 2. Transfer Characteristics

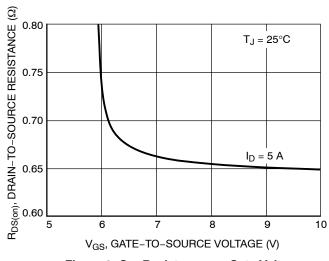


Figure 3. On-Resistance vs. Gate Voltage

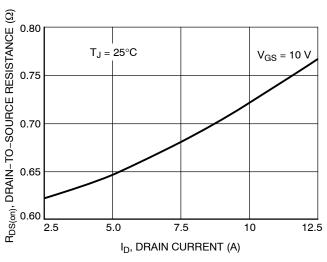


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

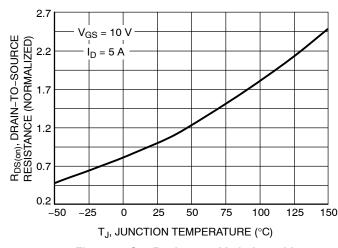


Figure 5. On–Resistance Variation with Temperature

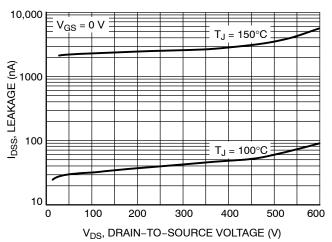


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

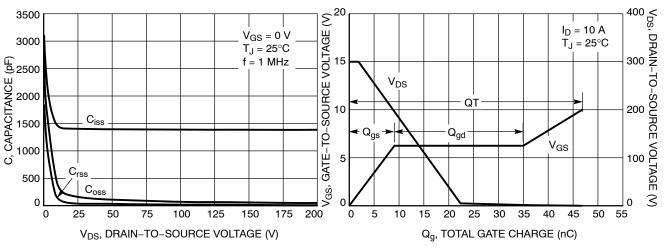


Figure 7. Capacitance Variation

Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

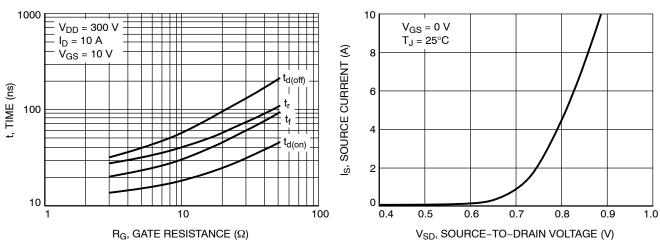


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

Figure 10. Diode Source Current vs. Forward Voltage

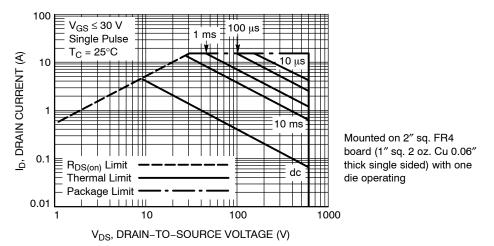


Figure 11. Maximum Rated Forward Biased Safe Operating Area for NDF10N60Z

TYPICAL CHARACTERISTICS

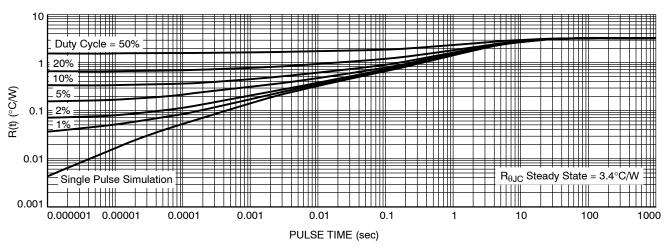


Figure 12. Thermal Impedance for NDF10N60Z

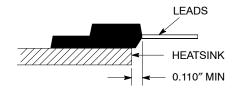
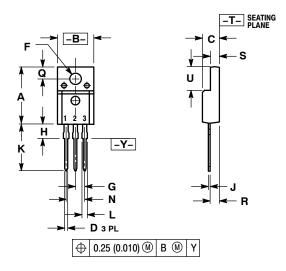


Figure 13. Mounting Position for Isolation Test

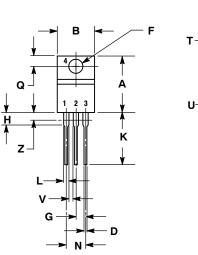
Measurement made between leads and heatsink with all leads shorted together.

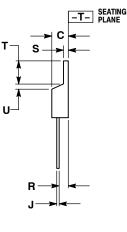
PACKAGE DIMENSIONS

TO-220FP CASE 221D-03 ISSUE K



TO-220AB CASE 221A-09 **ISSUE AE**





- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
 - CONTROLLING DIMENSION: INCH
- 221D-01 THRU 221D-02 OBSOLETE, NEW STANDARD 221D-03.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
Α	0.617	0.635	15.67	16.12
В	0.392	0.419	9.96	10.63
С	0.177	0.193	4.50	4.90
D	0.024	0.039	0.60	1.00
F	0.116	0.129	2.95	3.28
G	0.100	0.100 BSC		BSC
Н	0.118	0.135	3.00	3.43
J	0.018	0.025	0.45	0.63
K	0.503	0.541	12.78	13.73
L	0.048	0.058	1.23	1.47
N	0.200	BSC	5.08 BSC	
Q	0.122	0.138	3.10	3.50
R	0.099	0.117	2.51	2.96
S	0.092	0.113	2.34	2.87
U	0.239	0.271	6.06	6.88

PIN 1. GATE 2. DRAIN

SOURCE

NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI
- Y14.5M, 1982. CONTROLLING DIMENSION: INCH.
- DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
Α	0.570	0.620	14.48	15.75
В	0.380	0.405	9.66	10.28
С	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.161	3.61	4.09
G	0.095	0.105	2.42	2.66
Н	0.110	0.155	2.80	3.93
J	0.014	0.025	0.36	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
٧	0.045		1.15	
Z		0.080		2.04

STYLE 5:

GATE PIN 1.

DRAIN

3. SOURCE DRAIN

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