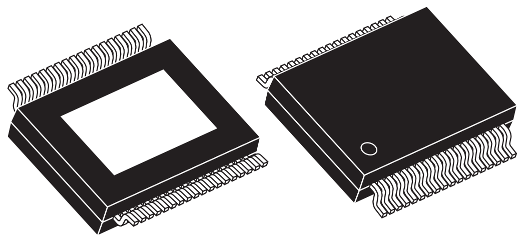
TDA7491P

10 W + 10 W dual BTL class-D audio amplifier

Features

- 10 W + 10 W continuous output power: R_L = 6 Ω, THD = 10% at V_{CC} = 11 V
- 9.5 W + 9.5 W continuous output power: R_L = 8 Ω, THD = 10% at V_{CC} = 12 V
- Wide range single supply operation (5 V - 18 V)
- High efficiency (η= 90%)
- Four selectable, fixed gain settings of nominally 20 dB, 26 dB, 30 dB and 32 dB
- Differential inputs minimize common-mode noise
- Filterless operation
- No ‘pop’ at turn-on/off
- Standby and mute features
- Short-circuit protection
- Thermal overload protection
- Externally synchronizable



PowerSSO-36 with exposed pad (or slug) down

Description

The TDA7491P is a dual BTL class-D audio amplifier with single power supply designed for LCD TVs and monitors.

Thanks to the high efficiency and a slug-down package, no heatsink is required.

Furthermore, the filterless operation allows a reduction in the external component count.

The TDA7491P is pin-to-pin compatible with the TDA7491LP and TDA7491HV.

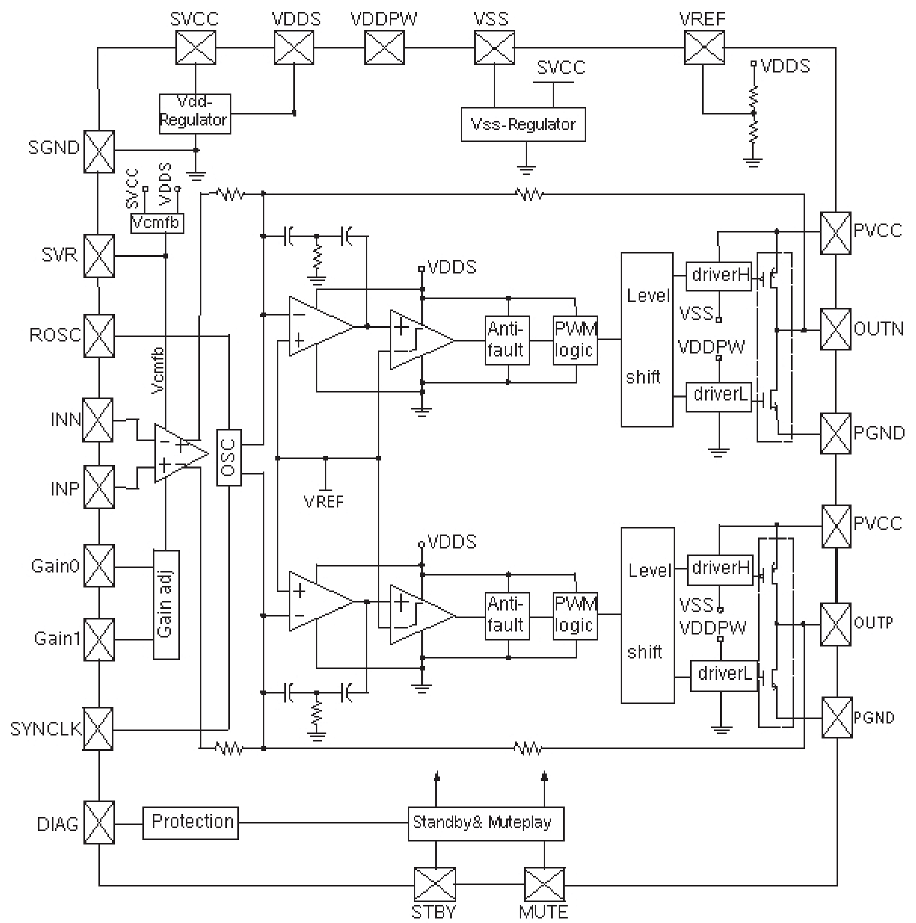
Table 1. Device summary

Order code	Operating Temp. range	Package	Packing
TDA7491P	0° to 70° C	PowerSSO-36 (slug down)	Tube
TDA7491P13TR	0° to 70° C	PowerSSO-36 (slug down)	Tape and reel

1 Device block diagram

Figure 1 shows the block diagram of one of the two identical channels of the TDA7491P.

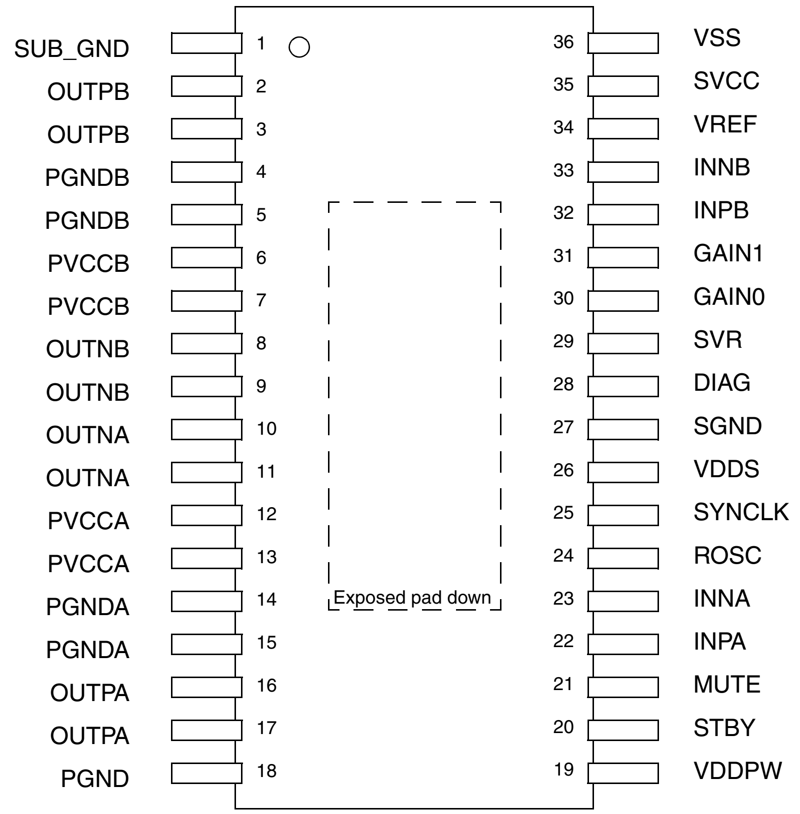
Figure 1. Internal block diagram (one channel only)



2 Pin description

2.1 Pin out

Figure 2. Pin connection (top view, PCB view)



2.2 Pin list

Table 1. Pin description list

Number	Name	Type	Description
1	SUB_GND	POWER	Connect to the frame
2,3	OUTPB	OUT	Positive PWM for right channel
4,5	PGNDB	POWER	Power stage round for right channel
6,7	PVCCB	POWER	Power supply for right channel
8,9	OUTNB	OUT	Negative PWM output for right channel
10,11	OUTNA	OUT	Negative PWM output for right channel
12,13	PVCCA	POWER	Power supply for left channel
14,15	PGNDA	POWER	Power stage round for left channel
16,17	OUTPA	OUT	Positive PWM output for left channel
18	PGND	POWER	Power stage round
19	VDDPW	OUT	3.3 V (nominal) regulator output referred to ground for power stage
20	STBY	INPUT	Standby mode control
21	MUTE	INPUT	Mute mode control
22	INPA	INPUT	Positive differential input of left channel
23	INNA	INPUT	Negative differential input of left channel
24	ROSC	OUT	Master oscillator frequency-setting pin
25	SYNCLCK	IN/OUT	Clock in/out for external oscillator
26	VDDS	OUT	3.3 V (nominal) regulator output referred to ground for signal blocks
27	SGND	POWER	Signal round
28	DIAG	OUT	Open-drain diagnostic output
29	SVR	OUT	Supply voltage rejection
30	GAIN0	INPUT	Gain setting input 1
31	GAIN1	INPUT	Gain setting input 2
32	INPB	INPUT	Positive differential input of right channel
33	INNB	INPUT	Negative differential input of right channel
34	VREF	OUT	Half VDDS (nominal) referred to ground
35	SVCC	POWER	Signal power supply
36	VSS	OUT	3.3 V (nominal) regulator output referred to power supply

3 Electrical specifications

3.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
VCC	DC supply voltage for pins PVCCA, PVCCB, SVCC	20	V
T_{op}	Operating temperature	0 to 70	°C
T_j	Junction temperature	–40 to 150	°C
T_{stg}	Storage temperature	–40 to 150	°C

3.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Min	Typ	Max	Unit
$R_{th\ j\text{-}case}$	Thermal resistance, junction to case		2	3	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance, junction to ambient (mounted on recommended PCB)(1)		24		

1. FR4 with vias to copper area of 9 cm² (see also *Section 7.9: Heatsink requirements on page 41*).

3.3 Electrical specifications

Unless otherwise stated, the results in *Table 4* below are given for the conditions: VCC = 11 V, R_L (load) = 6 Ω, R_{OSC} = 39 kΩ, C1 = 100 nF, f = 1 kHz, G_V = 20 dB, and Tamb = 25 °C.

Table 4. Electrical specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VCC	Supply voltage for pins PVCCA, PVCCB, SVCC		5		18	V
I_q	Total quiescent			26	35	mA
I_{qSTBY}	Quiescent current in standby			2.5	5.0	µA
V_{OS}	Output offset voltage	Play mode	-150		150	mV
V_{OS}	Output offset voltage	Mute mode	-60		60	mV
I_{OC}	Over current protection threshold	R_L = 0 Ω	3	5		A
T_j	Junction temperature at thermal shut-down			150		°C
R_i	Input resistance	Differential input	55	60		kΩ
V_{OV}	Over voltage protection threshold		19	21		

Table 4. Electrical specifications (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_{dsON}	Power transistor on resistance	High side		0.2		Ω
		Low side		0.2		
P_o	Output power	THD = 10%		10		W
		THD = 1%		8		
P_o	Output power	R_L = 8 Ω, THD = 10% Vcc= 12V		9.5		W
		R_L = 8 Ω, THD = 1% VCC = 12 V		7.2		
P_D	Dissipated power	P_o = 10 W + 10 W, THD = 10%		2.0		W
η	Efficiency	P_o = 10 W + 10 W	80	90		%
THD	Total harmonic distortion	P_o = 1 W		0.1	0.4	%
G_V	Closed loop gain	GAIN0 = L, GAIN1 = L	18	20	22	dB
		GAIN0 = L, GAIN1 = H	24	26	28	
		GAIN0 = H, GAIN1 = L	28	30	32	
		GAIN0 = H, GAIN1 = H	30	32	34	
ΔG_V	Gain matching		–1		1	dB
CT	Cross talk	f = 1 kHz		50		dB
eN	Total input noise	A Curve, G_V = 20 dB		20		µV
		f = 22 Hz to 22 kHz		25	35	
SVRR	Supply voltage rejection ratio	fr = 100 Hz, Vr = 0.5 V, C_{SVR} = 10 µF	40	50		dB
T_r, T_f	Rise and fall times			50		ns
f_{SW}	Switching frequency	Internal oscillator	290	310	330	kHz
f_{SWR}	Output switching frequency	With internal oscillator (1)	250			kHz
		With external oscillator (2)	250			
V_{inH}	Digital input high (H)		2.3			V
V_{inL}	Digital input low (L)				0.8	
Function mode	Standby, mute and play modes	STBY < 0.5 V, MUTE = X	Standby			
		STBY > 2.5 V, MUTE < 1 V	Mute			
		STBY > 2.5 V, MUTE > 2 V	Play			
A_{MUTE}	Mute attenuation	VMute = 1 V	60	80		dB

1. $f_{SW} = 10^6 / (64 * R_{OSC} + 440)$ kHz, $f_{SYNCLK} = 2 * f_{SW}$ with R1 = 3 kΩ (see *Figure 49*.)
2. $f_{SW} = f_{SYNCLK} / 2$ with the frequency of the external oscillator.

4 Characterization curves

The following characterization curves were made using the TDA7491P demo board. The LC filter for the 4 Ω load used 15 µH and 470 nF components, whilst that for the 6 Ω load used 22 µH and 220 nF and that for the 8 Ω load used 33 µH and 220 nF.

All other test conditions are given along side the corresponding curves.

4.1 With 4 Ω load at Vs = 10 V

Figure 3. THD vs output power (1 kHz)

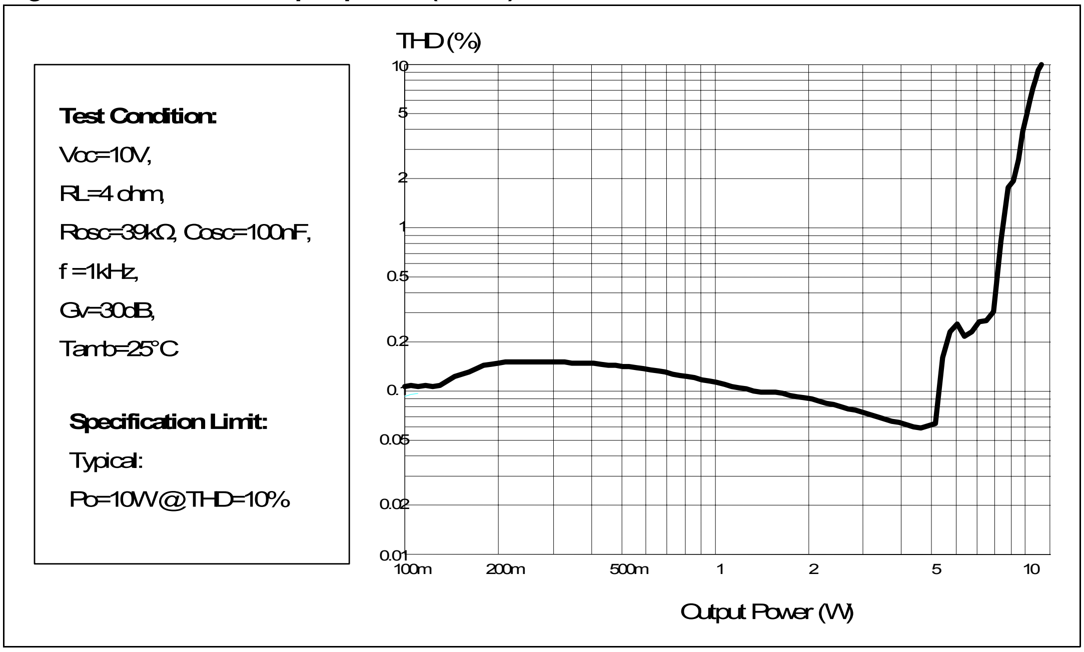


Figure 4. THD vs output power (100 Hz)

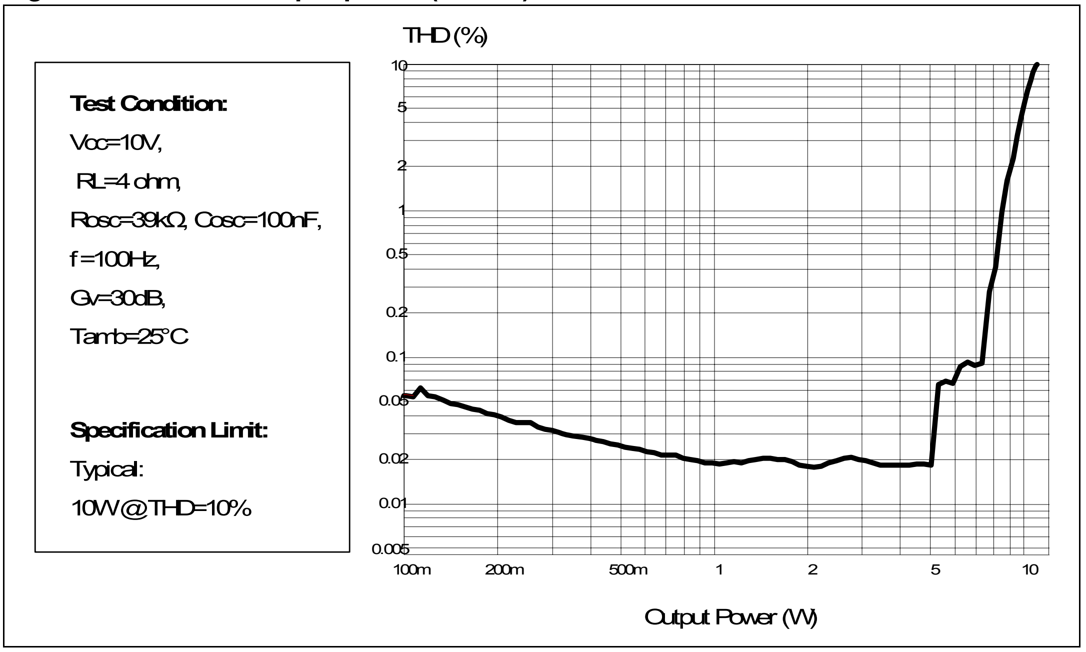


Figure 5. THD vs frequency

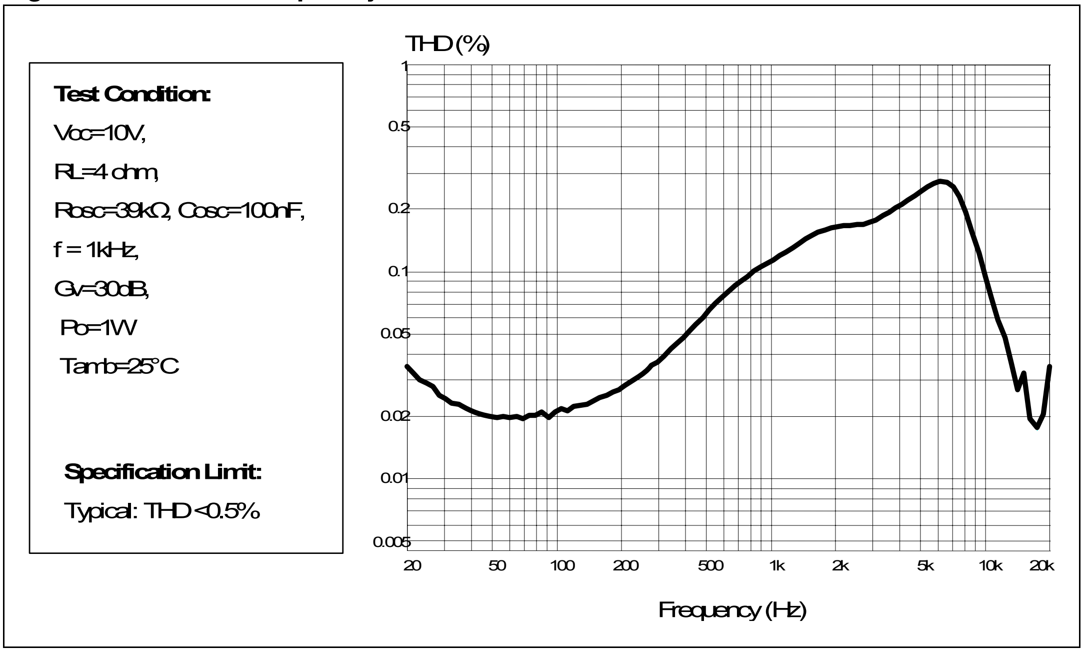


Figure 6. Frequency response

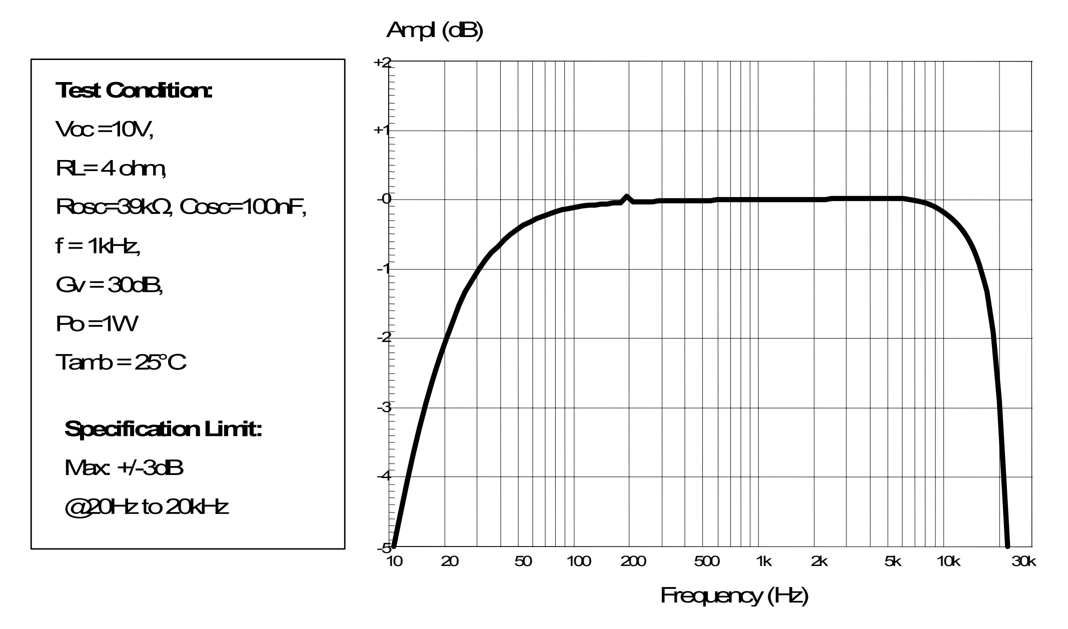


Figure 7. Crosstalk vs frequency

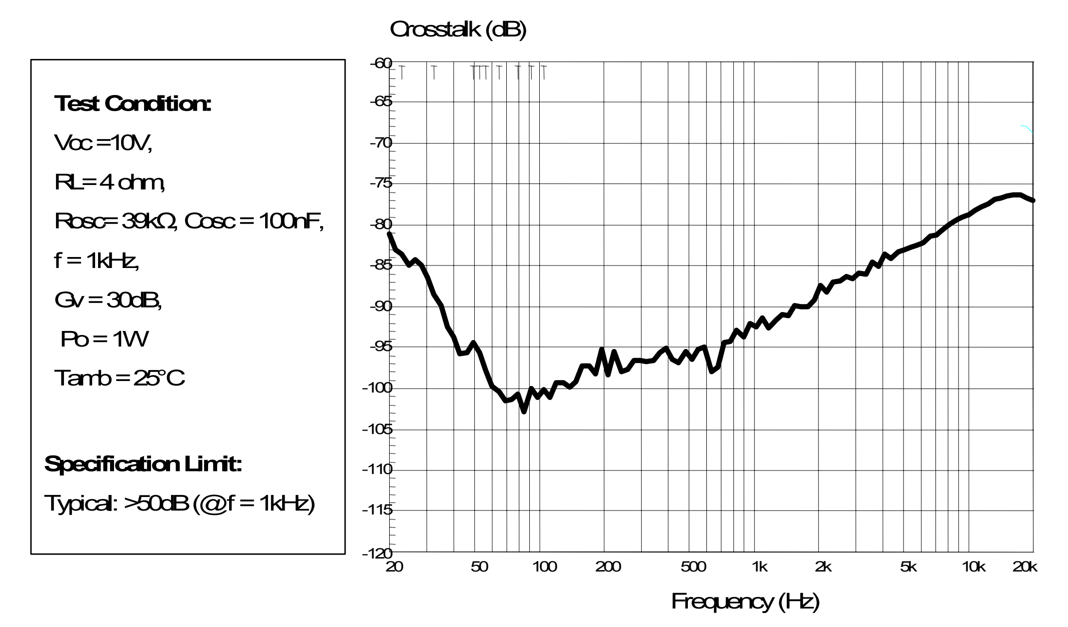


Figure 8. FFT (0 dB)

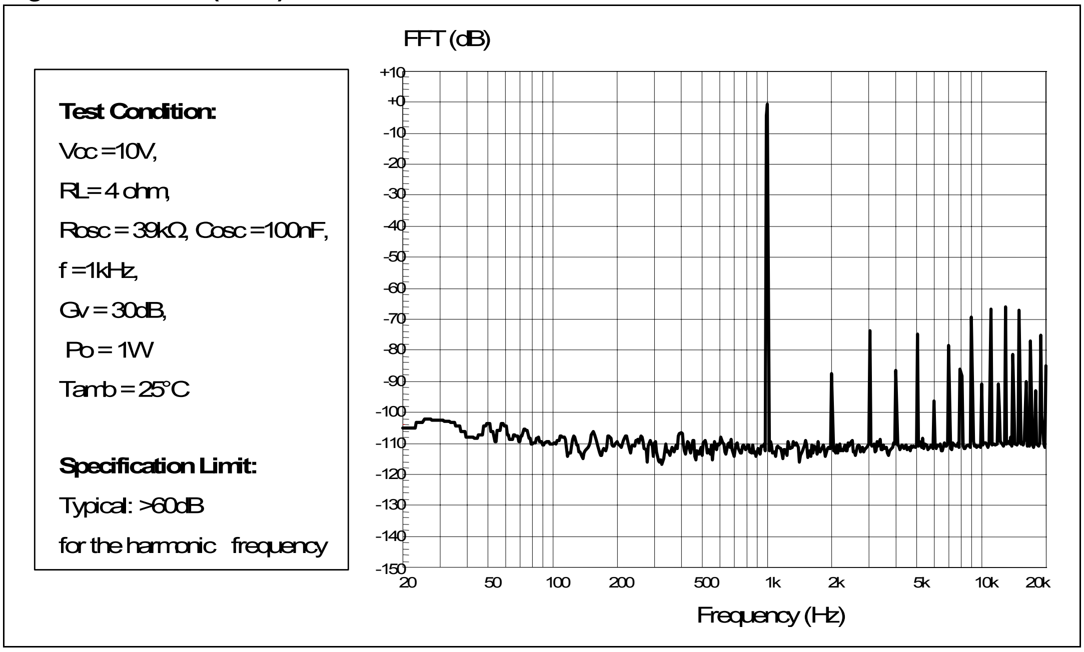


Figure 9. FFT (-60 dB)

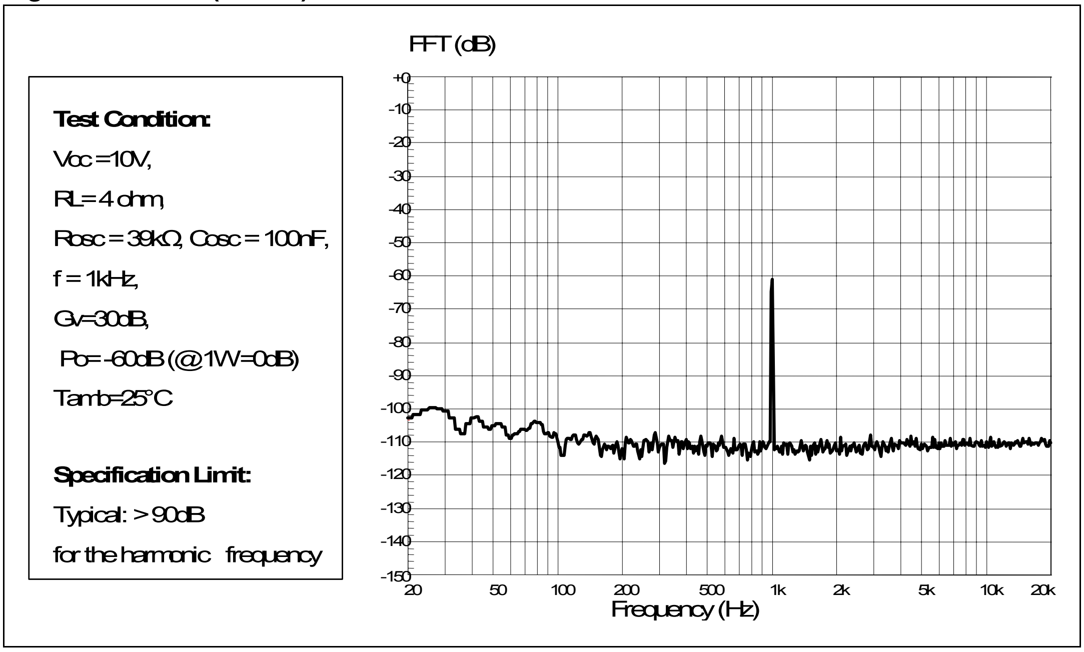


Figure 10. Power supply rejection ratio vs frequency

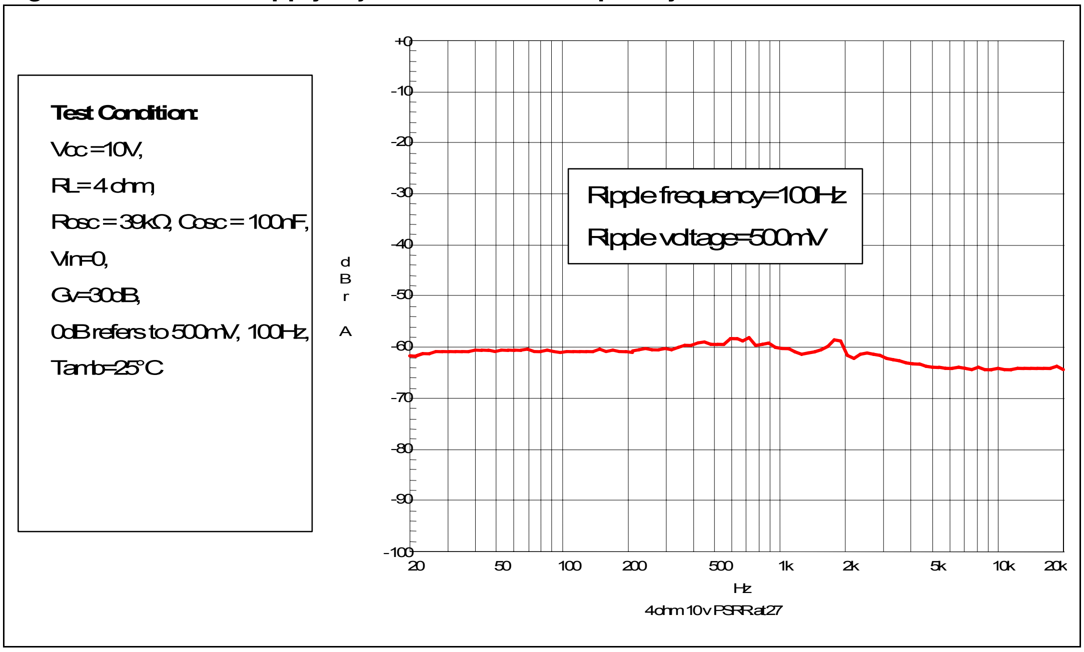


Figure 11. Power dissipation and efficiency vs output power

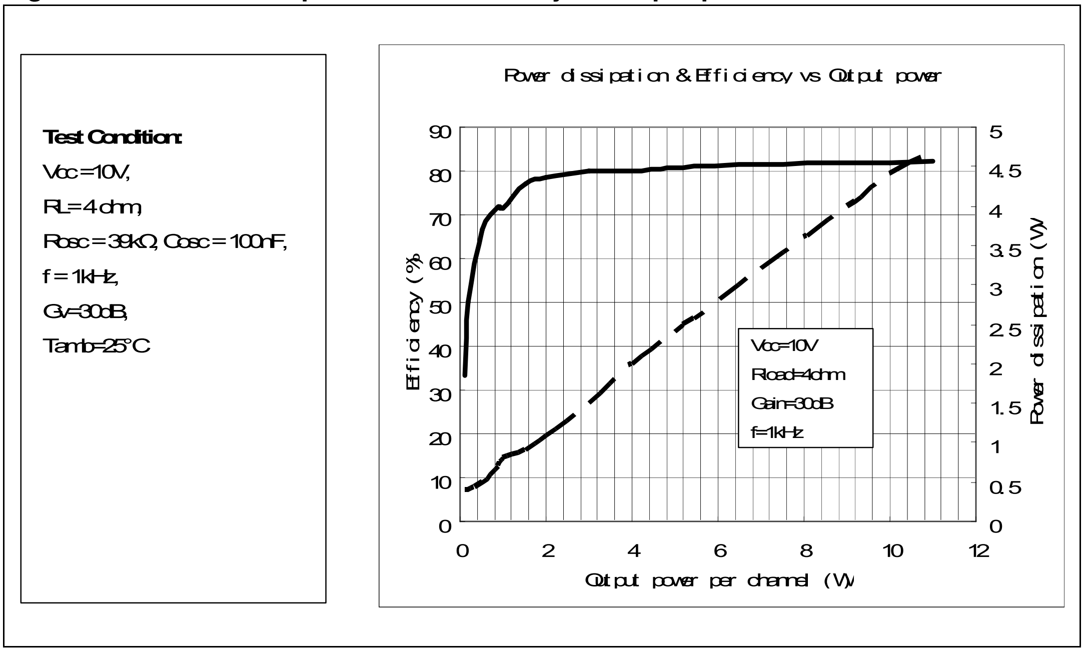


Figure 12. Closed-loop gain vs frequency

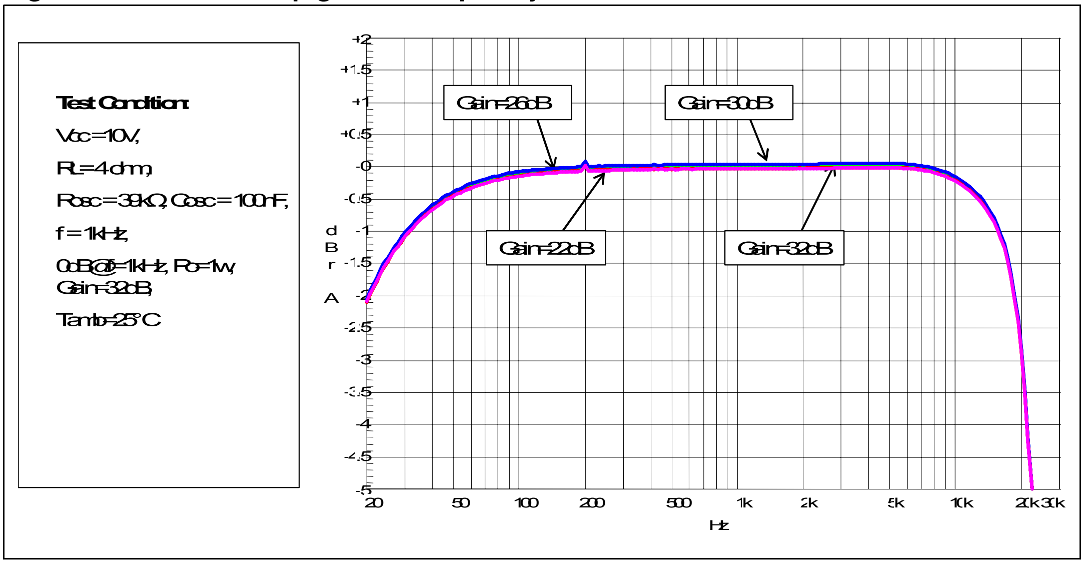


Figure 13. Current consumption vs voltage on pin MUTE

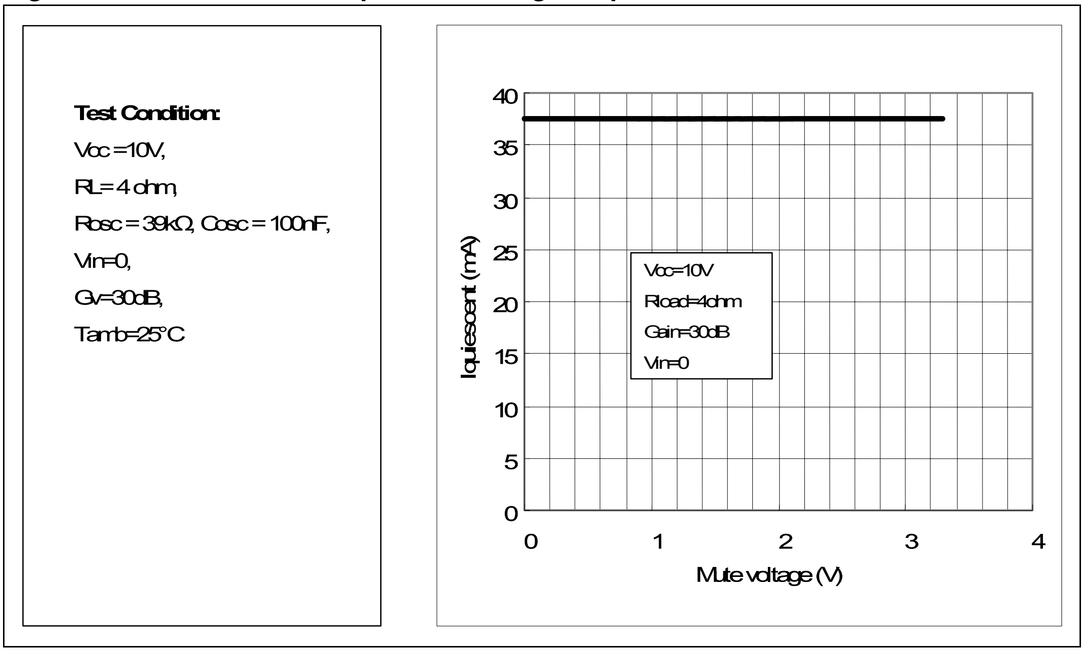


Figure 14. Attenuation vs voltage on pin MUTE

Test Condition:
Vcc=10V,
RL=4 ohm,
Rosc=39kΩ, Cosc=100nF,
0dB@f=1kHz,Po=1w,
Gv=30dB,
Tamb=25°C

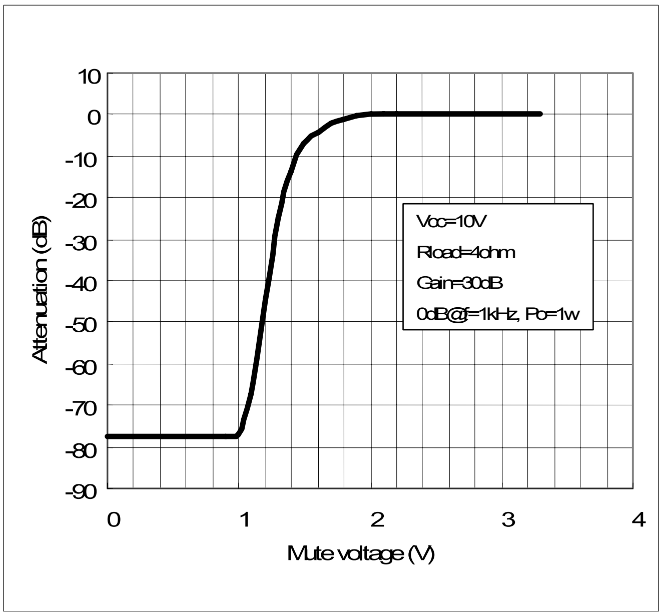


Figure 15. Current consumption vs voltage on pin STBY

Test Condition:
Vcc=10V,
RL=4ohm,
Rosc=39kΩ, Cosc=100nF,
Vin=0,
Gv=30dB,
Tamb=25°C

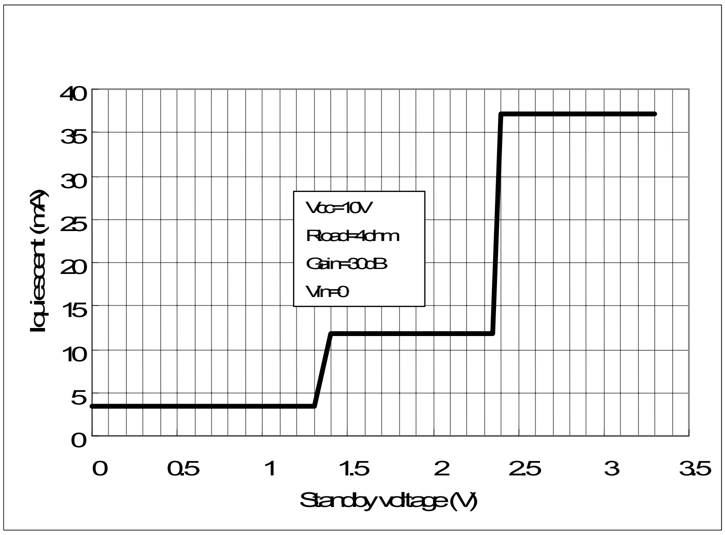
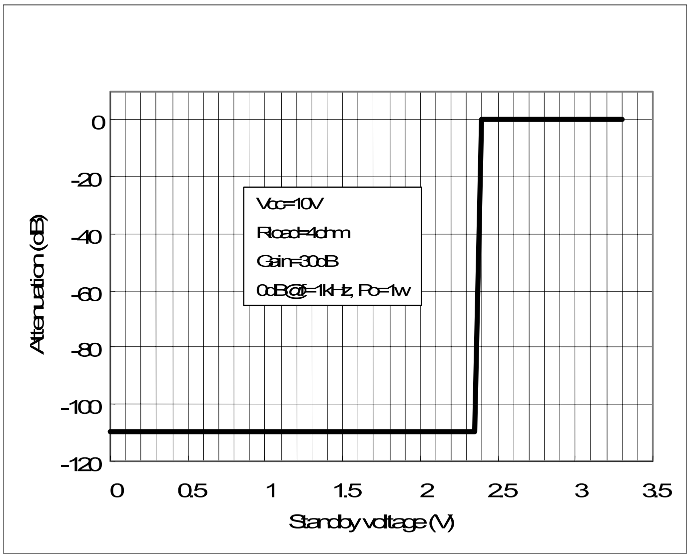


Figure 16. Attenuation vs voltage on pin STBY

Test Condition:
Vcc=10V,
RL=4 ohm,
Rosc=39kΩ, Cosc=100nF,
0dB@f=1kHz,Po=1w,
Gv=30dB,
Tamb=25°C



4.2 With 6 Ω load at Vs = 11 V

Figure 17. Output power vs supply voltage

Test Condition :
Vcc=5~11V,
RL=6 ohm,
Rosc=39kΩ, Cosc=100nF,
f =1kHz,
Gv=30dB,
Tamb=25°C

Specification Limit:
Typical:
Vs=11V,Rl =6 ohm
Po=10W@THD=10%
Po=8W@THD=1%

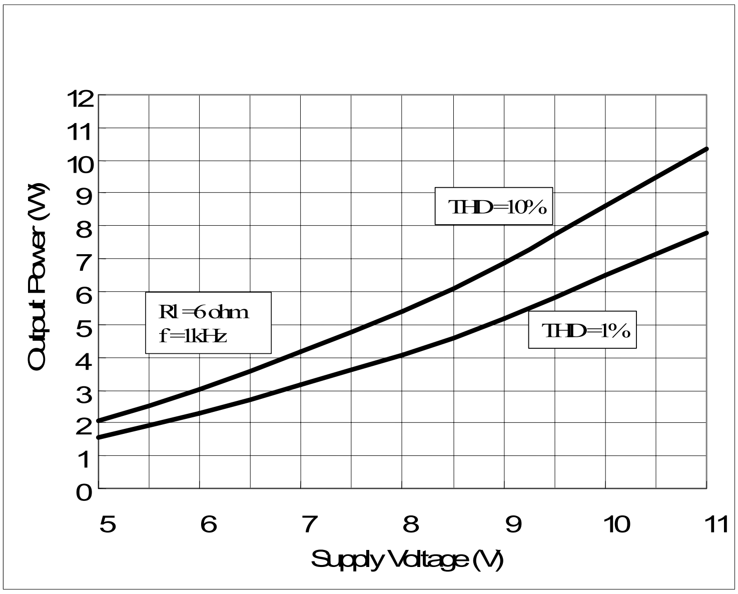


Figure 18. THD vs output power (1 kHz)

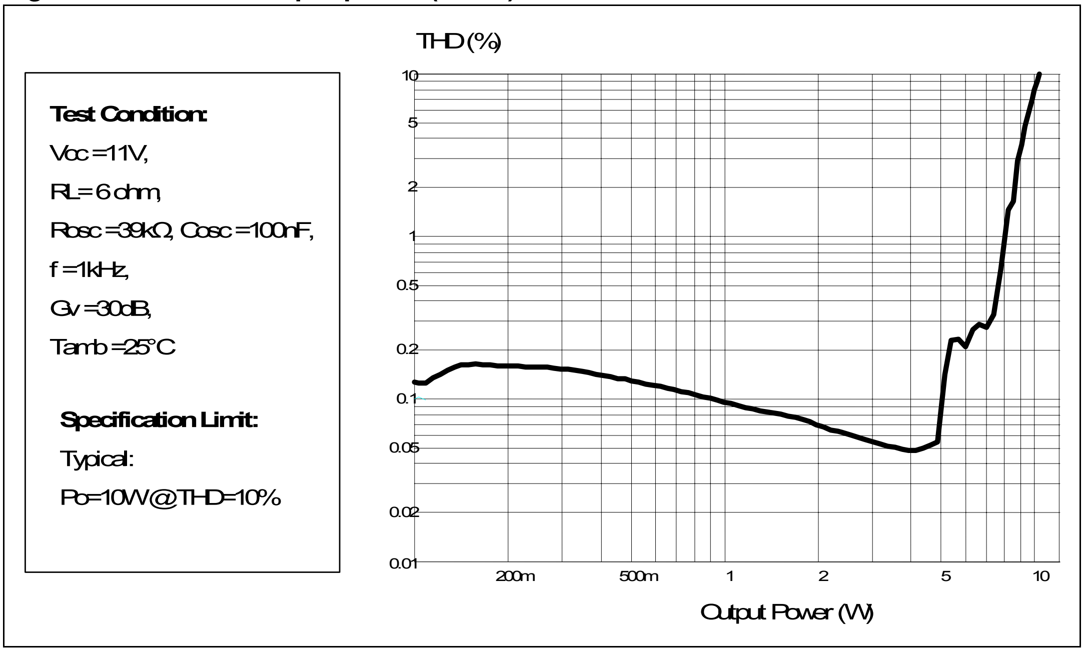


Figure 19. THD vs output power (100 Hz)

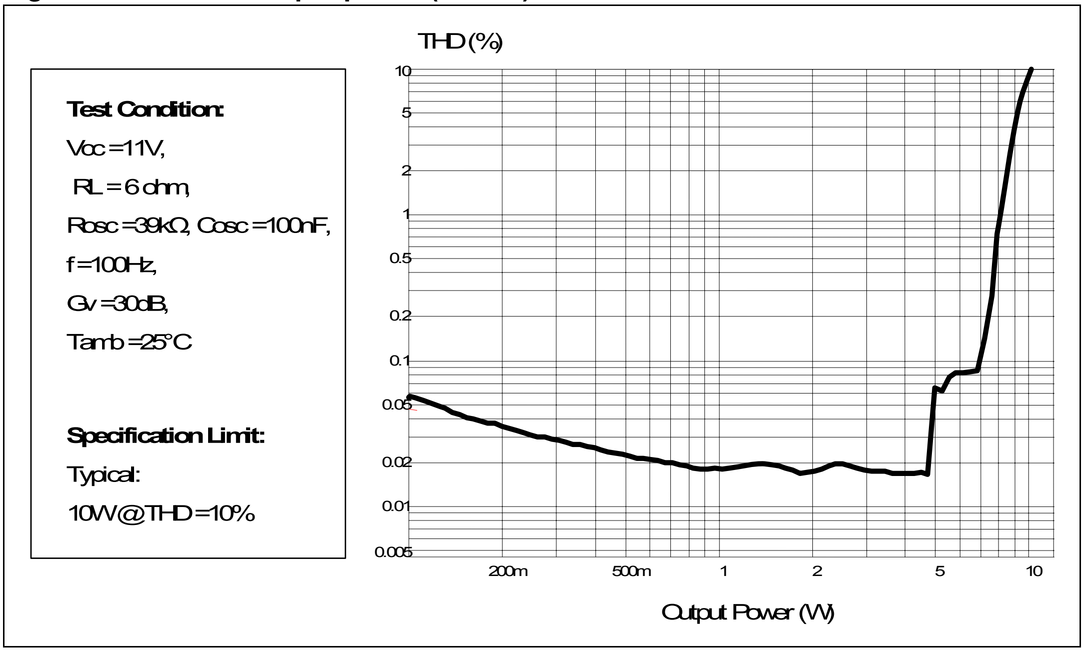


Figure 20. THD vs frequency

Test Condition:
Vcc=11V,
RL=6 ohm,
Rosc=39kΩ, Cosc=100nF,
f=1kHz,
Gv=30dB,
Po=1W
Tamb=25°C

Specification Limit:
Typical: THD<0.5%

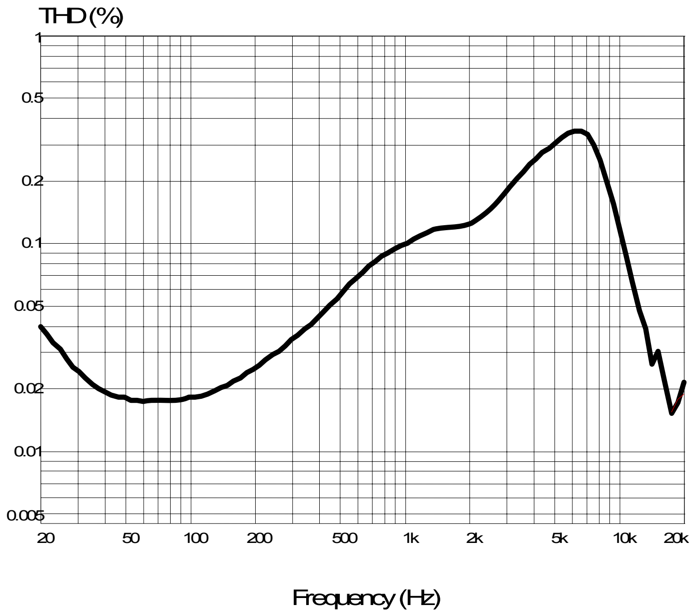


Figure 21. Frequency response

Test Condition:
Vcc=11V,
RL=6 ohm,
Rosc=39kΩ, Cosc=100nF,
f=1kHz,
Gv=30dB,
Po=1W
Tamb=25°C

Specification Limit:
Max: +/-3dB
@20Hz to 20kHz

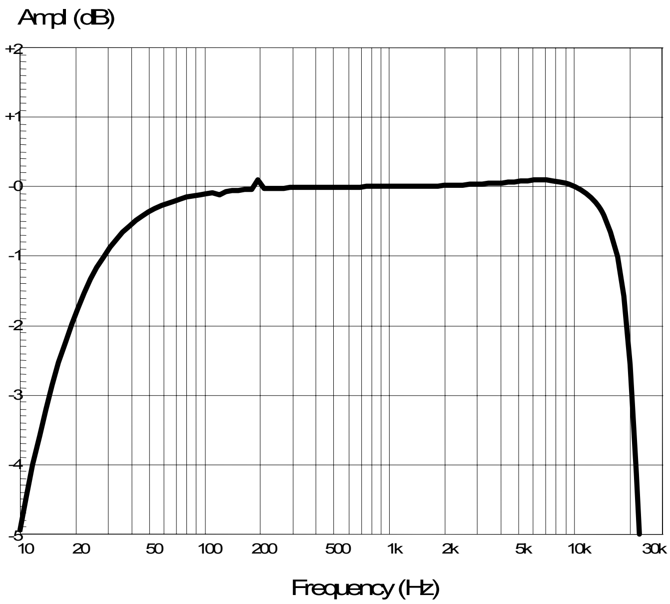


Figure 22. Crosstalk vs frequency

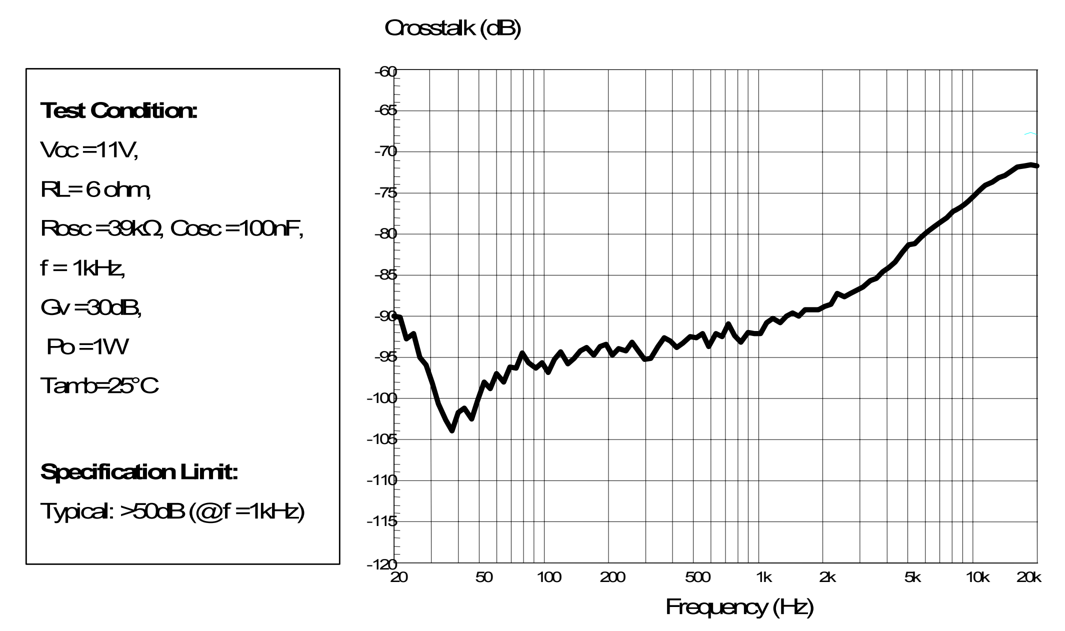


Figure 23. FFT (0 dB)

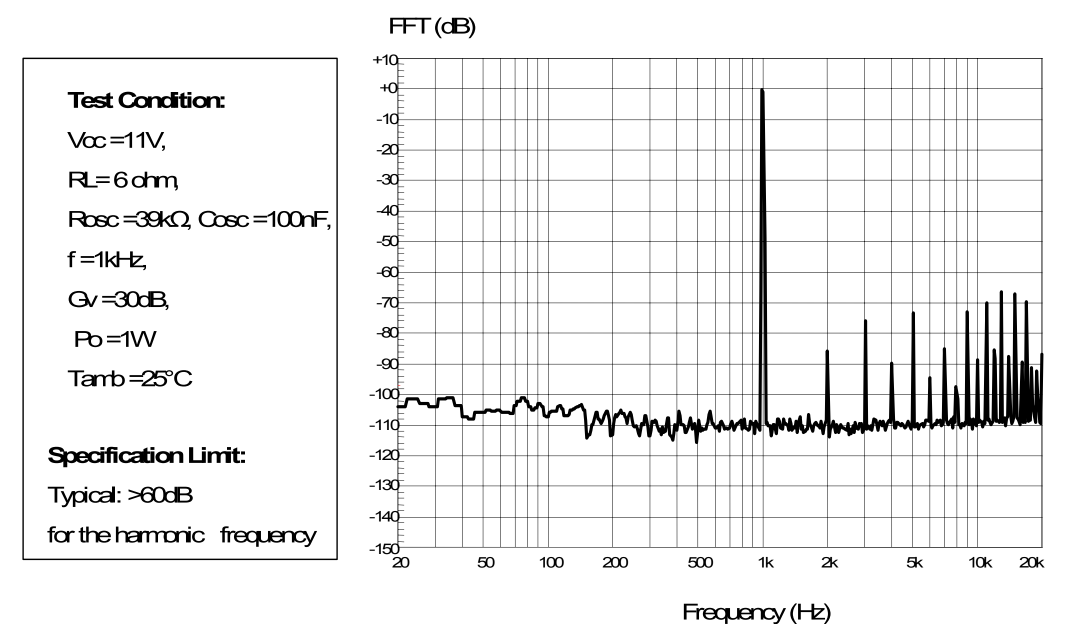


Figure 24. FFT (-60 dB)

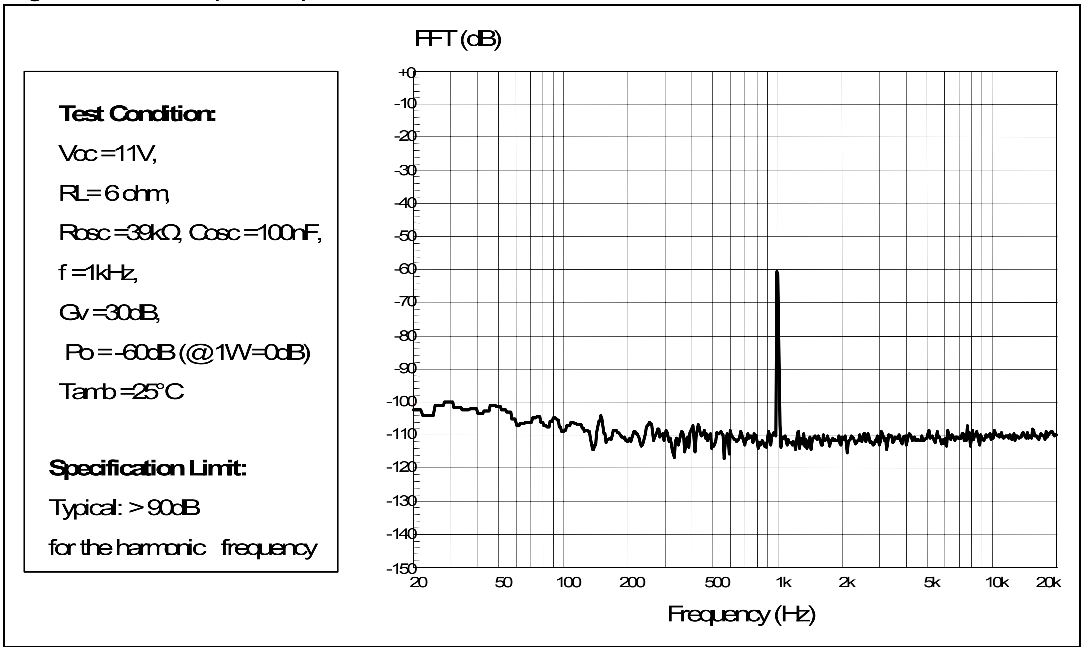


Figure 25. Power supply rejection ratio vs frequency

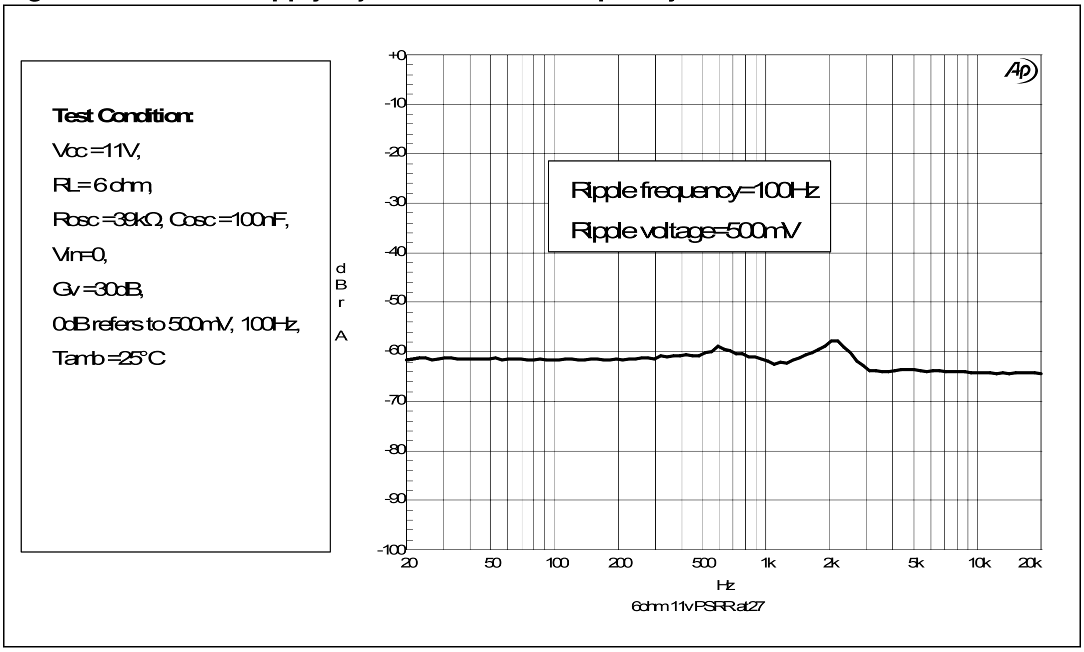


Figure 26. Power dissipation and efficiency vs output power

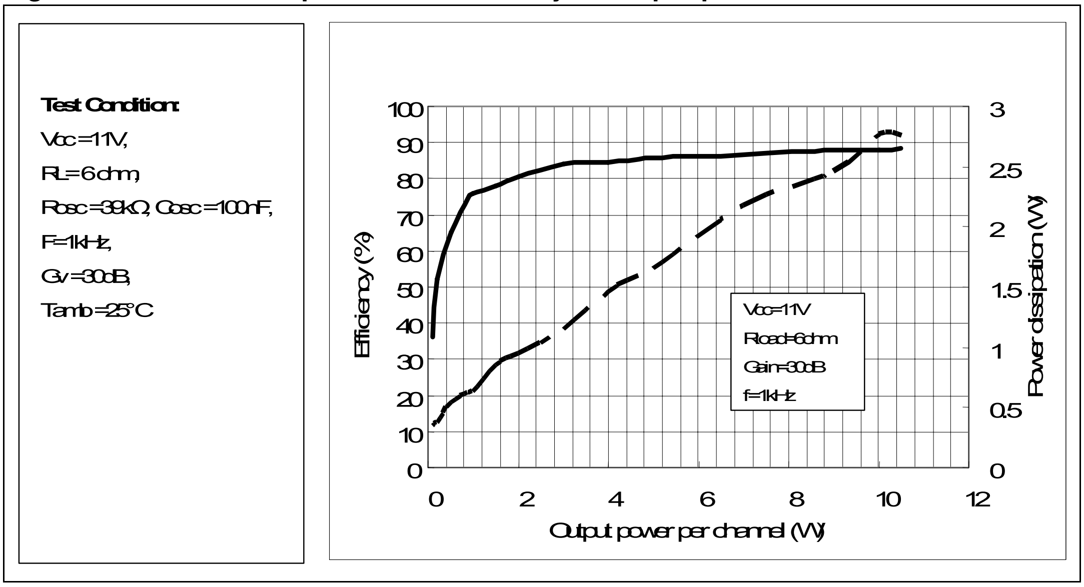


Figure 27. Closed-loop gain vs frequency

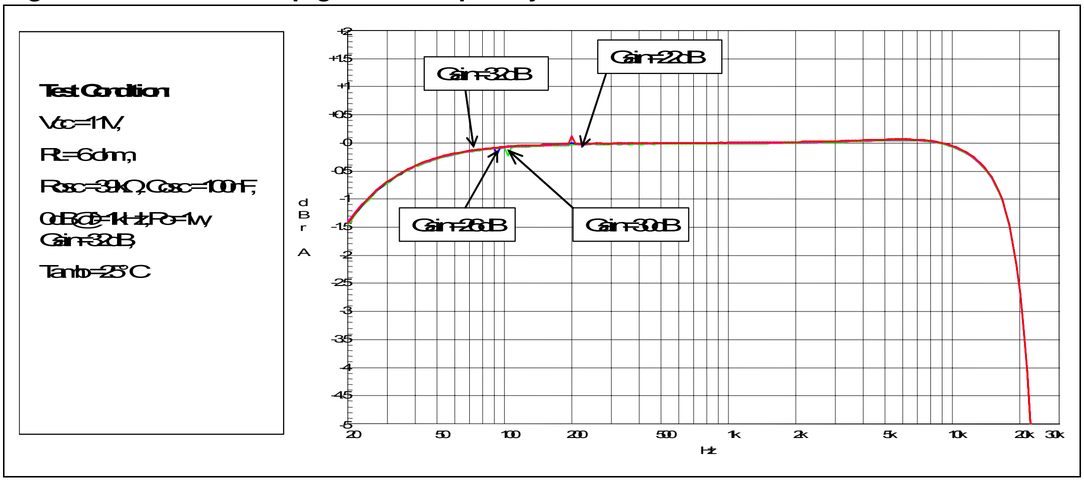


Figure 28. Current consumption vs voltage on pin MUTE

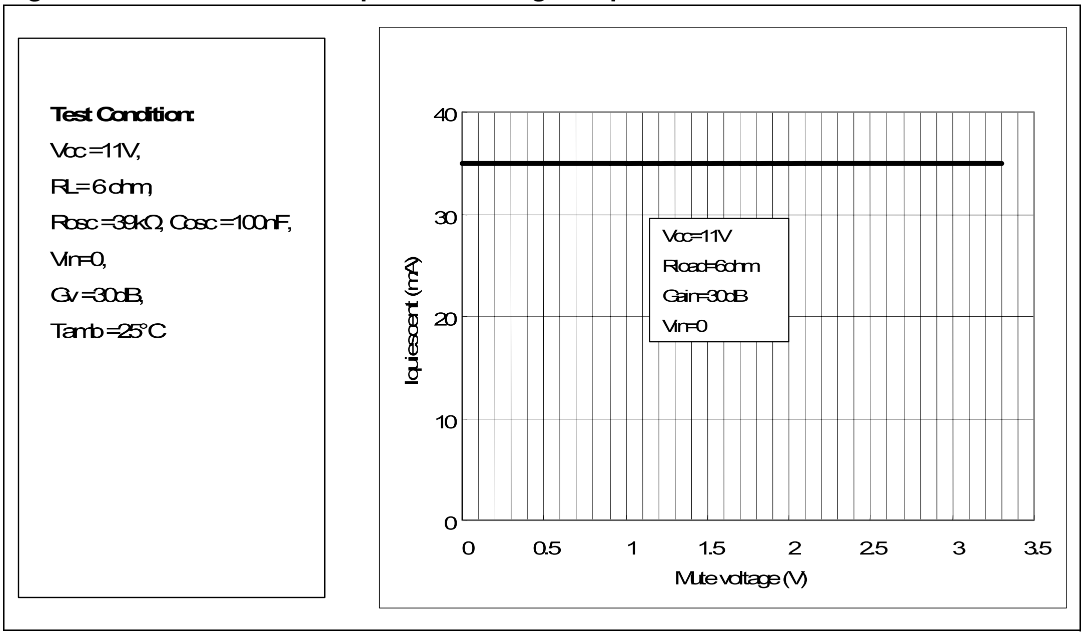


Figure 29. Attenuation vs voltage on pin MUTE

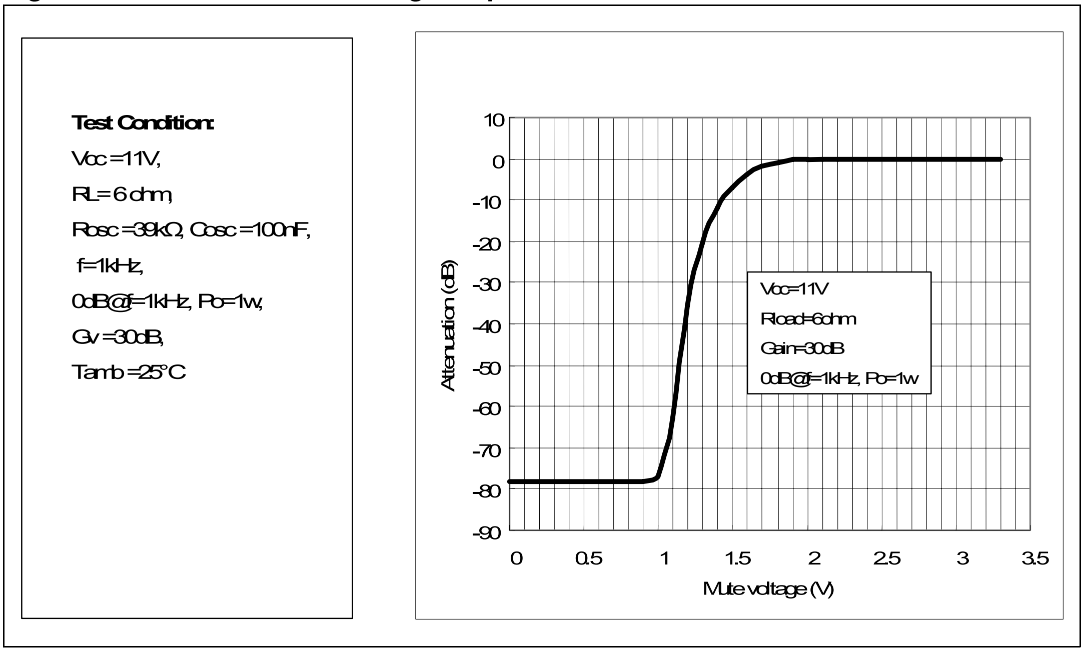


Figure 30. Current consumption vs voltage on pin STBY

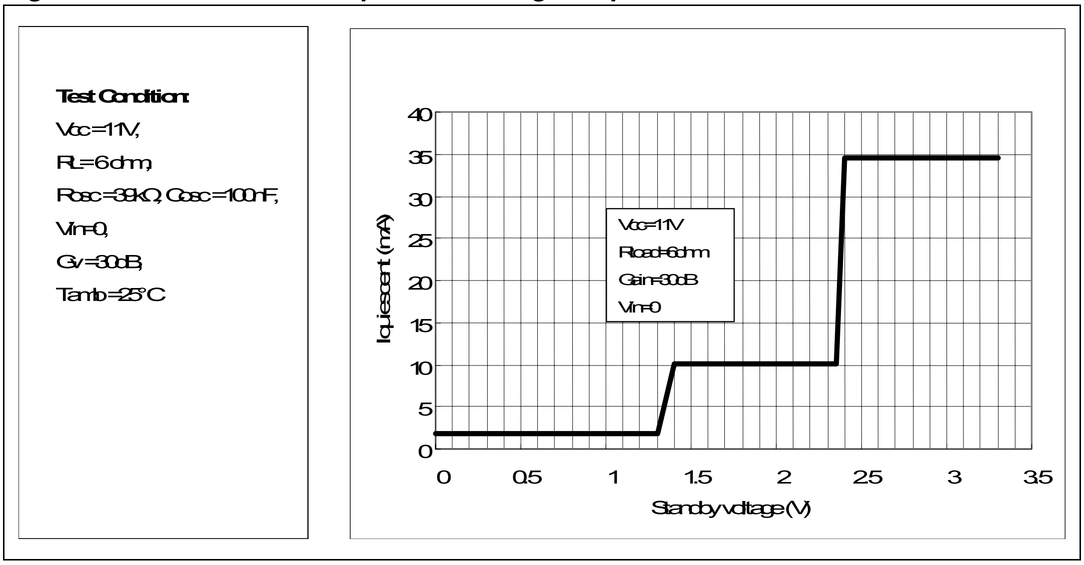
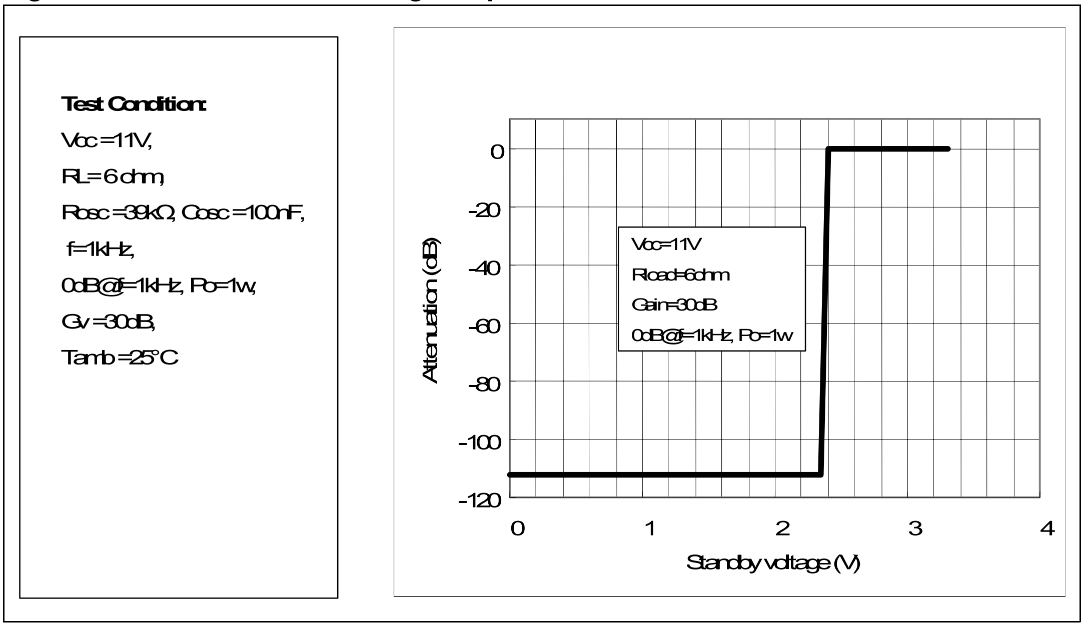


Figure 31. Attenuation vs voltage on pin STBY



4.3 With 8 Ω load at Vs = 12V

Figure 32. Output power vs supply voltage

Test Condition:
Vcc=5~12V,
RL=8ohm,
Rosc=39kΩ, Cosc=100nF,
f=1kHz,
Gv=30dB,
Tamb=25°C

Specification Limit:
Typical:
Vs=12V,Rl=8ohm
Po=9.5W@THD=10%
Po=7.2W@THD=1%

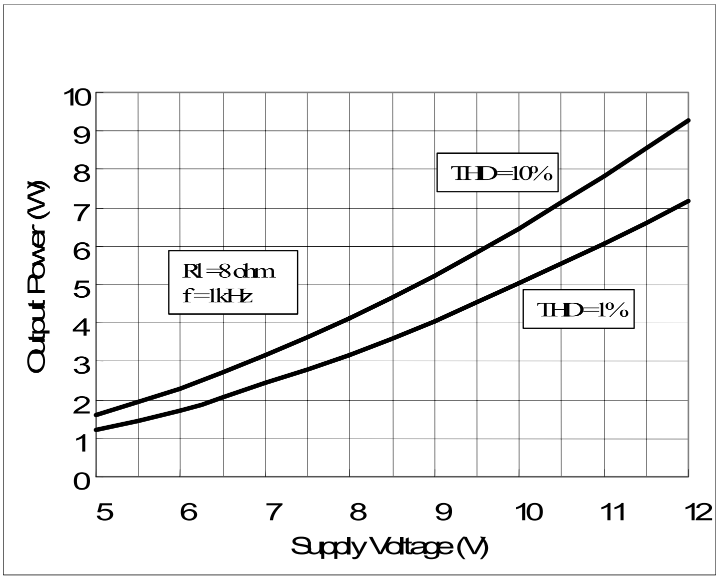


Figure 33. THD vs output power (1 kHz)

Test Condition:
Vcc=12V,
RL=8ohm,
Rosc=39kΩ, Cosc=100nF,
f=1kHz,
Gv=30dB,
Tamb=25°C

Specification Limit:
Typical:
Po=9.5W@THD=10%

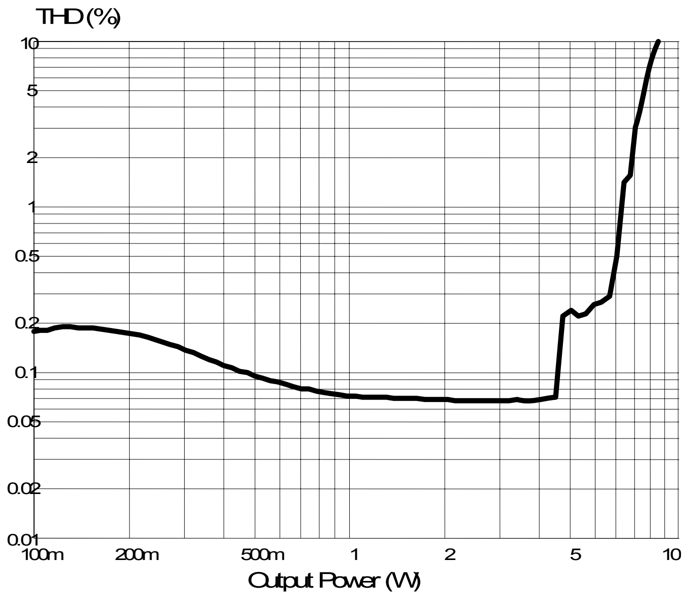


Figure 34. THD vs output power (100 Hz)

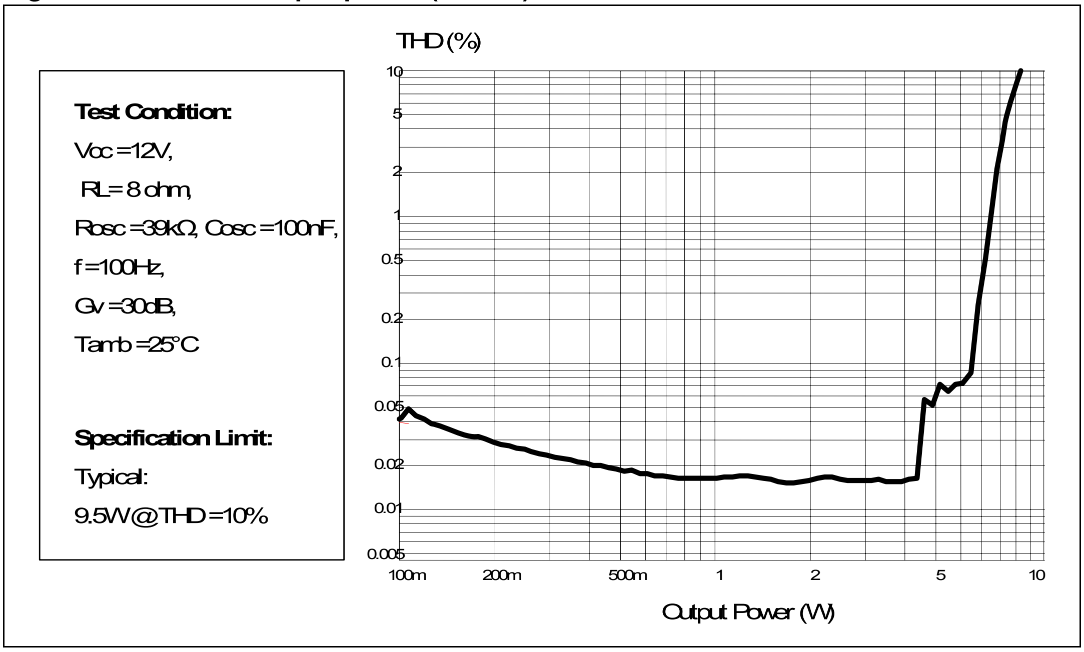


Figure 35. THD vs frequency

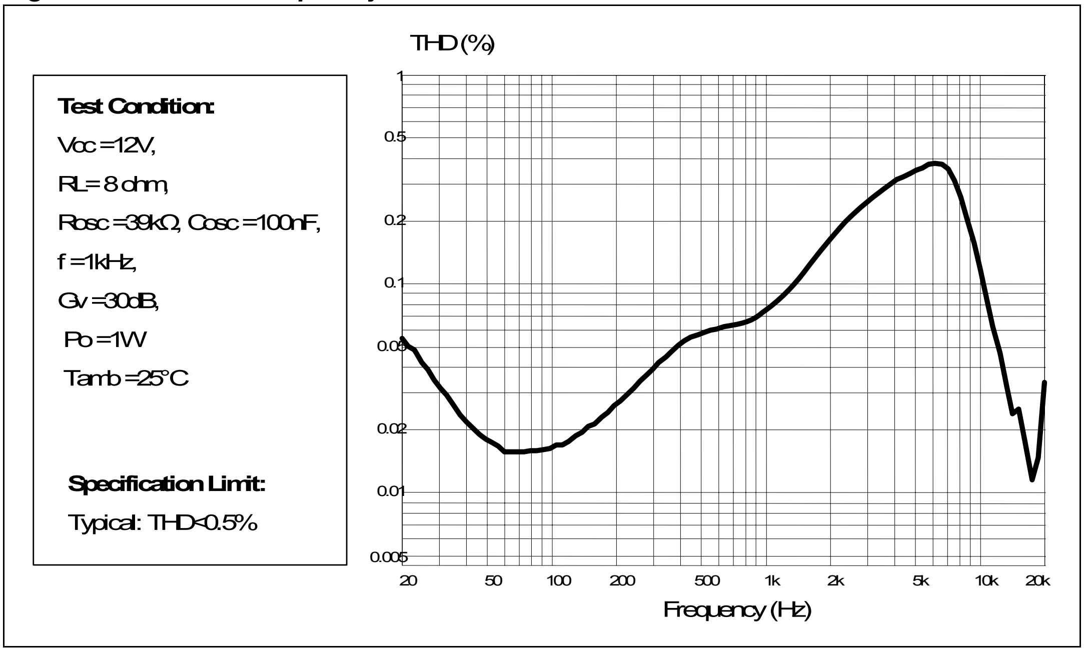


Figure 36. Frequency response

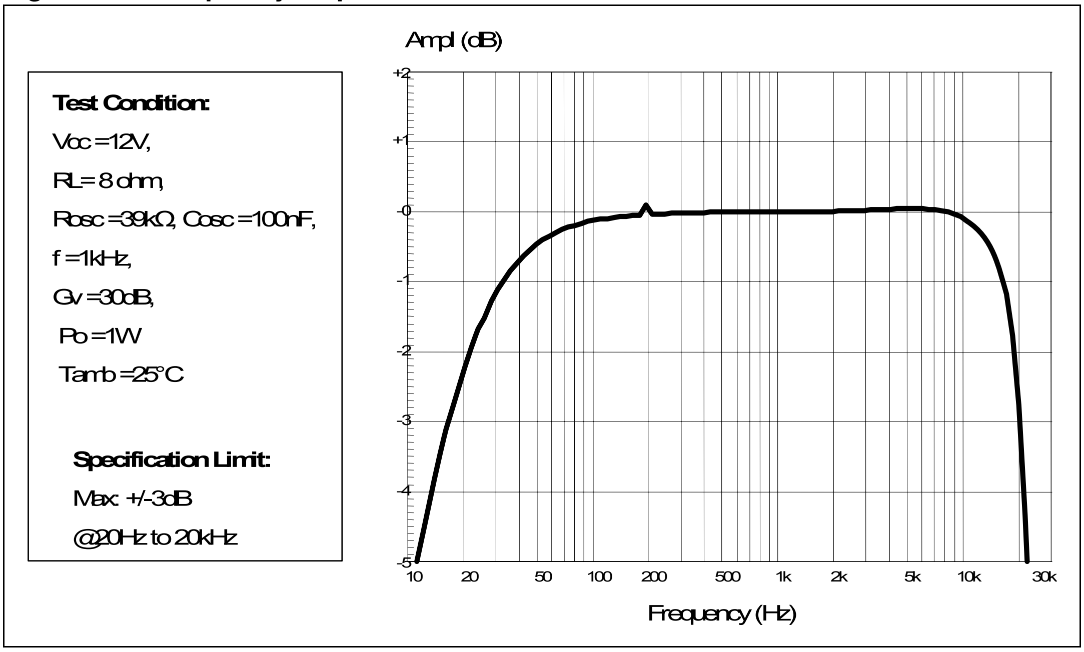


Figure 37. Crosstalk vs frequency

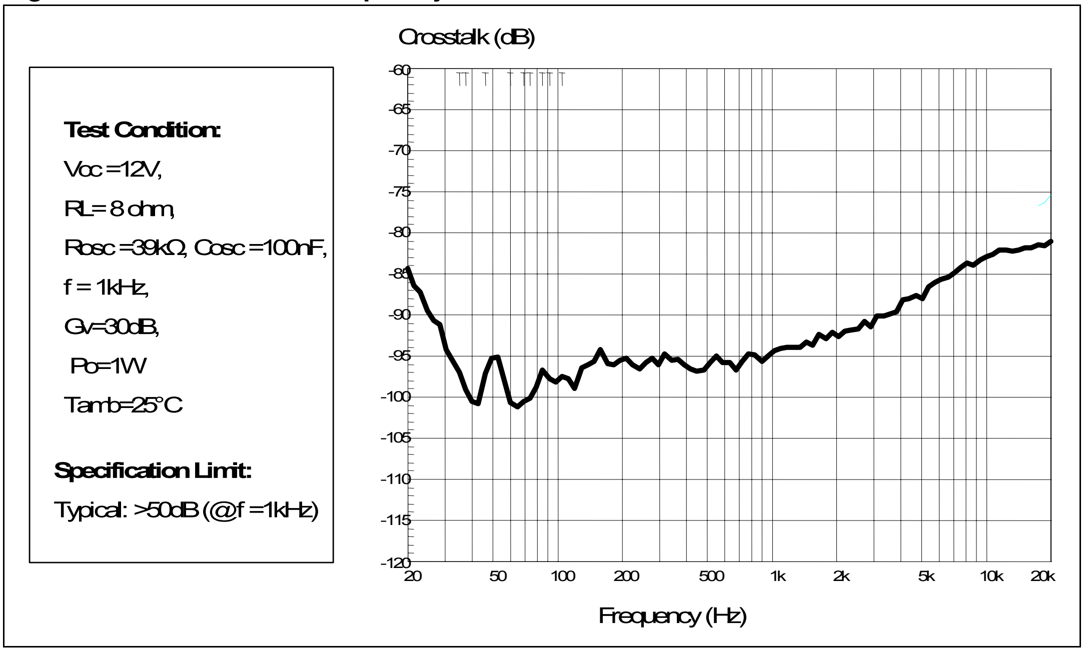


Figure 38. FFT (0 dB)

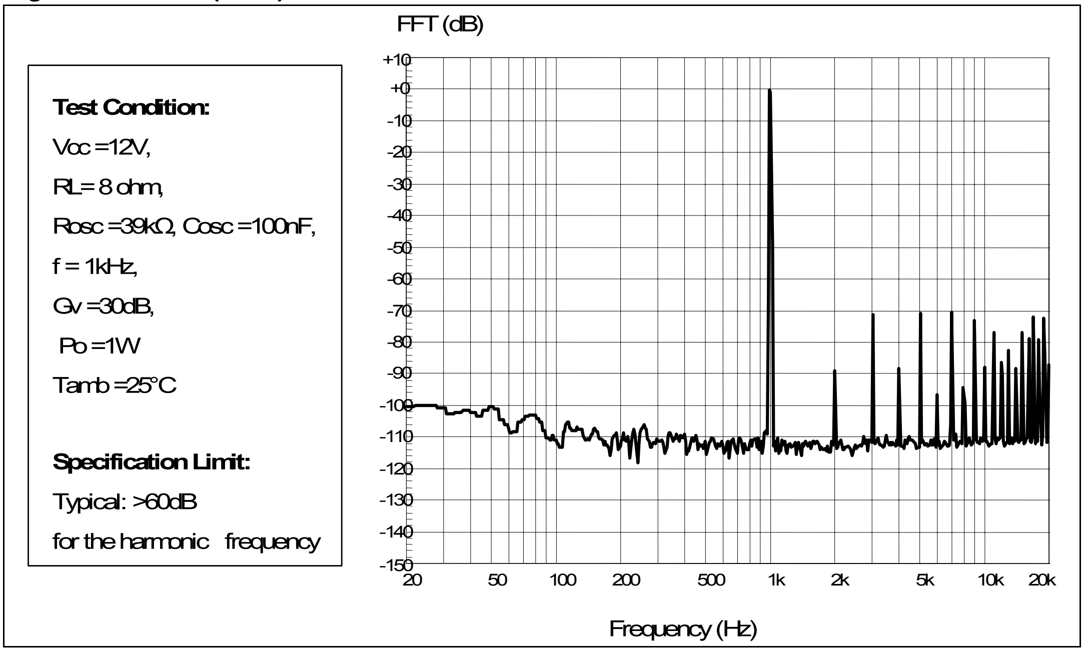


Figure 39. FFT (-60 dB)

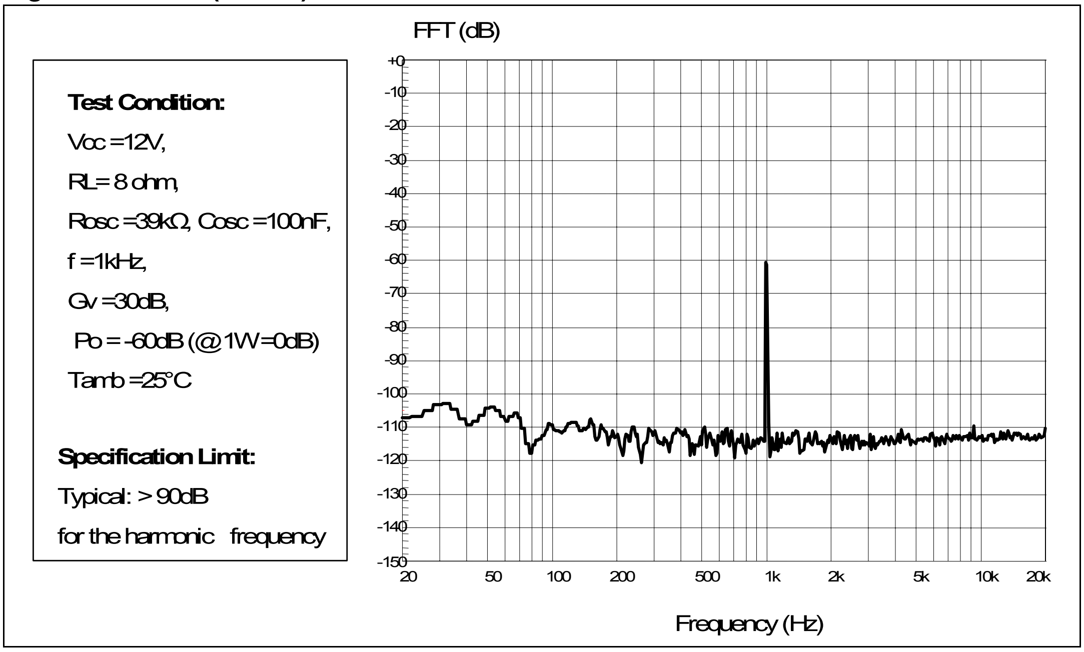


Figure 40. Power supply rejection ratio vs frequency

Test Condition:
Vcc=12V,
RL=8ohm,
Rosc=39kΩ, Cosc=100nF,
f=1kHz,
Gv=30dB,
0dB refers to 500mV, 100Hz,
Tamb=25°C

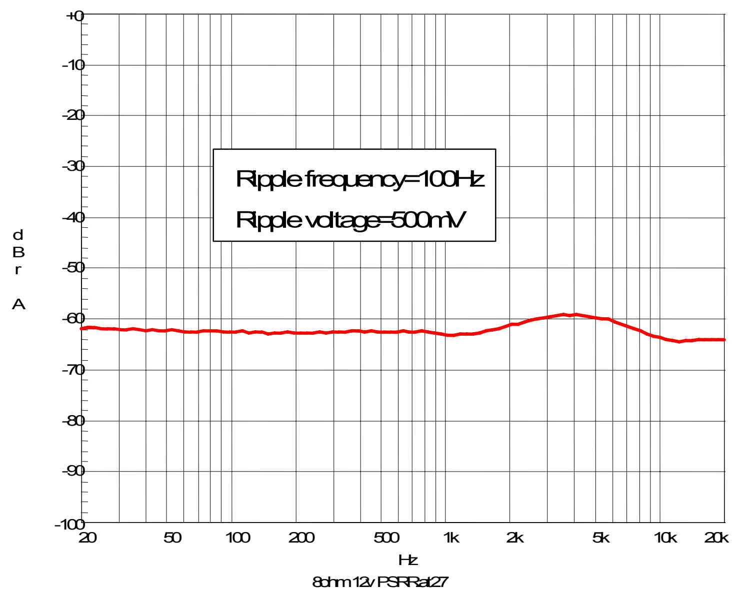


Figure 41. Power dissipation and efficiency vs output power

Test Condition:
Vcc=12V,
RL=8ohm,
Rosc=39kΩ, Cosc=100nF,
f=1kHz,
Gv=30dB,
Tamb=25°C

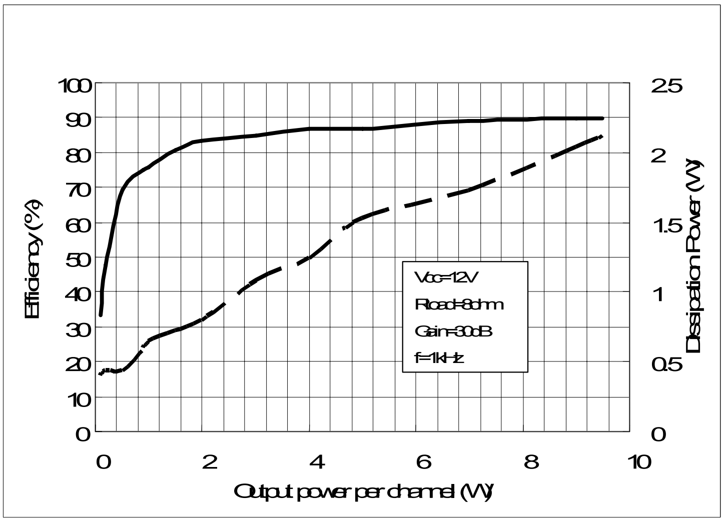


Figure 42. Closed-loop gain vs frequency

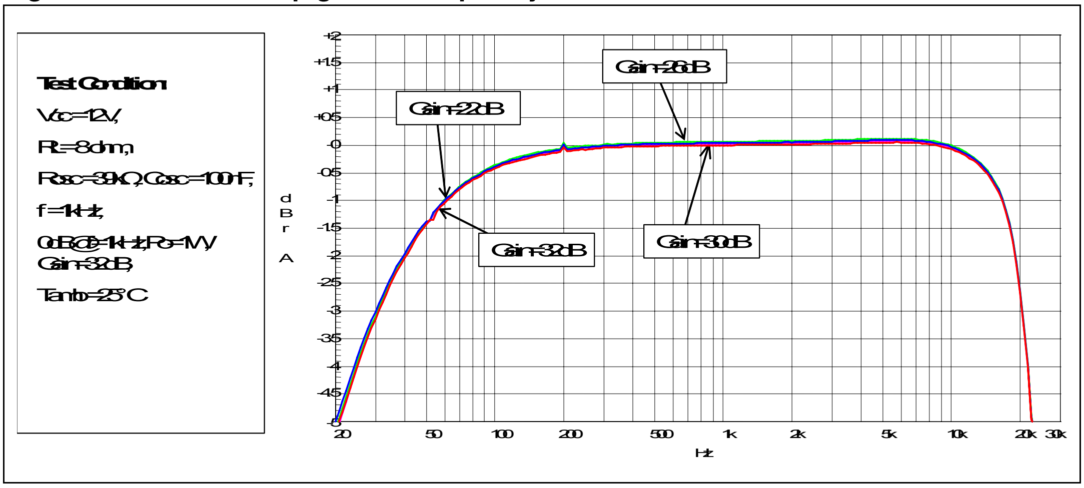


Figure 43. Current consumption vs voltage on pin MUTE

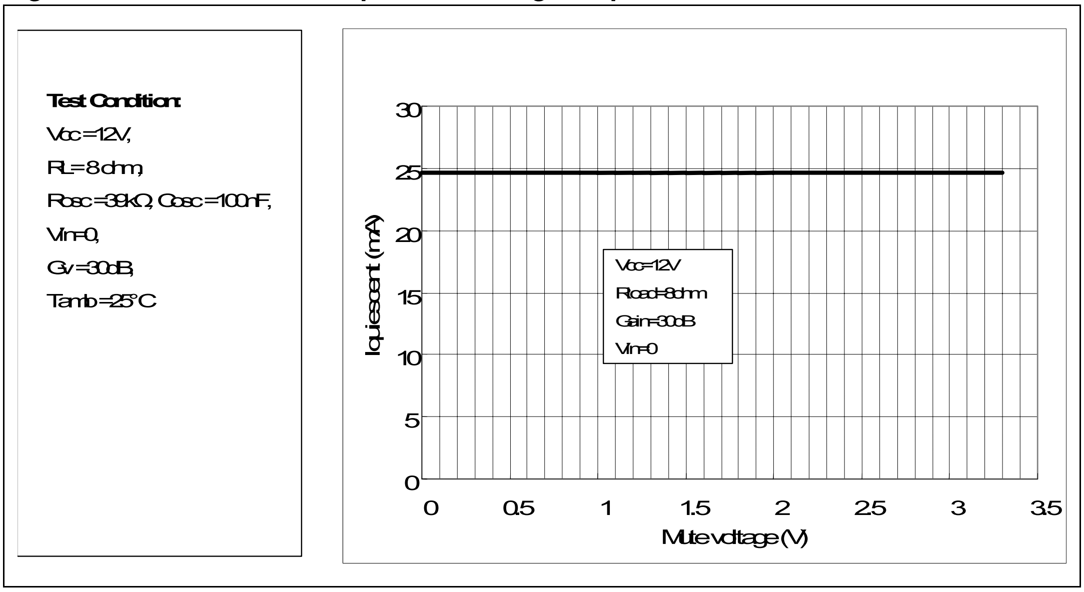


Figure 44. Attenuation vs voltage on pin MUTE

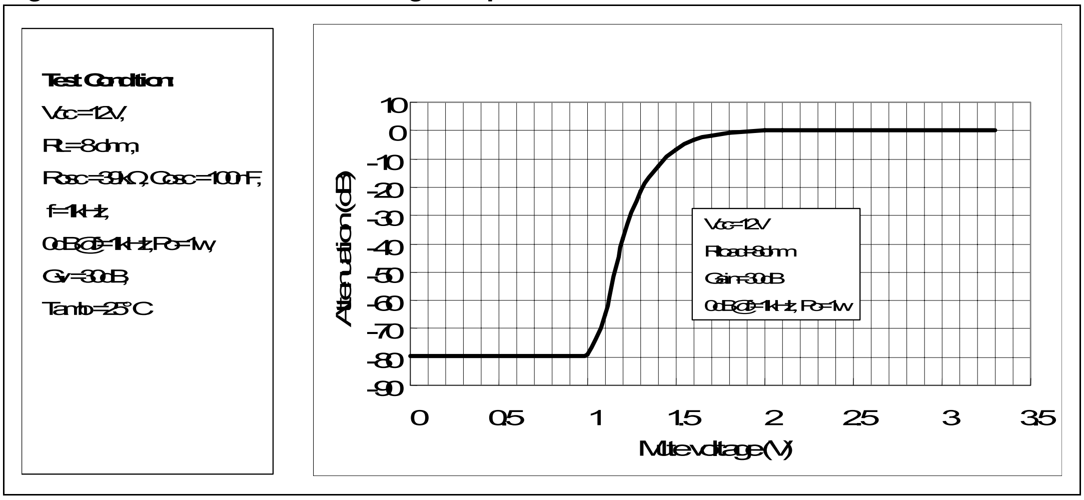


Figure 45. Current consumption vs voltage on pin STBY

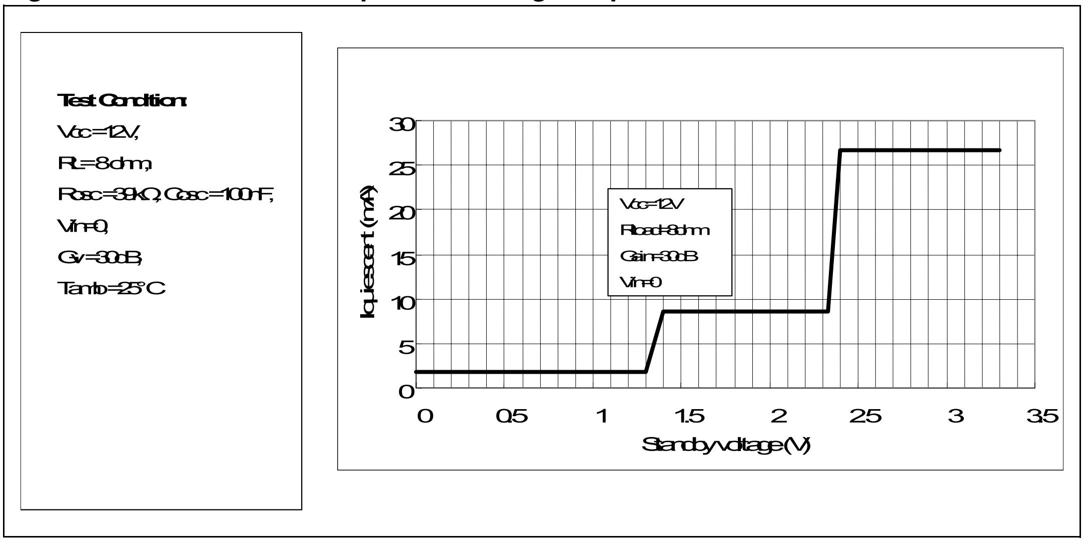


Figure 46. Attenuation vs voltage on pin STBY

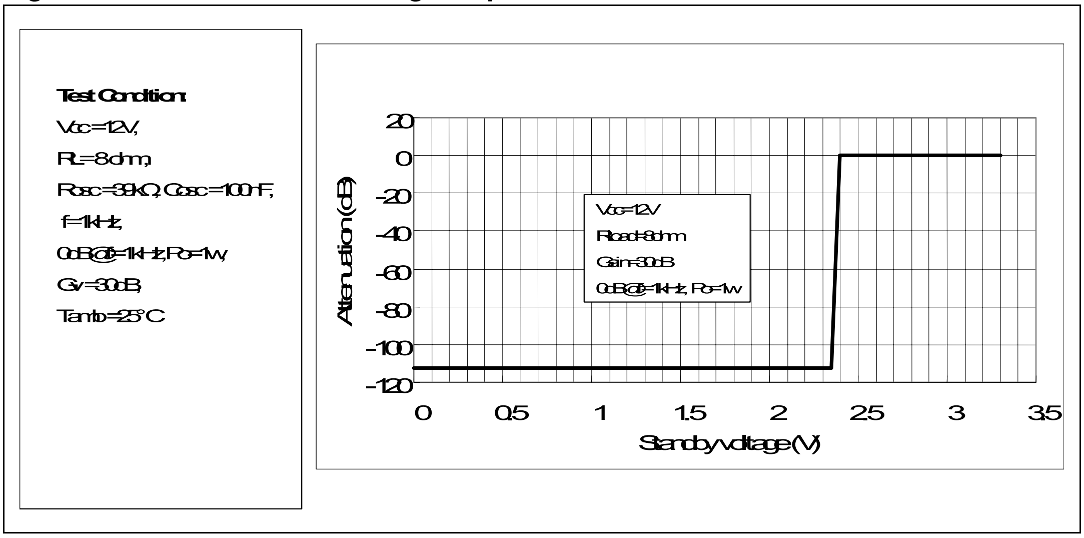
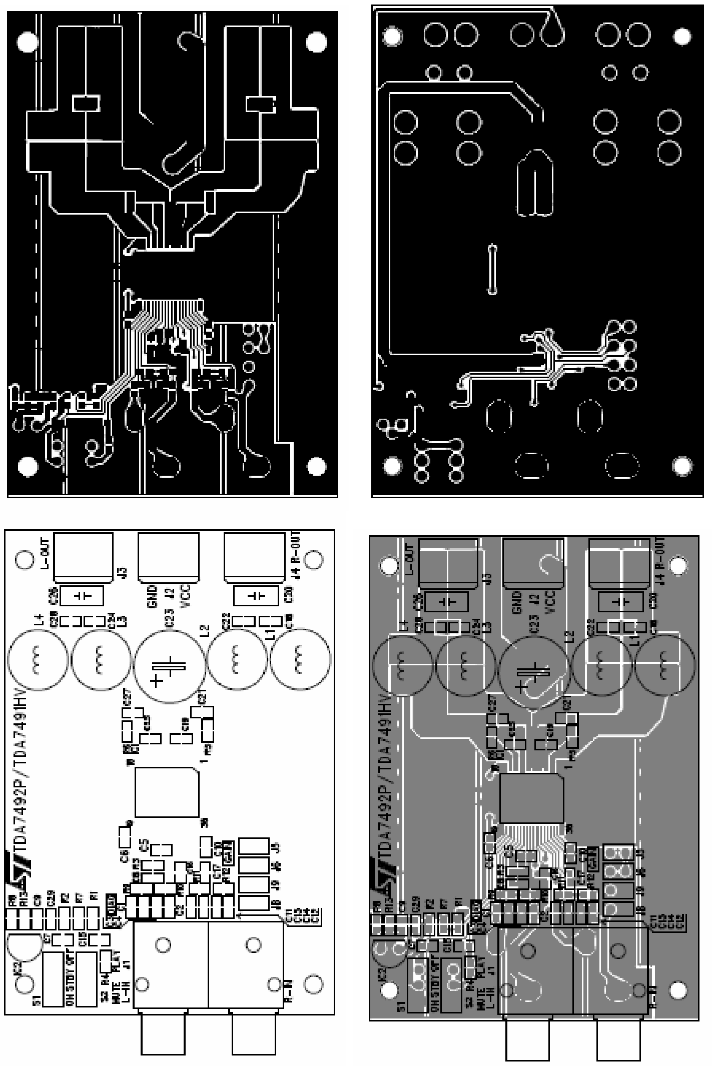


Figure 47. Test board (TDA7491P) layout



5 Package information

The TDA7491P comes in a 36-pin PowerSSO package with exposed pad (slug) down. *Figure 48* below shows the package outline and *Table 5* gives the dimensions.

Figure 48. PowerSSO-36 slug down outline drawing

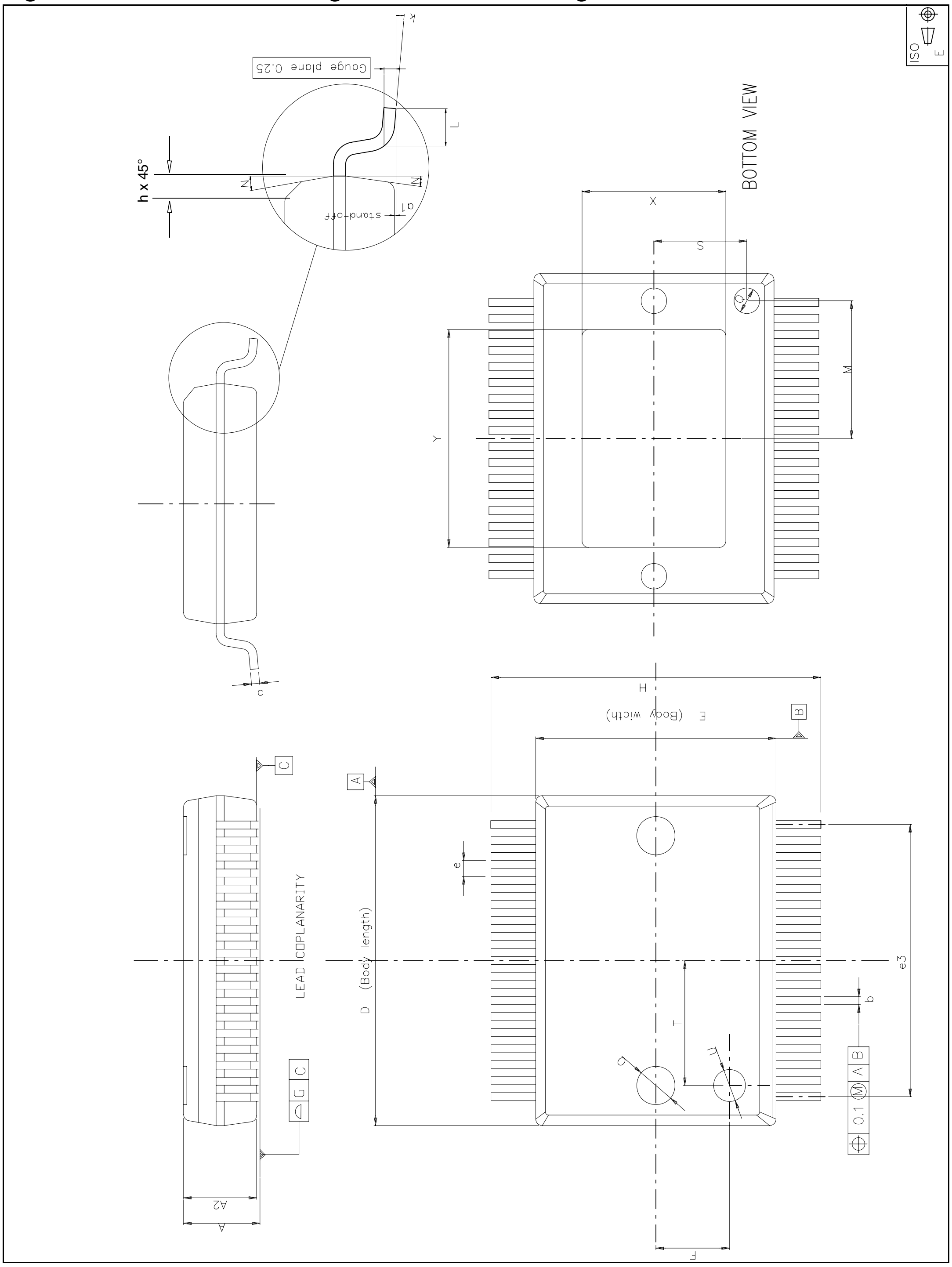


Table 5. PowerSSO-36 slug down dimensions

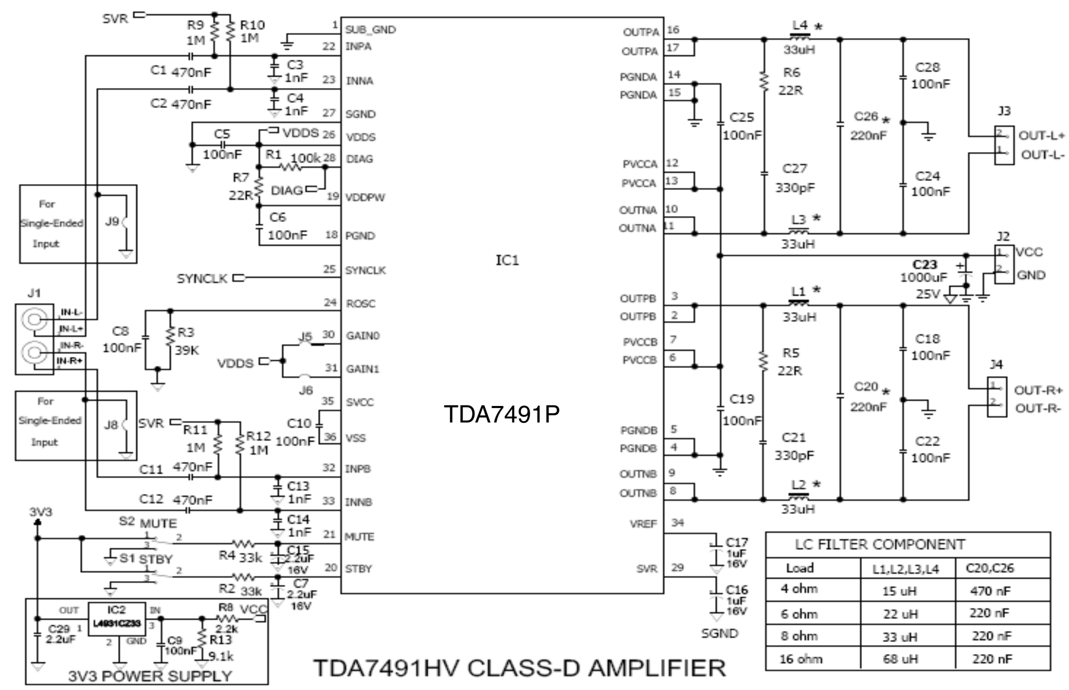
Symbol	Dimensions in mm			Dimensions in inch		
	Min	Typ	Max	Min	Typ	Max
A	2.15	-	2.47	0.085	-	0.097
A2	2.15	-	2.40	0.085	-	0.094
a1	0	-	0.10	0	-	0.004
b	0.18	-	0.36	0.007	-	0.014
c	0.23	-	0.32	0.009	-	0.013
D	10.10	-	10.50	0.398	-	0.413
E	7.40	-	7.60	0.291	-	0.299
e	-	0.5	-	-	0.020	
e3	-	8.5	-	-	0.335	
F	-	2.3	-	-	0.091	
G	-	-	0.10	-	-	0.004
H	10.10	-	10.50	0.398		0.413
h	-	-	0.40			0.016
k	0	-	8 degrees			8 degrees
L	0.60	-	1.00	0.024		0.039
M	-	4.30	-		0.169	
N	-	-	10 degrees			10 degrees
O	-	1.20	-		0.047	
Q	-	0.80	-		0.031	
S	-	2.90	-		0.114	
T	-	3.65	-		0.144	
U	-	1.00	-		0.039	
X	4.10		4.70	0.161		0.185
Y	6.50		7.10	0.256		0.280

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Pb-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark.

ECOPACK specifications are available at: http://www.st.com.

6 Application circuit

Figure 49. Application circuit



Input settings for gain:

GAIN0 : GAIN1	**Nominal gain**
0 V : 0 V	20 dB
0 V : 3.3 V	26 dB
3.3 V : 0 V	30 dB
3.3 V : 3.3 V	32 dB

Input settings for standby, mute and

STBY : MUTE	**Mode**
0 V : 0 V	Standby
0 V : 3.3 V	Standby
3.3 V : 0 V	Mute
3.3 V : 3.3 V	Play

7 Application information

7.1 Mode selection

The three operating modes of the TDA7491P are set by the two inputs STBY (pin 20) and MUTE (pin 21).

- Standby mode: all circuits are turned off, very low current consumption.
- Mute mode: inputs are connected to ground and the positive and negative PWM outputs are at 50% duty cycle.
- Play mode: the amplifiers are active.

The protection functions of the TDA7491P are realized by pulling down the voltages of the STBY and MUTE inputs shown in *Figure 50*. The input current of the corresponding pins must be limited to 200 µA.

Table 6. Mode settings

Mode Selection	STBY	MUTE
Standby	L (1)	X (don't care)
Mute	H (1)	L
Play	H	H

1. Drive levels defined in *Table 4: Electrical specifications on page 6*

Figure 50. STBY and MUTE circuit

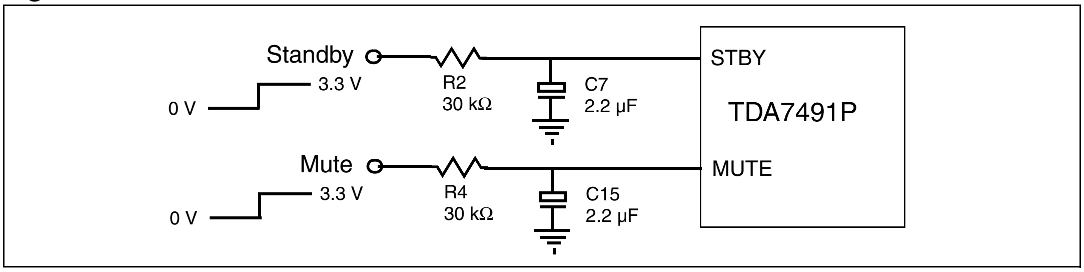
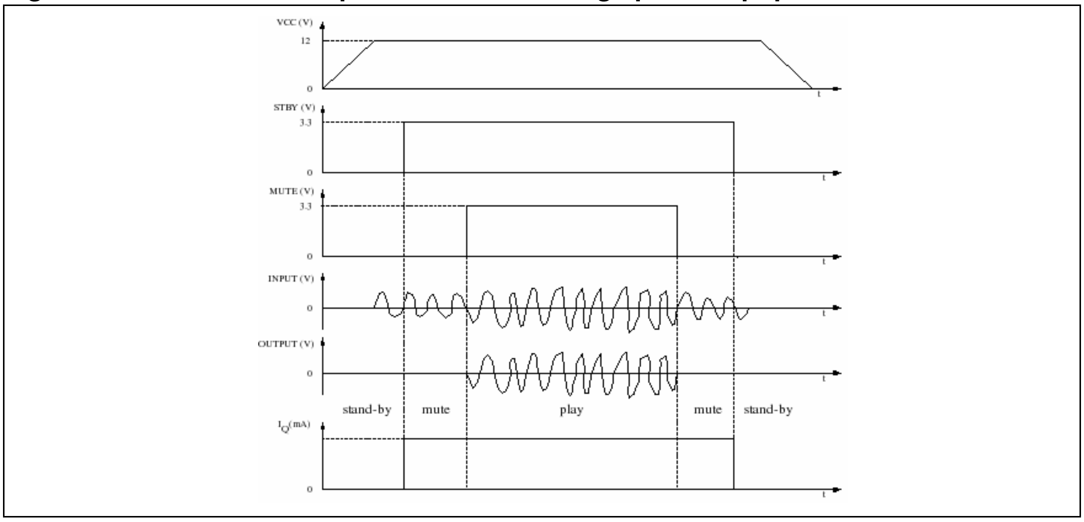


Figure 51. Turn on/off sequence for minimizing speaker "pop"



7.2 Gain setting

The gain of the TDA7491P is set by the two inputs, GAIN0 (pin 30) and GAIN1 (pin 31). Internally, the gain is set by changing the feedback resistors of the amplifier.

Table 7. Gain settings

GAIN0	GAIN1	Nominal gain, G_v (dB)
0	0	20
0	1	26
1	0	30
1	1	32

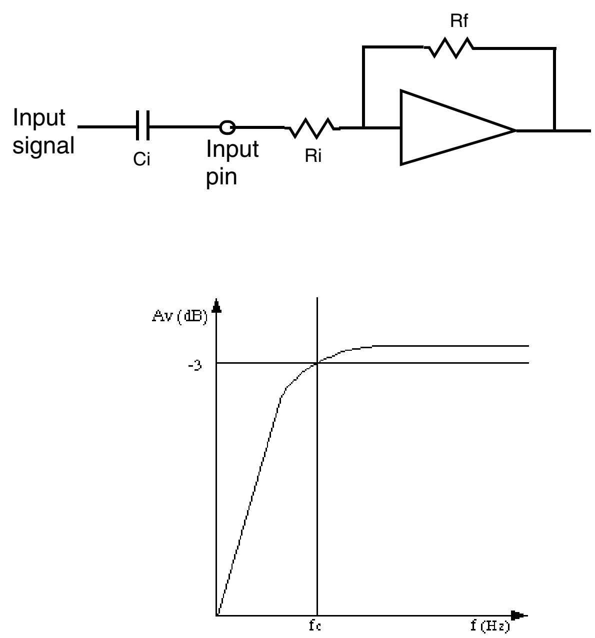
7.3 Input resistance and capacitance

The input impedance is set by an internal resistor Ri = 60 kΩ (typical). An input capacitor (Ci) is required to couple the AC input signal.

The equivalent circuit and frequency response of the input components are shown in *Figure 52*. For Ci = 220 nF the high-pass filter cut-off frequency is below 20 Hz:

$$fc = 1 / (2 * \pi * Ri * Ci)$$

Figure 52. Device input circuit and frequency response



7.4 Internal and external clocks

The clock of the class-D amplifier can be generated internally or can be driven by an external source.

If two or more class-D amplifiers are used in the same system, it is recommended that all devices operate at the same clock frequency. This can be implemented by using one TDA7491P as master clock, while the other devices are in slave mode (that is, externally clocked. The clock interconnect is via pin SYNCLK of each device. As explained below, SYNCLK is an output in master mode and an input in slave mode.

7.4.1 Master mode (internal clock)

Using the internal oscillator, the output switching frequency, f_{SW}, is controlled by the resistor, R_{OSC}, connected to pin ROSC:

$$f_{SW} = 10^6 / (64 * R_{OSC} + 440) \text{ kHz}$$

where R_{OSC} is in kΩ

In master mode, pin SYNCLK is used as a clock output pin, whose frequency is:

$$f_{SYNCLK} = 2 * f_{SW}$$

For master mode to operate correctly then resistor R_{OSC} must be less than 60 kΩ as given below in *Table 8*.

7.4.2 Slave mode (external clock)

In order to accept an external clock input the pin ROSC must be left open, that is, floating. This forces pin SYNCLK to be internally configured as an input as given in *Table 8*.

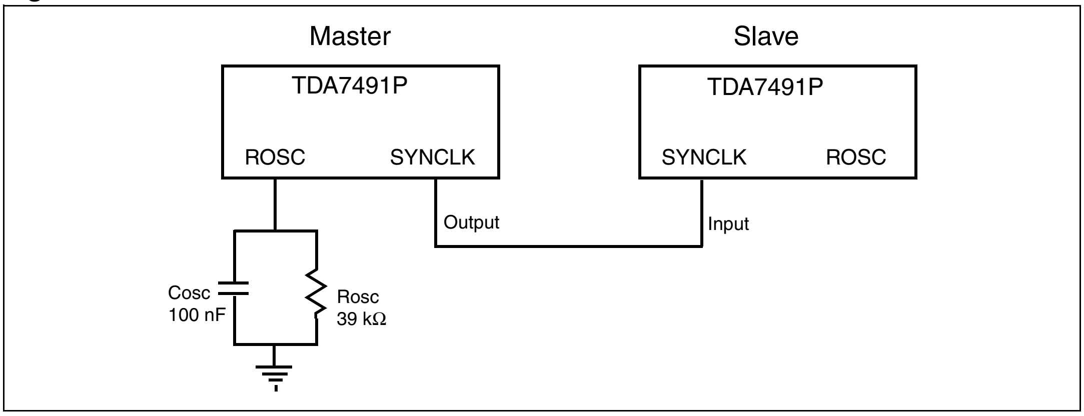
The output switching frequency of the slave devices is:

$$f_{SW} = f_{SYNCLK} / 2$$

Table 8. How to set up SYNCLK

Mode	ROSC	SYNCLK
Master	R_{OSC} < 60 kΩ	OUTPUT
Slave	Floating (not connected)	INPUT

Figure 53. Master and Slave Connection



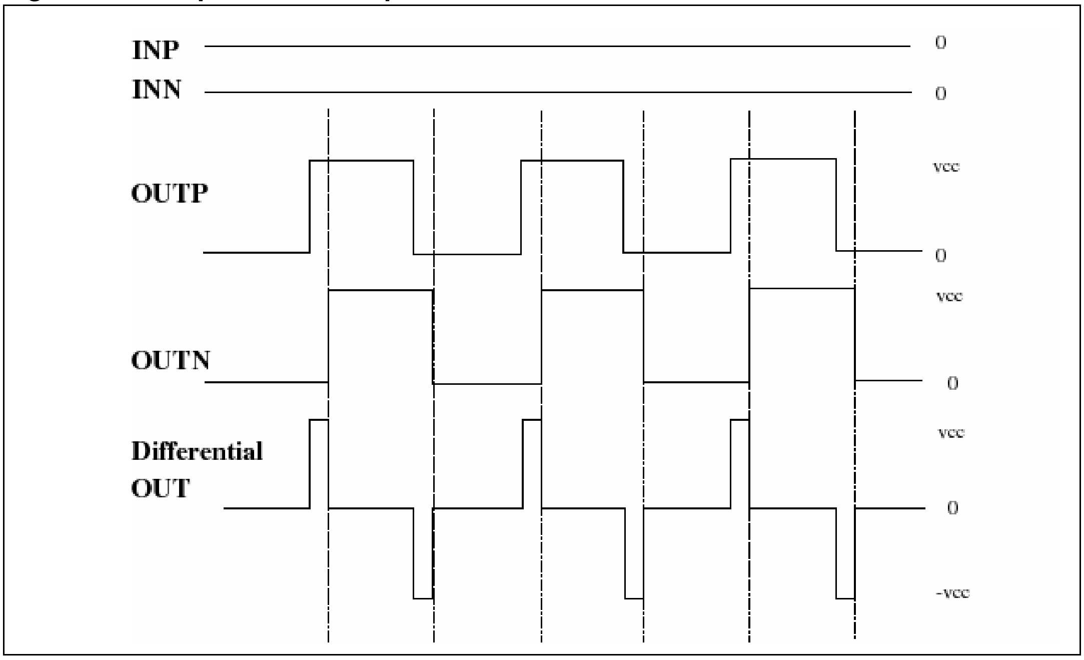
7.5 Filterless modulation

The output modulation scheme of the BTL is called unipolar pulse width modulation (PWM). The differential output voltages change between zero and +Vcc and between zero and -Vcc. This is in contrast to the traditional bipolar PWM outputs which change between +Vcc and -Vcc.

An advantage of this scheme is that it effectively doubles the switching frequency of the differential output waveform. The OUTP and OUTN are in the same phase when the input is zero, then the switching current is low and the loss in the load is small. In practice, a short delay is introduced between these two outputs in order to avoid the BTL output switching at the same time.

TDA7491P can be used without a filter before the speaker, because the frequency of the TDA7491P output is beyond the audio frequency, the audio signal can be recovered by the inherent inductance of the speaker and natural filter of the human ear.

Figure 54. Unipolar PWM output



7.6 Output low-pass filter

To avoid EMI problems, it may be necessary to use a low-pass filter before the speaker. The cutoff frequency should be larger than 22 kHz and much lower than the output switching frequency. It is necessary to choose the L-C component values depending on the loud speaker impedance. Some typical values, which give a cut-off frequency of 27 kHz, are shown in *Figure 55* and *Figure 56* below.

Figure 55. Typical LC filter for a 8 Ω speaker

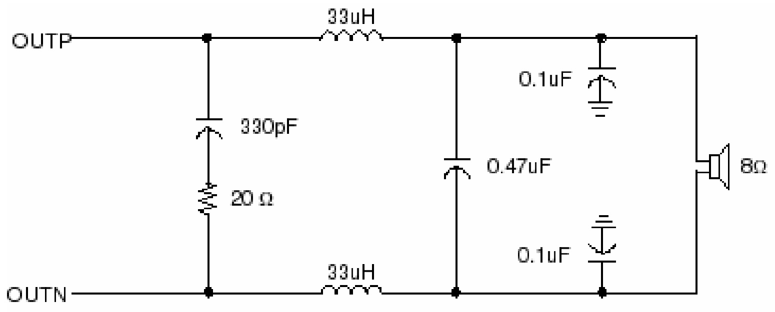
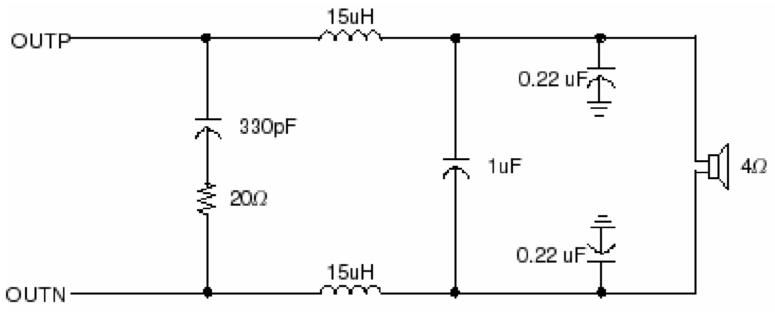


Figure 56. Typical LC filter for a 4 Ω speaker



7.7 Protection function

The TDA7491P is fully protected against over-voltages, under-voltages, over- currents and thermal overloads as explained here. See also *Table 4: Electrical specifications on page 6*.

Over voltage protection (OVP)

If the supply voltage exceeds 20 V (nominal) the over voltage protection is activated which forces the outputs to the high-impedance state. When the supply voltage drops to below the threshold value the device restarts.

Under voltage protection (UVP)

If the supply voltage drops below 4 V (nominal) the under voltage protection is activated which forces the outputs to the high-impedance state. When the supply voltage recovers the device restarts.

Over current protection (OCP)

If the output current exceeds 4 A (nominal) the over current protection is activated which forces the outputs to the high-impedance state. Periodically, the device attempts to restart. If the over-current condition is still present then the OCP remains active. The restart time, T_{OC}, is determined by the R-C components connected to pin STBY.

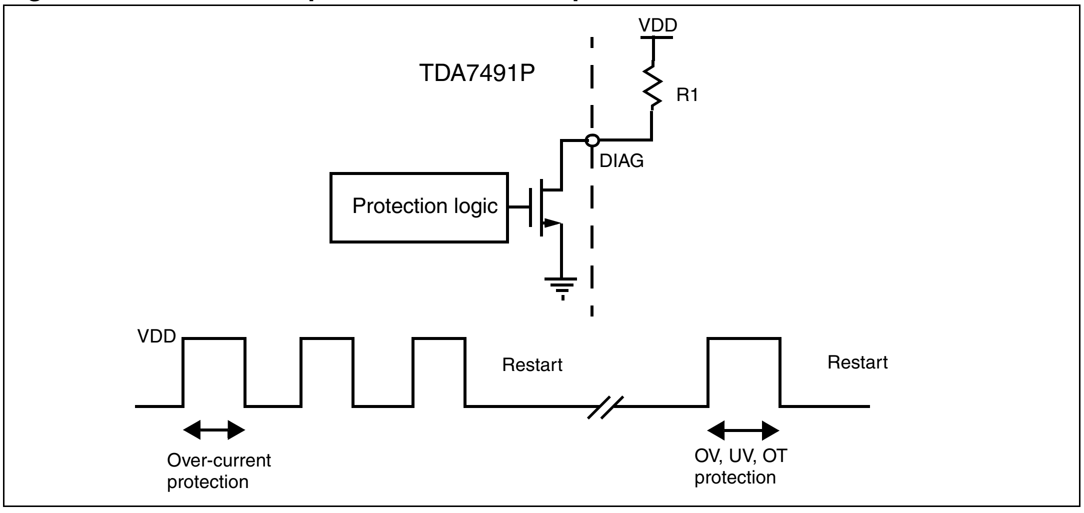
Thermal protection (OTP)

If the junction temperature, T_j, reaches 145 °C (nominally), the device goes to mute mode and the positive and negative PWM outputs are forced to 50% duty cycle. At Tj = 155 °C (nominally), the device shuts down and the output is forced to the high impedance state. When the device cools sufficiently the device restarts.

7.8 Diagnostic output

The output pin DIAG is an open drain transistor. When the protection is activated it is in the high-impedance state. The pin can be connected to a power supply (< 20 V) by a pull-up resistor whose value is limited by the maximum sinking current (200 μA) of the pin.

Figure 57. Behavior of pin DIAG for various protection conditions



7.9 Heatsink requirements

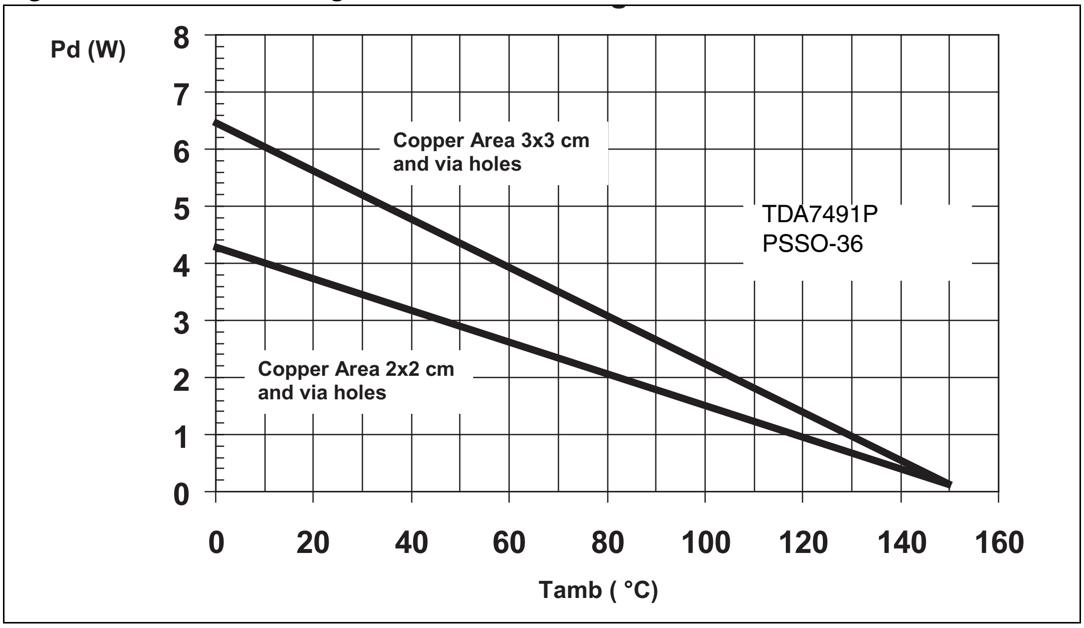
A thermal resistance of 24 °C/W can be obtained using the PCB copper ground layer with 16 vias connecting it to the contact area for the slug. Ensure that the copper ground area is a nominal 9 cm² for 24 °C/W.

Figure 58 shows the derating curves for copper areas of 4 cm² and 9 cm².

As with most amplifiers, the power dissipated within the device depends primarily on the supply voltage, the load impedance and the output modulation level.

The maximum estimated power dissipation for the TDA7491P is less than 2 W. When properly mounted on the above PCB the junction temperature could increase by 48° C. However, with a musical program the dissipated power is about 40% less, leading to a temperature increase of around 30° C. Even at the maximum recommended ambient temperature for consumer applications of 50 °C there is still a clear safety margin before the maximum junction temperature (150 °C) is reached.

Figure 58. Power derating curves for PCB used as heatsink



8 Revision history

Table 9. Document revision history

Date	Revision	Changes
02-Jul-2007	1	Initial release.
15-Oct-2008	2	Updated performance characterization curves.