LOW I_Q 30 µA, HIGH V_{IN}, DUAL OUTPUT, SUPPLY AND BOOST CONTROLLER

Check for Samples: TPS43330-Q1 , TPS43332-Q1

FEATURES

- Dual Output Synchronous Buck Controller
  - Peak Gate Drive Current 1.5 A
  - Out-of-Phase Switching Between BuckA and BuckB
  - Frequency Spread Spectrum (f_{SS}) (TPS43332 Only)
  - Independent Programmable Soft-Start Inputs (SSA, SSB)
  - Independent Power-Good Indicators (PGA, PGB)
  - Separate Enable Inputs (ENA, ENB)
  - Automatic Low-Power Mode Operation (Active When SYNC Terminal is Low)
  - Switching Frequency f_{SW_Buck} Range 150 kHz to 600 kHz Programmable Via External Resistor
  - External Synchronization Range: 150 kHz to 600 kHz
  - Low Current Consumption
    - 30 µA (typ) With Single-Output Operation in Low-Power Mode
    - 40 µA (typ) With Dual-Output Operation in Low-Power Mode
- Boost Controller for Low Input Voltage Operation
  - Peak Gate Drive Current 1.5 A
  - Switching Frequency Equals $f_{SW\_Buck}/2$
- Input Voltage Range: 2 V to 36 V, Transients up to 60 V
- Internal Voltage Reference ±1.5%
- Very Low Leakage Current in Shutdown: I_{sh} < 5 µA
- Short Circuit, Over Current, and Thermal Protection
- Thermally Enhanced Package for Efficient Heat Management
  - 38-Pin HTSSOP (DAP) PowerPAD™ Package

APPLICATIONS

- Automotive Systems
  - Infotainment
  - Navigation
  - Instrumentation Dashboard Cluster
- Multi-Rail DC Power Distribution Systems
  - Electronic Control Units

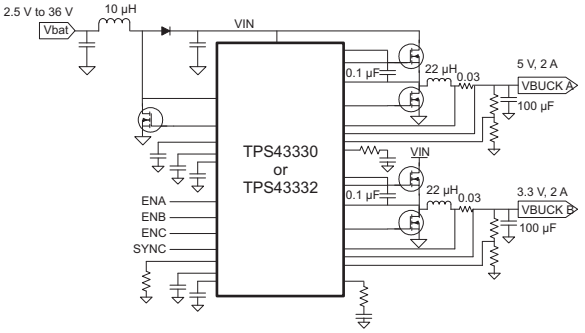
DESCRIPTION

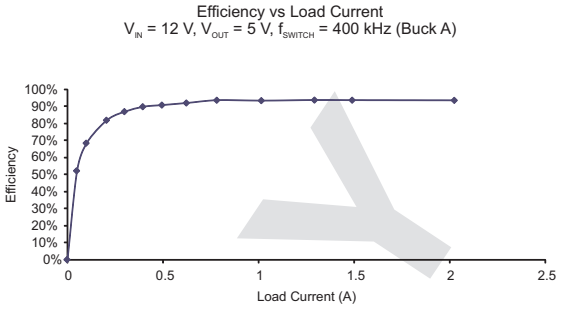
The TPS43330/2 is a dual Synchronous Current Mode Buck controller designed for the harsh environments of automotive applications and includes basic protection features such as thermal, soft-start and over current protection. In addition there is a non synchronous Voltage Mode Boost controller.

The TPS43330 provides a high efficient and fail safe power management solution for electronic control units. The two-step down output voltages of the device are ideally suited to deliver uC core and IO supply voltages. Due to the very low quiescent current the controller is ideal for applications that require a supply to microcontrollers and memories during ignition-off state. The seamless activation of the boost controller guarantees regulated supply lines during vehicle cranking profile or negative transients.

During short circuit conditions of the regulator output, the current through the MOSFET's can be limited for power dissipation by activation of the current fold back concept. The two independent soft start inputs allow ramp up of the output voltage independently during start up.

SIMPLIFIED SCHEMATIC





BLOCK DIAGRAM

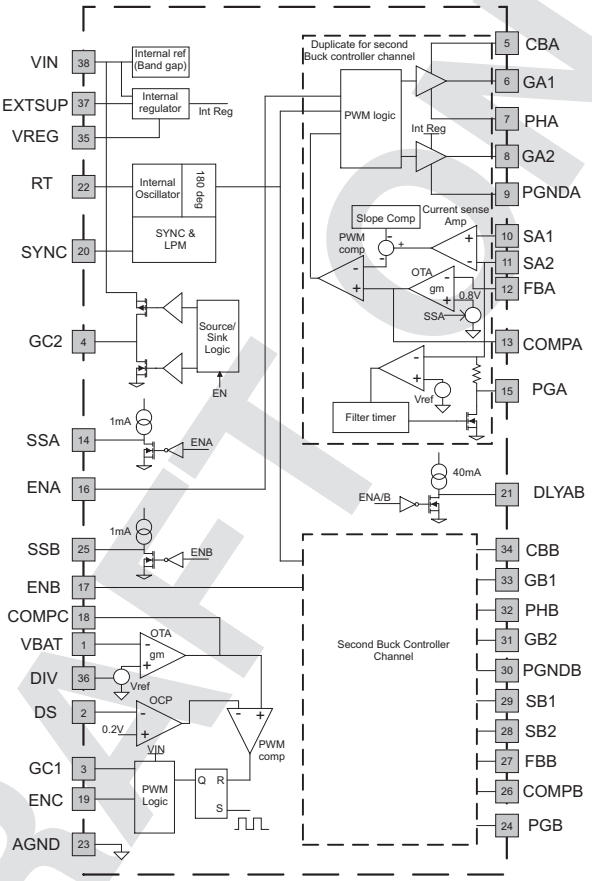


Figure 1. Block Diagram

ORDERING INFORMATION(1)

T_J	OPTION	PACKAGE(2)	ORDERABLE PART NUMBER
-40ºC to 150ºC	Frequency Hopping Spread Spectrum OFF	DAP	TPS43330QDAPQ1
-40ºC to 150ºC	Frequency Hopping Spread Spectrum ON	DAP	TPS43332QDAPQ1

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS(1)(2)

NO.				VALUE	UNIT
1.1	VIN, VBAT, ENA, ENB, GC2, DS	Unregulated input voltage(3)		-0.3 to 40	V
		Unregulated input voltage(4)		-0.3 to 60	V
1.2	CBA, CBB, GA1, GB1	Unregulated input voltage(3)		-0.3 to 68	V
1.3	PHA, PHB	Unregulated input voltage(5)		-1.0 to 60	V
1.4	SA1, SA2, SB1, SB2	Current sensing signal voltage(3)		-0.3 to 13	V
1.5	FBA, FBB, COMPA, ENC, COMPB, PGA, PGB, SYNC	Input voltage		-0.3 to 13	V
1.6	DLYAB, RT, GA2, GB2, GC1, VREG, COMPC, DIV, SSA, SSB	Input voltage		-0.3 to 8	V
1.7	VIN – GC2	Input voltage		-0.3 to 8	V
1.8	EXTSUP	Charge pump supply or external supply voltage		-0.3 to 13	V
1.9	Gx1, CBx	Input voltage		PHx - 0.3 to PHx + 8	V
1.10	T_J	Operating virtual junction temperature range,		-40 to 150	°C
1.11	T_S	Storage Temperature Range		-55 to 165	°C
1.12	T_{Lead}	Lead temperature (soldering, 10sec)		260	°C
1.13	ESD	Electrostatic discharge rating	Human-Body Model (HBM)(6)	2.0	kV

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.
(3) Absolute negative voltage on these pins not to go below –0.5 V for TBD ns.
(4) Absolute maximum voltage for less than 480ms
(5) Absolute negative voltage on these pins not to go below –1.0 V, and transients due to recirculation of an inductive load up to -2V for TBDnS.
(6) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin.

RECOMMENDED OPERATING CONDITIONS

NO.			MIN	MAX	UNIT
2.1	VIN, ENA, ENB, GC2, DS	Unregulated buck supply input voltage(1)	4.0	36	V
2.2	DLYAB, RT, COMPC, SSA, SSB, SYNC, DIV	Input voltage	0	5.25	V
2.3	SA1, SA2, SB1, SB2	Current sensing signal voltage	0	12	V
2.4	θ_{JA}	Thermal resistance, junction to ambient(2)		28	°C/W
2.5	θ_{JC}	Thermal resistance, junction to case(3)		10	°C/W
2.6	T_A	Operating Free-Air Temperature range(4)	-40	125	°C

(1) The minimum operating voltage is based on the VIN voltage being reduced from 7V initially
(2) This assumes a JEDEC JESD 51-5 standard board with thermal vias – See Power Pad section and application note from Texas Instruments SLMA002 for more information.
(3) This assumes junction to exposed thermal pad.
(4) This assumes $T_A = T_J$ – Power dissipation × θ_{JA} (junction to ambient).

DC ELECTRICAL CHARACTERISTICS

VIN = 8V to 18V, TJ = -40C to 150C (unless otherwise noted)

NO.	TEST(1)	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
3.0	**Input Supply**							
3.1	PT	V_{Bat}	Supply Voltage	Boost Controller enabled, after initial start up condition is satisfied	2.0		36.0	V
3.2	PT	V_{IN}	Device Operating Range	Boost Controller disabled(2) Input voltage required for Buck regulator on initial start up	6.5		36.0	V
				Buck regulator operating range AFTER initial start up	4.0		36.0	V
3.3	PT	$V_{IN\ UV}$	Buck Under Voltage Lockout	Vin Falling	3.5	3.6	3.8	V
						3.8	4	V
3.4	PT	$V_{INB-Off}$	Boost unlock threshold			8.5		V
3.5	PT	$I_{q\_LPM\_}$	LPM Quiescent Current: T_A = 25°C(3)	VIN=13V, BuckA: LPM, BuckB: off		30	40	µA
				VIN=13V, BuckB: LPM, BuckA: off				
				VIN=13V, BuckA, B: LPM		35	50	µA
3.6	PT	I_{q_LPM}	LPM Quiescent Current: T_A = 85°C(3)	VIN=13V, BuckA: LPM, BuckB: off		50	70	µA
				VIN=13V, BuckB: LPM, BuckA: off				
				VIN=13V, BuckA, B: LPM		60	80	µA
3.7	PT	I_{quies}	Quiescent Current: T_A = 25°C(4)	Normal operation, SYNC = 5V				mA
				VIN=13V, BuckA: CCM, BuckB: off		5	6	mA
				VIN=13V, BuckB: CCM, BuckA: off		5	6	mA
				VIN=13V, BuckA, B: CCM		7	7.5	mA
3.8	PT	I_{quies}	Quiescent Current: T_A = 85°C(4)	Normal operation, SYNC = 5V				mA
				VIN=13V, BuckA: CCM, BuckB: off		5.5	6	mA
				VIN=13V, BuckB: CCM, BuckA: off		5.5	6	mA
				VIN=13V, BuckA, B: CCM		5	8	mA
3.9	PT	I_{bat_sh}	Shutdown current at T_A = 25°C	BuckA, B: off, VBat=13V		5	10	µA
3.10	PT	I_{bat_sh}	Shutdown current at T_A = 125°C	BuckA, B: off, VBat=13V			10	µA
4.0	**Input voltage VBAT - Under voltage lock out**							
4.1	PT	$V_{BatULVO}$	Disable outputs	See figure 11: threshold 4, VBat decreasing	1.8	1.9	2.0	V
				VBat rising	2.4	2.5	2.6	V
4.2	PT	$UVLO_{Hys}$	Hysteresis		500	600	700	mV
4.3	PT	$UVLO_{filter}$	Filter time			5		µs
5.0	**Input voltage VIN - Over voltage lock out**							
5.1	PT	V_{OVLO}	Over Voltage shutdown	(based on VIN sense) Rising	45	46	47	V
				Falling	43	44	45	V
5.2	PT	$OVLO_{Hys}$	Hysteresis		1	2	3	V
5.3	PT	$OVLO_{filter}$	Filter time			5		µs
6.0	**Boost Controller**							
6.3	PT	$V_{boost7-VIN}$	Boost Vout 7V	DIV = low, VBat= 3.0V to 5V		7.0		V
6.4	PT	$V_{boost7-th}$	Boost mode threshold Boost Vout 7V	VBat falling – Boost enable threshold	7.5	8.0	8.5	V
				VBat rising – Boost disable threshold	8.0	8.5	9.0	V
				Hysteresis	0.4	0.5	0.6	V
6.5	PT	$V_{boost10-VIN}$	Boost Vout 10V	DIV = open, VBat= 3.0V to 5V		10		V
6.6	PT	$V_{boost10-th}$	Boost mode threshold Boost Vout 10V	VBat falling – Boost enable threshold	10.5	11	11.5	V
				VBat rising – Boost disable threshold	11.0	11.5	12.0	V
				Hysteresis	0.4	0.5	0.6	V

(1) PT = Production tested; CT = Characterization only, not production tested; Info = Information based on simulations and lab evaluation, not production tested

(2) For VIN = 4V to 7V the boost is disabled and controller operates as a buck regulator.

(3) Quiescent current specification does not include the current flow through the external feedback resistor divider. Quiescent current is measured with no load on the output and at 25°C with VBat = 13V, unless otherwise specified in the test.

(4) Quiescent current specification does not include the current flow through the external feedback resistor divider. Quiescent current is measured with no load on the output and at 25°C with VBat = 13V, unless otherwise specified in the test.

DC ELECTRICAL CHARACTERISTICS (continued)

VIN = 8V to 18V, TJ = -40C to 150C (unless otherwise noted)

NO.	TEST(1)	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
6.7	PT	$V_{boost10-VIN}$	Boost Vout 12V	DIV = high, VBat= 3.0V to 5V		12		V
	Boost Switch current limit							
6.8	PT	V_{DS}	Current limit sensing	DS input with respect to PGNDA	0.175	0.2	0.225	V
6.9	Info	t_{DS}	leading edge blanking			200		ns
	Gate Driver for Boost Controller							
6.10	Info	$I_{GC1\ Peak}$	Gate driver peak current	Not production tested(5)		1.5		A
6.11	PT	$R_{DS\ ON}$	Source and Sink driver	IGC1 current for external MOSFET = 100mA		3	5	Ω
	Boost regulator Switching frequency							
6.12	PT	$f_{sw-Boost}$	Divided from Buck switching freq			f_{SW_Buck} / 2		kHz
6.13	PT	D_{Boost}	Boost duty cycle		0		90	%
	Error Amplifier (OTA) for Boost Converters							
6.14	PT	gm	Forward Transconductance	COMPC = 0.8V; source/sink = 5µA, Test in feedback loop		1.0		mmhos
7.0	**Buck Controllers**							
7.1	PT	$V_{BuckA/B}$	adj. output voltage range	Closed loop	0.9		12	V
7.2	PT	V_{ref}, V_{ref_LPM}	internal reference voltage	Measure FBX pin, load = 0mA	0.788	0.800	0.812	V
				Internal tolerance on reference	-1.5		+1.5	%
7.3	PT	V_{sense}	V sense for forward OC in CCM	Voltage drop between sense pins	60	75	90	mV
7.4	PT		V sense for reverse OC in CCM	Voltage drop between sense pins	-90	-60	-30	mV
7.5	PT	$V_{I-Foldback}$	Current fold back threshold during output short	Decrease FBX and measure voltage at CompX		0.6		V
7.6	PT	t_{dead}	shoot through delay, blanking time		50	100	200	ns
7.7	PT	DC	Duty cycle		3.5		94	%
7.8	PT	DC_{LPM}	Duty Cycle LPM				80	%
7.9	PT	V_{sense_LPM}	LPM threshold		TBD		TBD	mV
7.10	PT	LPM delay	Transition time	ILoad = 5mA to 500mA in TBDus	TBD		TBD	us
	High Side external NMOS Gate Drivers for Buck Controller							
7.11	PT	I_{GX1_peak}	Gate driver peak current	Not production tested(6)		1.5		A
7.12	PT	$R_{DS\ ON}$	Source and Sink driver	IGXX current for external MOSFET = 200mA		3	5	Ω
	Low Side NMOS Gate Drivers for Buck Controller							
7.13	PT	I_{GX2_peak}	Gate driver peak current	Not production tested(6)		1.5		A
7.14	PT	$R_{DS\ ON}$	Source and sink driver	IGXX current for external MOSFET = 200mA		3	5	Ω
	Gate Driver for PMOS							
7.15	PT	$R_{DS\ ON}$	PMOS OFF			10	20	Ω
7.16	PT	I_{PMOS_ON}	Gate current	Vin =13.5V, Vgs = -5V	10			mA
7.17	PT	t_{delay_ON}	Turn ON delay	C = 10nf		5	10	µs
	Error Amplifier (OTA) for Buck Converters							
7.18	PT	Gm	Forward transconductance	COMPA, COMPB = 0.8V, source/sink = 5µA, Test in feedback loop		1.0		mMhos
8.0	**Digital Inputs: ENA, ENB, INHC, SYNC,**							
8.1	PT	V_{ih}	Higher threshold	VIN = 13V	1.5			V
8.2	PT	V_{il}	Lower threshold	VIN = 13V			0.7	V
8.3	PT	R_{ih_SYNC}	Resistance	VSYNC = 5V, SYNC: pull down to 0V		500		kΩ
8.4	PT	R_{il_INHC}	Resistance	VINHC = 0V enable Boost, INHC: pulldown resistance		500		kΩ
8.5	PT	I_{il_ENx}	Leakage current	VENx = 0V, ENA, ENB: pullup current source		0.5	2	µA

(5) Specified by design
(6) Specified by design

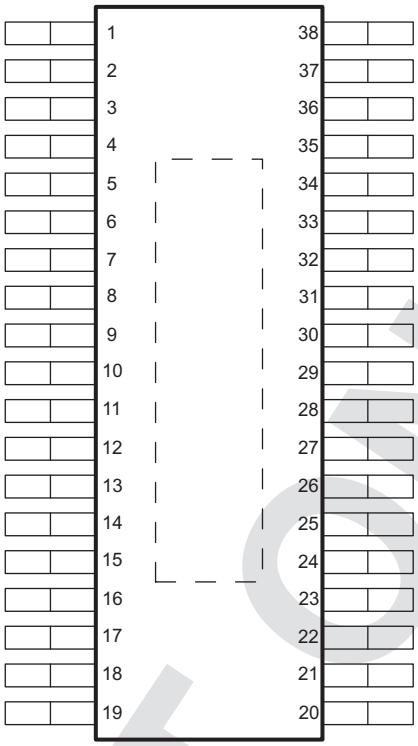
DC ELECTRICAL CHARACTERISTICS (continued)

VIN = 8V to 18V, TJ = -40C to 150C (unless otherwise noted)

NO.	TEST(1)	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
9.0	**Boost Output Voltage: DIV**							
9.1	PT	V_{ih_DIV}	Higher threshold		Vreg-0.2			V
9.2	PT	V_{il_DIV}	Lower threshold				0.2	V
9.3	PT	V_{oz_DIV}	open	floating		Vreg/2		V
10.0	**Switching Parameter – Buck DC-DC converters**							
10.1	PT	f_{SW_Buck}	Buck switching frequency	RT pin: GND	360	400	440	kHz
10.2	PT	f_{SW_Buck}	Buck switching frequency	RT pin: R7 = 60kΩ	360	400	440	kHz
10.3	PT	f_{SW_adj}	Buck adjustable range	using external resistor R7 (see equation)	150		600	kHz
10.4	PT	f_{SYNC}	Buck synch. range	External clock input	150		600	kHz
10.5	CT	f_{SS}	Spread Spectrum spreading	External clock input		5		%
11.0	**Internal Supply VREG**							
11.1	PT	V_{REG}	Internal regulated supply	VIN = 8V to 18V, EXTSUP = 0V	5.5	5.8V	6.1	V
			Load Regulation	IVREG = 0mA to 100mA, EXTSUP = 0V		0.2	1.0	%
11.2	PT	$V_{REG-EXTSUP}$	Internal Regulated supply	EXTSUP = 8.5V	7.2	7.5	7.8	V
			Load Regulation	IEXSUP = 0mA to 125mA, EXTSUP = 8.5V		0.2	1	%
11.3	PT	$V_{EXTSUP-VREG}$	Switch over voltage	IVREG = 0mA to 100mA , EXTSUP ramping positive	4.4	4.6	4.8	V
11.4	PT	$V_{EXTSUP-Hys}$	Switch over hysteresis			100		mV
11.5	PT	$I_{REG-Limit}$	Current Limit on VREG		100			mA
11.6	PT	$I_{REG\_EXTSUP-Limit}$	Current Limit on VEXSUP	IVREG = 0mA to 100mA, EXTSUP Ramping positive	125			mA
12.0	**Soft Start**							
12.1	PT	I_{SSx}	Soft Start source current	SSA and SSB = 0V	0.75	1	1.35	µA
13.0	**Oscillator (RT)**							
13.1	PT	V_{RT}	Oscillator reference voltage			1.2		V
13.2	CT		Spread Spectrum spreading			5		%
14.0	**Power Good / Delay**							
14.1	PT	PG_{pullup}	Pullup for A and B	internal pullup to Sx2		50		kΩ
14.2	PT	PG_{th1}	Power Good Threshold		-5	-7	-9	%
14.3	PT	PG_{hys}	Hysteresis			2		%
14.4	PT	PG_{drop}	Voltage drop	IPGA=5mA			450	mV
14.5	PT			IPGA=1mA			100	mV
14.6	PT	PG_{leak}	Leakage	VSx2 =VPGx=13V			1	µA
14.7	PT	$t_{deglitch}$	Deglitch Time	Power Good deglitch	2		16	us
14.8	PT	t_{delay}	Reset Delay	external capacitor: 1ms / nF, VBUCKX = 0.93 of set voltage	1		300	ms
14.9	PT	t_{delay_fix}	Fixed Reset Delay	No external capacitor, pin open		20	50	us
14.10	PT	I_{oh}	Activate current source	Current to charge external capacitor		40		µA
14.11	PT	I_{il}	Activate current sink	Current to discharge external capacitor		40		µA
15.0	**Over Temperature Protection**							
15.1	CT	$T_{shutdown}$	shutdown threshold	Junction temperature	150	170		°C
15.2	CT	T_{hys}		Hysteresis		15		°C

DEVICE INFORMATION

DAP PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

NO.	NAME	PULLUP/ DOWN	I/O	ANALOG/ DIGITAL	DESCRIPTION
1	VBAT		I	A	Battery Voltage sense for Boost Controller and Efficiency FET driver
2	DS		I	A	Drain Source Current Sense for Boost FET (protection circuit)
3	GC1		O	A	Gate Driver Boost NMOS FET
4	GC2		O	A	Gate Driver Reverse Diode PMOS FET
5	CBA		I	A	Bootstrap Capacitor – Buck Controller A
6	GA1		O	A	Gate Driver – Buck Controller A
7	PHA		O	A	Phase Information – Buck Controller A
8	GA2		O	A	Gate Driver – Buck Controller A
9	PGNDA		O	Ground	Power Ground Buck Controller A
10	SA1		I	A	Current Sense – Buck Controller A
11	SA2		I	A	Current Sense – Buck Controller A
12	FBA		I	A	Feedback Buck Controller A
13	COMPA		O	A	Compensation Buck Controller A
14	SSA		O	A	Soft Start for BuckA
15	PGA	Pullup resistor	O	D	Power Good – Buck Controller A (internal pullup)
16	ENA	Pullup current	I	A	ENABLE – Buck Controller A
17	ENB	Pullup current	I	A	ENABLE – Buck Controller B
18	COMPC		O	A	Compensation for Boost controller
19	ENC	Pulldown resistor	I	D	Enable – Boost Controller, internal pulldown
20	SYNC	Pulldown resistor	I	D	Synchronization Pin, internal pulldown
21	DLYAB		O	A	Power Good Delay – Buck Controller A + B
22	RT		O	A	Oscillator Pin (external Resistor to adjust freq.)
23	AGND		O	Ground	Analog Ground Pin
24	PGB	Pullup resistor	O	D	Power Good – Buck Controller B (internal pullup)
25	SSB		O	A	Soft Start for BuckB
26	COMPB		O	A	Compensation Buck Controller B
27	FBB		I	A	Feedback Buck Controller B
28	SB2		I	A	Current Sense – Buck Controller B
29	SB1		I	A	Current Sense – Buck Controller B
30	PGNDB		O	Ground	Power Ground Buck Controller B
31	GB2		O	A	Gate Driver – Buck Controller B
32	PHB		O	A	Phase Information – Buck Controller B
33	GB1		O	A	Gate Driver – Buck Controller B
34	CBB		I	A	Bootstrap Capacitor – Buck Controller B
35	VREG		O	A	Internal Power Supply Filter Cap, not supposed to power external circuitry
36	DIV		I	D	Boost Output Voltage Seelction
37	EXTSUP		I	Power Supply	External input for Buck gate drive supply
38	VIN		I	Power Supply	Supply Voltage, output of Boost controller and input voltage for Buck controller

DETAILED DESCRIPTION

BUCK CONTROLLER

PWM Operation

The switch mode power supply (SMPS) operates in a fixed frequency adaptive on time control pulse width modulation (PWM). Switching frequency is set by an external resistor or synchronized from an external clock input. The architecture for the output control is a totem-pole. The synchronous top N-channel MOSFET is turned on, or is SET at the beginning of each cycle. This MOSFET is turned off, or is RESET when the PWM comparator resets the latch. Once the high external FET is turned OFF, and after a small delay (shoot-through delay) the low side external FET is turned ON until the inductor current starts to reverse or the start of the next cycle is imitated. The low side FET will override every fourth cycle for 5% of the duty cycle to enable the bootstrap capacitor to replenish its charge. Asa result, the maximum achievable duty cycle will be 98.75%. During dropout at the maximum duty cycle, the buck will switch at 1/4th the normal switching frequency:

Current Mode

The current mode control is a sequence, of monitoring the output voltage and fed back to the transconductance amplifier and comparing this to the internal reference of 0.8V (typical). The inductor peak current also resets the latch and is controlled by the error amplifier output voltage on COMPA or COMPB dependent on the respective converter. An increase in the load output current causes a slight decrease in the output voltage and this is reflected in the feedback voltage on FBX terminals. This increases the output voltage of the error amplifier on COMPA or COMPB dependent on the respective converter, until the average inductor current can support then new load current.

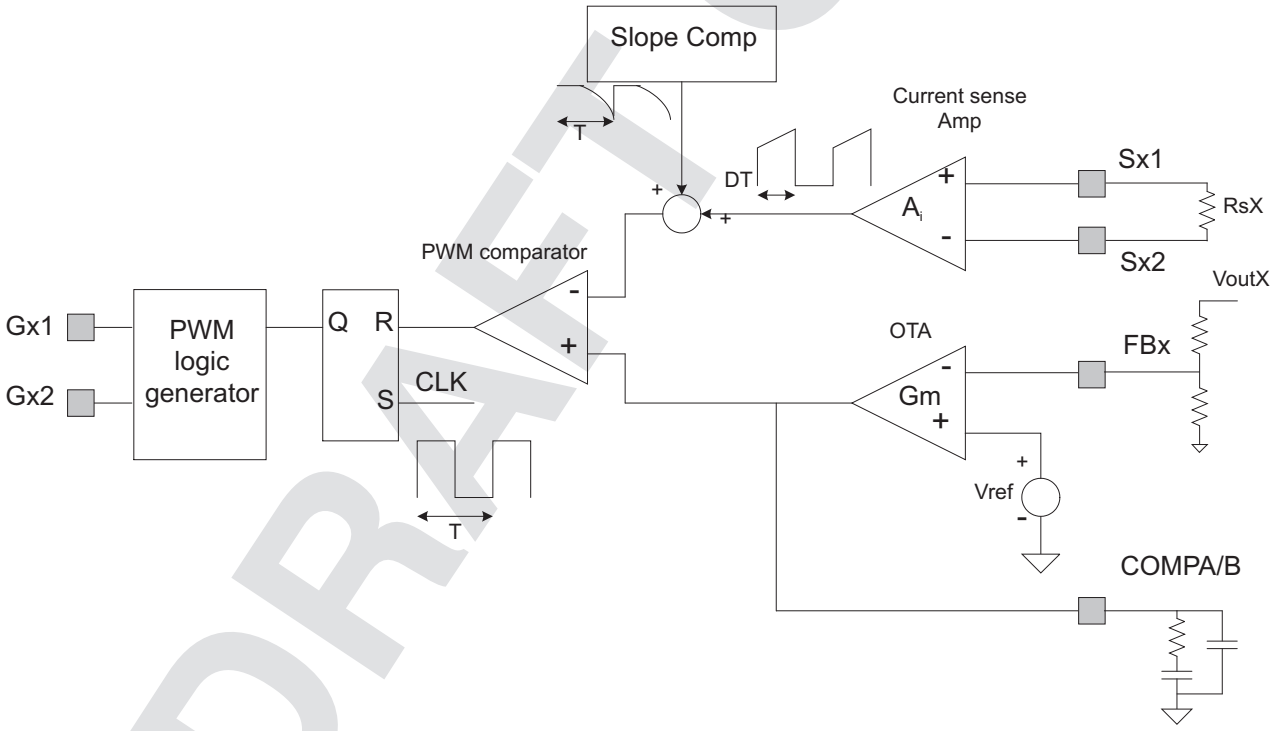


Figure 2. Current Mode Compensation

The Buck regulator converter has slope compensation implementation for stability with duty cycles greater than 50%. The current sense amplifier is summed with a corrective ramp generated at the start of every period. This is compared with the error amplifier output and the result is fed into a latch. The latched output controls the buffer driver for the external power switch.

The slope compensation is quadratic in nature. For optimal performance, inductor must be choseb to satisfy equation 1Equation 1.

$$\frac{L \times f_{SW}}{R_S} = 200 \quad (1)$$

Light Load PFM Mode

In Low Power PFM Mode the regulation topology is based on a Hysteretic Mode regulator. The voltage ripple on the output voltage is dependent on the external components. The top switch will be enabled to source current but the low side switch is disabled in this mode. This prevents the current from reversing and going negative, and the controller operates in discontinuous mode.

The following restrictions apply in LPM operation:

- Max duty cycle is 80% (exceeding this duty cycle causes the device to leave LPM)

Discontinuous mode (DCM) low-power mode (LPM) entry threshold is shown in Figure 3.

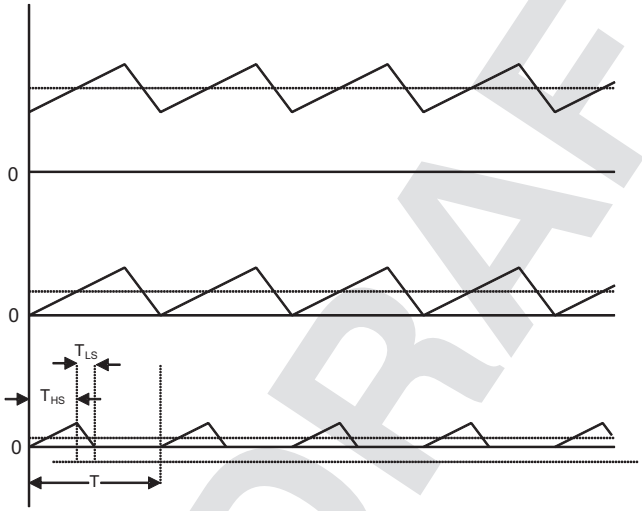


Figure 3. DCM Low-Power Mode

The criteria to enter low-power mode in DCM is shown in Equation 2, Equation 3, and Figure 4.

$$D^* = \frac{t_{HS} + t_{LS}}{t} \quad (2)$$

Where,

D* = 0.3 for specific number of cycles for the converter to enter low-power mode. The detection is carried out using a 10X clock internal to the device.

t_{HS} = On time for high side switch

t_{LS} = On time for low side switch

$$\frac{I_{LPM}}{I_{max}} = (D^*)^2 \frac{V_O \times (1 - \frac{V_O}{V_I})}{2 \times V_{SENSECL} \times K_{FL}} \quad (3)$$

Where,

I_{LPM} = Threshold for entry into low-power mode

I_{max} = Maximum output current

V_O = Output voltage

V_I = Input voltage

K_{FL} = Current sense transconductance

$V_{SENSECL}$ = Voltage threshold set for sense resistor to trip current limit

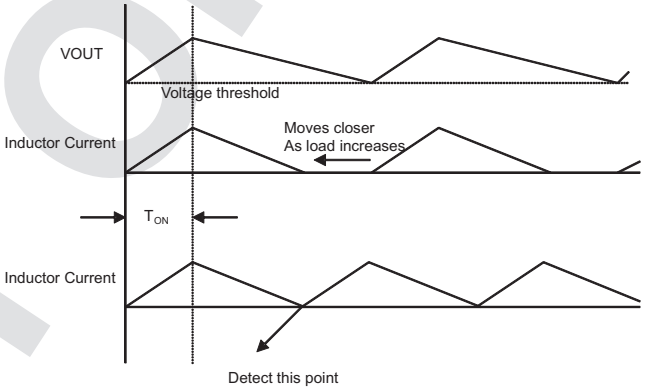


Figure 4. LPM Threshold

The control for low-power mode is based on output voltage VO and Inductor current. The tON is adaptive to load changes and detection of zero current in the inductor.

- The low-side FET is always OFF
- When VO falls below the threshold, the high-side FET is turned ON for a duration defined by VI and VO (see Equation 4).

$$t_{ON} = \frac{k}{V_I - V_O} \quad \text{(seconds)} \quad (4)$$

The criteria to exit low-power mode is shown in Equation 5.

$$\frac{I_{nom}}{I_{max}} = \frac{k \times f_{SW}}{2 \times V_{SENSECL} \times K_{FL}} \quad (5)$$

The low-power mode exit threshold is higher than the entry threshold; equating 5 and 7 for high VI gives Equation 6.

$$V_O \times (D^*)^2 = k \times f_{SW} \quad (6)$$

In discontinuous mode (DCM), the following assumptions are made to have LPM of 10% full average load current: Assume the peak ripple current in continuous conduction mode is 30% of full average load current.

$$I_{PK_{DCM}} = I_{PK_{ripple_{CCM}}} \times \frac{t_{ON}+t_{OFF}}{t} \quad (7)$$

$$I_{O_{avg_{DCM}}} = I_{PK_{DCM}} \times \frac{t_{ON}+t_{OFF}}{t} \quad (8)$$

$$I_{O_{avg_{DCM}}} = I_{PK_{ripple_{CCM}}} \times \frac{D^2}{2} \quad (9)$$

$$(D^*)^2 = \left(\frac{t_{ON}+t_{OFF}}{t}\right)^2 \quad (10)$$

$$I_{O_{avg_{DCM_{LPM}}}} = 0.1 \times I_{O_{avg_{CCM_{FullLoad}}}} = \frac{0.1}{0.3} \times I_{PK_{ripple_{CCM}}} = I_{PK_{ripple_{CCM}}} \times \frac{D^2}{2} \quad (11)$$

$$0.66 = (D_{LPM}^*)^2 \quad (12)$$

$$D_{LPM} = 0.8 \quad (13)$$

The lower boundary for exit threshold always higher than entry threshold. Higher boundary of exit threshold is less than 25% of maximum load current.

Internal-Regulator/External (EXTSUP) Power

Power supply for the source and sink circuitry which control the external power MOSFETs is derived from an internal regulator. This is an internal regulator powered from the VIN supply input or EXTSUP terminal. An external power supply can be supplied on the EXTSUP terminal, for when the system requires low power dissipation operation with higher range of the VIN supply, and regulation of the VBUCKX output.

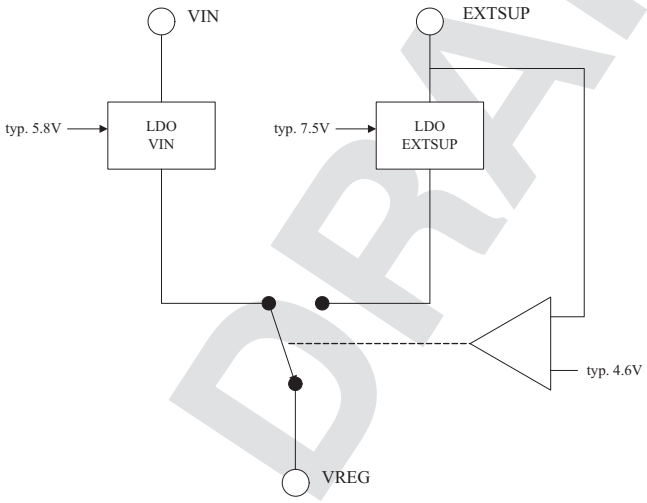


Figure 5. Internal Regulator Configuration

- If the EXTSUP terminal is open or less than 4.6V (typical), the internal regulator supplies VREG power from VIN. The internal regulator is a 5.8V supply (typically).
- If the EXTSUP terminal is above 4.6V (typically) the 5.8V regulator is turned OFF and a low drop out linear regulator is activated and supplies the VREG power from EXTSUP terminal.
- If the EXTSUP is less than 7.5V and greater than 4.6V, the 7.5V regulator is in drop out and the VREG supply is approximately equal to EXTSUP.

Power Good (PGA, PGB) and Delay Function (DLYAB)

The Power Good function (PGA and PGB) monitors their respective buck regulated output voltages (VBUCKA and VBUCKB). The operation is based on detecting when the output voltage of the respective regulator crosses the Power Good threshold PGthx.

The DLYAB terminal sets the frequency of an internal clock, which is used to count the delay period before the PGX terminals are asserted high.

$$f_{DLYAB} = 20 \times \frac{1}{t_{delay}} \quad (14)$$

Where,

$t_{delay} = 20/ f_{DLYAB} = C_{DLYAB} \times$ ms/nF

The programmable Reset delay will work independently for both Power Good Pins. Negative voltage dips on Buck Controller A and/or B (within the range of the adjusted power good delay) will not affect each other. Each power good pin will be released once the output voltage has recovered and once the set delay time is reached. The two power good function will operate independent for each output rail. The Reset delay timer setting is common to both supplies but with separate internal counters.

Buck Controller – Soft Start (SSA and SSB)

To limit the start-up inrush current, an internal soft start circuit is used to ramp up the soft start voltage from 0V to the internal device reference of 0.8V (typical). The initial start up for each controller is a function of an internal pull up current (1 µA typical) and the voltage ramp created by the capacitor on the SSX terminals. The switch duty cycle starts with narrow pulses and increases gradually as the soft start pin voltage ramps up. Each Buck controller has independent soft start circuitry. Alternatively the SSX terminals can be used to function as a tracking supply. This requires connecting the SSX pins through a resistor divider from the other supply to ground

$$\frac{\Delta V}{\Delta t} = \frac{I_{SS}}{C_{SS}} \times \frac{V}{s} \quad (15)$$

Where,

I_{SS} = 1 µA (typical)

ΔV = 0.8V

C_{SS} is the selected capacitor for the time required Δt

Enable VBUCKA and VBUCKB Controller (ENA and ENB)

These are digital input level thresholds for the two buck controller circuits. Forcing these terminals below 0.7V shuts down their respective buck converters in the application. These terminals are high voltage tolerant and can therefore be connected to voltages up to 36V for implementation of self bias from the main supply line. Both of these inputs have an internal pull up current of approximately 0.5 µA.

Bootstrap Capacitor Input (CBA and CBB)

These terminals are the bootstrap capacitor inputs for Buck switcher A and Buck switcher B respectively. These capacitors act as the voltage supply for the upper gate drive circuitry. The capacitors are re-charged on every low side synchronous switching action. In the case of 100% duty cycle for the upper FET, the device will automatically reduce the duty cycle to approximately 95% on every fifth cycle to allow these capacitors to re-charge.

Phase Reference for High-Side Bootstrap Supply (PHA and PHB)

These terminals provide a floating voltage reference for the high-side FET gate drive circuitry for switcher A and switcher B respectively. The phase input terminal is used to detect the reverse current in the converter using a second differential amplifier.

Current Sense BuckA and B (SX1 and SX2)

The current through the inductor is sensed by an external resistor. The current sense resistor nodes are fed into an internal differential amplifier for the respective Buck Regulators. The common mode range of the combined high-side and low-side current sense inputs supports the entire output voltage range.

Sense resistor selection for output current RsX = 75 mV/I_{OC}

The current sense amplifier A_I = 8.

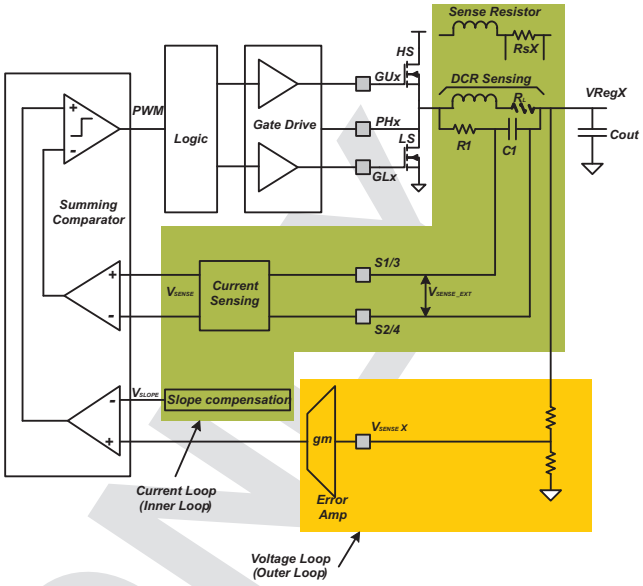


Figure 6. Over Current Sensing and Control

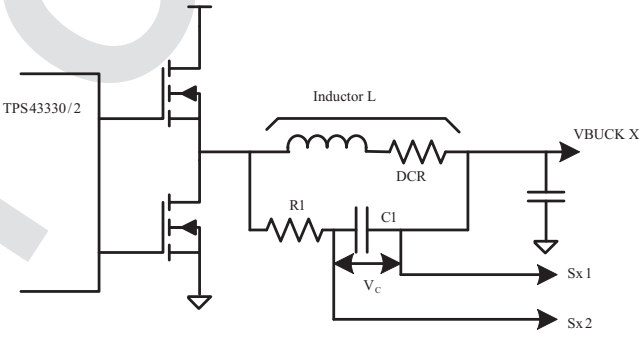


Figure 7. DCR Sensing Configuration

Inductor DCR Current Sense

This is a lossless current sense approach using the resistance of the inductor. The inductor consists of inductance L and resistance DCR with a time constant of the inductor given by L/DCR. Once these parameters are know then the value of R1 is chosen from Equation 16.

$$R1 = \frac{L}{DCR \times C1} \quad \text{(Ohms)} \tag{16}$$

The voltage V_C into the current sense amplifier of the TPS43330 is determined by Equation 17.

$$V_C = (V_I - V_O) \times \frac{V_O}{R1 \times C1 \times f_{SW} \times V_I} + I_{OC} \times DCR \quad \text{(Volts)} \tag{17}$$

From Equation 17 it can be seen that as the DC load increases the second term I_{OC} × DCR dominates and V_C is dependent on this term. The over current is set with V_C not to exceed 60 mV.

Regulated Output Sense Voltage Feedback (FBA and FBB)

These are the input pins for the voltage output feedback signals for buck regulator A and buck regulator B respectively. The external resistor network setting on these pins programs the desired regulated output voltages for each switch-mode converter. The output voltage setting is programmed with a resistor divider from VBUCKx to ground

$$VBUCKA=0.8V\times\left(1+\frac{R1}{R2}\right) \quad (18)$$

$$VBUCKB=0.8V\times\left(1+\frac{R3}{R4}\right) \quad (19)$$

Error Amplifier Outputs for VBUCKA and VBUCKB (COMPA and COMPB)

The error amplifier outputs are part of the switching regulator compensation nodes. The current comparator trip point for each of these channels is increased with the voltage on the error amplifier output

External Clock Input (SYNC)

This terminal is for external clock input for switching frequency synchronization of the buck converter. The external clock if present can over-ride the internal free running clock, by detecting TBD positive edges of consecutive pulses and synchronization to the external input signal. If the external clock input is removed, the system will synchronize to the internal clock signal of 400 kHz and low-power mode is allowed in this mode of operation. The regulators will operate with the external clock signal until the clock pulse is removed or the pin is open. The transition to the internal clock will be if there is a gap of TBD positive edge clock pulses. The boost controller will need a minimum of 6.5V to for startup operation. The VBAT has to be higher than the boost mode threshold to unlock the boost operation. Start up in boost mode is NOT possible until both conditions are satisfied.

Internal Clock (RT)

The operating switching frequency of the Buck regulators can be selected by the resistor value on the RT terminal. In this operation if there is an open circuit condition the switching frequency will default to 400kHz.

$$f_{SW}=\frac{X}{R7}(X=24k\Omega\times MHz)$$

$$f_{SW}=24\times\frac{10^{10}}{R7} \quad (20)$$

For example,

600kHz = 40 kΩ

400kHz =60 kΩ (R7 nom)

150kHz = 160 kΩ

BOOST CONTROLLER

During regular operating conditions the integrated Boost Controller is not active. The external components of the Boost converter act as filter at the input of a dual Buck Controller device. While the Boost Converter is not active the device will turn on an external MOS-FET in parallel to the diode of the Boost Converter in order to improve efficiency. The controller will need a minimum of 6.5V on the VIN input pin to start up operation. The Vbat has to be higher than the boost mode threshold to unlock the boost operation. Startup in boost mode is not possible until both conditions are satisfied.

Depending on the power consumption of the output voltages there can be large current ripples generated in Boost Mode. External Components need to be dimensioned accordingly and/or maximum time in Boost Mode has to be limited by the system. The boost controller will need a minimum of TBDV to start up the controller. The function of this circuitry is to maintain a constant input voltage to the TPS43330 device during low battery crank in a vehicle or when the boost controller is disabled and negative transient on the VIN input line occurs. Once the VIN line exceeds the setting for boost threshold (7V typical or 10V typical) the controller is disabled. During the boost operation the switching frequency of the converter is derived from the buck switching frequency divided by 2.

The voltage mode Boost Controller does includes a Drain-Sense monitor that will protect the external components form over current.

Output Voltage Selector for Boost Converter (DIV)

This terminal selects the output voltage set point of the Boost converter.

DIV = low → Boost converter Vout = 7V

DIV = open → Boost converter Vout = 10V

DIV = high → Boost converter Vout = 11V

Enable Boost Controller (ENC)

This is a digital input for the boost controller circuitry. Boost Controller is disabled with ENC = low and enabled with ENC = high. It has an internal pull-down resistor.

Boost Switch Drain Voltage Monitor (DS)

This terminal monitors the drain voltage of the low side boost regulator switch. If the voltage drop exceeds 0.2V typical the gate control voltage on GC1 is disabled (turns OFF the FET). This prevents the external FET from excessive power dissipation.

Current sensing configurations are shown in Figure 8 and Figure 9.

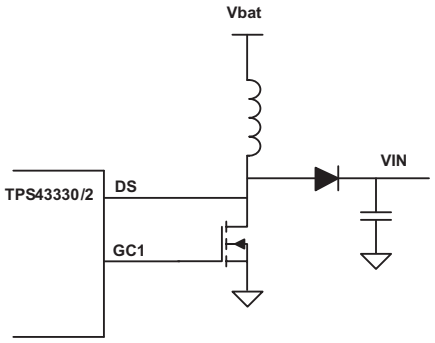


Figure 8. External Drain-Source Voltage Sensing

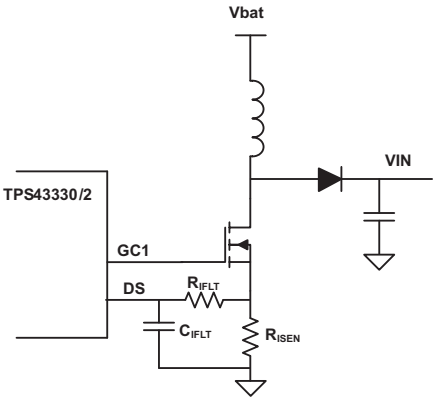


Figure 9. External Current Shunt Resistor

In method shown in Figure 8, the external FET must be capable of conducting currents up to $I = 0.225/R_{ds\ ON}$. In the method shown in Figure 9, the current is detected using an external shunt resistor in series with the FET. The current limit can be set by $I_{limit} = 0.225/R_{ISEN}$. Additional noise filter is required on the sensing terminal to improve the performance of the converter. These are components C_{ISEN} and R_{ISEN}, the values of these components are chosen such that the filter time is less than 0.1 of the normal pulse width of the converter.

The recommended time constant of filter is calculated by Equation 21.

$$R_{ISEN} \times C_{ISEN} < 0.1 \times t_{ON} \quad \text{(Typical range for RISEN = 1k}\Omega\text{ to 5k}\Omega\text{)} \tag{21}$$

Boost Converter Compensation (COMPC)

The error amplifier is a transconductance amplifier with the positive input connected to an internal reference of 0.8V and the negative input from a divider ratio of the input voltage. A compensation network is connected from the COMPC terminal to ground.

Thermal Shutdown

The TPS43330 protects itself from overheating with an internal thermal shutdown circuit. If the junction temperature exceeds the thermal shutdown trip point, the voltage reference is grounded and the all regulators are turned off. The part is restarted automatically when the junction temperature drops typically 15°C below the thermal shutdown trip point.

Frequency Hopping Spread Spectrum (FHSS) (TPS43332 Only)

The mode of operation is for the switching frequency to change from one value to another every cycle within a set boundary range of +/-5% of the fundemental switching frequency set. The implementation includes a 4-bit up/down counter which provides a random vector to set the charging current (up to 16 different current souces) of the capacitor which generates the ramp of the internal oscillator circuit. The pusedo random repeatability of the period is generated by a 12-bit linear feedback shift register, which allows different random sequences with a repeatability every 4096 cycles.

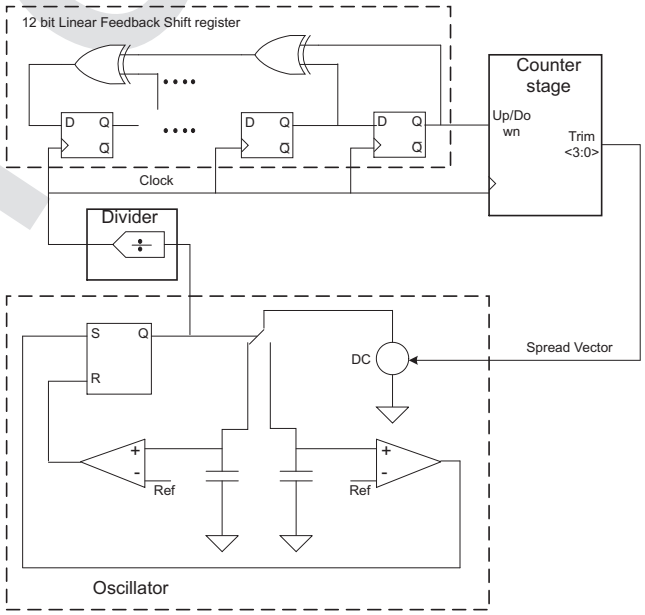


Figure 10. Frequency Hopping Control Logic

Table 1. Frequency Hopping Control

SPREAD SPECTRUM	SYNC TERMINAL	STATUS OF INTERNAL SPREAD SPECTRUM	COMMENTS
ON	External clock input	Not active	Can use external signal to do spread spectrum
ON	SYNC = Low	Not active	Device can enter discontinuous mode and enter PFM mode at light loads
ON	SYNC = High	Active	Operates in forced continuous mode
OFF	Don't care	Not Active	Default state on power up

Clock Frequency Set by Resistor on RT Terminal and Analog Modulation for Spread Spectrum

The resistor value on the RT terminal will set the clock frequency. An AC coupled signal on the RT to generate white noise approximately less than ±5% range of the set value.

Simplified Application Diagram

Two buck controllers with external NMOS-FET step down the battery voltage to two adjustable and independent output voltage rails. An integrated boost controller will boost the battery voltage for low voltage conditions (for example during cranking).

The buck controllers will always operate in a forced continuous conduction mode for SYNC = 1 or clock during normal operation. If low-power mode is enabled (SYNC = 0), the device can enter discontinuous conduction mode and transitions to PFM mode at light loads (hysteretic control loop).

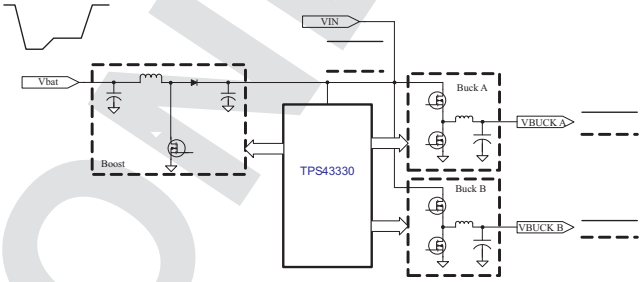


Figure 11. Simplified Block Diagram

Buck-Boost Configuration

The buck regulators operate in a synchronous mode with current mode control loop. This allows for improved performance during input line voltage excursions and achieves stable output voltage.

Common to both buck regulators:

- Reset delay timer setting (DLYAB)
- Oscillator frequency (RT)
- External synchronization (SYNC)
- Low power mode setting option (SYNC = low)

Independent for each channel:

- External compensation (COMPA and COMPB)
- Adjustable output voltage settings (FBA and FBB)
- Current limit (SA1, SA2 and SB1, SB2)
- Enable/inhibit (ENA and ENB)
- Soft start (SSA and SSB)
- Power good (PGA and PGB)

Each buck regulator is switched 180 degrees out of phase to minimize input ripple current. For reverse battery conditions, the body diode of the external boost converter NMOS-FET (Q5) in Figure 12 is conducting. The fuse (S1) in Figure 12 needs to be dimensioned to protect the external NMOS-FET (Q5) of the boost converter.

The boost converter is a voltage mode controller. It's designed for short boost cycles during battery voltage dips, for example during cranking. There is a separate PMOS-FET (Q6) gate driver which controls a FET in parallel to the diode (D1) of the boost circuit in order to reduce the power losses. The FET will be turned on during operation condition when the boost mode is not active. The boost converter will have two options to regulate the VIN input 7V and 10V through EEPROM setting.

Another option of reverse battery protection is shown in Figure 12.

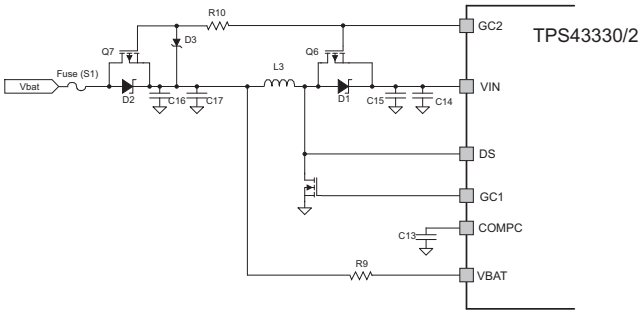


Figure 12. Reverse Battery Protection Option for Buck/Boost Configuration

The reverse battery protection diode (D2) protects the fuse (S1) and the pin VBAT. Power loss over the diode can be optimized by connecting a second PMOS-FET (Q7) in parallel.

Input Voltage / Car Battery Voltage

The Boost converter is activated when the input voltage falls below 7V typical (DIV=low). Operation in Boost will cause high RMS current for the input filter. To keep cost of external components low, boost mode operation should be limited by the system specification to a maximum time required by the cranking pulse. Otherwise components at the input need to be dimensioned accordingly.

Figure 13 represents the thresholds for input voltage falling after power up The input voltage must cross above the minimum Boost unlock threshold for the Boost to be activated.

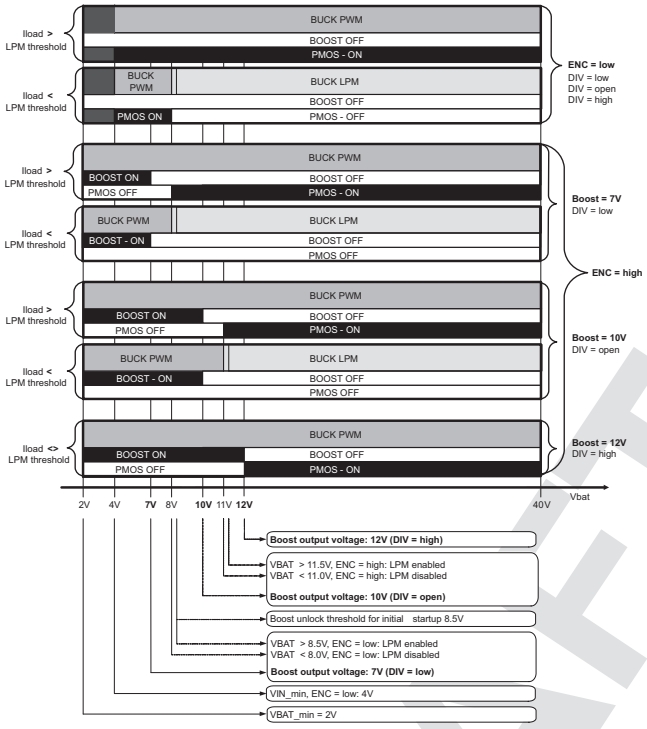


Figure 13. Operation Modes

Buck Controller

The buck converters are operation 180 degree out of phase in order to reduce the current ripple at the device input pin VIN. Operation of the buck controllers is independent of boost mode operation. If the boost converter is used, the output voltages will also remain stable during cranking pulses. The output terminals require filter capacitors with low ESR characteristics in order to minimize output ripple voltage.

Table 2. Mode of Operation

MODE OF OPERATION	DESCRIPTION
PWM mode	Current mode controller Source / sink mode operation (continuous conduction mode)
Low-power PFM mode	Hysteretic mode, with load current range TBD Source mode operation

Table 3. SYNC Pin Functionality

SYNC	DEVICE STATUS
Low	Buck controllers automatically switch between PWM and PFM mode operation depending on load current conditions Buck controllers enter PFM mode at light output load conditions → **Highest efficiency at light load conditions**
High	Buck controllers operate at internal oscillator frequency LPM inhibited → **Fixed switching frequency (400 kHz) also for light loads for noise control**
External synchronization signal	Buck controllers are synchronized to external frequency, look for consecutive edges within a specified time. LPM is inhibited.
Open	SYNC pin has an internal pulldown resistor, same behavior as described for 'Low'.

Buck Controller - Short Circuit Protection, Over Current Limit, and Fold Back Current

The two buck controllers have over current limit and short-circuit protection. The two sense pins for each Buck Controller monitor the current drop of an external current shunt in series with the output inductor.

Over current limit is a cycle by cycle peak current detection. If the current exceeds the programmed threshold, the high side switch is switched off the rest of the cycle.

A fold back current circuit is activated when the output voltage falls below 75% of the set value. The peak current limit is lowered proportional to the over current or short circuit condition. The fold back current limiting is enabled during soft start or tracking (providing the FBX voltage is keeping up with the SSX voltage) operation.

ENA and ENB terminals have internal pullups. SYNC and ENC terminals have internal pulldowns.

Table 4. Mode of Operation

ENABLE AND INHIBIT PINS				DEVICE STATUS		SYSTEM STATUS	QUIESCENT CURRENT (at light current loads)
ENA	ENB	ENC	SYNC	BUCK CONTROLLERS	BOOST CONTROLLER		
Low	Low	Low	X	Device shutdown	Boost disabled	Shutdown	~1 µA
Low	High		Low	BuckB running		BuckB: LPM enabled	~30 µA
			High			BuckB: LPM inhibited	mA range
High	Low		Low	BuckA running		BuckA: LPM enabled	~30 µA
			High			BuckA: LPM inhibited	mA range
High	High		Low	BuckA and BuckB running		BuckA/B: LPM enabled	~35 µA
			High			BuckA/B: LPM inhibited	mA range
Low	Low	High	X	Device shutdown	Boost disabled	Shutdown	~1 µA
Low	High		Low	BuckB running	Boost for Vbat < 7V (tbd)	BuckB: LPM enabled	~50 µA (no boost)
			High			BuckB: LPM inhibited	mA range (no boost)
High	Low		Low	BuckA running		BuckA: LPM enabled	~50 µA (no boost)
			High			BuckA: LPM inhibited	mA range (no boost)
High	High		Low	BuckA and BuckB running		BuckA/B: LPM enabled	~60 µA (no boost)
			High			BuckA/B: LPM inhibited	mA range (no boost)

External Voltage Supply (EXTSUP)

This pin is used in conjunction with external components for a capacitive charge pump circuit (see circuit below). This is required when the input voltage of the application is high and a low regulated output supply is required. This terminal can also be used to provide gate drive supply by another voltage source if available in the application (see application notes).

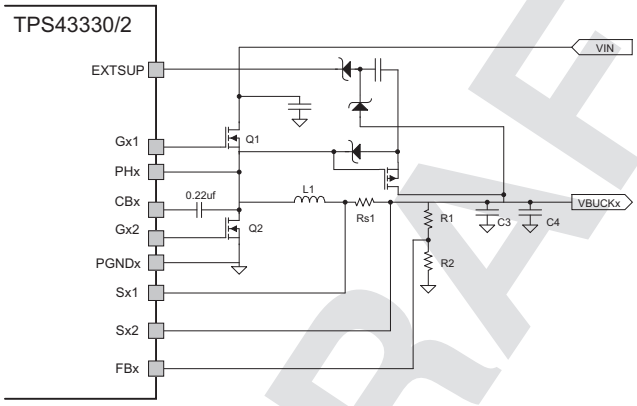


Figure 14. External Charge Pump

Under-Voltage Lockout

The TPS43330 incorporates an under voltage lockout circuit to keep the device disabled when the input voltage VIN is below the UVLO start voltage threshold. During power up, internal circuits are held inactive until VIN exceeds the UVLO start threshold voltage of 3.5V to 4V on VIN. Once the UVLO start threshold voltage is reached, device start-up begins. The initial start up voltage for the both the Buck and Boost mode operation is approximately 6.5V on the VIN terminal.

Over Voltage Shutdown Threshold

Above the over voltage threshold on VIN the buck converters will be disabled, when the condition is removed the converters will start up with a soft start sequence.

TYPICAL CHARACTERISTICS

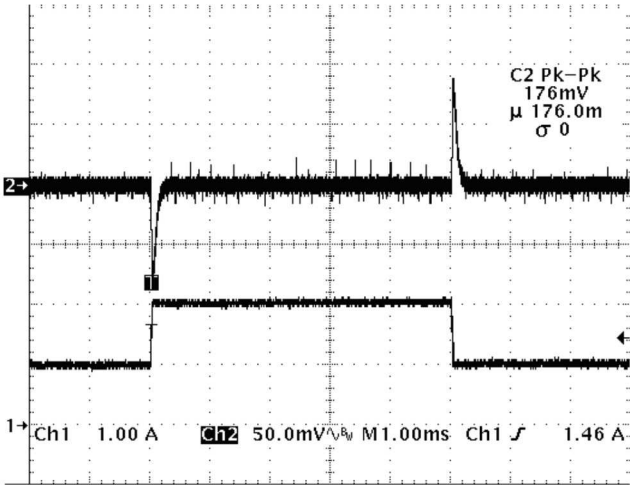


Figure 15. Load Transients in PWM Mode (VIN=12V, VBUCK A=5V)

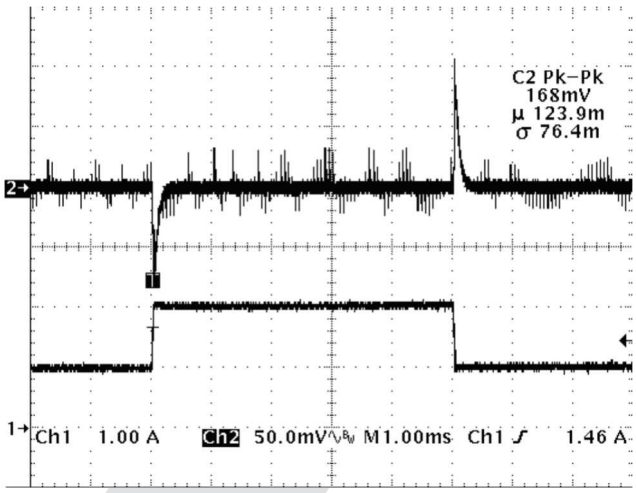


Figure 16. Load Transients in PWM Mode (VIN=12V, VBUCK B =3.3V)

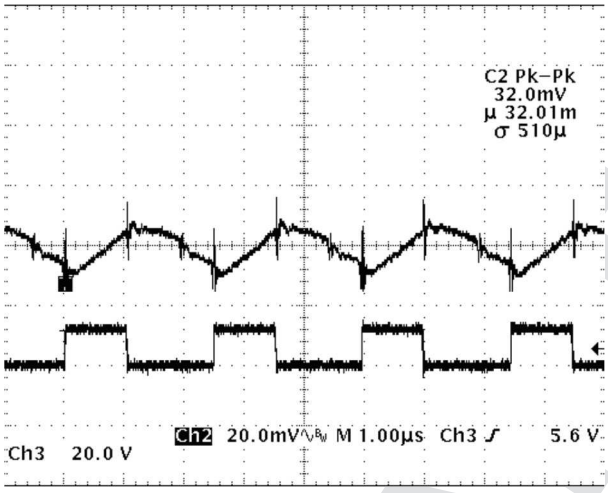


Figure 17. Output Voltage Ripple (VIN=12V, VBUCK A=5V)

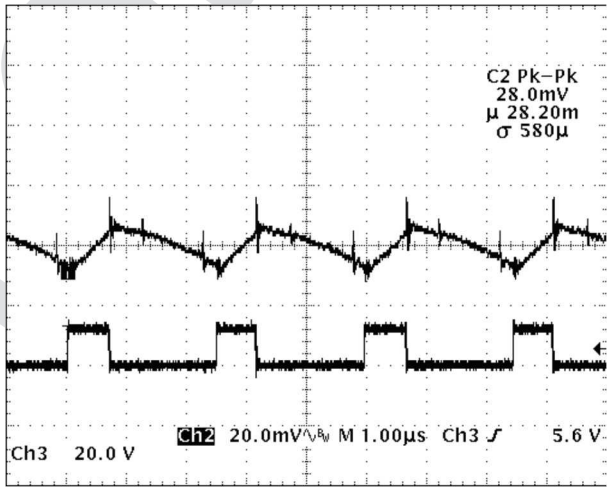


Figure 18. Output Voltage Ripple (VIN=12V, VBUCK B=3.3V)

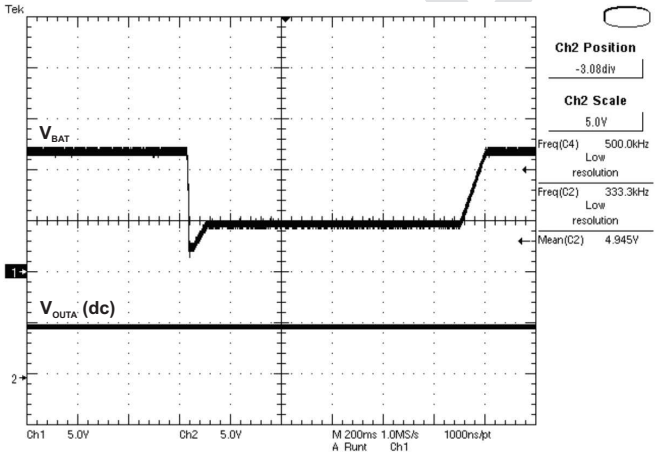


Figure 19. Cranking Pulse at Input (VBUCK A=5V)

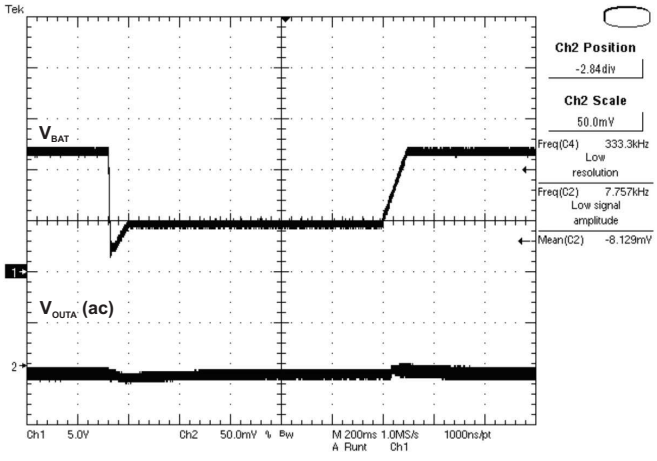


Figure 20. Cranking Pulse at Input Transient Response (VBUCK B=5V)

TYPICAL CHARACTERISTICS (continued)

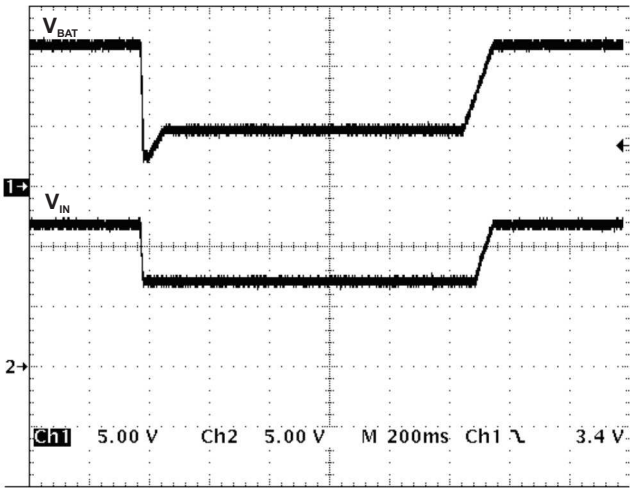


Figure 21. Cranking Pulse at Output Node of the Boost

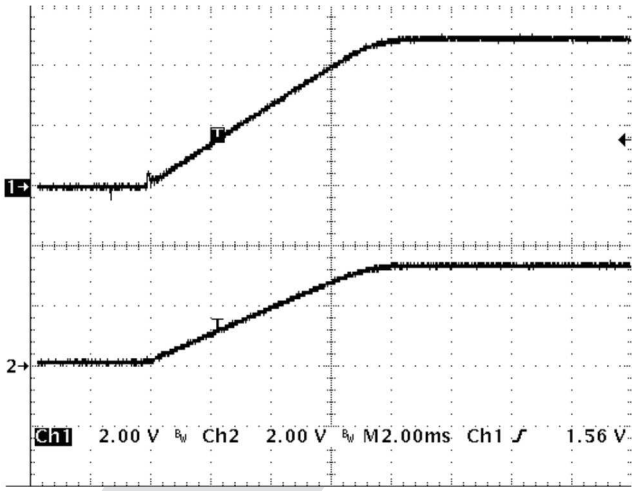


Figure 22. Soft Start-Up (VIN=12V, VBUCK X=3.3V, 5V)

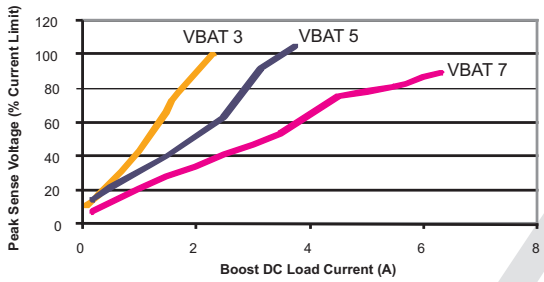


Figure 23. Peak current sense for Boost controller (VBAT at 3V, 5V, and 7V)

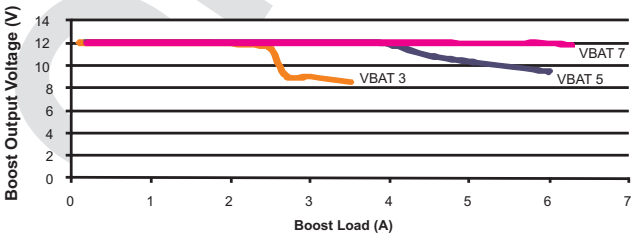


Figure 24. Output Current vs Different Input Voltages (VBAT at 3V, 5V, and 7V)

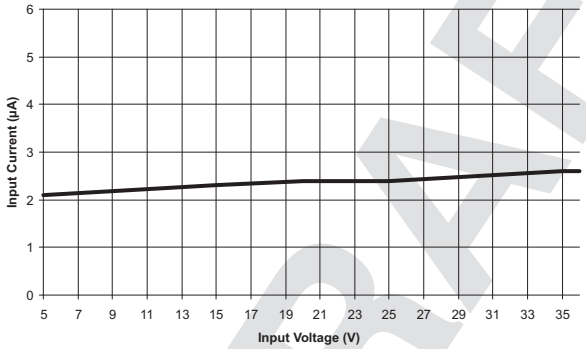


Figure 25. Shutdown Input Leakage Current vs Input Voltage VIN

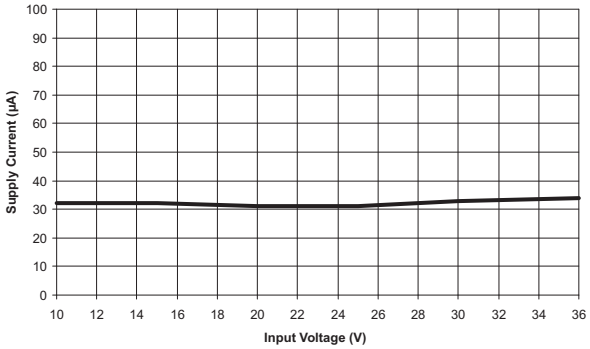


Figure 26. Quiescent Current vs Input Voltage VIN (VBUCK A Enabled)

TYPICAL CHARACTERISTICS (continued)

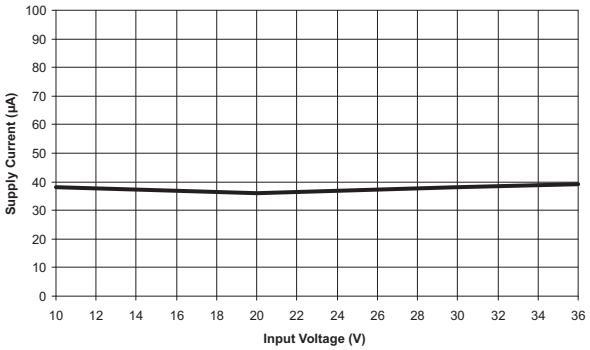


Figure 27. Quiescent Current vs Input Voltage VIN (VBUCK A and VBUCK B Enabled)

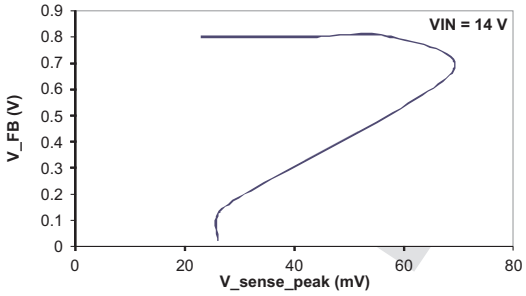


Figure 28. Buck Regulator Foldback Current Limit

APPLICATION INFORMATION

This is a starting point and theoretical representation of the values to be used for the application, further optimization of the components derived may be required to improve the performance of the device

Boost Converter

A Boost converter operating in continuous conduction mode (CCM) has a right-half-plane (RHP) zero with the transfer function. The RHP zero causes the converter to respond to a circuit disturbance in the opposite direction to that needed to support the output load transition (positive feedback). This complicates the loop compensation and limits the converter bandwidth, and requires an increase in the output filter capacitor.

The converter can de designed to operate in the discontinuous conduction mode (DCM) with a smaller inductance value of the inductor over the full range of the operating conditions. This may be difficult to achieve and other issues like instability may occur if the converter enters CCM.

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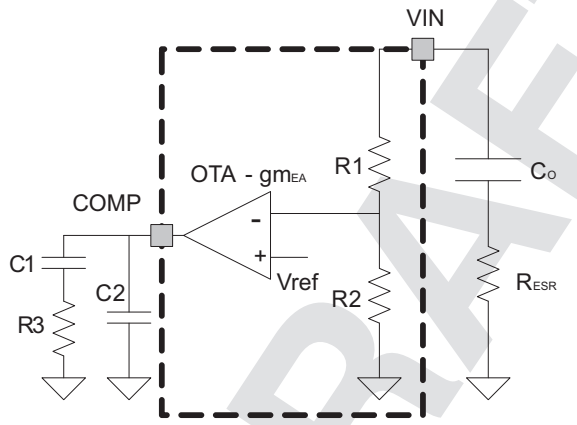

Figure 29. Compensation Circuit Components for Boost Controller

Where,

For 7V boost → R2 = 106kΩ (typical) and R1 = 821kΩ (typical)

For 10V boost → R2 = 106kΩ (typical) and R1 = 1.2MΩ (typical)

Discontinuous Conduction Mode (DCM operation)

The control to output transfer function for the boost in DCM has a single pole. The energy in the inductor is completely discharged during every switching cycle (inductor current is reduced to zero). The small inductor value for DCM compared to CCM operation will shift the RHP zero frequency close to the switching frequency, see Equation 22. In this mode the RHP is not a factor for compensation of the feedback loop, additionally the frequency of the pole associated with the inductor is also increased to a higher frequency derived from Equation 22.

Step 1: DCM Operation Inductor Selection

The maximum inductance to keep the boost converter running in DCM over the full operating range is given by Equation 22.

$$L_{max} = \frac{0.8 \times D_{CCM} \times (1-D_{CCM})^2 \times \left(\frac{V_O}{I_{Omax}}\right)}{2 \times f_{SW}} \quad \text{(Henries)} \tag{22}$$

Where,

$$D_{CCM} = 1 - \left(\frac{V_I}{V_O + V_D}\right) \tag{23}$$

V_O = Output Voltage

$I_{o\text{-}max}$ = Maximum Output Current

V_I = Minimum Input voltage

V_D = Forward voltage of Schottky diode

There are three elements of the output capacitor which contribute to the its impedance (output voltage ripple), the ESR, the ESL, and the capacitance.

Step 2: Duty Cycle in DCM

$$D_{DCM} = \frac{2(V_O + V_D) \times I_{Omax} \times f_{SW} \times L}{(V_I)^2} \tag{24}$$

Step 3: DCM Operation Output Capacitor C_O

During discontinuous conduction mode operation the minimum capacitance needed to limit the voltage ripple due to capacitor's capacitance is given by Equation 25.

$$C_{ODCM\text{-}min} \geq \frac{I_{Omax}\left(1 - \sqrt{\frac{2L}{R_{Lmin} \times t_S}}\right)}{f_{SW} \times \Delta V_O} \quad \text{(Farads)} \tag{25}$$

Where,

$R_{L\text{-}minimum}$ = minimum load resistance

t_s = clock period

f_{SW} = switching frequency

ΔV_O= output voltage ripple desired

The ESR of the output capacitor needed to limit the output ripple voltage is given by Equation 26.

$$ESR \le \frac{\Delta V_O}{\Delta I_O} \quad \text{(Ohms)} \tag{26}$$

Step 4: DCM Operation Input Capacitor C_I

$$C_{IN\text{-}DCM} = \frac{\Delta I_L \times D_{DCM}}{4 \times f_{SW} \times \Delta V_{ripple}} \quad \text{(Farads)} \tag{27}$$

Step 5: Input Current I_I

$$I_I = \frac{V_I}{2 \times L \times f_{SW}} \times D_{DCM}^2 \times I_O \quad \text{(Amps)} \tag{28}$$

Continuous Conduction Mode (CCM) Operation

In continuous conduction mode of operation the RHP zero complicates the loop compensation. This will limit the bandwidth of the converter and may require a larger value output filter capacitor to compensate for loop response. The benefit of this mode is a lower switch and inductor current compared to the DCM. This results in a reduced power dissipation and size of the power switch, input capacitor and output capacitor. May be necessary to increase the output filter capacitor value such that $f_{LC} \le f_{RHP}$.

Step 6: Duty Cycle in CCM

$$D_{DCM} = 1 - \frac{V_I}{V_O + V_D} \tag{29}$$

Step 7: CCM Operation Output Capacitor Selection

The minimum output capacitor required for a desired output ripple voltage is given by Equation 30.

$$C_{CCMmin} \ge \frac{I_{Omax}}{\Delta V_O} \times \left(1 - \frac{V_{IN}}{V_O}\right) \times \frac{1}{f_{SW}} \quad \text{(Farads)} \tag{30}$$

Step 8: CCM Operation Input Capacitor Selection

The minimum input capacitor required for a desired output ripple voltage is given by Equation 31.

$$C_{IN\text{-}CCM} = \frac{0.25 \times \Delta I_{Omax}}{f_{SW} \times \Delta V_{Iripple}} \quad \text{(Farads)} \tag{31}$$

Step 9: CCM Operation Inductor Selection

The minimum inductor value needed to ensure CCM from maximum to 25% of maximum load is determined by choosing value of the inductor to have a ripple current of approximately 40% of the maximum output load current at maximum input voltage of the system.

$$\Delta I_L = 0.4 \times I_O \quad \text{(Amps) for } V_{INmax} \tag{32}$$

To maintain CCM operation choose minimum load current $I_{O\text{-}DCM}$ for this operation.

The inductor value is given by Equation 33.

$$L = \frac{V_{IN}}{2 \times I_{O\text{-}DCM} \times f_{SW}} \times D_{CCM} \times (1 - D_{CCM}) \quad \text{(Henries)} \tag{33}$$

Where,

VIN = Typical operating voltage

Choosing an inductor value less than the one determined by Equation 33 may cause the converter to go into DCM operation during low output currents. This may not be a problem if the loop compensation allows for good phase margin.

The ripple current flowing through the output capacitor's ESR causes power dissipation in the capacitor. Equation 34 gives the RMS value of the ripple current flowing through the output capacitance.

$$I_{C\text{-}RMS} = I_O \times \sqrt{\frac{D}{1-D}} \quad \text{(Amps)} \tag{34}$$

Continuous inductor current mode operation, the ESR needed to limit the ripple voltage to ΔV_O volts peak-peak is:

$$ESR \le \frac{\Delta V_O}{\left(\frac{I_{Omax}}{1 - D_{max}} + \frac{\Delta I_L}{2}\right)} \quad \text{(Ohms)} \tag{35}$$

Input current for CCM is given by Equation 36.

$$I_I = \frac{I_O}{1-D} \quad \text{(Amps)} \tag{36}$$

Current Sensing and Over Current Protection

The internal current sense threshold is 0.2V. The peak converter current is TBD.

Step 10: CCM Operation Loop Frequency Compensation

Use the following guidelines to set the frequency poles, zeroes and crossover values:

- Crossover frequency at unity gain $f_c = f_{SW}/5$ or $f_{RHP}/3$ which ever is the lower of the two values
- Select the zero $f_z = f_c/10$
- Make the second pole $f_{P2} > 10 \times f_c$ (optional)

$$f_{LC} = 0.1 \times f_{RHP\text{-}Zero} \quad \text{(Hz)} \tag{37}$$

$$\frac{f_{RHP\text{-}Zero}}{f_{LC}} \ge M \tag{38}$$

The following requirements for compensating the loop have to be satisfied for the control-to-output gain of a CCM boost operation.

Where,

M = 10 for tantalum output capacitors

M = 15 for ceramic output capacitors

$$R3 = \frac{B}{Gm} \times \frac{R1+R2}{R2} \quad \text{(Ohms)} \tag{39}$$

Where,

B = 3.3V/V (gain of 10dB) at the desired f_Z
Gm = Transconductance of the amplifier

$$C1=\frac{1}{2\pi\times f_{P1}\times R3} \quad (Hz) \tag{40}$$

$$C2=\frac{1}{2\pi\times 0.1\times f_C\times R3} \quad (Hz) \tag{41}$$

$$f_C=0.33\times f_{RHP\text{-}Zero} \quad (Hz) \tag{42}$$

$$f_{LC}=\frac{1}{2\pi\sqrt{LC_O}}\times\frac{V_{IN}}{V_O} \quad (Hz) \tag{43}$$

Where,

L = Inductor value
C_O = Output capacitor
V_{IN} = Input voltage
V_O = Output voltage

$$f_{RHP\text{-}Zero}=\frac{RLmin}{2\pi L}\times\left(\frac{V_{IN}}{V_O}\right)^2 \quad (Hz) \tag{44}$$

$$f_{ESR}=\frac{1}{2\pi\times C_O\times R_{ESR}} \quad (Hz) \tag{45}$$

The compensation network (see Figure 30) is calculated using Equation 46 through Equation 48.

$$f_{P1}=\frac{1}{2\pi\times C1\times R_{EA}} \quad (Hz) \tag{46}$$

$$f_{P2}=\frac{1}{2\pi\times C2\times R3} \quad (Hz) \tag{47}$$

$$f_Z=\frac{1}{2\pi\times C1\times R3} \quad (Hz) \tag{48}$$

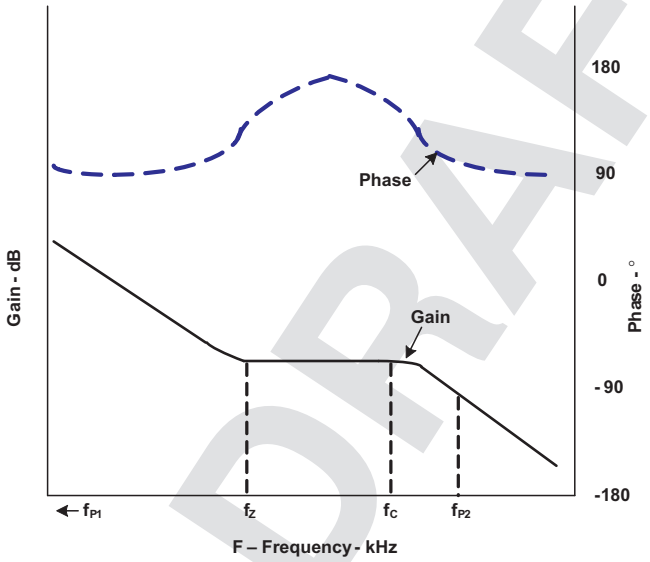

Figure 30. Boost Converter Loop Compensation for Stability Criteria

The Bode-Plot in Figure 30 is an illustration of stability criteria and is used to ensure converter performance based on the type of loop compensation implemented

BUCK CONTROLLER

Step 1: Maximum and Minimum Duty Cycles

$$D_{max}=\frac{V_O}{V_{I_{min}}} \tag{49}$$

$$D_{min}=\frac{V_O}{V_{I_{max}}} \tag{50}$$

Step2: Selection of Current Sensing Resistor

$$\text{Current sense resistor}=R_S=\frac{0.075}{1.25\times I_{Omax}} \quad (Ohms) \tag{51}$$

Step 3: Selection of Inductor

The following things must be considered when selecting the value of the inductor for the application.

Benefits of Low Inductor value

- Low inductor value gives high di/dt, which allows for fewer output capacitors for good load transient response
- Gives higher saturation current for the core due to fewer tunrs
- Fewer turns yields low DCR and therefore less DC inductor losses in the windings
- High di/dt provides faster response to load steps

Benefits of High Inductor value

- Low ripple current leads to lower conduction losses in MOSFETs
- Low ripple; means lower RMS ripple current for capaciotrs
- Low ripple; yeilds low AC inductor losses in the core (flux) and windings (skin effect)
- Low ripple; gives contineous inductor current flow over a wide load range

Factoring in the slope quadaratic compensation, the following equation is used to determine the recommeded inductor value for the converters.

$$L=K_{FLR}\times\frac{R_S}{f_{SW}} \quad (Henries) \tag{52}$$

Where ,

R_S = Current sense resistor
f_{SW} = Converter switching frequency
K_{FLR} = Coil selection constant = 200

Step 4: Ripple Current based on Inductor Chosen

$$\Delta I_{Lripple}=\frac{V_O}{f_{SW}\times L}\times\left(1-\frac{V_O}{V_I}\right) \quad (Amps) \tag{53}$$

Where,

V_I = Input voltage

ΔI_{L_ripple} = Inductor ripple current peak to peak (typically 20% to 40% of maximum load current)

f_{SW} = Converter switching frequency

V_O = Output voltage

L = Inductor value

The inductor RMS current is given by Equation 54.

$$\Delta I_{Lrms} = \sqrt{I_O^2 + \frac{1}{12}\left(\frac{V_O \times (V_I - V_O)}{V_I \times L \times f_{SW}}\right)^2} \quad \text{(Amps)} \tag{54}$$

Step 5: Selection of Output Capacitor C_O

The selection of the output capacitor will determine several parameters in the operation of the converter, the modulator pole, voltage droop on the out capacitor and the output ripple. During a load step from no load to full load or changes in the input voltage, the output capacitor must hold up the output voltage above a certain level for a specified time and NOT issue a reset, until the main regulator control loop responds to the change. The droop on the output voltage can be determine by Equation 56. The capacitance value determines the modulator pole and the roll off frequency due to the LC output filter double pole The output ripple voltage is a product of the output capacitor ESR and ripple current (see Equation 58).

Using Equation 55, the minimum capacitance needed to maintain desired output voltage during high to low load transition and prevent over shoot.

$$C_O > \frac{L \times \left(I_{Omax}^2 - I_{Omin}^2\right)}{V_{Omax}^2 - V_{Omin}^2} \quad \text{(Farads)} \tag{55}$$

Where,

$I_{o\text{-}max}$ is maximum output current

$I_{o\text{-}min}$ is minimum output current

The difference between the output current maximum to minimum is the worst case load step in the system

$V_{o\text{-}max}$ is maximum tolerance of regulated output voltage

$V_{o\text{-}min}$ is the minimum tolerance of regulated output voltage

Minimum capacitance needed for transient load response, using Equation 56.

$$C_O = \frac{2 \times \Delta I_O}{f_{SW} \times \Delta V_O} \quad \text{(Farads)} \tag{56}$$

Minimum capacitance needed for output voltage ripple ΔVO specification, using Equation 57.

$$C_O > \frac{1}{8 \times f_{SW}} \times \frac{1}{\left(\frac{V_{Oripple}}{I_{ripple}}\right)} \quad \text{(Farads)} \tag{57}$$

The most critical condition based on the calculations above indicates that the output capacitance has to be a minimum of 33 µF to keep the output voltage in regulation during load transients.

Additional capacitance de- ratings for temperature, aging and dc bias has to be factored, and so a value of 100 µF with ESR calculated using Equation 58 of less than 100mΩ should be used on the output stage.

Maximum ESR of the out capacitor based on output ripple voltage specification.

$$R_{ESR} < \frac{V_{Oripple}}{I_{ripple}} \quad \text{(Ohms)} \tag{58}$$

Output capacitor root mean square (RMS) ripple current. This is to prevent excess heating or failure due to high ripple currents. This parameter is sometimes specified by the manufacturer.

$$I_{O\text{-}RMS} = \frac{V_{OUT}(V_{Imax} - V_O)}{\sqrt{12} \times V_{Imax} \times L_O \times f_{SW}} \quad \text{(Amps)} \tag{59}$$

Physical size, cost, temperature and voltage characteristics are also important considerations and will depend on the type of capacitor you use. The chose of output capacitance and their repsective dielectric material is important when designing the converter.

The highest dielectric constants (Z5U and Y5V) exhibit the most variation in capacitance with dc voltage and temperature. The Y5V are available in larger values but lose 75% of the capacitance at the full dc voltage rating. The X7R and X5R show more variation than NPO but less than Y5V and have a good selection of small size, higher value capacitors. The capacitors with X5R dielectric lose 20% of capacitance at about 80% of the dc voltage rating. The X7R dielectric loses 10% of capacitance.

Step 6: Input Capacitor C_{IN}

The TPS43330 requires an input ceramic de-coupling capacitor type X5R or X7R and bulk capacitance to minimize input ripple voltage on each Buck Regulator input supply. The dc voltage rating of this input capacitance must be greater than the maximum input voltage. The capacitor must have an input ripple current rating higher than the maximum input ripple current of the converter for the application; this is determined by Equation 60.

The input capacitors for power regulators are chosen to have reasonable capacitance to volume ratio and fairly stable over temperature. The value of the input capacitance also determines the input ripple voltage of the regulator, shown by Equation 61.

$$I_{I\text{-}RMS} = I_O \times \sqrt{\frac{V_O}{V_{Imin}} \times \frac{V_{Imin} - V_O}{V_{Imin}}} \quad \text{(Amps)} \tag{60}$$

$$C_{IN} = \frac{0.25 \times \Delta I_{Omax}}{f_{SW} \times \Delta V_I} \quad \text{(Farads)} \tag{61}$$

Where,

ΔV_I = Input voltage ripple desired

Step 7: Soft Start Capacitor C_{SS}

The soft start capacitor determines the minimum time to reach the desired output voltage during a power up cycle. This is useful when a load requires a controlled voltage slew rate and helps to limit the current draw from the input voltage supply line. Equation 62 has to be satisfied in addition to the other conditions stated in the soft start section of this document.

$$C_{SS} = \frac{I_{SS} \times \Delta t}{\Delta V} \quad \text{(Farads)} \tag{62}$$

Where,

I_{SS} = 1 µA (typical)

C_{SS} = selected capacitor

ΔV = 0.8V (typical)

Δt = soft start time required

Step 8: Bootstrap Capacitor Selection C_{Boot}

$$C_{Boot} = \frac{Q_g}{\Delta V} \quad \text{(Farads)} \tag{63}$$

A CBoot ceramic capacitor must be connected between the PH and BOOT terminals for the converter to operate and regulate the desired output voltage. It is recommended to use a capacitor with X5R or better grade dielectric material and the voltage rating on this capacitor of at least 25V to allow for de rating.

Step 9: Current Loop Compensation (Buck Regulator Controller Buck 1 and Buck 2)

Small Signal Model for Frequency Compensation

The TPS43330 uses a transconductance amplifier for the error amplifier which supports three of the commonly used frequency compensation circuits. These compensation circuits are shown below as Type 2A, 2B, and 1. The Type 2 circuits most likely implemented in high bandwidth power supply designs using low ESR output capacitors. The Type 1 circuit will be used with power supply designs with high ESR output capacitors (RESR).

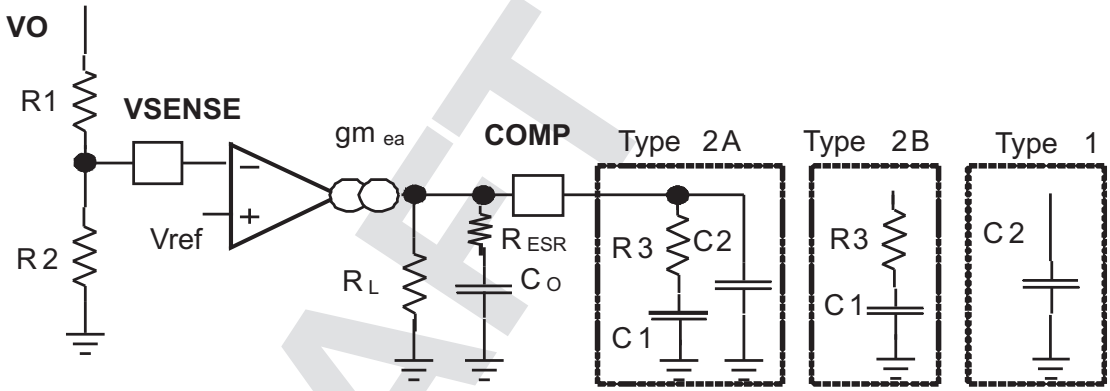

Figure 31. Buck Converter Loop Compensation Components

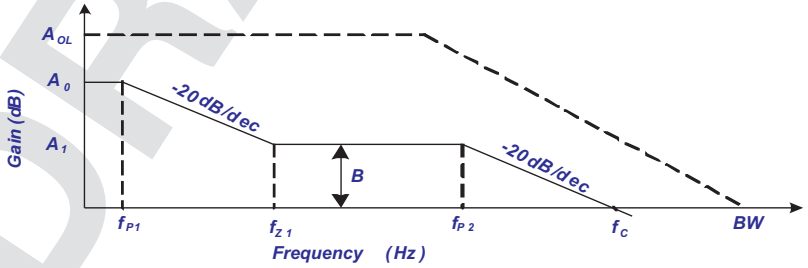

Figure 32. Frequency Response of the Type 2A and 2B Frequency Compensation

The higher the bandwidth the faster the load transient response. It is recommeded to place a pole at low frequency, The following are the basic loop compensation guidelines:

-
- In a loop response compensation it is desirable to have the crossover frequency at one-fifth of the switching frquency. $f_C < f_{SW} / 5$, but can be $f_{SW} / 20$ for highest switching frequency.
- Loop gain slope of -20dB/decade
- The first pole f_{P1} should be close to 0 Hz, so low frequency gain will be relatively high and help with dc regulation with load and line regulation.
- The first zero f_{Z1} should be at the first control loop pole [zero 1 compensation at $f_Z = 1 / (2\pi\sqrt{LC_O})$].
- The second pole at fP2 (pole 2 compensation at fZ1), created by capacitor C2, [pole 2 at $f_{P2} = 1 / (2\pi \times C_O \times R_{ESR})$].

The crossover frequency must be such that the error amplifier gain is high enough to allow propoer compenastion. Use Equation 64 through Equation 66 as a starting poingt to dertermine the crossover frequency. Use the lower value from the calaculations for an initial crossover frequency f_C

$$f_C = \sqrt{f_{P1} \times f_{P2}} \quad \text{(Hz)} \tag{64}$$

$$f_C = \sqrt{f_{P1} \times \frac{f_{SW}}{2}} \quad \text{(Hz)} \tag{65}$$

$$f_C \le \frac{f_{SW}}{5} \quad \text{(Hz) for all cases} \tag{66}$$

Once the crossover frequency is determined the gain of the modulator at this frequency f_C is given by Equation 67.

$$G_{mod\text{-}f_C} = \frac{6.6 \times R_L \times (2\pi \times f_C \times C_O \times R_{ESR} + 1)}{2\pi \times f_C \times C_O \times (I_L + R_{ESR}) + 1} \quad \text{(dB)} \tag{67}$$

Current loop transconductance is given by Equation 68.

$$K_{CFB} = \frac{1}{A_I \times R_S} \tag{68}$$

Where,

A_I = Current sense amplifier gain = 8 (for TPS43340)

R_S = Current sense resistor = 0.075 /(1.25 * $I_{O\ max}$)

Voltage divider gain beta is given by Equation 69.

$$\beta = \frac{V_{ref}}{V_O} \tag{69}$$

Where,

V_{ref} = Internal reference voltage (For TPS43340 = 0.8V)

V_O = Output voltage

Gain bandwith of converter (GBW) is given by Equation 70.

$$R3 = \frac{GBW \times 2\pi \times C_O}{Gm \times K_{CFB} \times \beta} \quad \text{(Ohms)} \tag{70}$$

Where,

GBW = The gain bandwidth. Typically the gain bandwidth is between 1/5 to 1/20 of the f_{SW} to cover the range of the switching frequencies.

gm = transconductance of error amplifier

K_{CFB} = Current loop transcondutance

C_O = Output capacitance

$$C1 = \frac{1}{2\pi \times R3 \times 0.1 \times GBW} \quad \text{(Farads)} \tag{71}$$

$$C2 = \frac{1}{\pi \times R3 \times f_{SW}} \quad \text{(Farads)} \tag{72}$$

$$A_0 = Gm_{ea} \times R_L \times \frac{R2}{R1+R2} \quad \text{(V/V)} \tag{73}$$

$$A_1 = Gm_{ea} \times \frac{R_L \times R3}{R_L + R3} \times \frac{R2}{R1+R2} \quad \text{(V/V)} \tag{74}$$

$$f_{P1} = \frac{1}{2\pi \times C_O \times R_L} + \frac{1\text{-}D\text{-}0.5}{2\pi \times L \times f_{SW} \times C_O} \quad \text{(Hz)} \tag{75}$$

$$f_{Z1} = \frac{1}{2\pi \times C1 \times R3} \quad \text{(Hz)} \tag{76}$$

$$f_{P2} = \frac{1}{2\pi \times C2 \times R3} \quad \text{(Hz) Type 2a} \tag{77}$$

$$f_{P2} = \frac{1}{2\pi \times C_O \times \frac{R3+R_L}{R3 \times R_L}} \quad \text{(Hz) Type 2a} \tag{78}$$

$$f_{P2} = \frac{1}{(2\pi \times C_O + C2) \times R_L} \quad \text{(Hz) Type 1} \tag{79}$$

Design Equations

	VBUCKA, VBUCKB	BOOST	COMMENTS
Duty Cycle D. (VBUCK A, B) - Eq.45 Boost CCM - Eq. 23 Boost DCM - Eq. 24	$D=\frac{V_O}{V_I}$	$D_{CCM}=1-\left(\frac{V_I}{V_O+V_D}\right)$ $D_{DCM}=\frac{2(V_O+V_D)\times I_{Omax}\times f_{SW}\times L}{(V_I)^2}$	
Current limit sense resistor R_S - 51	$R_S=\frac{0.075}{1.25\times I_{Omin}}$	$\frac{0.225}{R_{dsON}}$ (Vds sensing) $\frac{0.225}{R_{ISEN}}$ (External sense resistor)	Chose current limit of 25% more than maximum load
Inductor selection L. (VBUCK A, B) - Eq. 52 Boost CCM - Eq. 33 Boost DCM - Eq. 22	$L=\frac{200}{f_{SW}}\times R_S$	$L=\frac{V_{IN}}{2\times I_{O\text{-}DCM}\times f_{SW}}\times D_{CCM}\times(1\text{-}D_{CCM})$ (Henries) $L_{max}=\frac{0.8\times D_{CCM}\times(1\text{-}D_{CCM})^2\times\left(\frac{V_O}{I_{Omax}}\right)}{2\times f_{SW}}$ (Henries)	VBUCK A and VBUCK B, Rs is chosen based on current limit set for the application. Boost operation chose desired mode of DCM or CCM equation for inductor selection
Indcutor ripple current. (VBUCK A, B) - Eq. 53 Boost - Eq. 32	$\Delta I_{Lripple}=\frac{V_O}{f_{SW}\times L}\times\left(1-\frac{V_O}{V_I}\right)$ (Amps)	$\Delta I_L=0.4\times I_O$ (Amps) for V_{INmax}	Typically the inductor ripple current is ± 20% of maximum load current
Output capactior C_O. (VBUCK A, B) - Eq. 56 Boost CCM – Eq. 30 Boost DCM – Eq. 25	$C_O=\frac{2\times\Delta I_O}{f_{SW}\times\Delta V_O}$ (Farads)	$C_{CCMmin}\geq\frac{I_{Omax}}{\Delta V_O}\times\left(1-\frac{V_{IN}}{V_O}\right)\times\frac{1}{f_{SW}}$ (Farads) $C_{ODCM\text{-}min}\geq\frac{I_{Omax}\left(1-\sqrt{\frac{2L}{R_{Lmin}\times t_S}}\right)}{f_{SW}\times\Delta V_O}$ (Farads)	Ensure the ESR of the output capacitor is based on output voltage ripple due to load steps
Input capacitor C_{IN}. (VBUCK A, B) - Eq. 61 Boost CCM -Eq. 31 Boost DCM - Eq. 27	$C_{IN}=\frac{0.25\times\Delta I_{Omax}}{f_{SW}\times\Delta V_I}$ (Farads)	$C_{IN\text{-}CCM}=\frac{0.25\times\Delta I_{Omax}}{f_{SW}\times\Delta V_{Iripple}}$ (Farads) $C_{IN\text{-}DCM}=\frac{\Delta I_L\times D_{DCM}}{4\times f_{SW}\times\Delta V_{ripple}}$ (Farads)	Based Input capacitor value on input voltage ripple desired
Soft start C_{SS}. - Eq. 62	$C_{SS}=\frac{I_{SS}\times\Delta t}{\Delta V}$ (Farads)	$C_{SS}=\frac{I_{SS}\times\Delta t}{\Delta V}$ (Farads)	Chose the soft start time required Δt and then calculate C_{SS}
Bootstrap capacitor C_{Boot}. - Eq. 63	$C_{Boot}=\frac{Q_g}{\Delta V}$ (Farads)	$C_{Boot}=\frac{Q_g}{\Delta V}$ (Farads)	Chose the amount of ripple based on FET gate charge and opearting VIN
Compensation resistor for pole. (VBUCK A, B) - Eq. 70 Boost - Eq. 39	$R3=\frac{GBW\times2\pi\times C_O}{Gm\times K_{CFB}\times\beta}$ (Ohms)	$R3=\frac{B}{Gm}\times\frac{R1+R2}{R2}$ (Ohms)	To determine resistor R3 assume GBW ≈ $f_{SW}/5$ to $f_{SW}/20$ over the frequency range for buck controller
Compensation capacitor for zero. (VBUCK A, B) - Eq. 71 Boost - Eq. 40	$C1=\frac{1}{2\pi\times R3\times0.1\times GBW}$ (Farads)	$C1=\frac{1}{2\pi\times R3\times0.1\times f_C}$ Assume R3 > 10kΩ	C1 can be increased for faster settling time and noise immunity
Compensation capacitor for second pole. (VBUCK A, B) - Eq. 72 Boost - Eq. 41	$C2=\frac{1}{\pi\times R3\times f_{SW}}$ (Farads)	$C2=\frac{1}{2\pi\times10\times f_C\times R3}$ Assume R3 > 10kΩ	The value of C2 is also critcal for buffering the noise on COMP pin and so the value of capacitance is a trade off between noise and gain band width
Pole at low frequency with high dc gain. (VBUCK A, B) - Eq. 75 Boost - Eq. 46	$f_{P1}=\frac{1}{2\pi\times C_O\times R_L}+\frac{1\text{-}D\text{-}0.5}{2\pi\times L\times f_{SW}\times C_O}$ (Hz)	$f_{P1}=\frac{1}{2\pi\times C1\times R_{EA}}$ (Hz) Where, R_{EA} = 1MΩ to 100MΩ	First pole is usually at lower frequencies
Zero at control loop pole related to output filter LC. (VBUCK A, B) - Eq. 76 Boost - Eq. 48	$f_{Z1}=\frac{1}{2\pi\times C1\times R3}$ (Hz)	$f_Z=\frac{1}{2\pi\times C1\times R3}$ (Hz)	Place zero near the pole due to LC output filter
Second pole for type 2a. (VBUCK A, B) - Eq. 77 Boost - Eq. 47	$f_{P2}=\frac{1}{2\pi\times C2\times R3}$ (Hz) Type 2a	$f_{P2}=\frac{1}{2\pi\times C2\times R3}$ (Hz) (optional)	Place second pole at half switching frequency f_{SW}

	VBUCKA, VBUCKB	BOOST	COMMENTS
Second pole for type 2b (VBUCK A, B) - Eq. 78	$f_{P2}=\frac{1}{2\pi\times C_O\times\frac{R3+R_L}{R3\times R_L}}$ (Hz) Type 2a	Not applicable	
Second pole for type 1 (VBUCK A, B) - Eq. 79	$f_{P2}=\frac{1}{(2\pi\times C_O+C2)\times R_L}$ (Hz) Type 1	Not applicable	

Design Guide – Step by Step Design Procedure

The following example illustrates the design process and component selection for the TPS43330. The design goal parameters are given in the table below.

Parameter	VBUCK A	VBUCK B	Boost
Input Voltage VI	6V to 18V	6V to 18V	3V to 8V
	14V - typ	14V - typ	5V - typ
Input Ripple Voltage	±0.5V	±0.5V	±0.1V
Output Voltage VO	5V±2%	3.3V±2%	7V±5%
Max - Output Current IO	2A	2A	4A
Min – Output Current IO	0.1A	0.1A	0.1A
Load step output tolerance ΔVO	±0.2V	±0.12V	±0.5V
Current Output Load step ΔIO	0.1A to 2A	0.1A to 2A	0.1A to 4A
Converter switching frequency	400kHz	400kHz	200kHz

Schematic

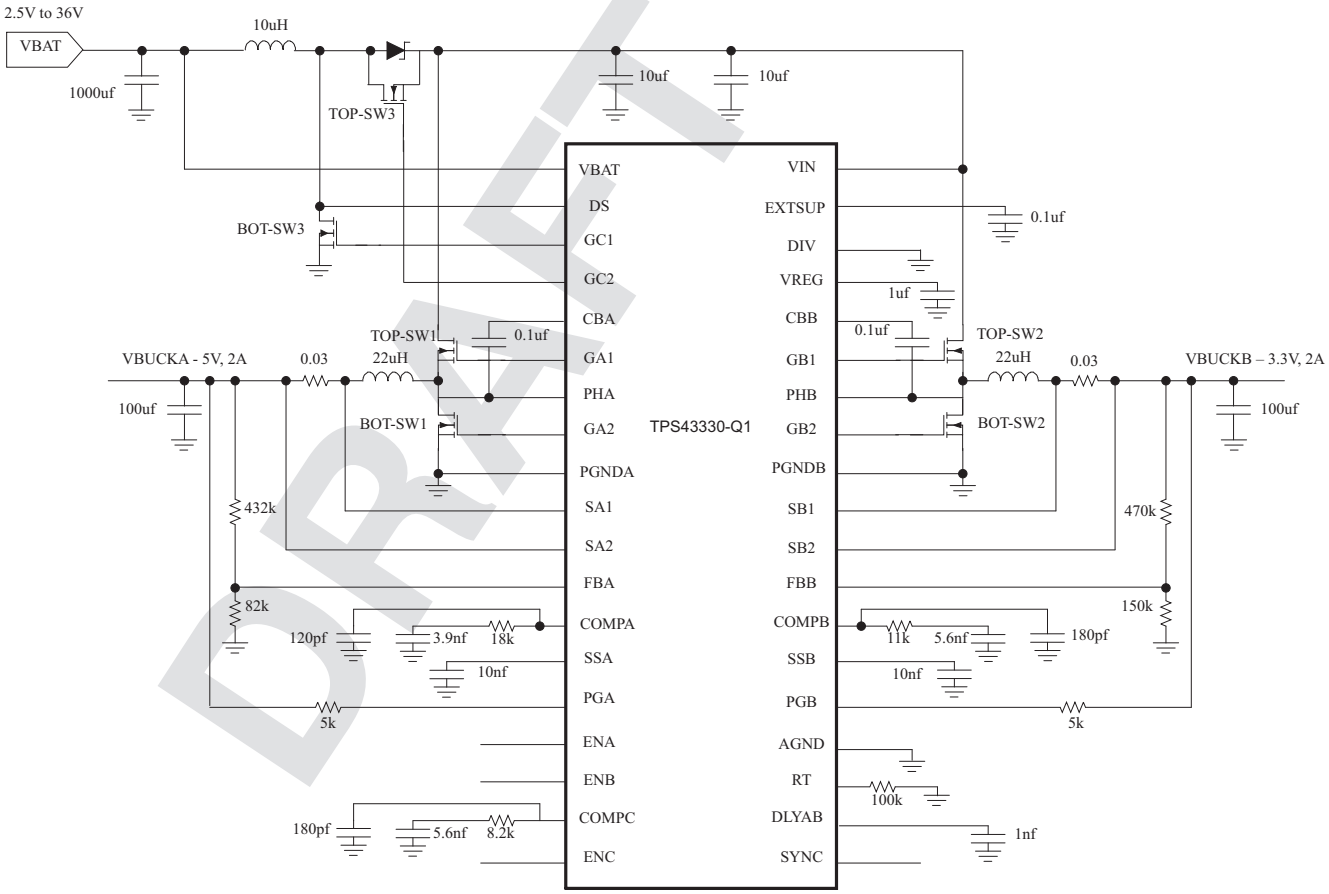

Figure 33. EVM Schematic

Selected Design Componenets

PARAMETER	VBUCK A (V_O = 5V, I_O = 2A)	VBUCK B (V_O = 3.3V, I_O = 2A)	BOOST (V_O = 7V, I_O = 4A)
Duty cycle D (VBUCK A, B) - Eq.45 Boost CCM - Eq. 20 Boost DCM - Eq. 21	$D=\frac{5}{14}=0.357$	$D=\frac{3.3}{14}=0.2357$	$D_{CCM}=1-\frac{5}{7+0.3}=0.315$
Current limit sense resistor R_S - Eq.47	$R_S = 0.075 / (1.25 * I_{Omax})$ $R_S = 0.03$	$R_S = 0.075 / (1.25 * I_{Omax})$ $R_S = 0.03$	Not Applicable
Inductor selection L. (VBUCK A, B) - Eq. 48 Boost CCM - Eq. 33 Boost DCM - Eq. 22	$L=\frac{200}{f_{SW}}\times R_S$ Where, L = 15 µH	$L=\frac{200}{f_{SW}}\times R_S$ Where, L = 15 µH	Select $I_{O-DCM} = 0.1 \times I_O$, Where L_{CCM} = 6 µH Chose L = 10 µH
Indcutor ripple current. (VBUCK A, B) - Eq. 53 Boost - Eq. 32	ΔI_{L_ripple} = 0.42 A, using higher L reduces ripple	ΔI_{L_ripple} = 0.42 A, using higher L reduces ripple	ΔI_{L_ripple} = 1.6 A, using higher L reduces ripple
Output Capactior C_O (VBUCK A, B) - Eq. 56 Boost CCM – Eq. 30 Boost DCM – Eq. 25	$C_O=\frac{2\times\Delta I_O}{f_{SW}\times\Delta V_O}$ (Farads) = 63.3 µF Use CO = 100 µF	$C_O=\frac{2\times\Delta I_O}{f_{SW}\times\Delta V_O}$ (Farads) = 63.3 µF Use C_O = 100 µF	$C_{CCMmin}\geq\frac{I_{Omax}}{\Delta V_O}\times\left(1-\frac{V_{IN}}{V_O}\right)\times\frac{1}{f_{SW}}$ (Farads) Where C_{CCM} = 11 µF, Choose C_{CCM} > 22 µF
Input Capacitor C_{IN} (VBUCK A, B) - Eq. 61 Boost CCM - Eq. 31 Boost DCM - Eq. 27	$C_{IN}=\frac{0.25\times\Delta I_{Omax}}{f_{SW}\times\Delta V_I}$ (Farads) = 2.3 µF Use C_{IN} = 10 µF	$C_{IN}=\frac{0.25\times\Delta I_{Omax}}{f_{SW}\times\Delta V_I}$ (Farads) = 2.3 µF Use C_{IN} = 10 µF	$C_{IN-CCM}=\frac{0.25\times\Delta I_{Omax}}{f_{SW}\times\Delta V_{Iripple}}$ (Farads) Where C_{IN} = 10 µF, Choose C_{IN} = 22 µF
Soft start C_{SS} - Eq. 62	$C_{SS}=\frac{1\mu A\times\Delta t}{0.8}$ Assume 8 ms for soft start C_{SS} = 10 nF	$C_{SS}=\frac{1\mu A\times\Delta t}{0.8}$ Assume 8 ms for soft start C_{SS} = 10 nF	Not appicable
Bootstrap capacitor C_{Boot} - Eq. 63	$C_{Boot}=\frac{Q_g}{\Delta V}$ (Farads) Assume voltage ripple of 0.3V,external FET Qg < 30nC. C_{Boot} = 0.1 µF	$C_{Boot}=\frac{Q_g}{\Delta V}$ (Farads) Assume voltage ripple of 0.3V,external FET Qg < 30nC. C_{Boot} = 0.1 µF	Not appicable
Compensation resistor for pole. (VBUCK A, B) - Eq. 70 Boost - Eq. 39	$R22=\frac{GBW\times2\pi\times C_O}{Gm\times K_{CFB}\times\beta}$ = 11.8k, assume GBW = f_{SW}/16. R22 = 11.8k	$R23=\frac{GBW\times2\pi\times C_O}{Gm\times K_{CFB}\times\beta}$ = 15.5k, assume GBW = f_{SW}/16. R23 = 15k	$R37=\frac{B}{Gm}\times\frac{R1+R2}{R2}$ Where, R1 = 821k, R2 = 106k and B = 3.3 R37 = 28.8k
Compensation capacitor for zero. (VBUCK A, B) - Eq. 71 Boost - Eq. 41	$C23=\frac{1}{2\pi\times R3\times0.1\times GBW}$ = 5.3 nF	$C26=\frac{1}{2\pi\times R3\times0.1\times GBW}$ = 5.8 nF	$C36=\frac{1}{2\pi\times R37\times0.1\times f_C}$ f_C = 40kHz, C36 = 1.38nF
Compensation capacitor for second pole. (VBUCK A, B) - Eq. 72 Boost - Eq. 41	$C21=\frac{1}{\pi\times f_{SW}\times R22}$ = 67 pF	$C22=\frac{1}{\pi\times f_{SW}\times R23}$ = 72 pF	$C38=\frac{1}{2\pi\times10\times f_C\times R37}$ = 13.8 pF
Pole at low frequency with high dc gain. (VBUCK A, B) - Eq. 75 Boost - Eq. 46	$f_{P1}=\frac{1}{2\pi\times C_O\times R_L}$ = 31Hz	$f_{P1}=\frac{1}{2\pi\times C_O\times R_L}$ = 31Hz	$f_{P1}=\frac{1}{2\pi\times C36\times R_{EA}}$ = 26Hz
Zero at control loop pole related to output filter LC. (VBUCK A, B) - Eq. 76 Boost - Eq. 48	$f_{Z1}=\frac{1}{2\pi\times C23\times R22}$ = 2.54kHz	$f_{Z1}=\frac{1}{2\pi\times C26\times R23}$ = 2.45kHz	$f_{Z1}=\frac{1}{2\pi\times C36\times R37}$ = 4kHz
Second pole for type 2a. (VBUCK A, B) - Eq. 77 Boost - Eq. 47	$f_{P2}=\frac{1}{2\pi\times C21\times R22}$ = 201kHz	$f_{P2}=\frac{1}{2\pi\times C22\times R23}$ = 142.6kHz	$f_{P2}=\frac{1}{2\pi\times C38\times R37}$ = 400kHz
Second pole for type 2b (VBUCK A, B) - Eq. 78	$f_{P2}=\frac{1}{2\pi\times C_O\times R22}$	$f_{P2}=\frac{1}{2\pi\times C_O\times R23}$	Not applicable

PARAMETER	VBUCK A (V_O = 5V, I_O = 2A)	VBUCK B (V_O = 3.3V, I_O = 2A)	BOOST (V_O = 7V, I_O = 4A)
Second pole for type 1 (VBUCK A, B) - Eq. 79	$f_{P2}=\frac{1}{(2\pi\times C_O+C21)\times R_L}$	$f_{P2}=\frac{1}{(2\pi\times C_O+C22)\times R_L}$	Not applicable

Power Dissipation

The power dissipation is largely dependent on the MOSFET driver current and input voltage. The drive current is proportional to the total gate charge of the external MOSFET.

Power dissipation buck regulator controller 1and 2 is given by Equation 80.

$$P_{GateDrive}=Qg\times V_{DR}\times f_{SW} \quad \text{(Watts)} \tag{80}$$

Assuming both high and low side MOSFETs are identical in a synchronous configuration, the total power dissipations is given by Equation 81.

$$P_{BuckController1}=2\times Qg\times f_{SW}\times VIN \quad \text{(Watts per channel)} \tag{81}$$

Dual channel controller the total power dissipation is given by Equation 82.

$$P_{BuckController1\&2}=4\times Qg\times f_{SW}\times VIN \quad \text{(Watts)} \tag{82}$$

IC power consumption is given by Equation 83.

$$P_{IC}=I_q\times VIN \quad \text{(Watts)} \tag{83}$$

Boost regulator driver power dissipation is given by Equation 84.

$$P_{BoostController}=(VINSB-VSTBY)\times I_{VSTBY} \quad \text{(Watts)} \tag{84}$$

Total power dissipation is given by Equation 85.

$$P_{Total}=P_{BuckController1\&2}+P_{BoostController}+P_{IC} \quad \text{(Watts)} \tag{85}$$

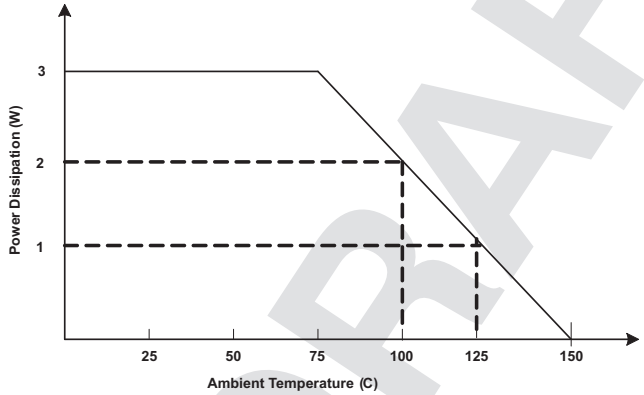

Figure 34. Power Dissipation Derating Profile for 48-Pin QFP PowerPAD Package

PCB Layout Guidelines

Grounding and Circuit Layout Considerations

The TPS43330 has two separate ground terminations (AGND and PGND) pins. The ground signal consists of a plane to minimize its impedance. Try to separate the low signal ground termination from the power ground signal. The high power noisy circuits like the output, synchronous rectifier, MOSFET driver decoupling capacitor and the input capacitor should be connected to the PGND plane. The AGND plane should only make a single point connection to the PGND plane.

The sensitive nodes like the feedback resistor divider, oscillator resistor (to set frequency), current sense, and compensation circuitry should be connected to the AGND plane.

Keep the high-current carrying loops to a minimum by ensuring optimal component placement. Ensure the bypass capacitors are located as close as possible to their respective power and ground pins.

Sensitive circuits such as sense feedback, frequency setting resistor for the oscillator, current sense and compensation circuits should not be located near the dv/dt nodes; these include the gate drive outputs, phase pins, and boost circuits (bootstrap).

PCB Layout

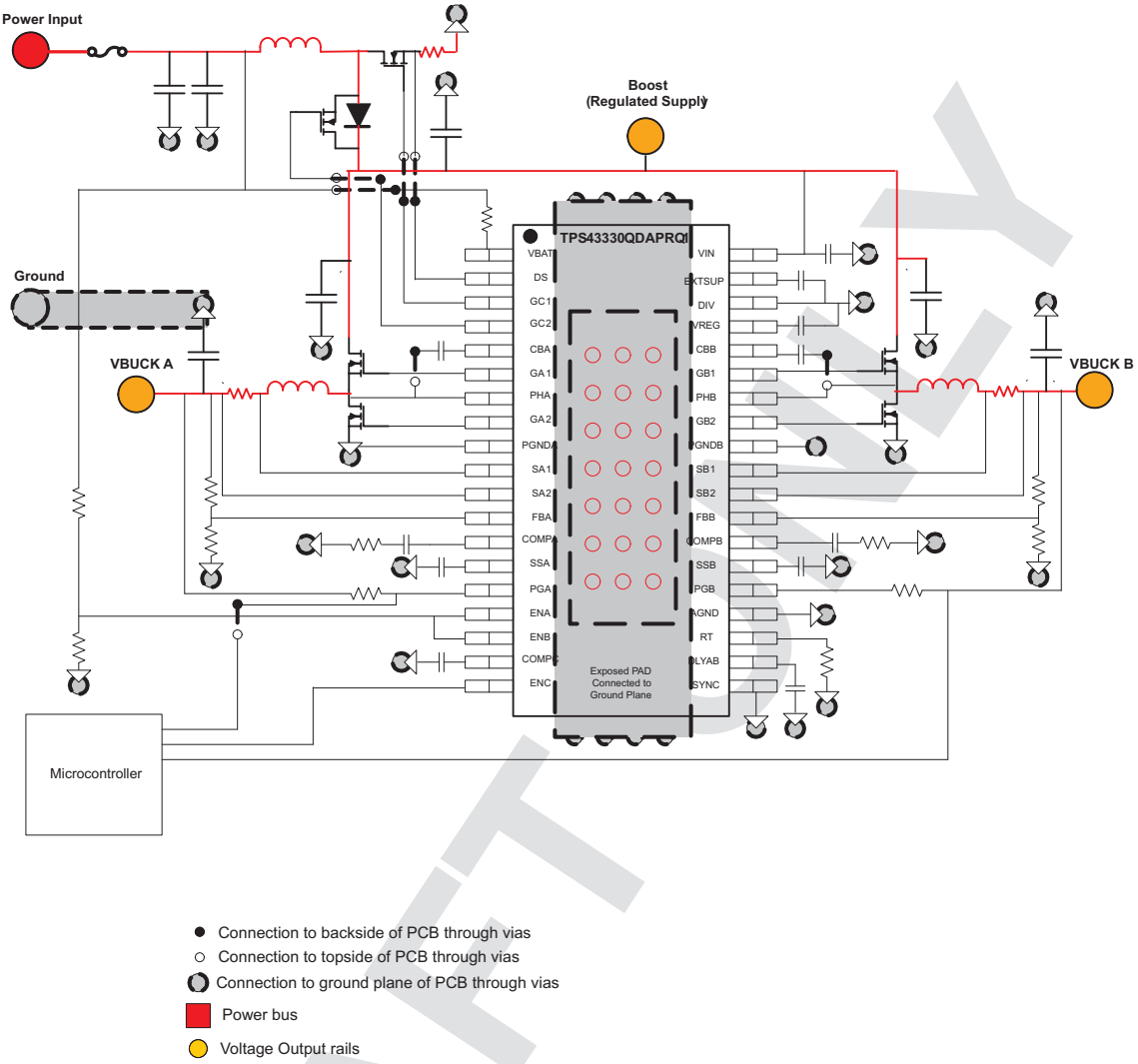

Figure 35. PCB Layout