Section I. Arria II GX Device Data Sheet

This section provides information about the Arria® II GX device data sheet. This section includes the following chapters:

- Chapter 1, Arria II GX Devices Data Sheet

Revision History

Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in this volume.

1. Arria II GX Devices Data Sheet

AIIGX53001-1.2

Introduction

This chapter describes the electrical and switching characteristics of the Arria® II GX device family.

This chapter contains the following sections:

Electrical Characteristics

The following sections describe the electrical characteristics.

Operating Conditions

When Arria II GX devices are implemented in a system, they are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of Arria II GX devices, system designers must consider the operating requirements in this chapter.

Arria II GX devices are offered in both commercial and industrial grades. Commercial devices are offered in –4 (fastest), –5, and –6 (slowest) speed grades. Industrial device is only offered in –5 speed grade.

In this chapter, a prefix associated with the operating temperature range is attached to the speed grades; commercial with the "C" prefix, and industrial with the "I" prefix. Commercial devices are therefore indicated as C4, C5, and C6 speed grade respectively, while the industrial device is indicated as I5.

Absolute Maximum Ratings

Absolute maximum ratings define the maximum operating conditions for Arria II GX devices. The values are based on experiments conducted with the device and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied under these conditions. Table 1–1 lists the absolute maximum ratings for Arria II GX devices.

Conditions beyond those listed in Table 1–1 may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Table 1–1. Arria II GX Device Absolute Maximum Ratings

Symbol	Description	Minimum	Maximum	Unit
V_{CC}	Supplies power to the core, periphery, I/O registers, PCIe HIP block, and transceiver PCS	-0.5	1.35	V
V_{CCCB}	Supplies power to the configuration RAM bits	-0.5	1.65	V
V_{CCBAT}	Battery back-up power supply for design security volatile key register	-0.5	3.75	V
V_{CCPD}	Supplies power to the I/O pre-drivers, differential input buffers, and MSEL circuitry	-0.5	3.75	V
V_{CCIO}	Supplies power to the I/O banks	-0.5	3.9	V
V_{CCD_PLL}	Supplies power to the digital portions of the PLL	-0.5	1.35	V
V_{CCA_PLL}	Supplies power to the analog portions of the PLL and device-wide power management circuitry	-0.5	3.75	V
V_I	DC input voltage	-0.5	4.0	V
V_{CCA}	Supplies power to the transceiver PMA regulator	—	2.625	V
V_{CCL_GXB}	Supplies power to the transceiver PMA TX, PMA RX, and clocking	—	1.21	V
V_{CCH_GXB}	Supplies power to the transceiver PMA output (TX) buffer	—	1.65	V
T_J	Operating junction temperature	-55	125	°C
T_{STG}	Storage temperature (no bias)	-65	150	°C

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage shown in Table 1–2 and undershoot to -2.0 V for magnitude of currents less than 100 mA and periods shorter than 20 ns.

Table 1–2 lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage over the device lifetime. The maximum allowed overshoot duration is specified as a percentage of high-time over the lifetime of the device. A DC signal is equivalent to 100% duty cycle. For example, a signal that overshoots to 4.3 V can only be at 4.3 V for 5.41% over the lifetime of the device: for a device lifetime of 10 years, this amounts to 5.41/10ths of a year.

Table 1–2. Maximum Allowed Overshoot During Transitions

Symbol	Description	Condition	Overshoot Duration as % of High Time	Unit
V_I (AC)	AC Input Voltage	4.0 V	100.000	%
		4.05 V	79.330	%
		4.1 V	46.270	%
		4.15 V	27.030	%
		4.2 V	15.800	%
		4.25 V	9.240	%
		4.3 V	5.410	%
		4.35 V	3.160	%
		4.4 V	1.850	%
		4.45 V	1.080	%
		4.5 V	0.630	%
		4.55 V	0.370	%
		4.6 V	0.220	%

Maximum Allowed I/O Operating Frequency

Table 1–3 defines the maximum allowed I/O operating frequency for I/Os using the specified I/O standards to ensure device reliability.

Table 1–3. Maximum Allowed I/O Operating Frequency

I/O Standard	I/O Frequency (MHz)
SSTL-18, SSTL -15 HSTL-18, HSTL-15	300
2.5-V LVCMOS	260
3.3-V and 3.0-V LVTTL 3.3-V, 3.0-V, 1.8-V, 1.5-V LVCMOS PCI and PCI-X SSTL-2	250
1.2-V LVCMOS HSTL-12	200

Recommended Operating Conditions

This section lists the functional operation limits for AC and DC parameters for Arria II GX devices. The steady-state voltage and current values expected from Arria II GX devices are provided in Table 1–4. All supplies are required to monotonically reach their full-rail values without plateaus within t_{RAMP}.

Table 1–4 shows the recommended operating conditions for Arria II GX device.

Table 1–4. Arria II GX Device Recommended Operating Conditions

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
V_{CC}	Supplies power to the core, periphery, I/O registers, PCIe HIP block, and transceiver PCS	—	0.87	0.90	0.93	V
V_{CCCB}	Supplies power to the configuration RAM bits	—	1.425	1.50	1.575	V
V_{CCBAT} *(2)*	Battery back-up power supply for design security volatile key registers	—	1.2	—	3.3	V
V_{CCPD}	Supplies power to the I/O pre-drivers, differential input buffers, and MSEL circuitry	—	3.135	3.3	3.465	V
		—	2.85	3.0	3.15	V
		—	2.375	2.5	2.625	V
V_{CCIO}	Supplies power to the I/O banks *(1)*	—	3.135	3.3	3.465	V
		—	2.85	3.0	3.15	V
		—	2.375	2.5	2.625	V
		—	1.71	1.8	1.89	V
		—	1.425	1.5	1.575	V
		—	1.14	1.2	1.26	V
V_{CCD_PLL}	Supplies power to the digital portions of the PLL	—	0.87	0.90	0.93	V
V_{CCA_PLL}	Supplies power to the analog portions of the PLL and device-wide power management circuitry	—	2.375	2.5	2.625	V
V_I	DC Input voltage	—	–0.5	—	3.6	V
V_O	Output voltage	—	0	—	V_{CCIO}	V
V_{CCA}	Supplies power to the transceiver PMA regulator	—	2.375	2.5	2.625	V
V_{CCL_GXB}	Supplies power to the transceiver PMA TX, PMA RX, and clocking	—	1.045	1.1	1.155	V
V_{CCH_GXB}	Supplies power to the transceiver PMA output (TX) buffer	—	1.425	1.5	1.575	V
T_J	Operating junction temperature	Commercial	0	—	85	C
		Industrial	–40	—	100	C
t_{RAMP}	Power Supply Ramp time	Normal POR	0.05	—	100	ms
		Fast POR	0.05	—	4	ms

Notes to Table 1–4:

(1) V_{CCIO} for 3C and 8C I/O banks where the configuration pins reside only supports 3.3-, 3.0-, 2.5-, or 1.8-V voltage levels.

(2) Altera recommends a 3.0-V nominal battery voltage when connecting V_{CCBAT} to a battery for volatile key backup. If you do not use the volatile security key, you may connect the V_{CCBAT} to either GND or a 3.0-V power supply.

DC Characteristics

This section lists the supply current, I/O pin leakage current, on-chip termination (OCT) accuracy and variation, input pin capacitance, internal weak pull-up and pull-down resistance, hot socketing, and Schmitt trigger input specifications.

Supply Current

Standby current is the current the device draws after the device is configured with no inputs or outputs toggling and no activity in the device. Since these currents vary largely with resources used, use the Excel-based Early Power Estimator (EPE) to get supply current estimates for your design.

For more information about power estimation tools, refer to the *Arria II GX EPE User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

I/O Pin Leakage Current

Table 1–5 defines the Arria II GX I/O pin leakage current specifications.

Table 1–5. Arria II GX I/O Pin Leakage Current

Symbol	Description	Conditions	Min	Typ	Max	Unit
I_I	Input pin	V_I = 0 V to $V_{CCIOMAX}$	–10	—	10	µA
I_{OZ}	Tri-stated I/O pin	V_O = 0 V to $V_{CCIOMAX}$	–10	—	10	µA

OCT Specifications

Table 1–6 lists the Arria II GX series OCT with and without calibration accuracy.

Table 1–6. OCT With and Without Calibration Specification for I/Os *(Note 1)*

Symbol	Description	Conditions	Calibration Accuracy		Unit
			Commercial	Industrial	
25-Ω R_S 3.0/2.5	25-Ω series OCT without calibration	V_{CCIO} = 3.0/2.5 V	± 30	± 40	%
50-Ω R_S 3.0/2.5	50-Ω series COT without calibration	V_{CCIO} = 3.0/2.5 V	± 30	± 40	%
25-Ω R_S 1.8	25-Ω series OCT without calibration	V_{CCIO} = 1.8 V	± 40	± 50	%
50-Ω R_S 1.8	50-Ω series OCT without calibration	V_{CCIO} = 1.8 V	± 40	± 50	%
25-Ω R_S 1.5/1.2	25-Ω series OCT without calibration	V_{CCIO} = 1.5/1.2 V	± 50	± 50	%
50-Ω R_S 1.5/1.2	50-Ω series OCT without calibration	V_{CCIO} = 1.5/1.2 V	± 50	± 50	%
25-Ω R_S 3.0/2.5/1.8/ 1.5/1.2	25-Ω series OCT with calibration	V_{CCIO} = 3.0/2.5/1.8/ 1.5/1.2 V	± 10	± 10	%
50-Ω R_S 3.0/2.5/1.8/ 1.5/1.2	50-Ω series OCT with calibration	V_{CCIO} = 3.0/2.5/1.8/ 1.5/1.2 V	± 10	± 10	%

Note to Table 1–6:

(1) OCT with calibration accuracy is valid at the time of calibration only.

OCT calibration is automatically performed at power-up for OCT-enabled I/Os. When voltage and temperature conditions change after calibration, the resistance may change. Use Equation 1–1 and Table 1–7 to determine the OCT variation when voltage and temperature vary after power-up calibration.

Equation 1–1. OCT Variation *(Note 1)*

$$R_{OCT} = R_{SCAL}\left(1 + \langle \frac{dR}{dT} \times \Delta T \rangle \pm \langle \frac{dR}{dV} \times \Delta V \rangle\right)$$

Notes to Equation 1–1:

(1) R_{OCT} value calculated from Equation 1–1 shows the range of OCT resistance with the variation of temperature and V_{CCIO}.
(2) R_{SCAL} is the OCT resistance value at power-up.
(3) ΔT is the variation of temperature with respect to the temperature at power-up.
(4) ΔV is the variation of voltage with respect to the V_{CCIO} at power-up.
(5) dR/dT is the percentage change of R_{SCAL} with temperature.
(6) dR/dV is the percentage change of R_{SCAL} with voltage.

Table 1–7 lists OCT variation with temperature and voltage after power-up calibration.

Table 1–7. OCT Variation after Power-up Calibration

Nominal Voltage	dR/dT (%/°C)	dR/dV(%/mV)
3.0	*(1)*	*(1)*
2.5	*(1)*	*(1)*
1.8	*(1)*	*(1)*
1.5	*(1)*	*(1)*
1.2	*(1)*	*(1)*

Note to Table 1–7:

(1) Pending silicon characterization.

Pin Capacitance

Table 1–8 shows the Arria II GX device family pin capacitance.

Table 1–8. Arria II GX Device Capacitance

Symbol	Description	Typical	Unit
C_{IODIFF}	Input capacitance on dual-purpose differential I/O pins	7.5	pF
C_{IOCLK}	Input capacitance on dual-purpose clock output/feedback pins and dedicated clock input pins	7	pF
C_{IOOCT}	Input capacitance on dual-purpose R_{UP} and R_{DN} pins	7	pF

Internal Weak Pull-Up and Weak Pull-Down Resistors

Table 1–9 lists the Arria II GX devices weak pull-up and pull-down resistor values.

Table 1–9. Arria II GX Internal Weak Pull-up and Weak Pull-Down Resistors *(Note 1)*

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
R_{PU}	Value of I/O pin pull-up resistor before and during configuration, as well as user mode if the programmable pull-up resistor option is enabled.	V_{CCIO} = 3.3 V ±5% *(2)*, *(3)*	7	25	41	kΩ
		V_{CCIO} = 3.0 V ±5% *(2)*, *(3)*	7	28	47	kΩ
		V_{CCIO} = 2.5 V ±5% *(2)*, *(3)*	8	35	61	kΩ
		V_{CCIO} = 1.8 V ±5% *(2)*, *(3)*	10	57	108	kΩ
		V_{CCIO} = 1.5 V ±5% *(2)*, *(3)*	13	82	163	kΩ
		V_{CCIO} = 1.2 V ±5% *(2)*, *(3)*	19	143	351	kΩ
R_{PD}	Value of TCK pin pull-down resistor	V_{CCIO} = 3.3 V ±5% *(4)*	6	19	29	kΩ
		V_{CCIO} = 3.0 V ±5% *(4)*	6	22	32	kΩ
		V_{CCIO} = 2.5 V ±5% *(4)*	6	25	42	kΩ
		V_{CCIO} = 1.8 V ±5% *(4)*	7	35	70	kΩ
		V_{CCIO} = 1.5 V ±5% *(4)*	8	50	112	kΩ

Notes to Table 1–9:

(1) All I/O pins have an option to enable weak pull-up except configuration, test, and JTAG pins. The weak pull-down feature is only available for JTAG TCK.

(2) Pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.

(3) $R_{PU} = (V_{CCIO} - V_I)/I_{R_{PU}}$. Minimum condition: -40°C; V_{CCIO} = VCC + 5%, V_I = VCC + 5% - 50 mV. Typical condition: 25°C; V_{CCIO} = VCC, V_I = 0 V. Maximum condition: 100°C; V_{CCIO} = VCC - 5%, V_I = 0 V; in which V_I refers to the voltage input at the I/O pin.

(4) $R_{PD} = V_I/I_{R_{PD}}$. Minimum condition: -40°C; V_{CCIO} = VCC + 5%, V_I = 50 mV. Typical condition: 25°C; V_{CCIO} = VCC, V_I = VCC - 5%. Maximum condition: 100°C; V_{CCIO} = VCC - 5%, V_I = VCC - 5%; in which V_I refers to the voltage input at the I/O pin.

Hot Socketing

Table 1–10 defines the hot socketing specification for Arria II GX devices.

Table 1–10. Arria II GX Hot Socketing Specifications

Symbol	Description	Maximum
$I_{IIOPIN(DC)}$	DC current per I/O pin	300 µA
$I_{IOPIN(AC)}$	AC current per I/O pin	8 mA *(1)*
$I_{XCVRTX(DC)}$	DC current per transceiver TX pin	100 mA
$I_{XCVRRX(DC)}$	DC current per transceiver RX pin	50 mA

Note to Table 1–10:

(1) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, |IIOPIN| = C dv/dt, in which "C" is I/O pin capacitance and "dv/dt" is slew rate.

Schmitt Trigger Input

The Arria II GX device supports Schmitt trigger input on TDI, TMS, TCK, nSTATUS, nCONFIG, nCE, CONF_DONE, and DCLK pins. A Schmitt trigger feature introduces hysteresis to the input signal for improved noise immunity, especially for signals with slow edge rates. Table 1–11 lists the hysteresis specifications across the supported V_{CCIO} range for Schmitt trigger inputs in Arria II GX devices.

Table 1–11. Arria II GX Schmitt Trigger Input Hysteresis Specifications

Symbol	Description	Condition	Minimum	Unit
$V_{Schmitt}$	Hysteresis for Schmitt trigger input	V_{CCIO} = 3.3 V	220	mV
		V_{CCIO} = 2.5 V	180	mV
		V_{CCIO} = 1.8 V	110	mV
		V_{CCIO} = 1.5 V	70	mV

I/O Standard Specifications

Table 1–12 through Table 1–17 list input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by Arria II GX devices. They also show the Arria II GX device family I/O standard specifications. V_{OL} and V_{OH} values are valid at the corresponding I_{OH} and I_{OL}, respectively.

For an explanation of terms used in Table 1–12 through Table 1–17, refer to "Glossary" on page 1–32.

Table 1–12 lists the Arria II GX single-ended I/O standards.

Table 1–12. Single-Ended I/O Standards (Part 1 of 2)

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
3.3 V LVTTL	3.135	3.3	3.465	-0.3	0.8	1.7	V_{CCIO} + 0.3	0.4	2.4	2	-2
3.3 V LVCMOS	3.135	3.3	3.465	-0.3	0.8	1.7	V_{CCIO} + 0.3	0.2	V_{CCIO} - 0.2	0.1	-0.1
3.0 V LVTTL	2.85	3	3.15	-0.3	0.8	1.7	V_{CCIO} + 0.3	0.4	2.4	2	-2
3.0 V LVCMOS	2.85	3	3.15	-0.3	0.8	1.7	V_{CCIO} + 0.3	0.2	V_{CCIO} - 0.2	0.1	-0.1
2.5 V LVCMOS	2.375	2.5	2.625	-0.3	0.7	1.7	V_{CCIO} + 0.3	0.4	2	1	-1
1.8 V LVCMOS	1.71	1.8	1.89	-0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.45	V_{CCIO} - 0.45	2	-2
1.5 V LVCMOS	1.425	1.5	1.575	-0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.25 * V_{CCIO}	0.75 × V_{CCIO}	2	-2
1.2 V LVCMOS	1.14	1.2	1.26	-0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.25 * V_{CCIO}	0.75 × V_{CCIO}	2	-2

Table 1–12. Single-Ended I/O Standards (Part 2 of 2)

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
3.0-V PCI	2.85	3	3.15	—	0.3 × V_{CCIO}	0.5 × V_{CCIO}	3.6	0.1 × V_{CCIO}	0.9 × V_{CCIO}	1.5	-0.5
3.0-V PCI-X	2.85	3	3.15	—	0.35 × V_{CCIO}	0.5 × V_{CCIO}	—	0.1 × V_{CCIO}	0.9 × V_{CCIO}	1.5	-0.5

Table 1–13 lists the Arria II GX single-ended SSTL and HSTL I/O reference voltage specifications.

Table 1–13. Single-Ended SSTL and HSTL I/O Reference Voltage Specifications

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04
SSTL-18 Class I, II	1.71	1.8	1.89	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04
SSTL-15 Class I, II	1.425	1.5	1.575	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	—	V_{CCIO}/2	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.68	0.75	0.9	—	V_{CCIO}/2	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.48 × V_{CCIO}	0.5 × V_{CCIO}	0.52 × V_{CCIO}	—	V_{CCIO}/2	—

Table 1–14 lists the Arria II GX single-ended SSTL and HSTL I/O standard signal specifications.

Table 1–14. Single-Ended SSTL and HSTL I/O Standard Signal Specifications (Part 1 of 2)

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{ol} (mA)	I_{oh} (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-2 Class I	-0.3	V_{REF} - 0.15	V_{REF} + 0.15	V_{CCIO} + 0.3	V_{REF} - 0.31	V_{REF} + 0.31	V_{TT} - 0.57	V_{TT} + 0.57	8.1	-8.1
SSTL-2 Class II	-0.3	V_{REF} - 0.15	V_{REF} + 0.15	V_{CCIO} + 0.3	V_{REF} - 0.31	V_{REF} + 0.31	V_{TT} - 0.76	V_{TT} + 0.76	16.2	-16.2
SSTL-18 Class I	-0.3	V_{REF} - 0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} -0.25	V_{REF} + 0.25	V_{TT} - 0.475	V_{TT} + 0.475	6.7	-6.7
SSTL-18 Class II	-0.3	V_{REF} - 0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} -0.25	V_{REF} + 0.25	0.28	V_{CCIO} - 0.28	13.4	-13.4
SSTL-15 Class I	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	V_{CCIO} + 0.3	V_{REF} - 0.175	V_{REF} + 0.175	0.2 × V_{CCIO}	0.8 × V_{CCIO}	8	-8
SSTL-15 Class II	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	V_{CCIO} + 0.3	V_{REF} - 0.175	V_{REF} + 0.175	0.2 × V_{CCIO}	0.8 × V_{CCIO}	16	-16
HSTL-18 Class I	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	V_{CCIO} + 0.3	V_{REF} -0.2	V_{REF} + 0.2	0.4	V_{CCIO} - 0.4	8	-8

Table 1–14. Single-Ended SSTL and HSTL I/O Standard Signal Specifications (Part 2 of 2)

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{ol} (mA)	I_{oh} (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
HSTL-18 Class II	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	V_{CCIO} + 0.3	V_{REF} -0.2	V_{REF} + 0.2	0.4	V_{CCIO} - 0.4	16	-16
HSTL-15 Class I	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	V_{CCIO} + 0.3	V_{REF} -0.2	V_{REF} + 0.2	0.4	V_{CCIO} - 0.4	8	-8
HSTL-15 Class II	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	V_{CCIO} + 0.3	V_{REF} -0.2	V_{REF} + 0.2	0.4	V_{CCIO} - 0.4	16	-16
HSTL-12 Class I	-0.15	V_{REF} - 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} -0.15	V_{REF} + 0.15	0.25 × V_{CCIO}	0.75 × V_{CCIO}	8	-8
HSTL-12 Class II	-0.15	V_{REF} - 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} -0.15	V_{REF} + 0.15	0.25 × V_{CCIO}	0.75 × V_{CCIO}	16	-16

Table 1–15 lists the Arria II GX differential SSTL I/O standards.

Table 1–15. Differential SSTL I/O Standards

I/O Standard	V_{CCIO} (V)			$V_{SWING(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{SWING(AC)}$ (V)		$V_{OX(AC)}$ (V)		
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.36	V_{CCIO}	$V_{CCIO}/2$ - 0.2	—	$V_{CCIO}/2$ + 0.2	0.7	V_{CCIO}	*(1)*	—	*(1)*
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	V_{CCIO}	$V_{CCIO}/2$ - 0.175	—	$V_{CCIO}/2$ + 0.175	0.5	V_{CCIO}	*(1)*	—	*(1)*
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	*(1)*	—	*(1)*	0.35	—	*(1)*	—	*(1)*

Note to Table 1–15:

(1) Pending silicon characterization.

Table 1–16 lists the Arria II GX HSTL I/O standards.

Table 1–16. Differential HSTL I/O Standards

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{CM(DC)}$ (V)			$V_{DIF(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-18 Class I	1.71	1.8	1.89	0.2	—	0.85	—	0.95	0.88	—	0.95	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.71	—	0.79	0.71	—	0.79	0.4	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	—	—	0.5 × V_{CCIO}	—	0.48 × V_{CCIO}	0.5 × V_{CCIO}	0.52 × V_{CCIO}	0.3	—

Table 1–17 lists the Arria II GX differential I/O standard specifications.

Table 1–17. Differential I/O Standard Specifications

I/O Standard	V_{CCIO} (V)			V_{TH} (mV)			V_{ICM} (V) *(4)*			V_{OD} (V) *(1)*			V_{OS} (V)		
	Min	Typ	Max	Min	Cond.	Max	Min	Cond.	Max	Min	Typ	Max	Min	Typ	Max
2.5V LVDS	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.05	D_{max} <= 700 Mbps	1.80	0.247	—	0.6	1.125	1.25	1.375
						—	1.05	D_{max} > 700 Mbps	1.55						
RSDS *(3)*	2.375	2.5	2.625	—	—	—	—	—	—	0.1	0.2	0.6	0.5	1.2	1.4
Mini-LVDS *(3)*	2.375	2.5	2.625	—	—	—	—	—	—	0.25	—	0.6	1	1.2	1.4
LVPECL *(2)*	2.375	2.5	2.625	300	—	—	0.6	D_{max} <= 700 Mbps	1.8	—	—	—	—	—	—
							1.0	D_{max} > 700 Mbps	1.6						

Notes to Table 1–17:

(1) R_L range: 90 <= RL <= 110 Ω.

(2) LVPECL input standard is supported at the dedicated clock input pins (GCLK) only.

(3) RSDS and mini-LVDS I/O standards are only supported for differential outputs.

(4) V_{IN} range: 0 <= V_{IN} <= 1.85 V.

(5) 1.5 V PCML transceiver I/O standard specifications are described in the section "Transceiver Performance Specifications" on page 1–12.

Power Consumption for Arria II GX Devices

Altera® offers two ways to estimate power for a design:

- the Excel-based Early Power Estimator.
- the Quartus® II PowerPlay Power Analyzer feature.

The interactive Excel-based Early Power Estimator is typically used prior to designing the FPGA in order to get a magnitude estimate of the device power. The Quartus II PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after place-and-route is complete. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities which, when combined with detailed circuit models, can yield very accurate power estimates.

For more information about power estimation tools, refer to the *Arria II GX EPE User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

Switching Characteristics

This section provides performance characteristics of the Arria II GX core and periphery blocks for commercial grade devices.

These characteristics can be designated as Preliminary or Final. Preliminary characteristics are created using simulation results, process data, and other known parameters. Final characteristics are based on actual silicon characterization and testing. These numbers reflect the actual performance of the device under worst-case silicon process, voltage, and junction temperature conditions.

The table title shows the designations as "Preliminary" for each table with preliminary characteristics.

Transceiver Performance Specifications

Table 1–18 lists the Arria II GX transceiver specifications.

Table 1–18. Arria II GX Transceiver Specification (Part 1 of 4)—Preliminary

Symbol/ Description	Conditions	C4			C5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Reference Clock											
Input frequency from REFCLK input pins	—	50	—	622.08	50	—	622.08	50	—	622.08	MHz
Input frequency from PLD input	—	50	—	200	50	—	200	50	—	200	MHz
Absolute V_{MAX} for a REFCLK pin	—	—	—	2.2	—	—	2.2	—	—	2.2	V
Absolute V_{MIN} for a REFCLK pin	—	-0.3	—	—	-0.3	—	—	-0.3	—	—	V
Rise/fall time	—	—	—	0.2	—	—	0.2	—	—	0.2	UI
Duty cycle	—	45	—	55	45	—	55	45	—	55	%

Table 1–18. Arria II GX Transceiver Specification (Part 2 of 4)—Preliminary

Symbol/ Description	Conditions	C4			C5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Peak-to-peak differential input voltage	—	200	—	2000	200	—	2000	200	—	2000	mV
Spread-spectrum modulating clock frequency	PCI Express	30	—	33	30	—	33	30	—	33	kHz
Spread-spectrum downspread	PCI Express	—	0 to -0.5%	—	—	0 to -0.5%	—	—	0 to -0.5%	—	
On-chip termination resistors	—	—	100	—	—	100	—	—	100	—	Ω
V_{ICM} (AC coupled)	—	—	1200	—	—	1200	—	—	1200	—	mV
V_{ICM} (DC coupled)	HCSL I/O standard for PCI Express reference clock	250	—	550	250	—	550	250	—	550	mV
R_{ref}	— —	—	2000 ± 1%	—	—	2000 ± 1%	—	—	2000 ± 1%	—	Ω
Transceiver Clocks											
Calibration block clock frequency	—	10	—	125	10	—	125	10	—	125	MHz
`fixedclk` clock frequency	PCI Express Receiver Detect	—	125	—	—	125	—	—	125	—	MHz
Transceiver block minimum power-down pulse width	—	—	1	—	—	1	—	—	1	—	µs
Receiver											
Data rate	—	600	—	3750	600	—	3125	600	—	3125	Mbps
Absolute V_{MAX} for a receiver pin *(1)*	—	—	—	1.5	—	—	1.5	—	—	1.5	V
Absolute V_{MIN} for a receiver pin	—	-0.4	—	—	-0.4	—	—	-0.4	—	—	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p)	V_{ICM} = 0.82 V setting	—	—	2.7	—	—	2.7	—	—	2.7	V
	V_{ICM} =1.1 V setting *(7)*	—	—	1.6	—	—	1.6	—	—	1.6	V
Minimum peak-to-peak differential input voltage V_{ID} (diff p-p)	Data Rate = 600 Mbps to 3.75 Gbps.	100	—	—	100	—	—	100	—	—	mV

Table 1–18. Arria II GX Transceiver Specification (Part 3 of 4)—Preliminary

Symbol/ Description	Conditions	C4			C5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{ICM}	V_{ICM} = 0.82 V setting	—	820	—	—	820	—	—	820	—	mV
	V_{ICM} =1.1 V setting *(7)*	—	1100	—	—	1100	—	—	1100	—	mV
Differential on-chip termination resistors	100–Ω setting	—	100	—	—	100	—	—	100	—	Ω
Return loss differential mode	PCI Express	50 MHz to 1.25 GHz: -10dB									
	XAUI	100 MHz to 2.5 GHz: -10dB									
Return loss common mode	PCI Express	50 MHz to 1.25 GHz: -6dB									
	XAUI	100 MHz to 2.5 GHz: -6dB									
Programmable PPM detector *(2)*	—	± 62.5, 100, 125, 200, 250, 300, 500, 1000									ppm
Run length	—	—	80	—	—	80	—	—	80	—	UI
Programmable equalization	—	—	—	7	—	—	7	—	—	7	dB
Signal detect/loss threshold	PCI Express (PIPE) Mode	65	—	175	65	—	175	65	—	175	mV
CDR LTR time *(3)*	—	—	—	75	—	—	75	—	—	75	µs
CDR minimum T1b *(4)*	—	15	—		15	—	—	15	—	—	µs
LTD lock time *(5)*	—	0	100	4000	0	100	4000	0	100	4000	ns
Data lock time from `rx_freqlocked` *(6)*	—	—	—	4000	—	—	4000	—	—	4000	ns
Programmable DC gain	DC Gain Setting = 0	—	0	—	—	0	—	—	0	—	dB
	DC Gain Setting = 1	—	3	—	—	3	—	—	3	—	dB
	DC Gain Setting = 2	—	6	—	—	6	—	—	6	—	dB
Transmitter											
Data rate		—	—	—	—	—	—	—	—	—	Mbps
V_{OCM}	0.65 V setting	—	650	—	—	650	—	—	650	—	mV
Differential on-chip termination resistors	100–Ω setting	—	100	—	—	100	—	—	100	—	Ω
Return loss differential mode	PCI Express	50 MHz to 1.25 GHz: -10dB									
	XAUI	312 MHz to 625 MHz: -10dB 625 MHz to 3.125 GHz: -10dB/decade slope									
Return loss common mode	PCI Express	50 MHz to 1.25 GHz: -6dB									
Rise time	—	50	—	200	50	—	200	50	—	200	ps

Table 1–18. Arria II GX Transceiver Specification (Part 4 of 4)—Preliminary

Symbol/ Description	Conditions	C4			C5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Fall time	—	50	—	200	50	—	200	50	—	200	ps
Intra-differential pair skew	—	—	—	15	—	—	15	—	—	15	ps
Intra-transceiver block skew	PCI Express (PIPE) ×4	—	—	120	—	—	120	—	—	120	ps
Inter-transceiver block skew	PCI Express (PIPE) ×8	—	—	300	—	—	300	—	—	300	ps
CMU PLL0 and CMU PLL1											
CMU PLL lock time from `CMUPLL_reset` deassertion	—	—	—	100	—	—	100	—	—	100	µs
PLD-Transceiver Interface											
Interface speed	—	25	—	200	25	—	160	25	—	130	MHz
Digital reset pulse width	—	Minimum is 2 parallel clock cycles									

Notes to Table 1–18:

(1) The device cannot tolerate prolonged operation at this absolute maximum.

(2) The rate matcher supports only up to +/-300 parts per million (ppm).

(3) Time taken to `rx_pll_locked` goes high from `rx_analogreset` deassertion. Refer to Figure 1–1.

(4) Time for which the CDR must be kept in lock-to-reference mode after `rx_pll_locked` goes high and before `rx_locktodata` is asserted in manual mode. Refer to Figure 1–1.

(5) Time taken to recover valid data after the `rx_locktodata` signal is asserted in manual mode. Refer to Figure 1–1.

(6) Time taken to recover valid data after the `rx_freqlocked` signal goes high in automatic mode. Refer to Figure 1–2.

(7) The 1.1-V RX V_{ICM} setting must be used if the input serial data standard is LVDS and the link is DC-coupled.

Figure 1–1 shows the lock time parameters in manual mode.

LTD = lock-to-data. LTR = lock-to-reference.

Figure 1–1. Lock Time Parameters for Manual Mode

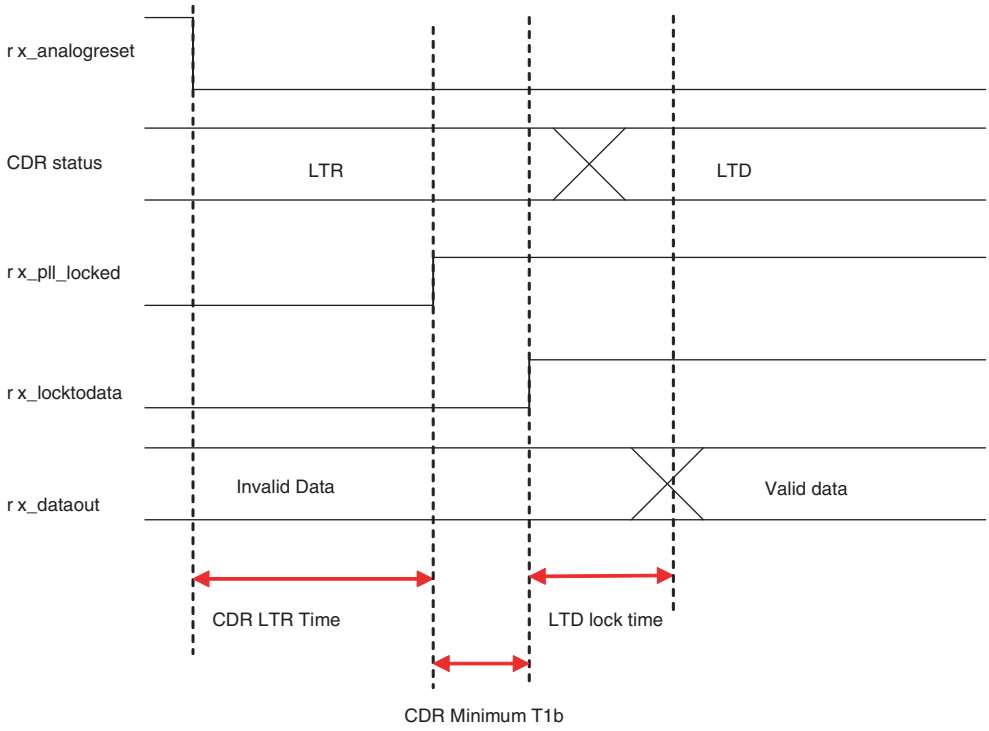


Figure 1–2 shows the lock time parameters in automatic mode.

Figure 1–2. Lock Time Parameters for Automatic Mode

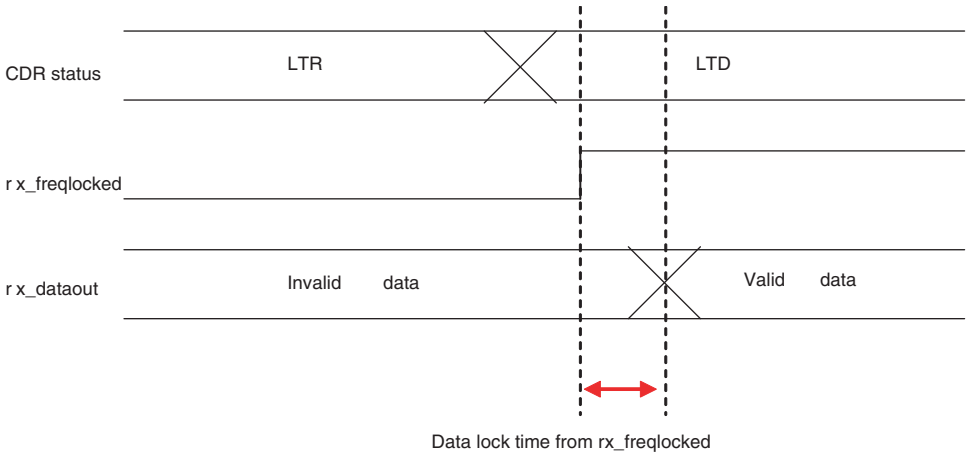


Figure 1–3 shows the differential receiver input waveform.

Figure 1–3. Receiver Input Waveform

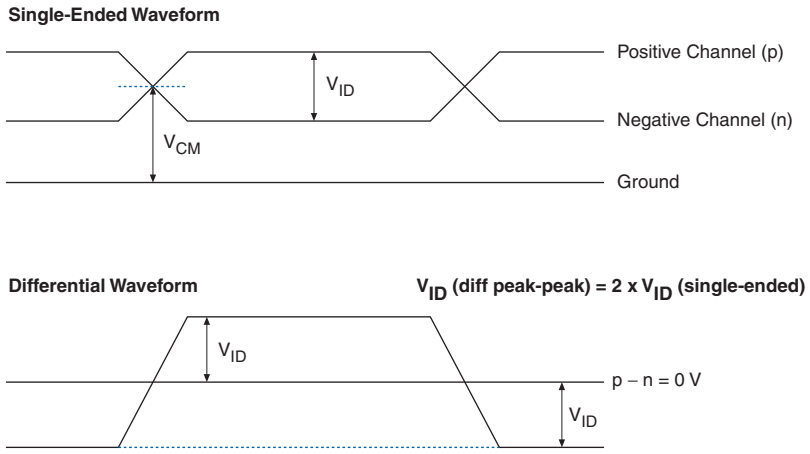


Figure 1–4 shows the transmitter output waveform.

Figure 1–4. Transmitter Output Waveform—Preliminary

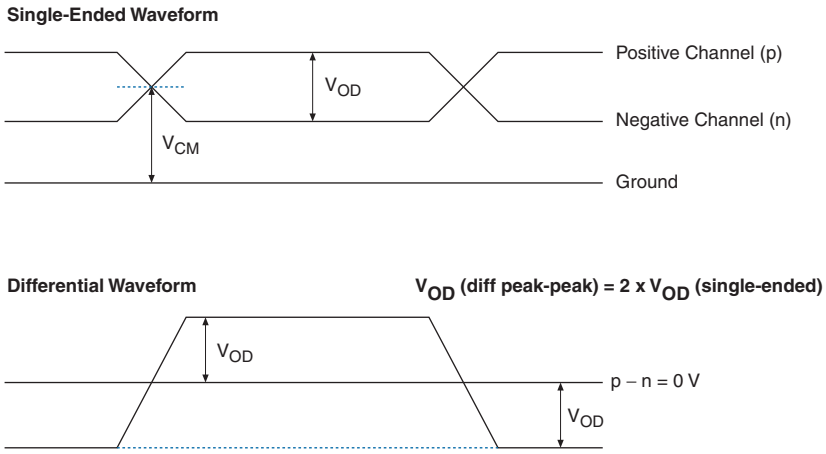


Table 1–19 shows the typical V_{OD} for TX term that equals 100 Ω. .

Table 1–19. Typical V_{OD} Setting, TX Term = 100 Ω—Preliminary

Symbol	V_{OD} Setting (mV)							
	200	400	600	700	800	900	1000	1200
V_{OD} Typical (mV)	200	400	600	700	800	900	1000	1200

Table 1–20 shows the typical V_{OD} for TX term that equals 150 Ω.

Table 1–20. Typical V_{OD} Setting, TX Term = 150 Ω—Preliminary

Symbol	V_{OD} Setting (mV)				
	300	600	900	1050	1200
V_{OD} Typical (mV)	300	600	900	1050	1200

Table 1–21 shows the Arria II GX transceiver block AC specifications.

Table 1–21. Arria II GX Transceiver Block AC Specification *(Note 1)*, *(2)* (Part 1 of 6)—Preliminary

Symbol/ Description	Conditions	C4			C5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SONET/SDH Receiver Jitter Tolerance											
Jitter tolerance at 622.08 Mbps	Jitter frequency = 0.03 KHz Pattern = PRBS23	> 15			> 15			> 15			UI
	Jitter frequency = 25 KHZ Pattern = PRBS23	> 1.5			> 1.5			> 1.5			UI
	Jitter frequency = 250 KHz Pattern = PRBS23	> 0.15			> 0.15			> 0.15			UI
Jitter tolerance at 2488.32 Mbps	Jitter frequency = 0.06 KHz Pattern = PRBS23	> 15			> 15			> 15			UI
	Jitter frequency = 100 KHZ Pattern = PRBS23	> 1.5			> 1.5			> 1.5			UI
	Jitter frequency = 1 MHz Pattern = PRBS23	> 0.15			> 0.15			> 0.15			UI
	Jitter frequency = 10 MHz Pattern = PRBS23	> 0.15			> 0.15			> 0.15			UI
Fibre Channel Transmit Jitter Generation *(3)*, *(10)*											
Total jitter FC-1	Pattern = CRPAT	—	—	0.23	—	—	0.23	—	—	0.23	UI
Deterministic jitter FC-1	Pattern = CRPAT	—	—	0.11	—	—	0.11	—	—	0.11	UI
Total jitter FC-2	Pattern = CRPAT	—	—	0.33	—	—	0.33	—	—	0.33	UI
Deterministic jitter FC-2	Pattern = CRPAT	—	—	0.2	—	—	0.2	—	—	0.2	UI
Fibre Channel Receiver Jitter Tolerance *(3)*, *(11)*											
Deterministic jitter FC-1	Pattern = CJTPAT	> 0.37			> 0.37			> 0.37			UI
Random jitter FC-1	Pattern = CJTPAT	> 0.31			> 0.31			> 0.31			UI

Table 1–21. Arria II GX Transceiver Block AC Specification *(Note 1)*, *(2)* (Part 2 of 6)—Preliminary

Symbol/ Description	Conditions	C4			C5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Sinusoidal jitter FC-1	Fc/25000		> 1.5			> 1.5			> 1.5		UI
	Fc/1667		> 0.1			> 0.1			> 0.1		UI
Deterministic jitter FC-2	Pattern = CJTPAT		> 0.33			> 0.33			> 0.33		UI
Random jitter FC-2	Pattern = CJTPAT		> 0.29			> 0.29			> 0.29		UI
Sinusoidal jitter FC-2	Fc/25000		> 1.5			> 1.5			> 1.5		UI
	Fc/1667		> 0.1			> 0.1			> 0.1		UI
XAUI Transmit Jitter Generation *(4)*											
Total jitter at 3.125 Gbps	Pattern = CJPAT	—	—	0.3	—	—	0.3	—	—	0.3	UI
Deterministic jitter at 3.125 Gbps	Pattern = CJPAT	—	—	0.17	—	—	0.17	—	—	0.17	UI
XAUI Receiver Jitter Tolerance *(4)*											
Total jitter			> 0.65			> 0.65			> 0.65		UI
Deterministic jitter			> 0.37			> 0.37			> 0.37		UI
Peak-to-peak jitter	Jitter frequency = 22.1 KHz		> 8.5			> 8.5			> 8.5		UI
Peak-to-peak jitter	Jitter frequency = 1.875 MHz		> 0.1			> 0.1			> 0.1		UI
Peak-to-peak jitter	Jitter frequency = 20 MHz		> 0.1			> 0.1			> 0.1		UI
PCI Express Transmit Jitter Generation *(5)*											
Total jitter at 2.5 Gbps (Gen1)	Compliance pattern	—	—	0.25	—	—	0.25	—	—	0.25	UI
PCI Express Receiver Jitter Tolerance *(5)*											
Total jitter at 2.5 Gbps (Gen1)	Compliance pattern		> 0.6			> 0.6			> 0.6		UI
Serial RapidIO Transmit Jitter Generation *(6)*											
Deterministic jitter (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	—	—	0.17	—	—	0.17	—	—	0.17	UI
Total jitter (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	—	—	0.35	—	—	0.35	—	—	0.35	UI
Serial RapidIO Receiver Jitter Tolerance *(6)*											
Deterministic jitter tolerance (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT		> 0.37			> 0.37			> 0.37		UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT		> 0.55			> 0.55			> 0.55		UI

Table 1–21. Arria II GX Transceiver Block AC Specification *(Note 1)*, *(2)* (Part 3 of 6)—Preliminary

Symbol/ Description	Conditions	C4			C5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Sinusoidal jitter tolerance (peak-to-peak)	Jitter Frequency = 22.1 KHz Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	> 8.5			> 8.5			> 8.5			UI
	Jitter Frequency = 1.875 MHz Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	> 0.1			> 0.1			> 0.1			UI
	Jitter Frequency = 20 MHz Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	> 0.1			> 0.1			> 0.1			UI
GIGE Transmit Jitter Generation *(7)*											
Deterministic jitter (peak-to-peak)	Pattern = CRPAT	—	—	0.14	—	—	0.14	—	—	0.14	UI
Total jitter (peak-to-peak)	Pattern = CRPAT	—	—	0.279	—	—	0.279	—	—	0.279	UI
GIGE Receiver Jitter Tolerance *(7)*											
Deterministic jitter tolerance (peak-to-peak)	Pattern = CJPAT	> 0.4			> 0.4			> 0.4			UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Pattern = CJPAT	> 0.66			> 0.66			> 0.66			UI
HiGig Transmit Jitter Generation *(8)*											
Deterministic jitter (peak-to-peak)	Data Rate = 3.75 Gbps Pattern = CJPAT	—	—	0.17	—	—	—	—	—	—	UI
Total jitter (peak-to-peak)	Data Rate = 3.75 Gbps Pattern = CJPAT	—	—	0.35	—	—	—	—	—	—	UI
HiGig Receiver Jitter Tolerance *(8)*											
Deterministic jitter tolerance (peak-to-peak)	Data Rate = 3.75 Gbps Pattern = CJPAT	> 0.37			—	—	—	—	—	—	UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Data Rate = 3.75 Gbps Pattern = CJPAT	> 0.65			—	—	—	—	—	—	UI

Table 1–21. Arria II GX Transceiver Block AC Specification *(Note 1)*, *(2)* (Part 4 of 6)—Preliminary

Symbol/ Description	Conditions	C4			C5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Sinusoidal jitter tolerance (peak-to-peak)	Jitter Frequency = 22.1 KHz Data Rate = 3.75 Gbps Pattern = CJPAT	> 8.5			—	—	—	—	—	—	UI
	Jitter Frequency = 1.875MHz Data Rate = 3.75 Gbps Pattern = CJPAT	> 0.1			—	—	—	—	—	—	UI
	Jitter Frequency = 20 MHz Data Rate = 3.75 Gbps Pattern = CJPAT	> 0.1			—	—	—	—	—	—	UI
SDI Transmitter Jitter Generation *(9)*											
Alignment jitter (peak-to-peak)	Data Rate = 1.485 Gbps (HD) Pattern = Color Bar Low-Frequency Roll-Off = 100 KHz	0.2	—	—	0.2	—	—	0.2	—	—	UI
	Data Rate = 2.97 Gbps (3G) Pattern = Color Bar Low-Frequency Roll-Off = 100 KHz	0.3	—	—	0.3	—	—	0.3	—	—	UI

Table 1–21. Arria II GX Transceiver Block AC Specification *(Note 1)*, *(2)* (Part 5 of 6)—Preliminary

Symbol/ Description	Conditions	C4			C5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SDI Receiver Jitter Tolerance *(9)*											
Sinusoidal jitter tolerance (peak-to-peak)	Jitter Frequency = 15 KHz Data Rate = 2.97 Gbps (3G) Pattern = Single Line Scramble Color Bar		> 2			> 2			> 2		UI
	Jitter Frequency = 100 KHz Data Rate = 2.97 Gbps (3G) Pattern = Single Line Scramble Color Bar		> 0.3			> 0.3			> 0.3		UI
	Jitter Frequency = 148.5 MHz Data Rate = 2.97 Gbps (3G) Pattern = Single Line Scramble Color Bar		> 0.3			> 0.3			> 0.3		UI

Table 1–21. Arria II GX Transceiver Block AC Specification *(Note 1)*, *(2)* (Part 6 of 6)—Preliminary

Symbol/ Description	Conditions	C4			C5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Sinusoidal Jitter Tolerance (peak-to-peak)	Jitter Frequency = 20 KHz Data Rate = 1.485 Gbps (HD) Pattern = 75% Color Bar		> 1			> 1			> 1		UI
	Jitter Frequency = 100 KHz Data Rate = 1.485 Gbps (HD) Pattern = 75% Color Bar		> 0.2			> 0.2			> 0.2		UI
	Jitter Frequency = 148.5 MHz Data Rate = 1.485 Gbps (HD) Pattern =75% Color Bar		> 0.2			> 0.2			> 0.2		UI

Notes to Table 1–21:

(1) Dedicated `refclk` pins were used to drive the input reference clocks.
(2) The Jitter numbers specified are valid for the stated conditions only.
(3) The jitter numbers for Fibre Channel are compliant to the FC-PI-4 Specification revision 6.10.
(4) The jitter numbers for XAUI are compliant to the IEEE802.3ae-2002 Specification.
(5) The jitter numbers for PCI Express (PIPE) are compliant to the PCIe Base Specification 2.0.
(6) The jitter numbers for Serial RapidIO are compliant to the RapidIO Specification 1.3.
(7) The jitter numbers for GIGE are compliant to the IEEE802.3-2002 Specification.
(8) The jitter numbers for HiGig are compliant to the IEEE802.3ae-2002 Specification.
(9) The HD-SDI and 3G-SDI jitter numbers are compliant to the SMPTE292M and SMPTE424M Specifications.
(10) The Fibre Channel transmitter jitter generation numbers are compliant to the specification at δ_T inter operability point.
(11) The Fibre Channel receiver jitter tolerance numbers are compliant to the specification at δ_R interpretability point.

Core Performance Specifications for Arria II GX Devices

This section describes the clock tree, phase-locked loop (PLL), digital signal processing (DSP), embedded memory, configuration, and JTAG specifications.

Clock Tree Specifications

Table 1–22 lists the clock tree specifications for Arria II GX devices.

Table 1–22. Arria II GX Clock Tree Performance (Part 1 of 2)—Preliminary

Device	Performance *(1)*			Unit
	C4	C5,I5	C6	
EP2AGX20	500	500	400	MHz
EP2AGX30	500	500	400	MHz
EP2AGX45	500	500	400	MHz
EP2AGX65	500	500	400	MHz

Table 1–22. Arria II GX Clock Tree Performance (Part 2 of 2)—Preliminary

Device	Performance *(1)*			Unit
	C4	C5,I5	C6	
EP2AGX95	500	500	400	MHz
EP2AGX125	500	500	400	MHz
EP2AGX190	500	500	400	MHz
EP2AGX260	500	500	400	MHz

Note to Table 1–22:

(1) The performance specifications are applicable to GCLK and RCLK networks.

PLL Specifications

Table 1–23 describes the PLL specifications for Arria II GX devices.

Table 1–23. Arria II GX PLL Specifications (Part 1 of 2)—Preliminary

Symbol	Description	Min	Typ	Max	Unit
f_{IN}	Input clock frequency (from clock input pins residing in top/bottom banks)	5	—	472.5 *(1)*	MHz
	Input clock frequency (from clock input pins residing in right banks)	5	—	500	MHz
f_{INPFD}	Input frequency to the PFD	5	—	325	MHz
f_{VCO}	PLL VCO operating Range *(2)*	600	—	1300	MHz
f_{INDUTY}	Input clock duty cycle	40	—	60	%
$f_{EINDUTY}$	External feedback clock input duty cycle	40	—	60	%
t_{INCCJ}	Input clock cycle to cycle jitter	—	—	*(4)*	ps
f_{OUT}	Output frequency for internal global or regional clock	—	—	472.5	MHz
f_{OUT_EXT}	Output frequency for external clock output	—	—	472.5 *(3)*	MHz
$t_{OUTDUTY}$	Duty cycle for external clock output (when set to 50%)	45	50	55	%
t_{OUTPJ_DC}	Dedicated clock output period jitter	—	—	*(4)*	ps
t_{OUTPJ_IO}	Regular I/O clock output period jitter	—	—	*(4)*	ps
t_{FCOMP}	External feedback clock compensation time	—	—	10	ns
$t_{CONFIGPLL}$	Time required to reconfigure PLL scan chains	—	*(4)*	—	SCANCLK cycles
$t_{CONFIGPHASE}$	Time required to reconfigure phase shift	1	—	1	SCANCLK cycles
$f_{SCANCLK}$	SCANCLK frequency	—	—	100	MHz
t_{LOCK}	Time required to lock from end of device configuration	—	—	*(4)*	ms
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	*(4)*	ms
f_{CLBW}	PLL closed-loop low bandwidth range	—	*(4)*	—	MHz
	PLL closed-loop medium bandwidth range	—	*(4)*	—	MHz
	PLL closed-loop high bandwidth range	—	*(4)*	—	MHz
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	*(4)*	—	ps

Table 1–23. Arria II GX PLL Specifications (Part 2 of 2)—Preliminary

Symbol	Description	Min	Typ	Max	Unit
t_{ARESET}	Minimum pulse width on `areset` signal	10	—	—	ns

Notes to Table 1–23:

(1) F_{IN} is limited by I/O F_{MAX}.

(2) The VCO frequency reported by the Quartus II software in the PLL summary section of the compilation report takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f_{VCO} specification.

(3) This specification is limited by the lower of the two: I/O F_{max} or F_{out} of the PLL.

(4) Pending silicon characterization.

DSP Block Specifications

Table 1–24 describes the Arria II GX DSP block performance specifications.

Table 1–24. Arria II GX DSP Block Performance Specifications *(Note 1)* —Preliminary

Mode	Resources Used	Performance			Unit
	Number of Multipliers	C4	C5,I5	C6	
9 x 9-bit multiplier	1	315	245	200	MHz
12 x 12-bit multiplier	1	315	245	200	MHz
18 x 18-bit multiplier	1	350	275	225	MHz
36 x 36-bit multiplier	1	285	220	180	MHz
18 x 18-bit Multiply Accumulator	4	315	245	200	MHz
18 × 18-bit Multiply Adder	4	315	245	200	MHz
18 × 18-bit Multiply Adder-Signed Full Precision	2	315	245	200	MHz
18 × 18-bit Multiply Adder with loopback *(2)*	2	250	195	160	MHz
36-bit Shift (32-bit data)	1	285	220	180	MHz
Double mode	1	285	220	180	MHz

Notes to Table 1–24:

(1) Maximum is for fully-pipelined block with **Round** and **Saturation** disabled.

(2) Maximum is for non-pipelined block with loopback input registers disabled and **Round** and **Saturation** disabled.

Embedded Memory Block Specifications

Table 1–25 describes the Arria II GX embedded memory block specifications.

Table 1–25. Arria II GX Embedded Memory Block Performance Specifications (Part 1 of 2)—Preliminary

Memory	Mode	Resources Used		Performance			Unit
		ALUTs	Embedded Memory	C4	C5,I5	C6	
Memory Logic Array Block (MLAB)	Single port 64 × 10	0	1	500	500	400	MHz
	Simple dual-port 32 × 20 single clock	0	1	500	500	400	MHz
	Simple dual-port 64 × 10 single clock	0	1	500	500	400	MHz

Table 1–25. Arria II GX Embedded Memory Block Performance Specifications (Part 2 of 2)—Preliminary

Memory	Mode	Resources Used		Performance			Unit
		ALUTs	Embedded Memory	C4	C5,I5	C6	
M9K Block	Single-port 256 × 36	0	1	390	350	295	MHz
	Single-port 256 × 36, with the **read-during-write** option set to **Old Data**	0	1	250	225	190	MHz
	Simple dual-port 256 × 36 single CLK	0	1	390	350	295	MHz
	Single-port 256 × 36 single CLK, with the **read-during-write** option set to **Old Data**	0	1	250	225	190	MHz
	True dual port 512 × 18 single CLK	0	1	390	350	295	MHz
	True dual-port 512 × 18 single CLK, with the **read-during-write** option set to **Old Data**	0	1	250	225	190	MHz

Configuration

Table 1–26 lists the Arria II GX configuration mode specifications.

Table 1–26. Arria II GX Configuration Mode Specifications—Preliminary

Programming Mode	DCLK F_{MAX}	Unit
Passive Serial	125	MHz
Fast Passive Parallel	125	MHz
Fast Active Serial	40	MHz
Remote Update only in Fast AS mode	10	MHz

JTAG Specifications

Table 1–27 lists the JTAG timing parameters and values for Arria II GX devices.

Table 1–27. Arria II GX JTAG Timing Parameters and Values—Preliminary

Symbol	Description	Min	Max	Unit
t_{JCP}	TCK clock period	30	—	ns
t_{JCH}	TCK clock high time	14	—	ns
t_{JCL}	TCK clock low time	14	—	ns
$t_{JPSU\ (TDI)}$	TDI JTAG port setup time	1	—	ns
$t_{JPSU\ (TMS)}$	TMS JTAG port setup time	3	—	ns
t_{JPH}	JTAG port hold time	5	—	ns
t_{JPCO}	JTAG port clock to output	—	11 *(1)*	ns
t_{JPZX}	JTAG port high impedance to valid output	—	14 *(1)*	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	14 *(1)*	ns

Note to Table 1–27:

(1) A 1-ns adder is required for each V_{CCIO} voltage step down from 3.3 V. For example, t_{JPCO} = 12 ns if V_{CCIO} of the TDO I/O bank = 2.5 V, or 13 ns if it equals to 1.8 V.

Periphery Performance

This section describes periphery performance, including high-speed I/O and external memory interface.

I/O performance supports several system interfacing, for example the high-speed I/O interface, external memory interface, and the PCI/PCI-X bus interface. I/O using SSTL-18 Class I termination standard can achieve up to the stated DDR2 SDRAM interfacing speed as indicated in Table 1–30 with typical DDR2 SDRAM memory interface setup. I/O using general-purpose I/O standards such as 3.0, 2.5, 1.8, or 1.5 LVTTL/LVCMOS are capable of typical 200 MHz interfacing frequency with 10pF load.

☞ Actual achievable frequency depends on design- and system-specific factors. You should perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

High-Speed I/O Specification

Table 1–28 lists the high-speed I/O timing for Arria II GX devices.

Table 1–28. High-Speed I/O Specifications **(Part 1 of 2)**

Symbol	Conditions	C4		C5,I5		C6		Unit
		Min	Max	Min	Max	Min	Max	
Clock								
f_{HSCLK_IN} (input clock frequency)	Clock boost factor, W = 1 to 40 *(1)*	5	500	5	472.5	5	472.5	MHz
f_{HSCLK_OUT} (output clock frequency)	—	5	500	5	472.5	5	472.5	MHz
Transmitter								
f_{HSDR_TX} (true LVDS output data rate)	SERDES factor, J = 3 to 10 (using dedicated SERDES)	150	1000 *(2)*	150	840	150	740	Mbps
	SERDES factor, J = 4 to 10 (using logic elements as SERDES)	*(3)*	945	*(3)*	740	*(3)*	640	Mbps
	SERDES factor, J = 2 (using DDR registers) and J = 1 (using SDR register)	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	Mbps
$f_{HSDR\_TX\_E3R}$ (emulated LVDS_E_3R output data rate)	SERDES factor, J = 4 to 10	*(3)*	640	*(3)*	640	*(3)*	550	Mbps
t_{TX_JITTER} *(4)*	Data rate between 600 Mbps to 1 Gbps	—	160	—	160	—	160	ps
	Data rate < 600 Mbps	—	0.1	—	0.1	—	0.1	UI

Table 1–28. High-Speed I/O Specifications **(Part 2 of 2)**

Symbol	Conditions	C4		C5,I5		C6		Unit
		Min	Max	Min	Max	Min	Max	
t_{TX_DCD}	True LVDS and Emulated LVDS_E_3R	45	55	45	55	45	55	%
t_{RISE} & t_{FALL}	True LVDS	—	200	—	200	—	200	ps
	Emulated LVDS_E_3R	—	350	—	350	—	350	ps
TCCS	True LVDS *(4)*	—	100	—	100	—	100	ps
	Emulated LVDS_E_3R	—	250	—	250	—	250	ps
Receiver *(5)*								
f_{HSDR_RX}	DPA mode *(5)*	150	1000	150	840	150	740	Mbps
	Non-DPA mode	*(3)*	945 *(5)*	*(3)*	740	*(3)*	640	Mbps
DPA run length	DPA mode	—	10000	—	10000	—	10000	UI
SW	Non-DPA mode *(4)*	—	300	—	300	—	300	ps

Notes to Table 1–28:

(1) $f_{HSCLK\_IN} = f_{HSDR} / W$. Use W to determine the supported selection of input reference clock frequencies for the desired data rate.

(2) This applies to interfacing with DPA receivers. For interfacing with non-DPA receivers, maximum supported data rate is 945 Mbps. Beyond 840 Mbps, PCB trace compensation is required.

(3) The minimum and maximum specification is dependent on the clock source (for example, PLL and clock pin) and the clock routing resource you use (global, regional, or local). The I/O differential buffer and input register do not have a minimum toggle rate.

(4) Specification is only applicable for true LVDS using dedicated SERDES.

(5) Dedicated SERDES and DPA features are only available on right banks.

(6) PCB trace compensation refers to the adjustment of PCB trace length for LVDS channels to improve channel-to-channel skews, and is required to support data rate beyond 840 Mbps.

Table 1–29 shows DPA lock time specifications for Arria II GX devices.

Table 1–29. DPA Lock Time Specifications—Preliminary

Standard	Training Pattern	Transition Density	Min
SPI-4	00000000001111111111	10%	*(1)*
Parallel Rapid I/O	00001111	25%	*(1)*
	10010000	50%	*(1)*
Miscellaneous	10101010	100%	*(1)*
	01010101	—	*(1)*

Note to Table 1–29:

(1) Pending silicon characterization.

External Memory Interface Specifications

Table 1–30 lists the maximum clock rate support for external memory interfaces with the half-rate controller for the Arria II GX device family.

☞ Use Table 1–30 for memory interface timing analysis.

Table 1–30. Arria II GX Maximum Clock Rate Support for External Memory Interfaces with Half-Rate Controller *(Note 1)*, *(2)*, *(3)*—Preliminary

Memory Standards	C4 Speed Grade (MHz)	C5,I5 Speed Grade (MHz)	C6 Speed Grade (MHz)
DDR3 SDRAM *(4)*	300	N/A	N/A
DDR2 SDRAM *(5)*	300 *(6)*	267 *(7)*	200
DDR SDRAM *(5)*	200	200	200
QDRII SRAM *(8)*, *(9)*	250	250	200

Notes to Table 1–30:

(1) These numbers are preliminary until characterization is final. The supported operating frequencies listed here are memory interface maximums for the FPGA device family. Your design's actual achievable performance is based on design- and system-specific factors, as well as static timing analysis of the completed design.

(2) The maximum clock rates are applicable to Class I termination. The maximum clock rates can be lower for Class II termination.

(3) The values apply to column I/Os, row I/Os, and wraparound interface. Column I/Os refer to top and bottom I/Os while row I/Os refer to the left and right I/Os. Wraparound interface refers to interfaces with multiple DQ/DQS groups wrapping over column I/Os and row I/Os of the device.

(4) Arria II GX devices support DDR3 SDRAM components only if no levelling support is required for DDR3 DIMMs. Interfaces with multiple DDR3 SDRAM components require component arrangement according to DDR2 DIMM tree topology.

(5) This applies to interfaces with both components and single rank modules.

(6) The 300-MHz DDR2 interface requires the use of 400-MHz DDR2 SDRAM modules or components.

(7) The 267-MHz DDR2 interface requires the use of 333-MHz DDR2 SDRAM modules or components.

(8) QDRII SRAM supports 1.8-V and 1.5-V HSTL I/O standards. However, Altera recommends using the 1.8-V HSTL I/O standard for maximum performance because of the higher I/O drive strength.

(9) Arria II GX devices feature I/Os capable of electrical support for QDRII. However, Altera does not currently supply a controller or PHY megafunction for QDRII interfaces.

Table 1–31 lists the maximum clock rate support for external memory interfaces with the full-rate controller for the Arria II GX device family.

Table 1–31. Arria II GX Maximum Clock Rate Support for External Memory Interfaces with Full-Rate PHY *(Note 1)*, *(2)*, *(3)*

Memory Standards	C4 Speed Grade (MHz)		C5,I5 Speed Grade (MHz)		C6 Speed Grade (MHz)	
	Row/Column I/Os	Wraparound Interface *(4)*	Row/Column I/Os	Wraparound Interface *(4)*	Row/Column I/Os	Wraparound Interface *(4)*
DDR2 SDRAM	267 *(5)*	233 *(5)*	233 *(6)*	200 *(6)*	200	167
DDR SDRAM	200	200	200	200	200	167

Notes to Table 1–31:

(1) These numbers are preliminary until characterization is final. The supported operating frequencies listed here are the maximum memory interface for the FPGA device family. Your design's actual achievable performance is based on design- and system-specific factors, as well as static timing analysis of the completed design.

(2) This applies to interfaces with both components and single-rank modules.

(3) It may be possible to close timing at a higher maximum clock rate than those stated above, depending on your design and the Quartus settings used. For more information, refer to the "Advanced Settings" section in the *External Memory PHY Interface (ALTMEMPHY) Megafunction User Guide*.

(4) Wraparound interface refers to interface with multiple DQS/DQ groups wrapping over column I/Os and row I/Os of the device.

(5) This interface requires the use of 333-MHz DDR2 SDRAM modules or components.

(6) This interface requires the use of 267-MHz DDR2 SDRAM modules or components.

DLL and DQS Logic Block Specifications

Table 1–32 lists DLL frequency range specifications for Arria II GX devices.

Table 1–32. Arria II GX DLL Frequency Range Specifications—Preliminary

Frequency Mode	Frequency Range (MHz)			Resolution (°)
	C4	C5,I5	C6	
0	90 – 150	90 – 140	90 – 120	22.5
1	120 – 200	120 – 190	120 – 170	30
2	150 – 240	150 – 230	150 – 200	36
3	180 – 300	180 – 290	180 – 250	45
4	240 – 370	240 – 350	240 – 310	30
5	290 – 450	290 – 420	290 – 370	36

Table 1–33 lists the DQS phase offset delay per stage for Arria II GX devices.

Table 1–33. DQS Phase Offset Delay Per Setting *(Note 1)*, *(2)*, *(3)*—Preliminary

Speed Grade	Min	Max	Unit
C4	7.0	13.0	ps
C5,I5	*(4)*	*(4)*	ps

Table 1–33. DQS Phase Offset Delay Per Setting *(Note 1)*, *(2)*, *(3)*—Preliminary

Speed Grade	Min	Max	Unit
C6	8.5	15.5	ps

Notes to Table 1–33:

(1) The valid settings for phase offset are -64 to +63 for frequency modes 0 to 3 and -32 to +31 for frequency modes 4 to 5.
(2) The typical value equals the average of the minimum and maximum values.
(3) Delay settings are linear.
(4) Pending silicon characterization.

Duty Cycle Distortion (DCD) Specifications

Table 1–34 lists the worst-case DCD for Arria II GX devices.

Table 1–34. Duty Cycle Distortion on Arria II GX I/O Pins *(Note 1)* —Preliminary

Symbol	C4		C5,I5		C6		Unit
	Min	Max	Min	Max	Min	Max	
Output Duty Cycle	45	55	45	55	45	55	%

Note to Table 1–34:

(1) Preliminary DCD specification applies to clock outputs from PLLs, global clock tree, and I/O elements (IOE) driving dedicated and general purpose I/O pins.

I/O Timing

Altera offers two ways to determine I/O timing:

- the Excel-based I/O Timing.
- the Quartus II Timing Analyzer.

The Excel-based I/O Timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis. The Quartus II Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after place-and-route is complete.

The Excel-based I/O Timing spreadsheet is downloadable from Arria II GX Devices Literature webpage.

Glossary

Table 1–35 shows the glossary for this chapter.

Table 1–35. Glossary (Part 1 of 4)

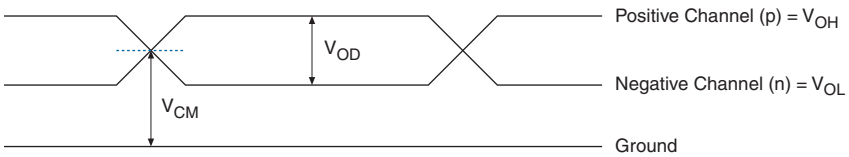
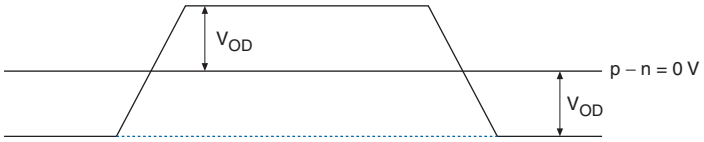
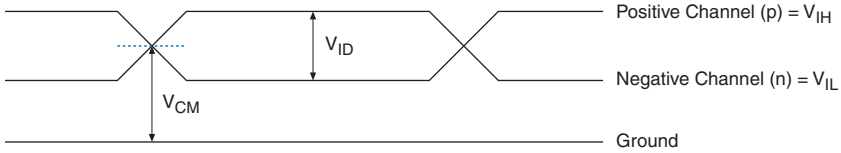
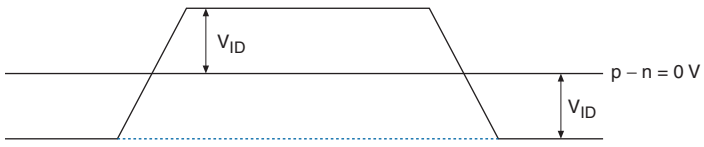
Letter	Subject	Definitions
A	—	—
B	—	—
C	—	—
D	Differential I/O Standards	*Receiver Input Waveforms* **Single-Ended Waveform**  **Differential Waveform**  *Transmitter Output Waveforms* **Single-Ended Waveform**  **Differential Waveform** 
E	—	—
F	f_{HSCLK}	Left/Right PLL input clock frequency.
	f_{HSDR}	High-Speed I/O Block: Maximum/minimum LVDS data transfer rate (f_{HSDR} = 1/TUI), non-DPA.
	$f_{HSDRDPA}$	High-Speed I/O Block: Maximum/minimum LVDS data transfer rate ($f_{HSDRDPA}$ = 1/TUI), DPA.

Table 1–35. Glossary (Part 2 of 4)

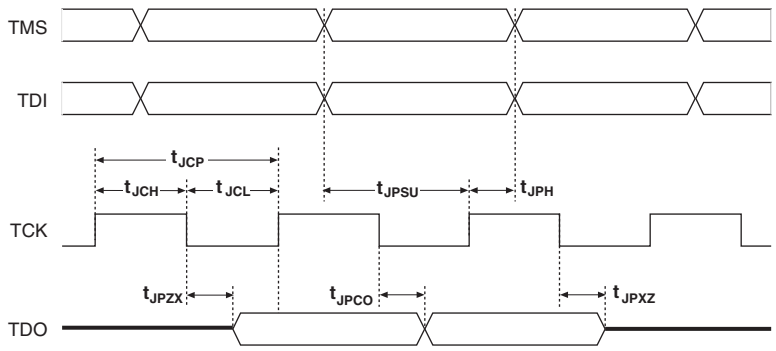
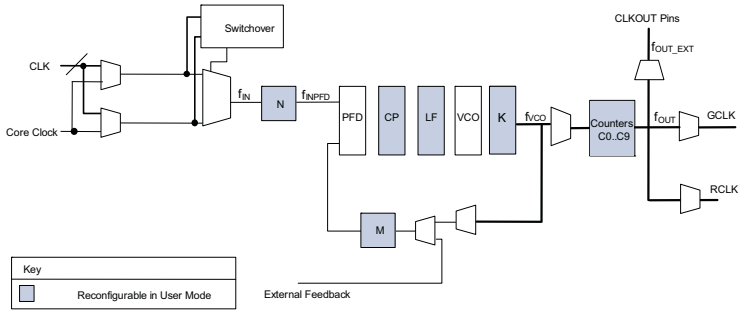
Letter	Subject	Definitions
G	—	—
H	—	—
I	—	—
J	J	High-Speed I/O Block: Deserialization factor (width of parallel data bus).
	JTAG Timing Specifications	JTAG Timing Specifications are in the following figure: 
K	—	—
L	—	—
M	—	—
N	—	—
O	—	—
P	PLL Specifications	The block diagram shown in the following figure highlights the PLL Specification parameters: **Diagram of PLL Specifications (1)**  **Note:** (1) CoreClock can only be fed by dedicated clock input pins or PLL outputs.
Q	—	—
R	R_L	Receiver differential input discrete resistor (external to the Arria II GX device).

Table 1–35. Glossary (Part 3 of 4)

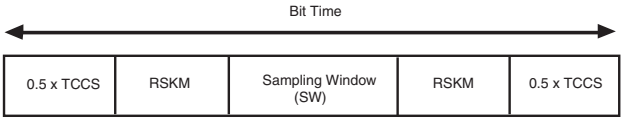
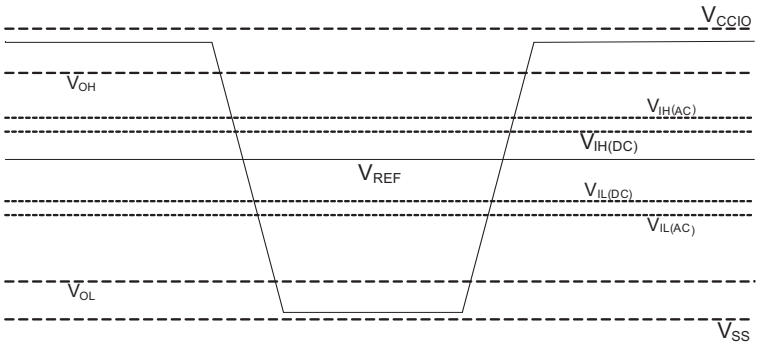
Letter	Subject	Definitions
S	SW (sampling window)	The period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window: *Timing Diagram* 
	Single-ended Voltage Referenced I/O Standard	The JEDEC standard for SSTL and HSTL I/O standards define both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. Once the receiver input has crossed the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the AC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing: *Single-Ended Voltage Referenced I/O Standard* 
T	t_C	High-speed receiver and transmitter input and output clock period.
	TCCS (channel-to-channel-skew)	The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the *Timing Diagram* figure under **S** in this table).
	t_{DUTY}	High-speed I/O Block: Duty cycle on high-speed transmitter output clock.
		Timing Unit Interval (TUI) The timing budget allowed for skew, propagation delays, and data sampling window. (TUI = 1/(Receiver Input Clock Frequency Multiplication Factor) = t_C/w)
	t_{FALL}	Signal high-to-low transition time (80-20%)
	t_{INCCJ}	Cycle-to-cycle jitter tolerance on PLL clock input
	t_{OUTPJ_IO}	Period jitter on general purpose I/O driven by a PLL
	t_{OUTPJ_DC}	Period jitter on dedicated clock output driven by a PLL
	t_{RISE}	Signal low-to-high transition time (20-80%)
U	—	—

Table 1–35. Glossary (Part 4 of 4)

Letter	Subject	Definitions
V	$V_{CM(DC)}$	DC Common Mode Input Voltage.
	V_{ICM}	Input Common Mode Voltage: The common mode of the differential signal at the receiver.
	V_{ID}	Input differential Voltage Swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
	$V_{DIF(AC)}$	AC differential Input Voltage: Minimum AC input differential voltage required for switching.
	$V_{DIF(DC)}$	DC differential Input Voltage: Minimum DC input differential voltage required for switching.
	V_{IH}	Voltage Input High: The minimum positive voltage applied to the input which will be accepted by the device as a logic high.
	$V_{IH(AC)}$	High-level AC input voltage
	$V_{IH(DC)}$	High-level DC input voltage
	V_{IL}	Voltage Input Low: The maximum positive voltage applied to the input which will be accepted by the device as a logic low.
	$V_{IL(AC)}$	Low-level AC input voltage
	$V_{IL(DC)}$	Low-level DC input voltage
	V_{OCM}	Output Common Mode Voltage: The common mode of the differential signal at the transmitter.
	V_{OD}	Output differential Voltage Swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter.
W	W	High-Speed I/O BLOCK: Clock Boost Factor
X	—	—
Y	—	—
Z	—	—

Document Revision History

Table 1–36 shows the revision history for this chapter.

Table 1–36. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
June 2009, v1.2	■ Updated Table 1–1, Table 1–3, Table 1–6, Table 1–7, Table 1–17, Table 1–22, Table 1–24, Table 1–25, Table 1–28, Table 1–29, Table 1–30, Table 1–32, Table 1–33, and Table 1–34. ■ Added Table 1–31. ■ Updated Equation 1–1.	—
March 2009, v1.1	Added “I/O Timing” section.	—
February 2009, v1.0	Initial release.	—