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TMS320F28032, TMS320F28033
TMS320F28034, TMS320F28035
Piccolo Microcontrollers

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1 TMS320F2803x (Piccolo™) MCUs

1.1 Features

- **High-Efficiency 32-Bit CPU (TMS320C28x™)**
  - **60 MHz (16.67-ns Cycle Time)**
  - **16 x 16 and 32 x 32 MAC Operations**
  - **16 x 16 Dual MAC**
  - **Harvard Bus Architecture**
  - **Atomic Operations**
  - **Fast Interrupt Response and Processing**
  - **Unified Memory Programming Model**
  - **Code-Efficient (in C/C++ and Assembly)**
- **Programmable Control Law Accelerator (CLA)**
  - **32-bit floating-point math accelerator**
  - **Executes code independently of the main CPU**
- **Low Device and System Cost:**
  - **Single 3.3-V Supply**
  - **No Power Sequencing Requirement**
  - **Integrated Power-on Reset and Brown-out Reset**
  - **Low Power**
  - **No Analog Support Pins**
- **Clocking:**
  - **2 Internal Zero-pin Oscillators**
  - **On-chip Crystal Oscillator/External Clock Input**
  - **Dynamic PLL Ratio Changes Supported**
  - **Watchdog Timer Module**
  - **Missing Clock Detection Circuitry**
- **Up to 45 Individually Programmable, Multiplexed GPIO Pins With Input Filtering**
- **Peripheral Interrupt Expansion (PIE) Block That Supports All Peripheral Interrupts**

- **Three 32-Bit CPU Timers**
- **Independent 16-bit Timer in Each ePWM Module**
- **On-Chip Memory**
  - **Flash, SARAM, OTP, Boot ROM Available**
- **128-Bit Security Key/Lock**
  - **Protects Secure Memory Blocks**
  - **Prevents Firmware Reverse Engineering**
- **Serial Port Peripherals**
  - **One SCI (UART) Module**
  - **Two SPI Modules**
  - **One Inter-Integrated-Circuit (I2C) Bus**
  - **One Local Interconnect Network (LIN) Bus**
  - **One Enhanced Controller Area Network (eCAN) Bus**
- **Advanced Emulation Features**
  - **Analysis and Breakpoint Functions**
  - **Real-Time Debug via Hardware**
- **Enhanced Control Peripherals**
  - **Enhanced Pulse Width Modulator (ePWM)**
  - **High-resolution PWM (HRPWM)**
  - **Enhanced Capture (eCAP)**
  - **Enhanced Quadrature Encoder Pulse (eQEP)**
  - **Analog-to-Digital Converter (ADC)**
  - **On-Chip Temperature Sensor**
  - **Comparator**
- **2803x Packages**
  - **64-Pin PAG Plastic Small-Outline Package (TQFP)**
  - **80-Pin PN Plastic Quad Flatpack (LQFP)**

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1.2 Description

The F2803x Piccolo™ family of microcontrollers provides the power of the C28x™ core and Control Law Accelerator (CLA) coupled with highly integrated control peripherals in low pin-count devices. This family is code compatible with previous C28-based code, as well as providing a high level of analog integration.

An internal voltage regulator allows for single rail operation. Enhancements have been made to the HRPWM module to allow for dual-edge control (frequency modulation). Analog comparators with internal 10-bit references have been added and can be routed directly to control the PWM outputs. The ADC converts from 0 to 3.3-V fixed full scale range and supports ratio-metric V_{REFHI}/V_{REFLO} references. The ADC interface has been optimized for low overhead/latency.

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1.3 Getting Started

This section gives a brief overview of the steps to take when first developing for a C28x device. For more detail on each of these steps, see the following:

- *Getting Started With TMS320C28x Digital Signal Controllers* (literature number SPRAAM0).
- C2000 Getting Started Website (http://www.ti.com/c2000getstarted)
- TMS320F28x MCU Development and Experimenter's Kits (http://www.ti.com/f28xkits)

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2 Hardware Features

Table 2-1 lists the features of the TMS320F2803x devices.

Table 2-1. Hardware Features

FEATURE		TYPE	28032 (60 MHz)		28033 (60 MHz)		28034 (60 MHz)		28035 (60 MHz)	
Package Type			64-Pin PAG TQFP	80-Pin PN LQFP	64-Pin PAG TQFP	80-Pin PN LQFP	64-Pin PAG TQFP	80-Pin PN LQFP	64-Pin PAG TQFP	80-Pin PN LQFP
Instruction cycle		–	16.67 ns		16.67 ns		16.67 ns		16.67 ns	
Control Law Accelerator		0	No		Yes		No		Yes	
On-chip flash (16-bit word)		–	32K		32K		64K		64K	
On-chip SARAM (16-bit word)		–	10K		10K		10K		10K	
Code security for on-chip flash/SARAM/OTP blocks		–	Yes		Yes		Yes		Yes	
Boot ROM (8K X16)		–	Yes		Yes		Yes		Yes	
One-time programmable (OTP) ROM (16-bit word)		–	1K		1K		1K		1K	
ePWM outputs		1	12	14	12	14	12	14	12	14
eCAP inputs		0	1		1		1		1	
eQEP modules		0	1		1		1		1	
Watchdog timer		–	Yes		Yes		Yes		Yes	
12-Bit ADC	MSPS	3	4.6		4.6		4.6		4.6	
	Conversion Time		216.67 ns		216.67 ns		216.67 ns		216.67 ns	
	Channels		14	16	14	16	14	16	14	16
	Temperature Sensor		Yes		Yes		Yes		Yes	
32-Bit CPU timers		–	3		3		3		3	
HiRES ePWM Channels		1	6	7	6	7	6	7	6	7
Comparators w/ Integrated DACs		0	3		3		3		3	
Inter-integrated circuit (I2C)		0	1		1		1		1	
Enhanced Controller Area Network (eCAN)		0	1		1		1		1	
Local Interconnect Network (LIN)		0	1		1		1		1	
Serial Peripheral Interface (SPI)		1	1	2	1	2	1	2	1	2
Serial Communications Interface (SCI)		0	1		1		1		1	
I/O pins (shared)	GPIO	–	33	45	33	45	33	45	33	45
	AIO	–	6		6		6		6	
External interrupts		–	3		3		3		3	
Supply voltage (nominal)		–	3.3 V		3.3 V		3.3 V		3.3 V	
Temperature options	T: - 40°C to 105°C	–	Yes		Yes		Yes		Yes	
	S: - 40°C to 125°C	–	TBD		TBD		TBD		TBD	
Product status		–	TMX		TMX		TMX		TMX	

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2.1 Pin Assignments

Figure 2-1 shows the 64-pin PAG Plastic Small Outline Package (TQFP) pin assignments. Figure 2-2 shows the 80-pin PN Plastic Quad Flatpack (LQFP) pin assignments.
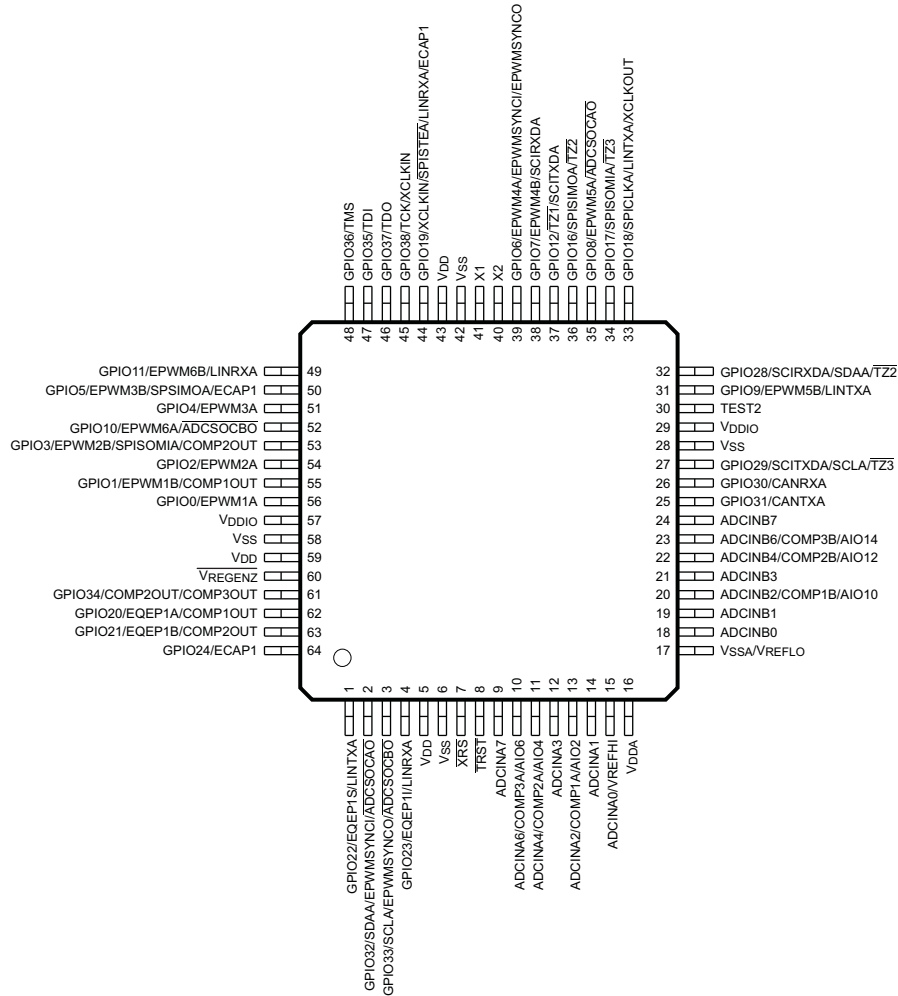
Figure 2-1. 2803x 64-Pin PAG TQFP (Top View)

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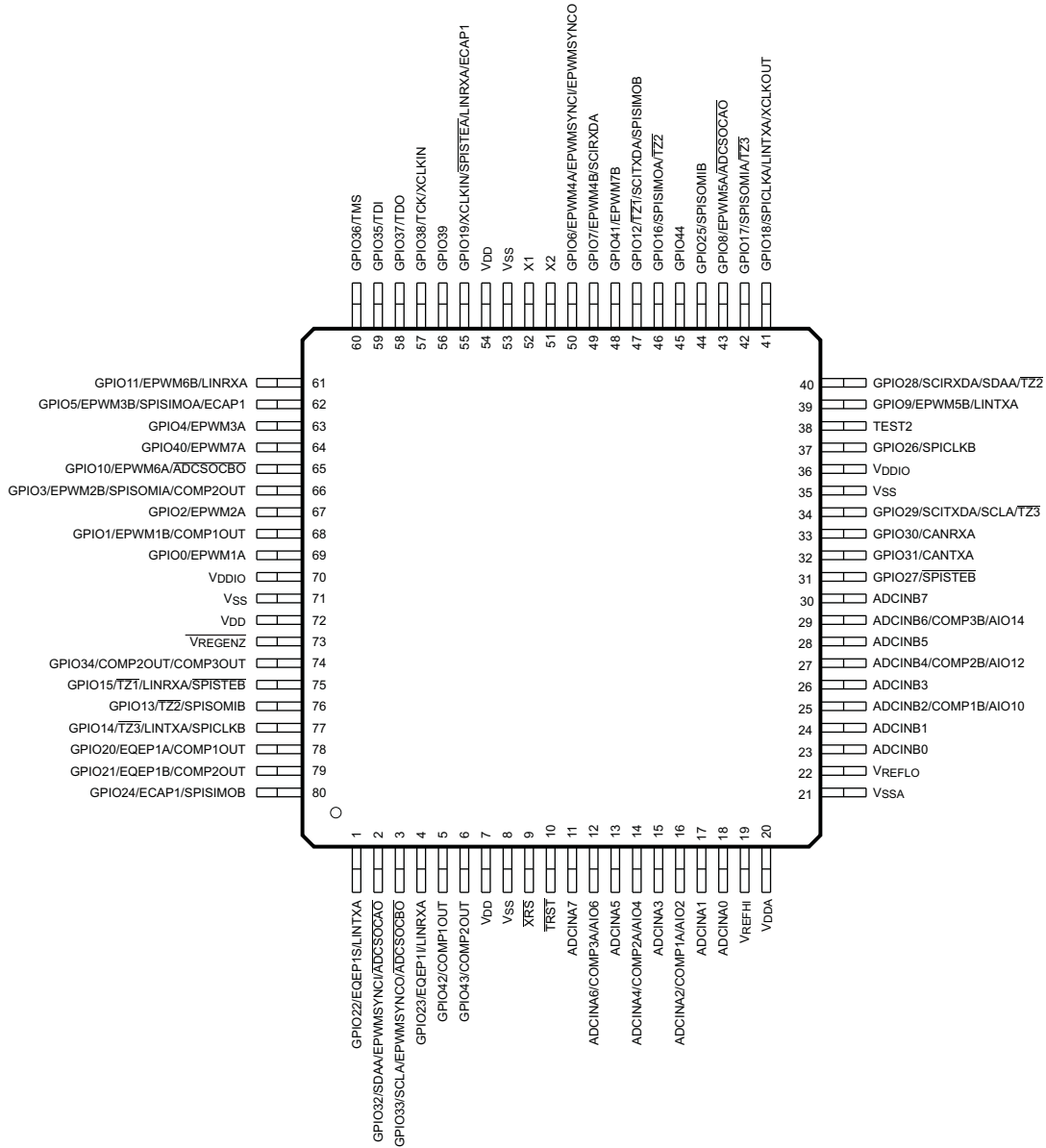
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Figure 2-2. 2803x 80-Pin PN LQFP (Top View)

2.2 Signal Descriptions

Table 2-2. TERMINAL FUNCTIONS[1]

TERMINAL			I/O/Z	DESCRIPTION
NAME	PN PIN #	PAG PIN #		
JTAG				
$\overline{\text{TRST}}$	10	8	I	JTAG test reset with internal pulldown. $\overline{\text{TRST}}$, when driven high, gives the scan system control of the operations of the device. If this signal is not connected or driven low, the device operates in its functional mode, and the test reset signals are ignored. NOTE: $\overline{\text{TRST}}$ is an active high test pin and must be maintained low at all times during normal device operation. An external pulldown resistor is recommended on this pin. The value of this resistor should be based on drive strength of the debugger pods applicable to the design. A 2.2-kΩ resistor generally offers adequate protection. Since this is application-specific, it is recommended that each target board be validated for proper operation of the debugger and the application. (↓)
TCK	See GPIO38		I	See GPIO38. JTAG test clock with internal pullup (↑)
TMS	See GPIO36		I	See GPIO36. JTAG test-mode select (TMS) with internal pullup. This serial control input is clocked into the TAP controller on the rising edge of TCK. (↑)
TDI	See GPIO35		I	See GPIO35. JTAG test data input (TDI) with internal pullup. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK. (↑)
TDO	See GPIO37		O/Z	See GPIO37. JTAG scan out, test data output (TDO). The contents of the selected register (instruction or data) are shifted out of TDO on the falling edge of TCK. (8 mA drive)
FLASH				
TEST2	38	30	I/O	Test Pin. Reserved for TI. Must be left unconnected.
CLOCK				
XCLKOUT	See GPIO18		O/Z	See GPIO18. Output clock derived from SYSCLKOUT. XCLKOUT is either the same frequency, one-half the frequency, or one-fourth the frequency of SYSCLKOUT. This is controlled by bits 1:0 (XCLKOUTDIV) in the XCLK register. At reset, XCLKOUT = SYSCLKOUT/4. The XCLKOUT signal can be turned off by setting XCLKOUTDIV to 3. The mux control for GPIO18 must also be set to XCLKOUT for this signal to propogate to the pin.
XCLKIN	See GPIO19 and GPIO38		I	See GPIO19 and GPIO38. External oscillator input. Pin source for the clock is controlled by the XCLKINSEL bit in the XCLK register, GPIO38 is the default selection. This pin feeds a clock from an external 3.3-V oscillator. In this case, the X1 pin, if available, must be tied to GND and the on-chip crystal oscillator must be disabled via bit 14 in the CLKCTL register. If a crystal/resonator is used, the XCLKIN path must be disabled by bit 13 in the CLKCTL register. Note: Designs that use the GPIO38/TCK/XCLKIN pin to supply an external clock for normal device operation may need to incorporate some hooks to disable this path during debug using the JTAG connector. This is to prevent contention with the TCK signal, which is active during JTAG debug sessions. The zero-pin internal oscillators may be used during this time to clock the device.
X1	52	41	I	On-chip crystal-oscillator input. To use this oscillator, a quartz crystal or a ceramic resonator must be connected across X1 and X2. In this case, the XCLKIN path must be disabled by bit 13 in the CLKCTL register. If this pin is not used, it must be tied to GND. (I)
X2	51	40	O	On-chip crystal-oscillator output. A quartz crystal or a ceramic resonator must be connected across X1 and X2. If X2 is not used, it must be left unconnected. (O)

(1) I = Input, O = Output, Z = High Impedance, OD = Open Drain, ↑ = Pullup, ↓ = Pulldown

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Table 2-2. TERMINAL FUNCTIONS (continued)

TERMINAL			I/O/Z	DESCRIPTION
NAME	**PN PIN #**	**PAG PIN #**		
RESET				
$\overline{\text{XRS}}$	9	7	I/O	Device Reset (in) and Watchdog Reset (out). Piccolo devices have a built-in power-on-reset (POR) and brown-out-reset (BOR) circuitry. As such, no external circuitry is needed to generate a reset pulse. During a power-on or brown-out condition, this pin is driven low by the device. See the electrical section for thresholds of the POR/BOR block. This pin is also driven low by the MCU when a watchdog reset occurs. During watchdog reset, the $\overline{\text{XRS}}$ pin is driven low for the watchdog reset duration of 512 OSCCLK cycles. If need be, an external circuitry may also drive this pin to assert a device reset. In this case, it is recommended that this pin be driven by an open-drain device An R-C circuit must be connected to this pin for noise immunity reasons. Regardless of the source, a device reset causes the device to terminate execution. The program counter points to the address contained at the location 0x3FFFC0. When reset is deactivated, execution begins at the location designated by the program counter. The output buffer of this pin is an open-drain with an internal pullup. (I/OD)
ADC, COMPARATOR, ANALOG I/O				
ADCINA7	11	9	I	ADC Group A, Channel 7 input
ADCINA6 COMP3A AIO6	12	10	I I/O	ADC Group A, Channel 6 input Comparator Input 3A Digital AIO 6
ADCINA5	13	–		
ADCINA4 COMP2A AIO4	14	11	I I I/O	ADC Group A, Channel 4 input Comparator Input 2A Digital AIO 4
ADCINA3	15	12	I	ADC Group A, Channel 3 input
ADCINA2 COMP1A AIO2	16	13	I I I/O	ADC Group A, Channel 2 input Comparator Input 1A Digital AIO 2
ADCINA1	17	14	I	ADC Group A, Channel 1 input
ADCINA0	18	15	I	ADC Group A, Channel 0 input
VREFHI	19	15		ADC External Reference – only used when in ADC external reference mode. See ADC Section.
ADCINB7	30	24	I	ADC Group B, Channel 7 input
ADCINB6 COMP3B AIO14	29	23	I I/O	ADC Group B, Channel 6 input Comparator Input 3B Digital AIO 14
ADCINB5	28	–		
ADCINB4 COMP2B AIO12	27	22	I I I/O	ADC Group B, Channel 4 input Comparator Input 2B Digital AIO12
ADCINB3	26	21	I	ADC Group B, Channel 3 input
ADCINB2 COMP1B AIO10	25	20	I I I/O	ADC Group B, Channel 2 input Comparator Input 1B Digital AIO 10
ADCINB1	24	19	I	ADC Group B, Channel 1 input
ADCINB0	23	18		
VREFLO	22	17		
CPU AND I/O POWER				
V_{DDA}	20	16		Analog Power Pin
V_{SSA}	21	17		Analog Ground Pin
V_{DD}	7	5		CPU and Logic Digital Power Pins – no supply source needed when using internal VREG. Tie with 1.2 µF (minimum) ceramic capacitor to ground when using internal VREG.
V_{DD}	54	43		
V_{DD}	72	59		

Table 2-2. TERMINAL FUNCTIONS (continued)

TERMINAL			I/O/Z	DESCRIPTION
NAME	PN PIN #	PAG PIN #		
V_{DDIO}	36	29		Digital I/O and Flash Power Pin – Single Supply source when VREG is enabled
V_{DDIO}	70	57		
V_{SS}	8	6		Digital Ground Pins
V_{SS}	35	28		
V_{SS}	53	42		
V_{SS}	71	58		
VOLTAGE REGULATOR CONTROL SIGNAL				
$\overline{\text{VREGENZ}}$	73	60	I	Internal VREG Enable/Disable – pull low to enable VREG, pull high to disable VREG
GPIO AND PERIPHERAL SIGNALS				
GPIO0	69	56	I/O/Z	General purpose input/output 0
EPWM1A			O	Enhanced PWM1 Output A and HRPWM channel
–			–	–
–			–	–
GPIO1	68	55	I/O/Z	General purpose input/output 1
EPWM1B			O	Enhanced PWM1 Output B
–			–	–
COMP1OUT			O	Direct output of Comparator 1
GPIO2	67	54	I/O/Z	General purpose input/output 2
EPWM2A			O	Enhanced PWM2 Output A and HRPWM channel
–			–	–
–			–	–
GPIO3	66	53	I/O/Z	General purpose input/output 3
EPWM2B			O	Enhanced PWM2 Output B
SPISOMIA			I/O	SPI-A slave out, master in
COMP2OUT			O	Direct output of Comparator 2
GPIO4	63	51	I/O/Z	General purpose input/output 4
EPWM3A			O	Enhanced PWM3 output A and HRPWM channel
–			–	–
–			–	–
GPIO5	62	50	I/O/Z	General purpose input/output 5
EPWM3B			O	Enhanced PWM3 output B
SPISIMOA			I/O	SPI slave in, master out
ECAP1			I/O	Enhanced Capture input/output 1
GPIO6	50	39	I/O/Z	General purpose input/output 6
EPWM4A			O	Enhanced PWM4 output A and HRPWM channel
EPWMSYNCI			I	External ePWM sync pulse input
EPWMSYNCO			O	External ePWM sync pulse output
GPIO7	49	38	I/O/Z	General purpose input/output 7
EPWM4B			O	Enhanced PWM4 output B
SCIRXDA			I	SCI-A receive data
–			–	–
GPIO8	43	35	I/O/Z	General purpose input/output 8
EPWM5A			O	Enhanced PWM5 output A
–			–	–
$\overline{\text{ADCSOCAO}}$			O	ADC start-of-conversion A

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Table 2-2. TERMINAL FUNCTIONS (continued)

NAME	PN PIN #	PAG PIN #	I/O/Z	DESCRIPTION
GPIO9	39	31	I/O/Z	General purpose input/output 9
EPMW5B			O	Enhanced PWM5 output B
LINTXA				LIN transmit A
–				–
GPIO10	65	52	I/O/Z	General purpose input/output 10
EPWM6A			O	Enhanced PWM6 output A
–				–
$\overline{ADCSOCBO}$			O	ADC start-of-conversion B
GPIO11	61	49	I/O/Z	General purpose input/output 11
EPWM6B				Enhanced PWM6 output B
LINRXA				LIN receive A
–				–
GPIO12	47	37	I/O/Z	General purpose input/output 12
$\overline{TZ1}$			I	Trip Zone input 1
SCITXDA			O	SCI-A transmit data
SPISIMOB			I/O	SPI slave in, master out [2]
GPIO13	76	–	I/O/Z	General purpose input/output 13
$\overline{TZ2}$			I	Trip Zone input 2
SPISOMIB			I/O	SPI slave out, master in
–				–
GPIO14	77	–	I/O/Z	General purpose input/output 14
$\overline{TZ3}$			I	Trip zone input 3
LINTXA			O	LIN transmit
SPICLKB			I/O	SPI-B clock input/output
GPIO15	75	–	I/O/Z	General purpose input/output 15
$\overline{TZ1}$			I	Trip zone input 1
LINRXA			I	LIN receive
$\overline{SPISTEB}$			I/O	SPI-B slave transmit enable input/output
GPIO16	46	36	I/O/Z	General purpose input/output 16
SPISIMOA			I/O	SPI slave in, master out
–				–
$\overline{TZ2}$			I	Trip Zone input 2
GPIO17	42	34	I/O/Z	General purpose input/output 17
SPISOMIA			I/O	SPI-A slave out, master in
–				–
$\overline{TZ3}$			I	Trip zone input 3
GPIO18	41	33	I/O/Z	General purpose input/output 18
SPICLKA			I/O	SPI-A clock input/output
LINTXA			O	LIN transmit
XCLKOUT			O/Z	Output clock derived from SYSCLKOUT. XCLKOUT is either the same frequency, one-half the frequency, or one-fourth the frequency of SYSCLKOUT. This is controlled by bits 1:0 (XCLKOUTDIV) in the XCLK register. At reset, XCLKOUT = SYSCLKOUT/4. The XCLKOUT signal can be turned off by setting XCLKOUTDIV to 3. The mux control for GPIO18 must also be set to XCLKOUT for this signal to propogate to the pin.

(2)   SPI-B peripheral is only available in the PN package

Table 2-2. TERMINAL FUNCTIONS (continued)

NAME	PN PIN #	PAG PIN #	I/O/Z	DESCRIPTION
GPIO19	55	44	I/O/Z	General purpose input/output 19
XCLKIN				External Oscillator Input. The path from this pin to the clock block is not gated by the mux function of this pin. Care must be taken not to enable this path for clocking if it is being used for the other periperhal functions
SPISTEA			I/O	SPI-A slave transmit enable input/output
LINRXA			I	LIN receive
ECAP1			I/O	Enhanced Capture input/output 1
GPIO20	78	62	I/O/Z	General purpose input/output 20
EQEP1A			I	Enhanced QEP1 input A
–				–
COMP1OUT			O	Direct output of Comparator 1
GPIO21	79	63	I/O/Z	General purpose input/output 21
EQEP1B			I	Enhanced QEP1 input B
–				–
COMP2OUT			O	Direct output of Comparator 2
GPIO22	1	1	I/O/Z	General purpose input/output 22
EQEP1S			I/O	Enhanced QEP1 strobe
LINTXA			O	LIN transmit
–				–
GPIO23	4	4	I/O/Z	General purpose input/output 23
EQEP1I			I/O	Enhanced QEP1 index
LINRXA			I	LIN receive
–				–
GPIO24	80	64	I/O/Z	General purpose input/output 24
ECAP1			I/O	Enhanced Capture input/output 1
SPISIMOB			I/O	SPI-B slave in, master out [1]
–				–
GPIO25	44	-	I/O/Z	General purpose input/output 25
SPISOMIB			I/O	SPI-B slave out , master in
–				–
–				–
GPIO26	37	-	I/O/Z	General purpose input/output 26
–				–
SPICLKB			I/O	SPI-B clock input/output
–				–
GPIO27	31	-	I/O/Z	General purpose input/output 27
–				–
SPISTEB			I/O	SPI-B slave transmit enable input/output
–				–
GPIO28	40	32	I/O/Z	General purpose input/output 28
SCIRXDA			I	SCI receive data
SDAA			I/OC	I2C data open-drain bidirectional port
TZ2			I	Trip zone input 2

(1)   SPI-B peripheral is only available in the PN package

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Table 2-2. TERMINAL FUNCTIONS (continued)

TERMINAL			I/O/Z	DESCRIPTION
NAME	PN PIN #	PAG PIN #		
GPIO29	34	27	I/O/Z	General purpose input/output 2
SCITXDA			O	SCI transmit data
SCLA			I/OC	I2C clock open-drain bidirectional port
$\overline{TZ3}$			I	Trip zone input 3
GPIO30	33	26	I/O/Z	General purpose input/output 30
CANRXA			I	CAN receive
–				–
–				–
GPIO31	32	25	I/O/Z	General purpose input/output 31
CANTXA			O	CAN transmit
–				–
–				–
GPIO32	2	2	I/O/Z	General purpose input/output 32
SDAA			I/OC	I2C data open-drain bidirectional port
EPWMSYNCI			I	Enhanced PWM external sync pulse input
$\overline{ADCSOCAO}$			O	ADC start-of-conversion A
GPIO33	3	3	I/O/Z	General-Purpose Input/Output 33
SCLA			I/OC	I2C clock open-drain bidirectional port
EPWMSYNCO			O	Enhanced PWM external synch pulse output
$\overline{ADCSOCBO}$			O	ADC start-of-conversion B
GPIO34	74	61	I/O/Z	General-Purpose Input/Output 34
COMP2OUT			O	Direct output of Comparator 2
COMP3OUT			O	Direct output of Comparator 3
–				–
GPIO35	59	47	I/O/Z	General-Purpose Input/Output 35
TDI			I	JTAG test data input (TDI) with internal pullup. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK
GPIO36	60	48	I/O/Z	General-Purpose Input/Output 36
TMS			I	JTAG test-mode select (TMS) with internal pullup. This serial control input is clocked into the TAP controller on the rising edge of TCK.
GPIO37	58	46	I/O/Z	General-Purpose Input/Output 37
TDO			O/Z	JTAG scan out, test data output (TDO). The contents of the selected register (instruction or data) are shifted out of TDO on the falling edge of TCK (8 mA drive)
GPIO38	57	45	I/O/Z	General-Purpose Input/Output 38
TCK			I	JTAG test clock with internal pullup
XCLKIN			I	External Oscillator Input. The path from this pin to the clock block is not gated by the mux function of this pin. Care must be taken to not enable this path for clocking if it is being used for the other functions.
–				–
GPIO39	56	-	I/O/Z	General-Purpose Input/Output 39
–				–
–				–
–				–
GPIO40	64	-	I/O/Z	General-Purpose Input/Output 40
EPWM7A			O	Enhanced PWM7 output A
–				–
–				–

Table 2-2. TERMINAL FUNCTIONS (continued)

TERMINAL			I/O/Z	DESCRIPTION
NAME	PN PIN #	PAG PIN #		
GPIO41	48	-	I/O/Z	General-Purpose Input/Output 41
EPWM7B			O	Enhanced PWM7 output B
–				–
–				–
GPIO42	5	-	I/O/Z	General-Purpose Input/Output 42
COMP1OUT			O	Direct output of Comparator 1
–				–
–				–
GPIO43	6	-	I/O/Z	General-Purpose Input/Output 43
COMP2OUT			O	Direct output of Comparator 2
–				–
–				–
GPIO44	45	-	I/O/Z	General-Purpose Input/Output 44
–				–
–				–
–				–

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3 Functional Overview

3.1 Block Diagram
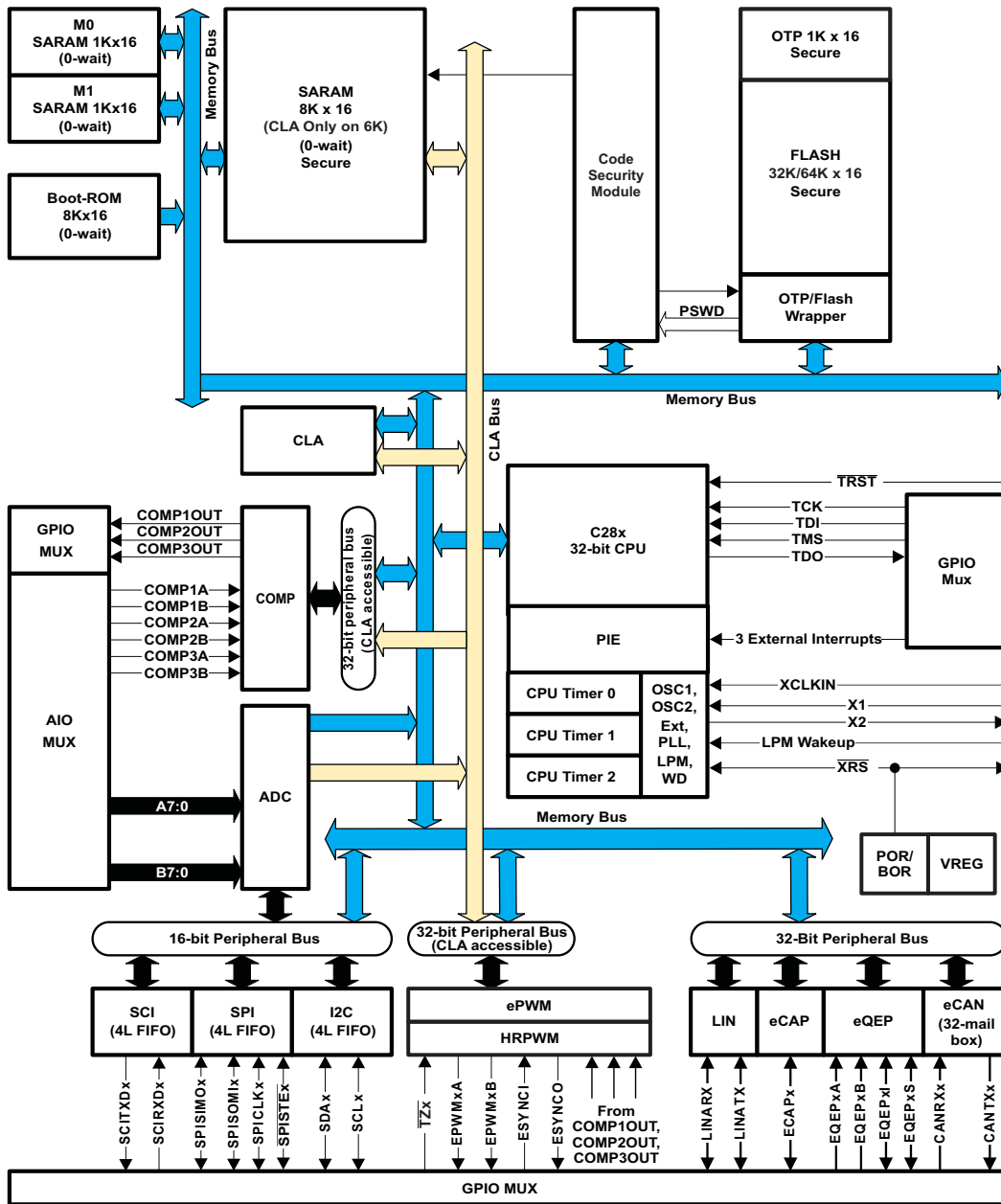
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A. Not all peripheral pins are available at the same time due to multiplexing.

Figure 3-1. Functional Block Diagram

3.2 Memory Maps

In Figure 3-2 and Figure 3-3, the following apply:

- Memory blocks are not to scale.

- Peripheral Frame 0, Peripheral Frame 1 and Peripheral Frame 2 memory maps are restricted to data memory only. A user program cannot access these memory maps in program space.

- *Protected* means the order of Write-followed-by-Read operations is preserved rather than the pipeline order.

- Certain memory ranges are EALLOW protected against spurious writes after configuration.

- Locations 0x3D7C80 – 0x3D7CC0 contain the internal oscillator and ADC calibration routines. These locations are not programmable by the user.

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Data Space	Prog Space

Low 64K
(24x/240x Equivalent Data Space)

Address	Data Space	Prog Space
0x00 0000	*M0 Vector RAM (Enabled if VMAP = 0)*	
0x00 0040	M0 SARAM (1K x 16, 0-Wait)	
0x00 0400	M1 SARAM (1K x 16, 0-Wait)	
0x00 0800	Peripheral Frame 0	Reserved
0x00 0D00	PIE Vector - RAM (256 x 16) (Enabled if VMAP = 1, ENPIE = 1)	
0x00 0E00	Peripheral Frame 0	
0x00 2000	Reserved	
0x00 6000	Peripheral Frame 1 (4K x 16, Protected)	Reserved
0x00 7000	Peripheral Frame 2 (4K x 16, Protected)	
0x00 8000	L0 SARAM (2K x 16) (0-Wait, Secure Zone + ECSL, Dual Mapped)	
0x00 8800	L1 DPSARAM (1K x 16) (0-Wait, Secure Zone + ECSL, CLA Data RAM 0)	
0x00 8C00	L2 DPSARAM (1K x 16) (0-Wait, Secure Zone + ECSL, CLA Data RAM 1)	
0x00 9000	L3 DPSARAM (4K x 16) (0-Wait, Secure Zone + ECSL, CLA Prog RAM)	
0x00 A000	Reserved	
0x3D 7800	User OTP (1K x 16, Secure Zone + ECSL)	
0x3D 7C00	Reserved	
0x3D 7C80	Calibration Data	
0x3D 7CC0	Get_mode function	
0x3D 7CE0	Reserved	
0x3D 7E80	PARTID	
0x3D 7E81	Reserved	
0x3D 8000	Reserved	
0x3E 8000	FLASH (64K x 16, 8 Sectors, Secure Zone + ECSL)	
0x3F 0000		
0x3F 7FF8	128-Bit Password	
0x3F 8000	L0 SARAM (2K x 16) (0-Wait, Secure Zone + ECSL, Dual Mapped)	
0x3F 8800	Reserved	
0x3F E000	Boot ROM (8K x 16, 0-Wait)	
0x3F FFC0	Vector (32 Vectors, Enabled if VMAP = 1)	

High 64K
(24x/240x Equivalent Program Space)

Figure 3-2. 28034/28035 Memory Map

Data Space	Prog Space
M0 Vector RAM (Enabled if VMAP = 0) 0x00 0000	
M0 SARAM (1K x 16, 0-Wait) 0x00 0040	
M1 SARAM (1K x 16, 0-Wait) 0x00 0400	
Peripheral Frame 0 0x00 0800	
PIE Vector - RAM (256 x 16) (Enabled if VMAP = 1, ENPIE = 1) 0x00 0D00	Reserved
Peripheral Frame 0 0x00 0E00	
Reserved 0x00 2000	
Peripheral Frame 1 (4K x 16, Protected) 0x00 6000	Reserved
Peripheral Frame 2 (4K x 16, Protected) 0x00 7000	
L0 SARAM (2K x 16) (0-Wait, Secure Zone + ECSL, Dual Mapped) 0x00 8000	
L1 DPSARAM (1K x 16) (0-Wait, Secure Zone + ECSL, CLA Data RAM 0) 0x00 8800	
L2 DPSARAM (1K x 16) (0-Wait, Secure Zone + ECSL, CLA Data RAM 1) 0x00 8C00	
L3 DPSARAM (4K x 16) (0-Wait, Secure Zone + ECSL, CLA Prog RAM) 0x00 9000	
Reserved 0x00 A000	
User OTP (1K x 16, Secure Zone + ECSL) 0x3D 7800	
Reserved 0x3D 7C00	
Calibration Data 0x3D 7C80	
Get_mode function 0x3D 7CC0	
Reserved 0x3D 7CE0	
PARTID 0x3D 7E80	
Reserved 0x3D 7E81	
Reserved 0x3D 8000	
FLASH (32K x 16, 8 Sectors, Secure Zone + ECSL) 0x3F 0000	
128-Bit Password 0x3F 7FF8	
L0 SARAM (2K x 16) (0-Wait, Secure Zone + ECSL, Dual Mapped) 0x3F 8000	
Reserved 0x3F 8800	
Boot ROM (8K x 16, 0-Wait) 0x3F E000	
Vector (32 Vectors, Enabled if VMAP = 1) 0x3F FFC0	

Low 64K (24x/240x Equivalent Data Space)

High 64K (24x/240x Equivalent Program Space)

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Figure 3-3. 28032/28033 Memory Map

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Table 3-1. Addresses of Flash Sectors in F28034/28035

ADDRESS RANGE	PROGRAM AND DATA SPACE
0x3E 8000 - 0x3E 9FFF	Sector H (8K x 16)
0x3E A000 - 0x3E BFFF	Sector G (8K x 16)
0x3E C000 - 0x3E DFFF	Sector F (8K x 16)
0x3E E000 - 0x3E FFFF	Sector E (8K x 16)
0x3F 0000 - 0x3F 1FFF	Sector D (8K x 16)
0x3F 2000 - 0x3F 3FFF	Sector C (8K x 16)
0x3F 4000 - 0x3F 5FFF	Sector B (8K x 16)
0x3F 6000 - 0x3F 7F7F	Sector A (8K x 16)
0x3F 7F80 - 0x3F 7FF5	Program to 0x0000 when using the Code Security Module
0x3F 7FF6 - 0x3F 7FF7	Boot-to-Flash Entry Point (program branch instruction here)
0x3F 7FF8 - 0x3F 7FFF	Security Password (128-Bit) (Do not program to all zeros)

Table 3-2. Addresses of Flash Sectors in F28032/28033

ADDRESS RANGE	PROGRAM AND DATA SPACE
0x3F 0000 - 0x3F 0FFF	Sector H (4K x 16)
0x3F 1000 - 0x3F 1FFF	Sector G (4K x 16)
0x3F 2000 - 0x3F 2FFF	Sector F (4K x 16)
0x3F 3000 - 0x3F 3FFF	Sector E (4K x 16)
0x3F 4000 - 0x3F 4FFF	Sector D (4K x 16)
0x3F 5000 - 0x3F 5FFF	Sector C (4K x 16)
0x3F 6000 - 0x3F 6FFF	Sector B (4K x 16)
0x3F 7000 - 0x3F 7F7F	Sector A (4K x 16)
0x3F 7F80 - 0x3F 7FF5	Program to 0x0000 when using the Code Security Module
0x3F 7FF6 - 0x3F 7FF7	Boot-to-Flash Entry Point (program branch instruction here)
0x3F 7FF8 - 0x3F 7FFF	Security Password (128-Bit) (Do not program to all zeros)

NOTE

- When the code-security passwords are programmed, all addresses between 0x3F 7F80 and 0x3F 7FF5 cannot be used as program code or data. These locations must be programmed to 0x0000.
- If the code security feature is not used, addresses 0x3F 7F80 through 0x3F 7FEF may be used for code or data. Addresses 0x3F 7FF0 – 0x3F 7FF5 are reserved for data and should not contain program code.

Table 3-3 shows how to handle these memory locations.

Table 3-3. Impact of Using the Code Security Module

ADDRESS	FLASH	
	CODE SECURITY ENABLED	CODE SECURITY DISABLED
0x3F 7F80 - 0x3F 7FEF	Fill with 0x0000	Application code and data
0x3F 7FF0 - 0x3F 7FF5		Reserved for data only

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Peripheral Frame 1 and Peripheral Frame 2 are grouped together to enable these blocks to be write/read peripheral block protected. The protected mode makes sure that all accesses to these blocks happen as written. Because of the pipeline, a write immediately followed by a read to different memory locations, will appear in reverse order on the memory bus of the CPU. This can cause problems in certain peripheral applications where the user expected the write to occur first (as written). The CPU supports a block protection mode where a region of memory can be protected so that operations occur as written (the penalty is extra cycles are added to align the operations). This mode is programmable and by default, it protects the selected zones.

The wait-states for the various spaces in the memory map area are listed in Table 3-4.

Table 3-4. Wait-states

AREA	WAIT-STATES (CPU)	COMMENTS
M0 and M1 SARAMs	0-wait	Fixed
Peripheral Frame 0	0-wait	
Peripheral Frame 1	0-wait (writes) 2-wait (reads)	Cycles can be extended by peripheral generated ready.
Peripheral Frame 2	0-wait (writes) 2-wait (reads)	Fixed. Cycles cannot be extended by the peripheral.
L0 SARAM	0-wait data and program	Assumes no CPU conflicts
L1 SARAM	0-wait data and program	Assumes no CPU conflicts
L2 SARAM	0-wait data and program	Assumes no CPU conflicts
L3 SARAM	0-wait data and program	Assumes no CPU conflicts
OTP	Programmable 1-wait minimum	Programmed via the Flash registers. 1-wait is minimum number of wait states allowed.
FLASH	Programmable 0-wait Paged min 1-wait Random min Random ≥ Paged	Programmed via the Flash registers.
FLASH Password	16-wait fixed	Wait states of password locations are fixed.
Boot-ROM	0-wait	

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3.3 Brief Descriptions

3.3.1 CPU

The 2803x (C28x) family is a member of the TMS320C2000™ microcontroller (MCU) platform. The C28x-based controllers have the same 32-bit fixed-point architecture as existing C28x MCUs. It is a very efficient C/C++ engine, enabling users to develop not only their system control software in a high-level language, but also enabling development of math algorithms using C/C++. The device is as efficient at MCU math tasks as it is at system control tasks that typically are handled by microcontroller devices. This efficiency removes the need for a second processor in many systems. The 32 x 32-bit MAC 64-bit processing capabilities enable the controller to handle higher numerical resolution problems efficiently. Add to this the fast interrupt response with automatic context save of critical registers, resulting in a device that is capable of servicing many asynchronous events with minimal latency. The device has an 8-level-deep protected pipeline with pipelined memory accesses. This pipelining enables it to execute at high speeds without resorting to expensive high-speed memories. Special branch-look-ahead hardware minimizes the latency for conditional discontinuities. Special store conditional operations further improve performance.

3.3.2 Control Law Accelerator (CLA)

The C28x control law accelerator is a single-precision (32-bit) floating-point unit that extends the capabilities of the C28x CPU by adding parallel processing. The CLA is an independent processor with its own bus structure, fetch mechanism, and pipeline. Eight individual CLA tasks, or routines, can be specified. Each task is started by software or a peripheral such as the ADC, an ePWM, or CPU Timer 0. The CLA executes one task at a time to completion. When a task completes the main CPU is notified by an interrupt to the PIE and the CLA automatically begins the next highest-priority pending task. The CLA can directly access the ADC Result registers and the ePWM+HRPWM registers. Dedicated message RAMs provide a method to pass additional data between the main CPU and the CLA.

3.3.3 Memory Bus (Harvard Bus Architecture)

As with many MCU-type devices, multiple busses are used to move data between the memories and peripherals and the CPU. The memory bus architecture contains a program read bus, data read bus, and data write bus. The program read bus consists of 22 address lines and 32 data lines. The data read and write busses consist of 32 address lines and 32 data lines each. The 32-bit-wide data busses enable single cycle 32-bit operations. The multiple bus architecture, commonly termed Harvard Bus, enables the C28x to fetch an instruction, read a data value and write a data value in a single cycle. All peripherals and memories attached to the memory bus prioritize memory accesses. Generally, the priority of memory bus accesses can be summarized as follows:

Highest:	Data Writes	(Simultaneous data and program writes cannot occur on the memory bus.)
	Program Writes	(Simultaneous data and program writes cannot occur on the memory bus.)
	Data Reads	
	Program Reads	(Simultaneous program reads and fetches cannot occur on the memory bus.)
Lowest:	Fetches	(Simultaneous program reads and fetches cannot occur on the memory bus.)

3.3.4 Peripheral Bus

To enable migration of peripherals between various Texas Instruments (TI) MCU family of devices, the devices adopt a peripheral bus standard for peripheral interconnect. The peripheral bus bridge multiplexes the various busses that make up the processor Memory Bus into a single bus consisting of 16 address lines and 16 or 32 data lines and associated control signals. Three versions of the peripheral bus are supported. One version supports only 16-bit accesses (called peripheral frame 2). Another version supports both 16- and 32-bit accesses (called peripheral frame 1).

3.3.5 Real-Time JTAG and Analysis

The devices implement the standard IEEE 1149.1 JTAG[1] interface for in-circuit based debug. Additionally, the devices support real-time mode of operation allowing modification of the contents of memory, peripheral, and register locations while the processor is running and executing code and servicing interrupts. The user can also single step through non-time-critical code while enabling time-critical interrupts to be serviced without interference. The device implements the real-time mode in hardware within the CPU. This is a feature unique to the 28x family of devices, requiring no software monitor. Additionally, special analysis hardware is provided that allows setting of hardware breakpoint or data/address watch-points and generating various user-selectable break events when a match occurs. These devices do not support boundary scan; however, IDCODE and BYPASS features are available if the following considerations are taken into account. The IDCODE does not come by default. The user needs to go through a sequence of SHIFT IR and SHIFT DR state of JTAG to get the IDCODE. For BYPASS instruction, the first shifted DR value would be 1.

3.3.6 Flash

The F28035/34 devices contain 64K x 16 of embedded flash memory, segregated into eight 8K x 16 sectors. The F28033/32 devices contain 32K x 16 of embedded flash memory, segregated into eight 4K x 16 sectors. All devices also contain a single 1K x 16 of OTP memory at address range 0x3D 7800 – 0x3D 7BFF. The user can individually erase, program, and validate a flash sector while leaving other sectors untouched. However, it is not possible to use one sector of the flash or the OTP to execute flash algorithms that erase/program other sectors. Special memory pipelining is provided to enable the flash module to achieve higher performance. The flash/OTP is mapped to both program and data space; therefore, it can be used to execute code or store data information. Addresses 0x3F 7FF0 – 0x3F 7FF5 are reserved for data variables and should not contain program code.

NOTE

The Flash and OTP wait-states can be configured by the application. This allows applications running at slower frequencies to configure the flash to use fewer wait-states.

Flash effective performance can be improved by enabling the flash pipeline mode in the Flash options register. With this mode enabled, effective performance of linear code execution will be much faster than the raw performance indicated by the wait-state configuration alone. The exact performance gain when using the Flash pipeline mode is application-dependent.

For more information on the Flash options, Flash wait-state, and OTP wait-state registers, see the *TMS320x2803x Piccolo System Control and Interrupts Reference Guide* (literature number SPRUGL8).

3.3.7 M0, M1 SARAMs

All devices contain these two blocks of single access memory, each 1K x 16 in size. The stack pointer points to the beginning of block M1 on reset. The M0 and M1 blocks, like all other memory blocks on C28x devices, are mapped to both program and data space. Hence, the user can use M0 and M1 to execute code or for data variables. The partitioning is performed within the linker. The C28x device presents a unified memory map to the programmer. This makes for easier programming in high-level languages.

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(1) IEEE Standard 1149.1-1990 Standard Test Access Port and Boundary Scan Architecture

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3.3.8   L0, L1, L2, and L3 SARAMs

The device contains a total of 8K x 16 of single-access memory. Block L0 is 2K in size and is dual mapped to both program and data space. Blocks L1 and L2 are both 1K in size and are shared with the CLA which can ultilize these blocks for its data space. Block L3 is 4K in size and is shared with the CLA which can ultilize this block for its program space.

3.3.9   Boot ROM

The Boot ROM is factory-programmed with boot-loading software. Boot-mode signals are provided to tell the bootloader software what boot mode to use on power up. The user can select to boot normally or to download new software from an external connection or to select boot software that is programmed in the internal Flash/ROM. The Boot ROM also contains standard tables, such as SIN/COS waveforms, for use in math-related algorithms.

Table 3-5. Boot Mode Selection

MODE	GPIO37/TDO	GPIO34/COMP2OUT/ COMP3OUT	$\overline{\text{TRST}}$	MODE
3	1	1	0	GetMode
2	1	0	0	Wait (see Section 3.3.10 for description)
1	0	1	0	SCI
0	0	0	0	Parallel IO
EMU	x	x	1	Emulation Boot

3.3.9.1   Emulation Boot

When the emulator is connected, the GPIO37/TDO pin cannot be used for boot mode selection. In this case, the boot ROM detects that an emulator is connected and uses the contents of two reserved SARAM locations in the PIE vector table to determine the boot mode. If the content of either location is invalid, then the *Wait* boot option is used. All boot mode options can be accessed in emulation boot.

3.3.9.2   GetMode

The default behavior of the *GetMode* option is to boot to flash. This behavior can be changed to another boot option by programming two locations in the OTP. One of the following loaders can be specified: SCI, SPI, I2C, or OTP. If the content of either OTP location is invalid, then boot to flash is used

3.3.10   Security

The devices support high levels of security to protect the user firmware from being reverse engineered. The security features a 128-bit password (hardcoded for 16 wait-states), which the user programs into the flash. One code security module (CSM) is used to protect the flash/OTP and the L0/L1 SARAM blocks. The security feature prevents unauthorized users from examining the memory contents via the JTAG port, executing code from external memory or trying to boot-load some undesirable software that would export the secure memory contents. To enable access to the secure blocks, the user must write the correct 128-bit KEY value that matches the value stored in the password locations within the Flash.

In addition to the CSM, the emulation code security logic (ECSL) has been implemented to prevent unauthorized users from stepping through secure code. Any code or data access to flash, user OTP, or L0 memory while the emulator is connected will trip the ECSL and break the emulation connection. To allow emulation of secure code, while maintaining the CSM protection against secure memory reads, the user must write the correct value into the lower 64 bits of the KEY register, which matches the value stored in the lower 64 bits of the password locations within the flash. Note that dummy reads of all 128 bits of the password in the flash must still be performed. If the lower 64 bits of the password locations are all ones (unprogrammed), then the KEY value does not need to match.

When initially debugging a device with the password locations in flash programmed (i.e., secured), the CPU will start running and may execute an instruction that performs an access to a protected ECSL area. If this happens, the ECSL will trip and cause the emulator connection to be cut.

The solution is to use the *Wait* boot option. This will sit in a loop around a software breakpoint to allow an emulator to be connected without tripping security. Piccolo devices do not support a hardware wait-in-reset mode.

NOTE

- When the code-security passwords are programmed, all addresses between 0x3F7F80 and 0x3F7FF5 cannot be used as program code or data. These locations must be programmed to 0x0000.

- If the code security feature is not used, addresses 0x3F7F80 through 0x3F7FEF may be used for code or data. Addresses 0x3F7FF0 – 0x3F7FF5 are reserved for data and should not contain program code.

The 128-bit password (at 0x3F 7FF8 – 0x3F 7FFF) must not be programmed to zeros. Doing so would permanently lock the device.

Disclaimer

Code Security Module Disclaimer

THE CODE SECURITY MODULE (CSM) INCLUDED ON THIS DEVICE WAS DESIGNED TO PASSWORD PROTECT THE DATA STORED IN THE ASSOCIATED MEMORY (EITHER ROM OR FLASH) AND IS WARRANTED BY TEXAS INSTRUMENTS (TI), IN ACCORDANCE WITH ITS STANDARD TERMS AND CONDITIONS, TO CONFORM TO TI'S PUBLISHED SPECIFICATIONS FOR THE WARRANTY PERIOD APPLICABLE FOR THIS DEVICE.

TI DOES NOT, HOWEVER, WARRANT OR REPRESENT THAT THE CSM CANNOT BE COMPROMISED OR BREACHED OR THAT THE DATA STORED IN THE ASSOCIATED MEMORY CANNOT BE ACCESSED THROUGH OTHER MEANS. MOREOVER, EXCEPT AS SET FORTH ABOVE, TI MAKES NO WARRANTIES OR REPRESENTATIONS CONCERNING THE CSM OR OPERATION OF THIS DEVICE, INCLUDING ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

IN NO EVENT SHALL TI BE LIABLE FOR ANY CONSEQUENTIAL, SPECIAL, INDIRECT, INCIDENTAL, OR PUNITIVE DAMAGES, HOWEVER CAUSED, ARISING IN ANY WAY OUT OF YOUR USE OF THE CSM OR THIS DEVICE, WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO LOSS OF DATA, LOSS OF GOODWILL, LOSS OF USE OR INTERRUPTION OF BUSINESS OR OTHER ECONOMIC LOSS.

3.3.11 *Peripheral Interrupt Expansion (PIE) Block*

The PIE block serves to multiplex numerous interrupt sources into a smaller set of interrupt inputs. The PIE block can support up to 96 peripheral interrupts. On the F2803x, 54 of the possible 96 interrupts are used by peripherals. The 96 interrupts are grouped into blocks of 8 and each group is fed into 1 of 12 CPU interrupt lines (INT1 to INT12). Each of the 96 interrupts is supported by its own vector stored in a dedicated RAM block that can be overwritten by the user. The vector is automatically fetched by the CPU on servicing the interrupt. It takes 8 CPU clock cycles to fetch the vector and save critical CPU registers. Hence the CPU can quickly respond to interrupt events. Prioritization of interrupts is controlled in hardware and software. Each individual interrupt can be enabled/disabled within the PIE block.

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3.3.12   External Interrupts (XINT1-XINT3)

The devices support three masked external interrupts (XINT1-XINT3). Each of the interrupts can be selected for negative, positive, or both negative and positive edge triggering and can also be enabled/disabled. These interrupts also contain a 16-bit free running up counter, which is reset to zero when a valid interrupt edge is detected. This counter can be used to accurately time stamp the interrupt. There are no dedicated pins for the external interrupts. XINT1, XINT2, and XINT3 interrupts can accept inputs from GPIO0 – GPIO31 pins.

3.3.13   Internal Zero Pin Oscillators, Oscillator, and PLL

The device can be clocked by either of the two internal zero-pin oscillators, an external oscillator, or by a crystal attached to the on-chip oscillator circuit (48-pin devices only). A PLL is provided supporting up to 12 input-clock-scaling ratios. The PLL ratios can be changed on-the-fly in software, enabling the user to scale back on operating frequency if lower power operation is desired. Refer to the Electrical Specification section for timing details. The PLL block can be set in bypass mode.

3.3.14   Watchdog

Each device contains two watchdogs: CPU-Watchdog that monitors the core and NMI-Watchdog that is a missing clock-detect circuit. The user software must regularly reset the CPU-watchdog counter within a certain time frame; otherwise, the CPU-watchdog generates a reset to the processor. The CPU-watchdog can be disabled if necessary. The NMI-Watchdog engages only in case of a clock failure and can either generate an interrupt or a device reset.

3.3.15   Peripheral Clocking

The clocks to each individual peripheral can be enabled/disabled to reduce power consumption when a peripheral is not in use. Additionally, the system clock to the serial ports (except I2C) can be scaled relative to the CPU clock.

3.3.16   Low-power Modes

The devices are full static CMOS devices. Three low-power modes are provided:

IDLE: Place CPU in low-power mode. Peripheral clocks may be turned off selectively and
            only those peripherals that need to function during IDLE are left operating. An
            enabled interrupt from an active peripheral or the watchdog timer will wake the
            processor from IDLE mode.

STANDBY: Turns off clock to CPU and peripherals. This mode leaves the oscillator and PLL
            functional. An external interrupt event will wake the processor and the peripherals.
            Execution begins on the next valid cycle after detection of the interrupt event

HALT: This mode basically shuts down the device and places it in the lowest possible power
            consumption mode. If the internal zero-pin oscillators are used as the clock source,
            the HALT mode turns them off, by default. To keep these oscillators from shutting
            down, the INTOSCnHALTI bits in CLKCTL register may be used. The zero-pin
            oscillators may thus be used to clock the CPU-watchdog in this mode. If the on-chip
            crystal oscillator is used as the clock source, it is shut down in this mode. A reset or
            an external signal (through a GPIO pin) or the CPU-watchdog can wake the device
            from this mode.

3.3.17   Peripheral Frames 0, 1, 2 (PFn)

The device segregates peripherals into three sections. The mapping of peripherals is as follows:

PF0:   PIE: PIE Interrupt Enable and Control Registers Plus PIE Vector Table

      Flash: Flash Waitstate Registers

      Timers: CPU-Timers 0, 1, 2 Registers

	CSM:	Code Security Module KEY Registers
	ADC:	ADC Result Registers
	CLA	Control Law Accelrator Registers and Message RAMs
PF1:	GPIO:	GPIO MUX Configuration and Control Registers
	eCAN:	Enhanced Control Area Network Configuration and Control Registers
	LIN:	Local Interconnect Network Configuration and Control Registers
	ePWM:	Enhanced Pulse Width Modulator Module and Registers
	eCAP:	Enhanced Capture Module and Registers
	eQEP:	Enhanced Quadrature Encoder Pulse Module and Registers
	Comparators:	Comparator Modules
PF2:	SYS:	System Control Registers
	SCI:	Serial Communications Interface (SCI) Control and RX/TX Registers
	SPI:	Serial Port Interface (SPI) Control and RX/TX Registers
	ADC:	ADC Status, Control, and Configuration Registers
	I2C:	Inter-Integrated Circuit Module and Registers
	XINT:	External Interrupt Registers

3.3.18 General-Purpose Input/Output (GPIO) Multiplexer

Most of the peripheral signals are multiplexed with general-purpose input/output (GPIO) signals. This enables the user to use a pin as GPIO if the peripheral signal or function is not used. On reset, GPIO pins are configured as inputs. The user can individually program each pin for GPIO mode or peripheral signal mode. For specific inputs, the user can also select the number of input qualification cycles. This is to filter unwanted noise glitches. The GPIO signals can also be used to bring the device out of specific low-power modes.

3.3.19 32-Bit CPU-Timers (0, 1, 2)

CPU-Timers 0, 1, and 2 are identical 32-bit timers with presettable periods and with 16-bit clock prescaling. The timers have a 32-bit count down register, which generates an interrupt when the counter reaches zero. The counter is decremented at the CPU clock speed divided by the prescale value setting. When the counter reaches zero, it is automatically reloaded with a 32-bit period value. CPU-Timer 2 is connected to INT14 of the CPU. It can be clocked by any one of the following:

- SYSCLKOUT (default)
- Internal zero-pin oscillator 1 (INTOSC1)
- Internal zero-pin oscillator 2 (INTSOC2)
- External clock source

CPU-Timer 1 is for general use and can be connected to INT13 of the CPU. CPU-Timer 0 is also for general use and is connected to the PIE block.

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3.3.20 Control Peripherals

The devices support the following peripherals that are used for embedded control and communication:

ePWM:	The enhanced PWM peripheral supports independent/complementary PWM generation, adjustable dead-band generation for leading/trailing edges, latched/cycle-by-cycle trip mechanism. Some of the PWM pins support the HRPWM high resolution duty and period features. The type 1 module found on 2803x devices also supports increased dead-band resolution, enhanced SOC and interrupt generation, and advanced triggering including trip functions based on comparator outputs.
eCAP:	The enhanced capture peripheral uses a 32-bit time base and registers up to four programmable events in continuous/one-shot capture modes. This peripheral can also be configured to generate an auxiliary PWM signal.
eQEP:	The enhanced QEP peripheral uses a 32-bit position counter, supports low-speed measurement using capture unit and high-speed measurement using a 32-bit unit timer. This peripheral has a watchdog timer to detect motor stall and input error detection logic to identify simultaneous edge transition in QEP signals.
ADC:	The ADC block is a 12-bit converter. It has up to 13 single-ended channels pinned out, depending on the device. It contains two sample-and-hold units for simultaneous sampling.
Comparator:	Each comparator block consists of one analog comparator along with an internal 10-bit reference for supplying one input of the comparator.

3.3.21 Serial Port Peripherals

The devices support the following serial communication peripherals:

SPI:	The SPI is a high-speed, synchronous serial I/O port that allows a serial bit stream of programmed length (one to sixteen bits) to be shifted into and out of the device at a programmable bit-transfer rate. Normally, the SPI is used for communications between the MCU and external peripherals or another processor. Typical applications include external I/O or peripheral expansion through devices such as shift registers, display drivers, and ADCs. Multi-device communications are supported by the master/slave operation of the SPI. The SPI contains a 4-level receive and transmit FIFO for reducing interrupt servicing overhead.
SCI:	The serial communications interface is a two-wire asynchronous serial port, commonly known as UART. The SCI contains a 4-level receive and transmit FIFO for reducing interrupt servicing overhead.
I2C:	The inter-integrated circuit (I2C) module provides an interface between a MCU and other devices compliant with Philips Semiconductors Inter-IC bus (I2C-bus) specification version 2.1 and connected by way of an I2C-bus. External components attached to this 2-wire serial bus can transmit/receive up to 8-bit data to/from the MCU through the I2C module. The I2C contains a 4-level receive and transmit FIFO for reducing interrupt servicing overhead.
eCAN:	This is the enhanced version of the CAN peripheral. It supports 32 mailboxes, time stamping of messages, and is CAN 2.0B-compliant.
LIN:	LIN 1.3 or 2.0 compatible peripheral. Can also be configured as additional SCI port

3.4 Register Map

The devices contain four peripheral register spaces. The spaces are categorized as follows:

Peripheral Frame 0: These are peripherals that are mapped directly to the CPU memory bus. See Table 3-6.

Peripheral Frame 1   These are peripherals that are mapped to the 32-bit peripheral bus. See Table 3-7.

Peripheral Frame 2: These are peripherals that are mapped to the 16-bit peripheral bus. See Table 3-8.

Table 3-6. Peripheral Frame 0 Registers[1]

NAME	ADDRESS RANGE	SIZE (×16)	EALLOW PROTECTED[2]
Device Emulation Registers	0x00 0880 - 0x00 09FF	384	Yes
FLASH Registers[3]	0x00 0A80 - 0x00 0ADF	96	Yes
Code Security Module Registers	0x00 0AE0 - 0x00 0AEF	16	Yes
ADC registers (0 wait read only)	0x00 0B00 - 0x00 0B0F	16	No
CPU–TIMER0/1/2 Registers	0x00 0C00 - 0x00 0C3F	64	No
PIE Registers	0x00 0CE0 - 0x00 0CFF	32	No
PIE Vector Table	0x00 0D00 - 0x00 0DFF	256	No
CLA Registers	0x00 1400 - 0x00 147F	128	Yes
CLA to CPU Message RAM (CPU writes ignored)	0x00 1480 - 0x00 14FF	128	NA
CPU to CLA Message RAM (CLA writes ignored)	0x00 1500 - 0x00 157F	128	NA

(1) Registers in Frame 0 support 16-bit and 32-bit accesses.
(2) If registers are EALLOW protected, then writes cannot be performed until the EALLOW instruction is executed. The EDIS instruction disables writes to prevent stray code or pointers from corrupting register contents.
(3) The Flash Registers are also protected by the Code Security Module (CSM).

Table 3-7. Peripheral Frame 1 Registers

NAME	ADDRESS RANGE	SIZE (×16)	EALLOW PROTECTED
eCAN-A registers	0x00 6000 - 0x00 61FF	512	[1]
Comparator 1 registers	0x00 6400 - 0x00 641F	32	[1]
Comparator 2 registers	0x00 6420 - 0x00 643F	32	[1]
Comparator 3 registers	0x00 6440 - 0x00 645F	32	[1]
ePWM1 + HRPWM1 registers	0x00 6800 - 0x00 683F	64	[1]
ePWM2 + HRPWM2 registers	0x00 6840 - 0x00 687F	64	[1]
ePWM3 + HRPWM3 registers	0x00 6880 - 0x00 68BF	64	[1]
ePWM4 + HRPWM4 registers	0x00 68C0 - 0x00 68FF	64	[1]
ePWM5 + HRPWM5 registers	0x00 6900 - 0x00 693F	64	[1]
ePWM6 + HRPWM6 registers	0x00 6940 - 0x00 697F	64	[1]
ePWM7 + HRPWM7 registers	0x00 6980 - 0x00 69BF	64	[1]
eCAP1 registers	0x00 6A00 - 0x00 6A1F	32	No
eQEP1 registers	0x00 6B00 - 0x00 6B3F	64	[1]
LIN-A registers	0x00 6C00 - 0x00 6C7F	128	[1]
GPIO registers	0x00 6F80 - 0x00 6FFF	128	[1]

(1) Some registers are EALLOW protected. See the module reference guide for more information.

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Table 3-8. Peripheral Frame 2 Registers

NAME	ADDRESS RANGE	SIZE (×16)	EALLOW PROTECTED
System Control Registers	0x00 7010 - 0x00 702F	32	Yes
SPI-A Registers	0x00 7040 - 0x00 704F	16	No
SCI-A Registers	0x00 7050 - 0x00 705F	16	No
NMI Watchdog Interrupt Registers	0x00 7060 - 0x00 706F	16	Yes
External Interrupt Registers	0x00 7070 - 0x00 707F	16	Yes
ADC Registers	0x00 7100 - 0x00 717F	32	(1)
I2C-A Registers	0x00 7900 - 0x00 793F	64	(1)
SPI-B Registers	0x00 7740 - 0x00 774F	16	No

(1) Some registers are EALLOW protected. See the module reference guide for more information.

3.5 Device Emulation Registers

These registers are used to control the protection mode of the C28x CPU and to monitor some critical device signals. The registers are defined in Table 3-9.

Table 3-9. Device Emulation Registers

NAME	ADDRESS RANGE	SIZE (x16)	DESCRIPTION			EALLOW PROTECTED
DEVICECNF	0x0880 0x0881	2	Device Configuration Register			Yes
PARTID[1]	0x3D 7E80	1	Part ID Register	TMS320F28035PN	0x00BF	No
				TMS320F28035PAG	0x00BE	
				TMS320F28034PN	0x00BB	
				TMS320F28034PAG	0x00BA	
				TMS320F28033PN	0x00B7	
				TMS320F28033PAG	0x00B6	
				TMS320F28032PN	0x00B3	
				TMS320F28032PAG	0x00B2	
CLASSID	0x0882	1	Class ID Register	TMS320F28035	0x00BF	No
				TMS320F28034	0x00BB	
				TMS320F28033	0x00B7	
				TMS320F28032	0x00B3	
REVID	0x0883	1	Revision ID Register	0x0000 - Silicon Rev. 0 - TMX		No

(1) For TMS320F2803x devices, the PARTID register location differs from the TMS320F2802x devices' location of 0x3D7FFF.

3.6 Interrupts

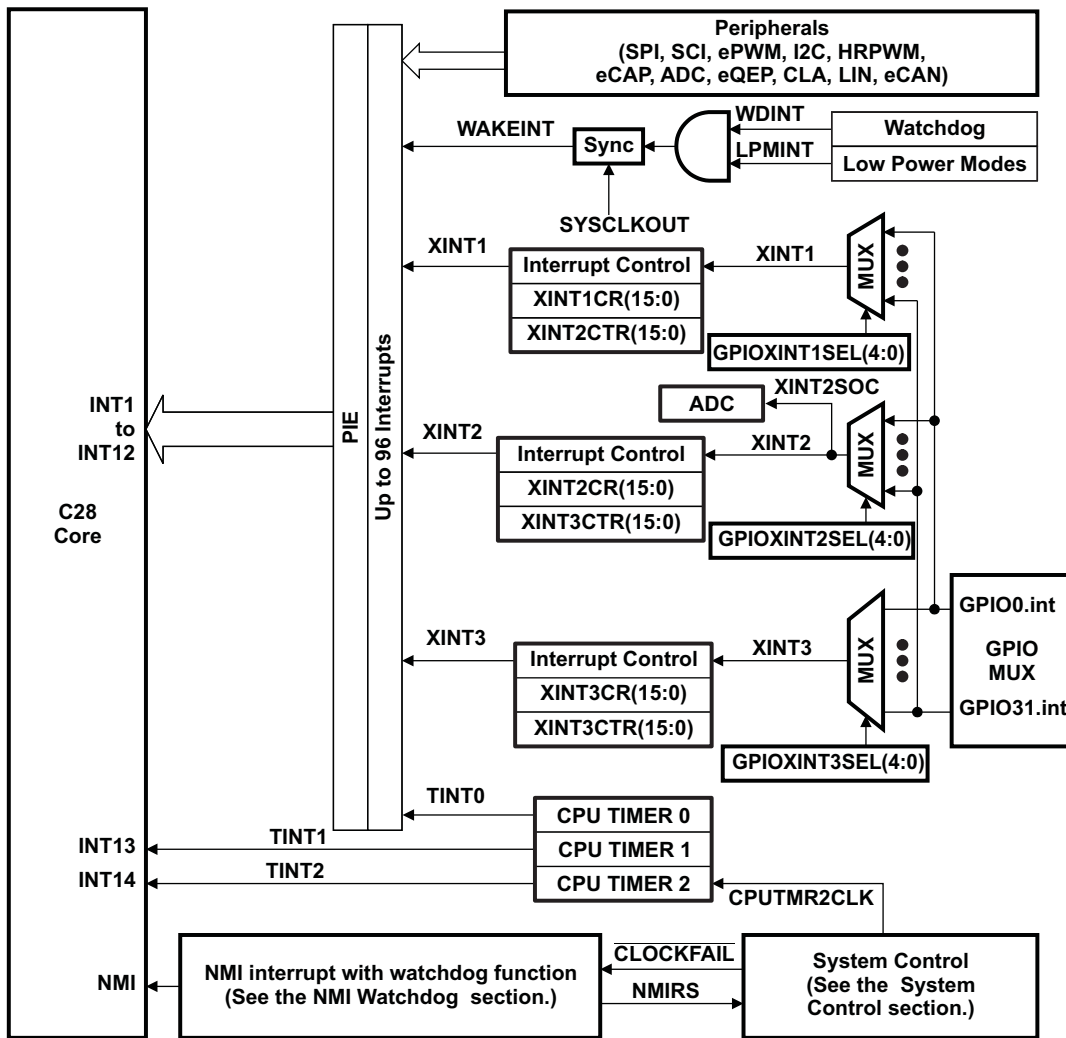Figure 3-4 shows how the various interrupt sources are multiplexed.

Figure 3-4. External and PIE Interrupt Sources

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Eight PIE block interrupts are grouped into one CPU interrupt. In total, 12 CPU interrupt groups, with 8 interrupts per group equals 96 possible interrupts. Table 3-10 shows the interrupts used by 2803x devices.

The TRAP #VectorNumber instruction transfers program control to the interrupt service routine corresponding to the vector specified. TRAP #0 attempts to transfer program control to the address pointed to by the reset vector. The PIE vector table does not, however, include a reset vector. Therefore, TRAP #0 should not be used when the PIE is enabled. Doing so will result in undefined behavior.

When the PIE is enabled, TRAP #1 through TRAP #12 will transfer program control to the interrupt service routine corresponding to the first vector within the PIE group. For example: TRAP #1 fetches the vector from INT1.1, TRAP #2 fetches the vector from INT2.1, and so forth.
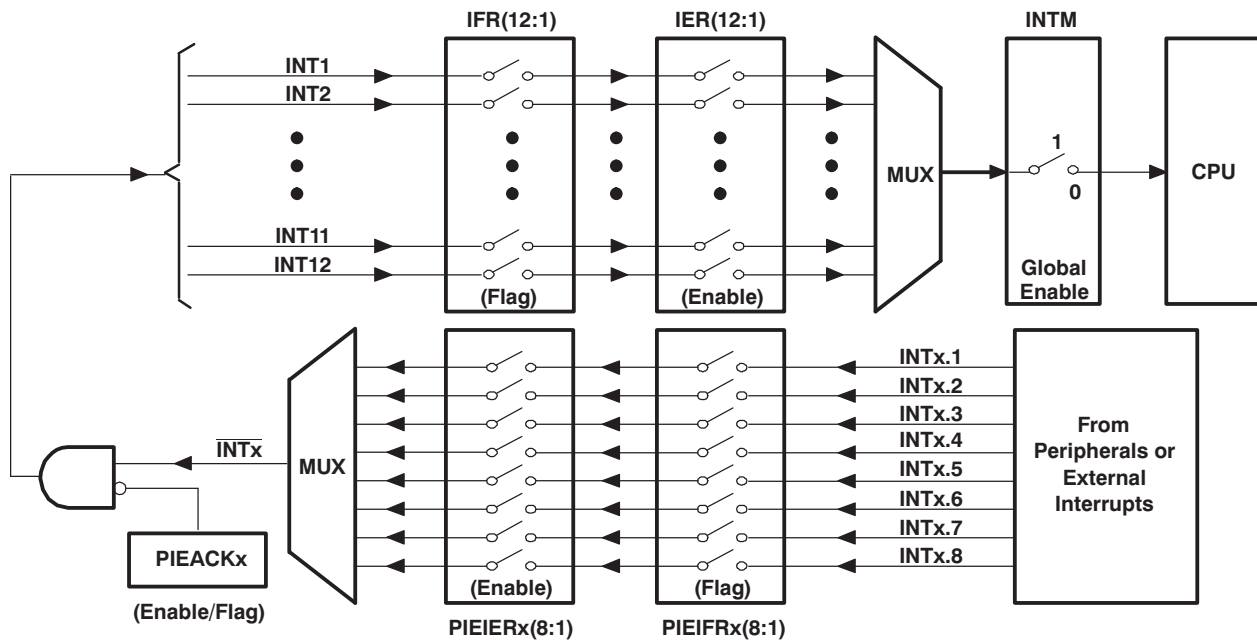
Figure 3-5. Multiplexing of Interrupts Using the PIE Block

Table 3-10. PIE MUXed Peripheral Interrupt Vector Table

	INTx.8	INTx.7	INTx.6	INTx.5	INTx.4	INTx.3	INTx.2	INTx.1
INT1.y	WAKEINT	TINT0	ADCINT9	XINT2	XINT1	Reserved	ADCINT2	ADCINT1
	(LPM/WD)	(TIMER 0)	(ADC)	Ext. int. 2	Ext. int. 1	–	(ADC)	(ADC)
	0xD4E	0xD4C	0xD4A	0xD48	0xD46	0xD44	0xD42	0xD40
INT2.y	Reserved	EPWM7_TZINT	EPWM6_TZINT	EPWM5_TZINT	EPWM4_TZINT	EPWM3_TZINT	EPWM2_TZINT	EPWM1_TZINT
	–	(ePWM7)	(ePWM6)	(ePWM5)	(ePWM4)	(ePWM3)	(ePWM2)	(ePWM1)
	0xD5E	0xD5C	0xD5A	0xD58	0xD56	0xD54	0xD52	0xD50
INT3.y	Reserved	EPWM7_INT	EPWM6_INT	EPWM5_INT	EPWM4_INT	EPWM3_INT	EPWM2_INT	EPWM1_INT
	–	(ePWM7)	(ePWM6)	(ePWM5)	(ePWM4)	(ePWM3)	(ePWM2)	(ePWM1)
	0xD6E	0xD6C	0xD6A	0xD68	0xD66	0xD64	0xD62	0xD60
INT4.y	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	ECAP1_INT
	–	–	–	–	–	–	–	(eCAP1)
	0xD7E	0xD7C	0xD7A	0xD78	0xD76	0xD74	0xD72	0xD70
INT5.y	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	EQEP1_INT
	–	–	–	–	–	–	–	(eQEP1)
	0xD8E	0xD8C	0xD8A	0xD88	0xD86	0xD84	0xD82	0xD80
INT6.y	Reserved	Reserved	Reserved	Reserved	SPITXINTB	SPIRXINTB	SPITXINTA	SPIRXINTA
	–	–	–	–	(SPI-B)	(SPI-B)	(SPI-A)	(SPI-A)
	0xD9E	0xD9C	0xD9A	0xD98	0xD96	0xD94	0xD92	0xD90
INT7.y	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	–	–	–	–	–	–	–	–
	0xDAE	0xDAC	0xDAA	0xDA8	0xDA6	0xDA4	0xDA2	0xDA0
INT8.y	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	I2CINT2A	I2CINT1A
	–	–	–	–	–	–	(I2C-A)	(I2C-A)
	0xDBE	0xDBC	0xDBA	0xDB8	0xDB6	0xDB4	0xDB2	0xDB0
INT9.y	Reserved	Reserved	ECAN1_INTA	ECAN0_INTA	LIN1_INTA	LIN0_INTA	SCITXINTA	SCIRXINTA
	–	–	(CAN-A)	(CAN-A)	(LIN-A)	(LIN-A)	(SCI-A)	(SCI-A)
	0xDCE	0xDCC	0xDCA	0xDC8	0xDC6	0xDC4	0xDC2	0xDC0
INT10.y	ADCINT8	ADCINT7	ADCINT6	ADCINT5	ADCINT4	ADCINT3	ADCINT2	ADCINT1
	(ADC)	(ADC)	(ADC)	(ADC)	(ADC)	(ADC)	(ADC)	(ADC)
	0xDDE	0xDDC	0xDDA	0xDD8	0xDD6	0xDD4	0xDD2	0xDD0
INT11.y	CLA1_INT8	CLA1_INT7	CLA1_INT6	CLA1_INT5	CLA1_INT4	CLA1_INT3	CLA1_INT2	CLA1_INT1
	(CLA)	(CLA)	(CLA)	(CLA)	(CLA)	(CLA)	(CLA)	(CLA)
	0xDEE	0xDEC	0xDEA	0xDE8	0xDE6	0xDE4	0xDE2	0xDE0
INT12.y	LUF	LVF	Reserved	Reserved	Reserved	Reserved	Reserved	XINT3
	(CLA)	(CLA)	–	–	–	–	–	Ext. Int. 3
	0xDFE	0xDFC	0xDFA	0xDF8	0xDF6	0xDF4	0xDF2	0xDF0

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Table 3-11. PIE Configuration and Control Registers

NAME	ADDRESS	SIZE (x16)	DESCRIPTION[1]
PIECTRL	0x0CE0	1	PIE, Control Register
PIEACK	0x0CE1	1	PIE, Acknowledge Register
PIEIER1	0x0CE2	1	PIE, INT1 Group Enable Register
PIEIFR1	0x0CE3	1	PIE, INT1 Group Flag Register
PIEIER2	0x0CE4	1	PIE, INT2 Group Enable Register
PIEIFR2	0x0CE5	1	PIE, INT2 Group Flag Register
PIEIER3	0x0CE6	1	PIE, INT3 Group Enable Register
PIEIFR3	0x0CE7	1	PIE, INT3 Group Flag Register
PIEIER4	0x0CE8	1	PIE, INT4 Group Enable Register
PIEIFR4	0x0CE9	1	PIE, INT4 Group Flag Register
PIEIER5	0x0CEA	1	PIE, INT5 Group Enable Register
PIEIFR5	0x0CEB	1	PIE, INT5 Group Flag Register
PIEIER6	0x0CEC	1	PIE, INT6 Group Enable Register
PIEIFR6	0x0CED	1	PIE, INT6 Group Flag Register
PIEIER7	0x0CEE	1	PIE, INT7 Group Enable Register
PIEIFR7	0x0CEF	1	PIE, INT7 Group Flag Register
PIEIER8	0x0CF0	1	PIE, INT8 Group Enable Register
PIEIFR8	0x0CF1	1	PIE, INT8 Group Flag Register
PIEIER9	0x0CF2	1	PIE, INT9 Group Enable Register
PIEIFR9	0x0CF3	1	PIE, INT9 Group Flag Register
PIEIER10	0x0CF4	1	PIE, INT10 Group Enable Register
PIEIFR10	0x0CF5	1	PIE, INT10 Group Flag Register
PIEIER11	0x0CF6	1	PIE, INT11 Group Enable Register
PIEIFR11	0x0CF7	1	PIE, INT11 Group Flag Register
PIEIER12	0x0CF8	1	PIE, INT12 Group Enable Register
PIEIFR12	0x0CF9	1	PIE, INT12 Group Flag Register
Reserved	0x0CFA 0x0CFF	6	Reserved

(1) The PIE configuration and control registers are not protected by EALLOW mode. The PIE vector table is protected.

3.6.1 External Interrupts

Table 3-12. External Interrupt Registers

NAME	ADDRESS	SIZE (x16)	DESCRIPTION
XINT1CR	0x00 7070	1	XINT1 configuration register
XINT2CR	0x00 7071	1	XINT2 configuration register
XINT3CR	0x00 7072	1	XINT3 configuration register
XINT1CTR	0x00 7078	1	XINT1 counter register
XINT2CTR	0x00 7079	1	XINT2 counter register
XINT3CTR	0x00 707A	1	XINT3 counter register

Each external interrupt can be enabled/disabled or qualified using positive, negative, or both positive and negative edge. For more information, see the *TMS320x2803x Piccolo System Control and Interrupts Reference Guide* (literature number SPRUGL8).

3.7 VREG/BOR/POR

Although the core and I/O circuitry operate on two different voltages, these devices have an on-chip voltage regulator (VREG) to generate the V_{DD} voltage from the V_{DDIO} supply. This eliminates the cost and space of a second external regulator on an application board. Additionally, internal power-on reset (POR) and brown-out reset (BOR) circuits monitor both the V_{DD} and V_{DDIO} rails during power-up and run mode, eliminating a need for any external voltage supervisory circuits.

3.7.1 On-chip Voltage Regulator (VREG)

A linear regulator generates the core voltage (V_{DD}) from the V_{DDIO} supply. Therefore, although capacitors are required on each V_{DD} pin to stabilize the generated voltage, power need not be supplied to these pins to operate the device. Conversely, the VREG can be disabled, should power or redundancy be the primary concern of the application.

3.7.1.1 Using the On-chip VREG

To utilize the on-chip VREG, the $\overline{VREGENZ}$ pin should be pulled low and the appropriate recommended operating voltage should be supplied to the V_{DDIO} and V_{DDA} pins. In this case, the V_{DD} voltage needed by the core logic will be generated by the VREG. Each V_{DD} pin requires on the order of 1.2 µF (minimum) capacitance for proper regulation of the VREG. These capacitors should be located as close as possible to the V_{DD} pins.

3.7.1.2 Disabling the On-chip VREG

To conserve power, it is also possible to disable the on-chip VREG and supply the core logic voltage to the V_{DD} pins with a more efficient external regulator. To enable this option, the $\overline{VREGENZ}$ pin must be pulled high.

3.7.2 On-chip Power-On Reset (POR) and Brown-Out Reset (BOR) Circuit

Two on-chip supervisory circuits, the power-on reset (POR) and the brown-out reset (BOR) remove the burden of monitoring the V_{DD} and V_{DDIO} supply rails from the application board. The purpose of the POR is to create a clean reset throughout the device during the entire power-up procedure. The trip point is a looser, lower trip point than the BOR, which watches for dips in the V_{DD} or V_{DDIO} rail during device operation. The POR function is present on both V_{DD} and V_{DDIO} rails at all times. After initial device power-up, the BOR function is present on V_{DDIO} at all times, and on V_{DD} when the internal VREG is enabled ($\overline{VREGENZ}$ pin is pulled low). Both functions pull the $\overline{XRS}$ pin low when one of the voltages is below their respective trip point. See Section 6 for the various trip points as well as the delay time from the voltage rising past the trip point and the release of the $\overline{XRS}$ pin. Figure 3-6 shows the VREG, POR, and BOR.

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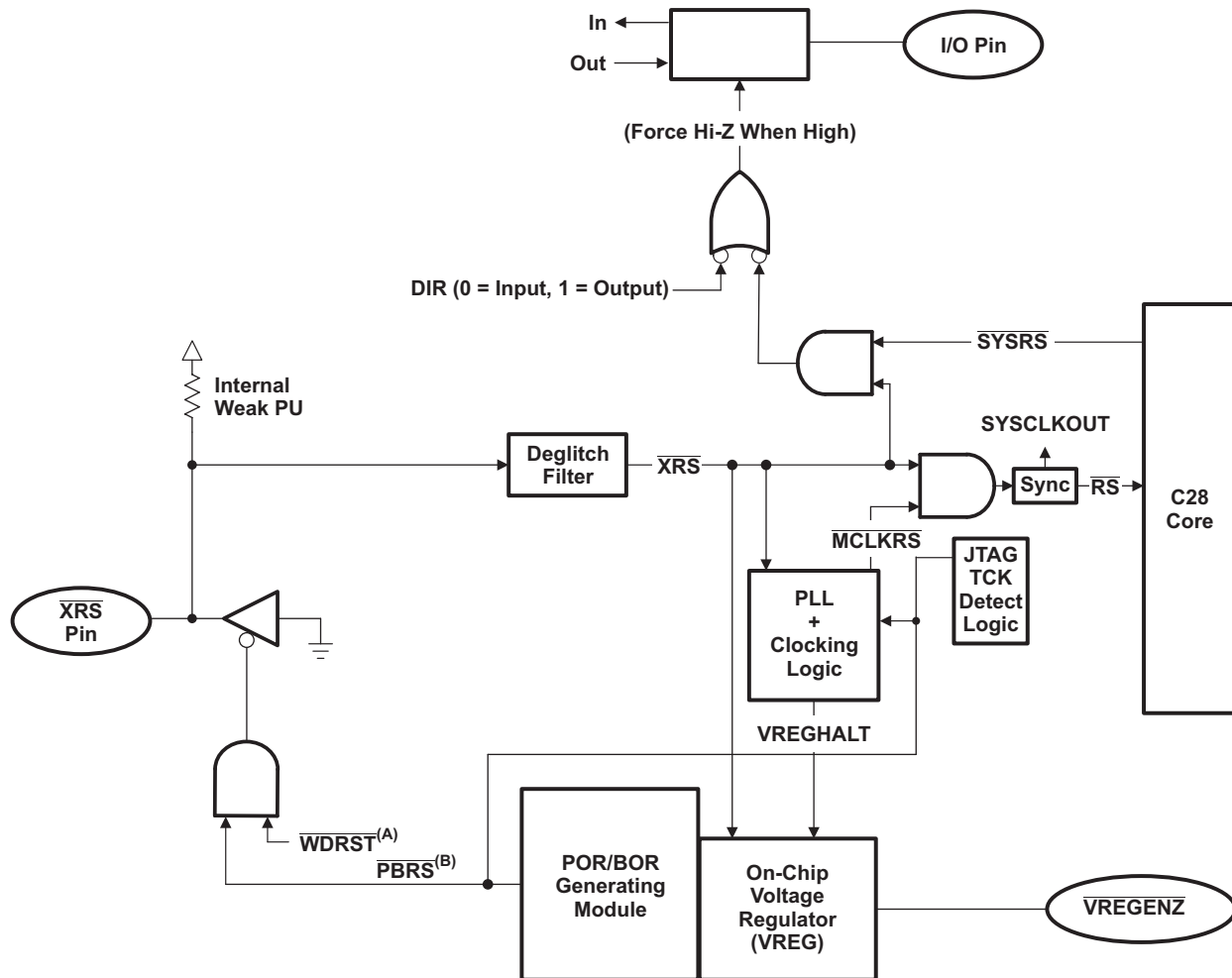
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A. $\overline{\text{WDRST}}$ is the reset signal from the CPU-watchdog.

B. $\overline{\text{PBRS}}$ is the reset signal from the POR/BOR module.

**Figure 3-6. VREG + POR + BOR + Reset Signal Connectivity**

3.8 System Control

This section describes the oscillator and clocking mechanisms, the watchdog function and the low power modes.

Table 3-13. PLL, Clocking, Watchdog, and Low-Power Mode Registers

NAME	ADDRESS	SIZE (x16)	DESCRIPTION[1]
XCLK	0x00 7010	1	XCLKOUT Control
PLLSTS	0x00 7011	1	PLL Status Register
CLKCTL	0x00 7012	1	Clock Control Register
PLLLOCKPRD	0x00 7013	1	PLL Lock Period
INTOSC1TRIM	0x00 7014	1	Internal Oscillator 1 Trim Register
INTOSC2TRIM	0x00 7016	1	Internal Oscillator 2 Trim Register
LOSPCP	0x00 701B	1	Low-Speed Peripheral Clock Prescaler Register
PCLKCR0	0x00 701C	1	Peripheral Clock Control Register 0
PCLKCR1	0x00 701D	1	Peripheral Clock Control Register 1
LPMCR0	0x00 701E	1	Low Power Mode Control Register 0
PCLKCR3	0x00 7020	1	Peripheral Clock Control Register 3
PLLCR	0x00 7021	1	PLL Control Register
SCSR	0x00 7022	1	System Control and Status Register
WDCNTR	0x00 7023	1	Watchdog Counter Register
WDKEY	0x00 7025	1	Watchdog Reset Key Register
WDCR	0x00 7029	1	Watchdog Control Register

(1) All registers in this table are EALLOW protected.

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Figure 3-7 shows the various clock domains that are discussed. Figure 3-8 shows the various clock sources (both internal and external) that can provide a clock for device operation.
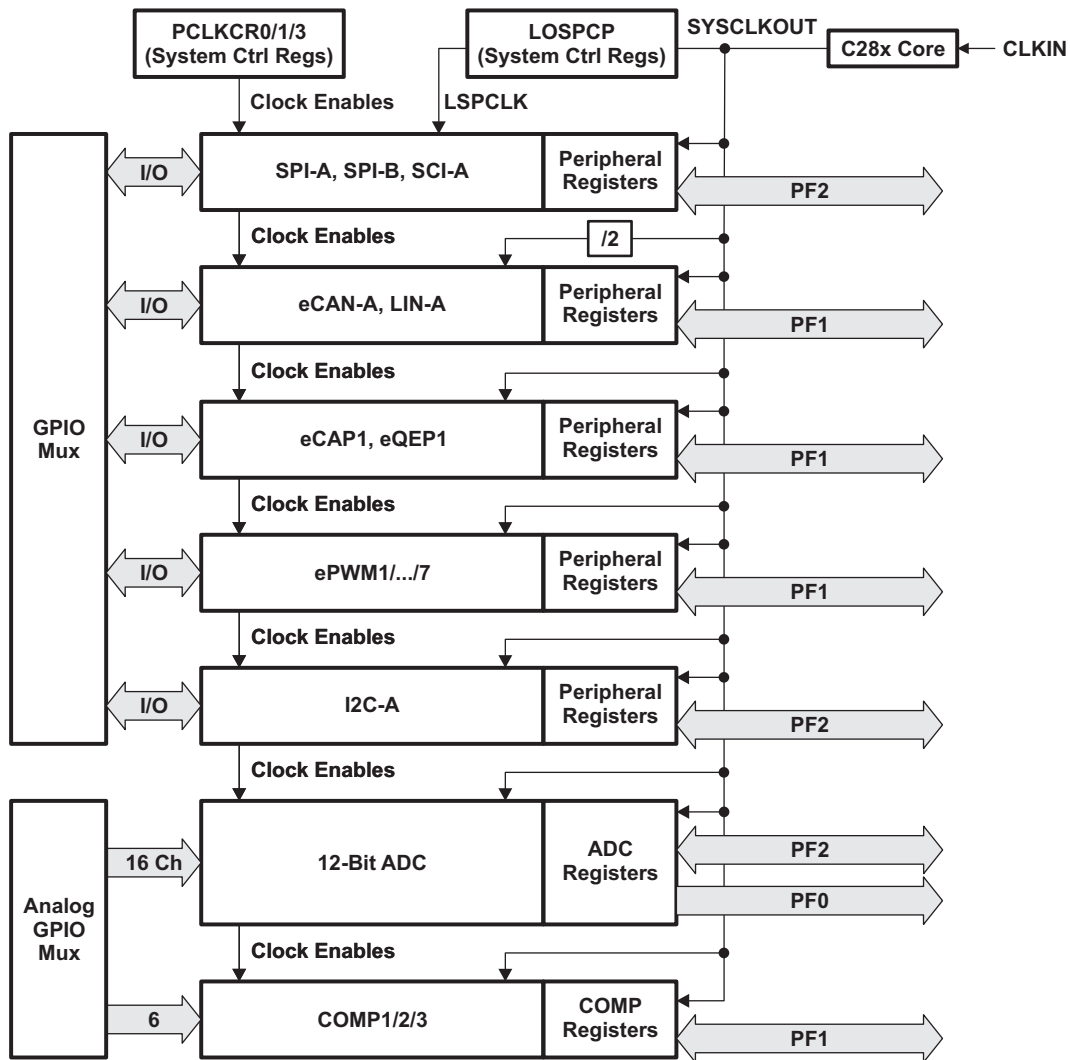
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A.   CLKIN is the clock into the CPU. It is passed out of the CPU as SYSCLKOUT (that is, CLKIN is the same frequency as SYSCLKOUT).

Figure 3-7. Clock and Reset Domains

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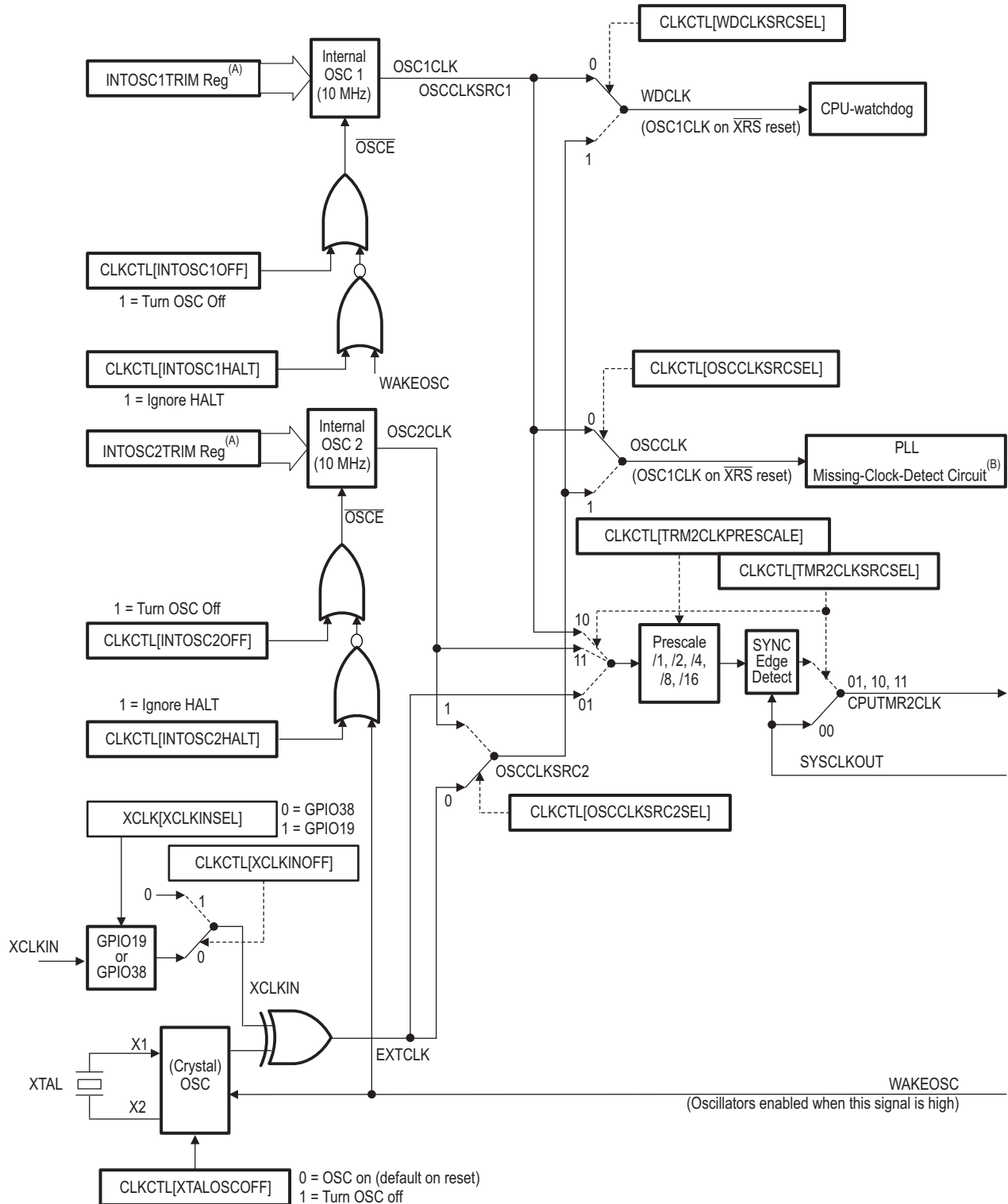
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A.   Register loaded from TI OTP-based calibration function.

B.   See Section 3.8.4 for details on missing clock detection.

Figure 3-8. Clock Tree

3.8.1 Internal Zero Pin Oscillators

The F2803x devices contain two independent internal zero pin oscillators. By default both oscillators are turned on at power up, and internal oscillator 1 is the default clock source at this time. For power savings, unused oscillators may be powered down by the user. The center frequency of these oscillators is determined by their respective oscillator trim registers, written to in the calibration routine as part of the boot ROM execution. See the electrical section for more information on these oscillators.

3.8.2 Crystal Oscillator Option

The typical specifications for the external quartz crystal (fundamental mode, parallel resonant) are listed in Table 3-14. Furthermore, ESR range = 30 to 150 Ω.

Table 3-14. Typical Specifications for External Quartz Crystal

FREQUENCY (MHz)	R_d (Ω)	C_{L1} (pF)	C_{L2} (pF)	C_L (pF)
5	2200	18	18	12
10	470	15	15	12
15	0	12	15	12
20	0	12	12	12
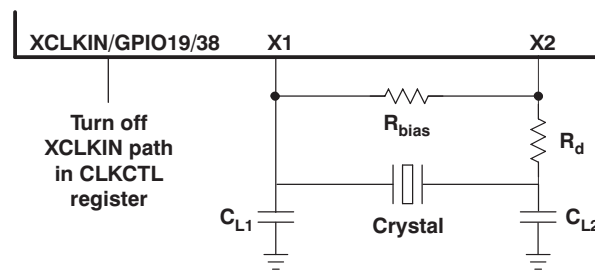
A.   X1/X2 pins are available in 48-pin package only.

Figure 3-9. Using the On-chip Crystal Oscillator

NOTE

1. C_{L1} and C_{L2} are the total capacitance of the circuit board and components excluding the IC and crystal. The value is usually approximately twice the value of the crystal's load capacitance.

2. R_{bias} is generally 2.0 MΩ.

3. The load capacitance of the crystal is described in the crystal specifications of the manufacturers.

4. TI recommends that customers have the resonator/crystal vendor characterize the operation of their device with the MCU chip. The resonator/crystal vendor has the equipment and expertise to tune the tank circuit. The vendor can also advise the customer regarding the proper tank component values that will produce proper start up and stability over the entire operating range.
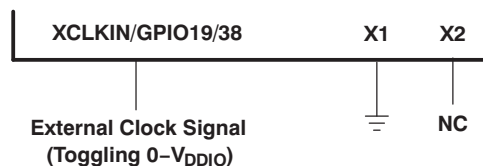
Figure 3-10. Using a 3.3-V External Oscillator

3.8.3 PLL-Based Clock Module

The devices have an on-chip, PLL-based clock module. This module provides all the necessary clocking signals for the device, as well as control for low-power mode entry. The PLL has a 4-bit ratio control PLLCR[DIV] to select different CPU clock rates. The watchdog module should be disabled before writing to the PLLCR register. It can be re-enabled (if need be) after the PLL module has stabilized, which takes 1 ms. The input clock and PLLCR[DIV] bits should be chosen in such a way that the output frequency of the PLL (VCOCLK) is at least 50 MHz.

Table 3-15. PLL Settings

PLLCR[DIV] VALUE[1][2]	SYSCLKOUT (CLKIN)		
	PLLSTS[DIVSEL] = 0 or 1[3]	PLLSTS[DIVSEL] = 2	PLLSTS[DIVSEL] = 3
0000 (PLL bypass)	OSCCLK/4 (Default)[1]	OSCCLK/2	OSCCLK
0001	(OSCCLK * 1)/4	(OSCCLK * 1)/2	–
0010	(OSCCLK * 2)/4	(OSCCLK * 2)/2	–
0011	(OSCCLK * 3)/4	(OSCCLK * 3)/2	–
0100	(OSCCLK * 4)/4	(OSCCLK * 4)/2	–
0101	(OSCCLK * 5)/4	(OSCCLK * 5)/2	–
0110	(OSCCLK * 6)/4	(OSCCLK * 6)/2	–
0111	(OSCCLK * 7)/4	(OSCCLK * 7)/2	–
1000	(OSCCLK * 8)/4	(OSCCLK * 8)/2	–
1001	(OSCCLK * 9)/4	(OSCCLK * 9)/2	–
1010	(OSCCLK * 10)/4	(OSCCLK * 10)/2	–
1011	(OSCCLK * 11)/4	(OSCCLK * 11)/2	–
1100	(OSCCLK * 12)/4	(OSCCLK * 12)/2	–

(1) The PLL control register (PLLCR) and PLL Status Register (PLLSTS) are reset to their default state by the $\overline{XRS}$ signal or a watchdog reset only. A reset issued by the debugger or the missing clock detect logic has no effect.
(2) This register is EALLOW protected. See the *TMS320x2803x Piccolo System Control and Interrupts Reference Guide* (literature number SPRUGL8) for more information.
(3) By default, PLLSTS[DIVSEL] is configured for /4. (The boot ROM changes this to /1.) PLLSTS[DIVSEL] must be 0 before writing to the PLLCR and should be changed only after PLLSTS[PLLLOCKS] = 1.

Table 3-16. CLKIN Divide Options

PLLSTS [DIVSEL]	CLKIN DIVIDE
0	/4
1	/4
2	/2
3	/1[1]

(1) This mode can be used only when the PLL is bypassed or off.

The PLL-based clock module provides four modes of operation:

- **INTOSC1 (Internal Zero-pin Oscillator 1):** This is the on-chip internal oscillator 1. This can provide the clock for the Watchdog block, core and CPU-Timer 2

- **INTOSC2 (Internal Zero-pin Oscillator 2):** This is the on-chip internal oscillator 2. This can provide the clock for the Watchdog block, core and CPU-Timer 2. Both INTOSC1 and INTOSC2 can be independently chosen for the Watchdog block, core and CPU-Timer 2.

- **Crystal/Resonator Operation:** The on-chip (crystal) oscillator enables the use of an external crystal/resonator attached to the device to provide the time base. The crystal/resonator is connected to the X1/X2 pins. Some devices may not have the X1/X2 pins. See for details.

- **External Clock Source Operation:** If the on-chip (crystal) oscillator is not used, this mode allows it to be bypassed. The device clocks are generated from an external clock source input on the XCLKIN pin. Note that the XCLKIN is multiplexed with GPIO19 or GPIO38 pin. The XCLKIN input can be selected as GPIO19 or GPIO38 via the XCLKINSEL bit in XCLK register. The CLKCTL[XCLKINOFF] bit

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disables this clock input (forced low). If the clock source is not used or the respective pins are used as GPIOs, the user should disable at boot time.

Before changing clock sources, ensure that the target clock is present. If a clock is not present, then that clock source must be disabled (using the CLKCTL register) before switching clocks.

Table 3-17. Possible PLL Configuration Modes

PLL MODE	REMARKS	PLLSTS[DIVSEL]	CLKIN AND SYSCLKOUT
PLL Off	Invoked by the user setting the PLLOFF bit in the PLLSTS register. The PLL block is disabled in this mode. This can be useful to reduce system noise and for low power operation. The PLLCR register must first be set to 0x0000 (PLL Bypass) before entering this mode. The CPU clock (CLKIN) is derived directly from the input clock on either X1/X2, X1 or XCLKIN.	0, 1 2 3	OSCCLK/4 OSCCLK/2 OSCCLK/1
PLL Bypass	PLL Bypass is the default PLL configuration upon power-up or after an external reset ($\overline{XRS}$). This mode is selected when the PLLCR register is set to 0x0000 or while the PLL locks to a new frequency after the PLLCR register has been modified. In this mode, the PLL itself is bypassed but the PLL is not turned off.	0, 1 2 3	OSCCLK/4 OSCCLK/2 OSCCLK/1
PLL Enable	Achieved by writing a non-zero value n into the PLLCR register. Upon writing to the PLLCR the device will switch to PLL Bypass mode until the PLL locks.	0, 1 2	OSCCLK*n/4 OSCCLK*n/2

3.8.4 Loss of Input Clock (NMI Watchdog Function)

The 2803x devices may be clocked from either one of the internal zero-pin oscillators (INTOSC1/INTOSC2), the on-chip crystal oscillator, or from an external clock input. Regardless of the clock source, in PLL-enabled and PLL-bypass mode, if the input clock to the PLL vanishes, the PLL will issue a limp-mode clock at its output. This limp-mode clock continues to clock the CPU and peripherals at a typical frequency of 1-5 MHz.

When the limp mode is activated, a $\overline{CLOCKFAIL}$ signal is generated that is latched as an NMI interrupt. Depending on how the NMIRESETSEL bit has been configured, a reset to the device can be fired immediately or the NMI watchdog counter can issue a reset when it overflows. In addition to this, the Missing Clock Status (MCLKSTS) bit is set. The NMI interrupt could be used by the application to detect the input clock failure and initiate necessary corrective action such as switching over to an alternative clock source (if available) or initiate a shut-down procedure for the system.

If the software does not respond to the clock-fail condition, the NMI watchdog triggers a reset after a preprogrammed time interval. Figure 3-11 shows the interrupt mechanisms involved.
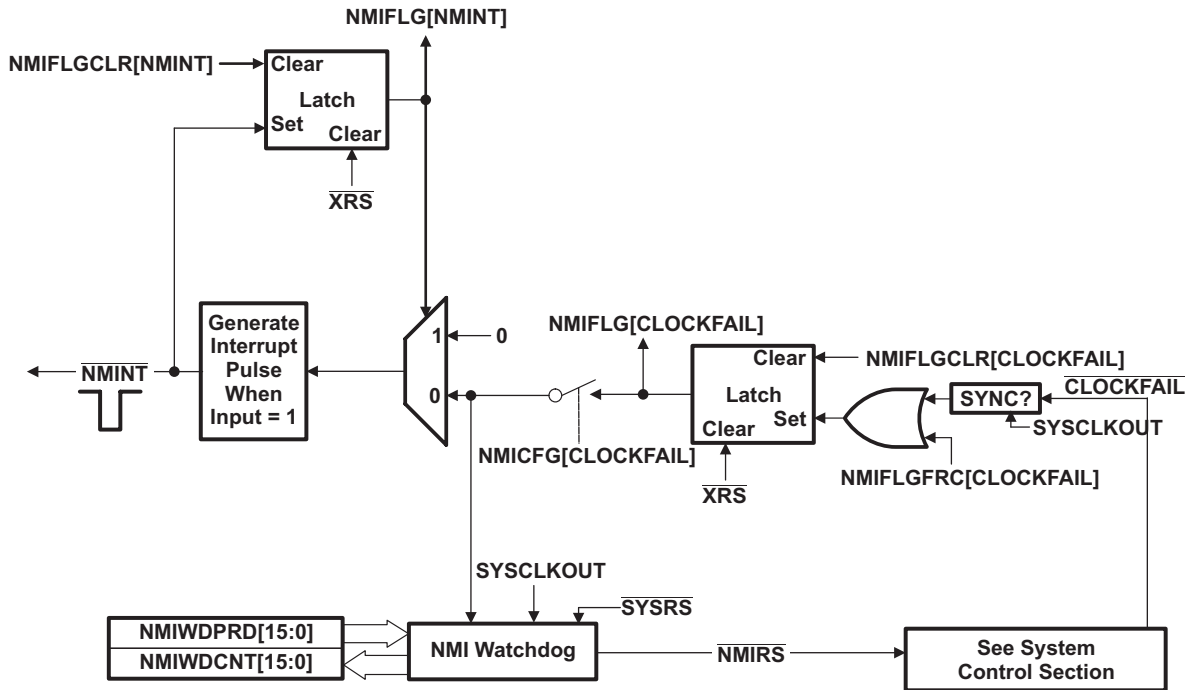
Figure 3-11. NMI-watchdog

3.8.5 CPU-Watchdog Module

The CPU-watchdog module on the 2803x device is similar to the one used on the 281x/280x/283xx devices. This module generates an output pulse, 512 oscillator clocks wide (OSCCLK), whenever the 8-bit watchdog up counter has reached its maximum value. To prevent this, the user must disable the counter or the software must periodically write a 0x55 + 0xAA sequence into the watchdog key register that resets the watchdog counter. Figure 3-12 shows the various functional blocks within the watchdog module.

Normally, when the input clocks are present, the CPU-watchdog counter decrements to initiate a CPU-watchdog reset or WDINT interrupt. However, when the external input clock fails, the CPU-watchdog counter stops decrementing (i.e., the watchdog counter does not change with the limp-mode clock).

NOTE

The CPU-watchdog is different from the NMI watchdog. It is the legacy watchdog that is present in all 28x devices.

NOTE

Applications in which the correct CPU operating frequency is absolutely critical should implement a mechanism by which the MCU will be held in reset, should the input clocks ever fail. For example, an R-C circuit may be used to trigger the $\overline{\text{XRS}}$ pin of the MCU, should the capacitor ever get fully charged. An I/O pin may be used to discharge the capacitor on a periodic basis to prevent it from getting fully charged. Such a circuit would also help in detecting failure of the flash memory.

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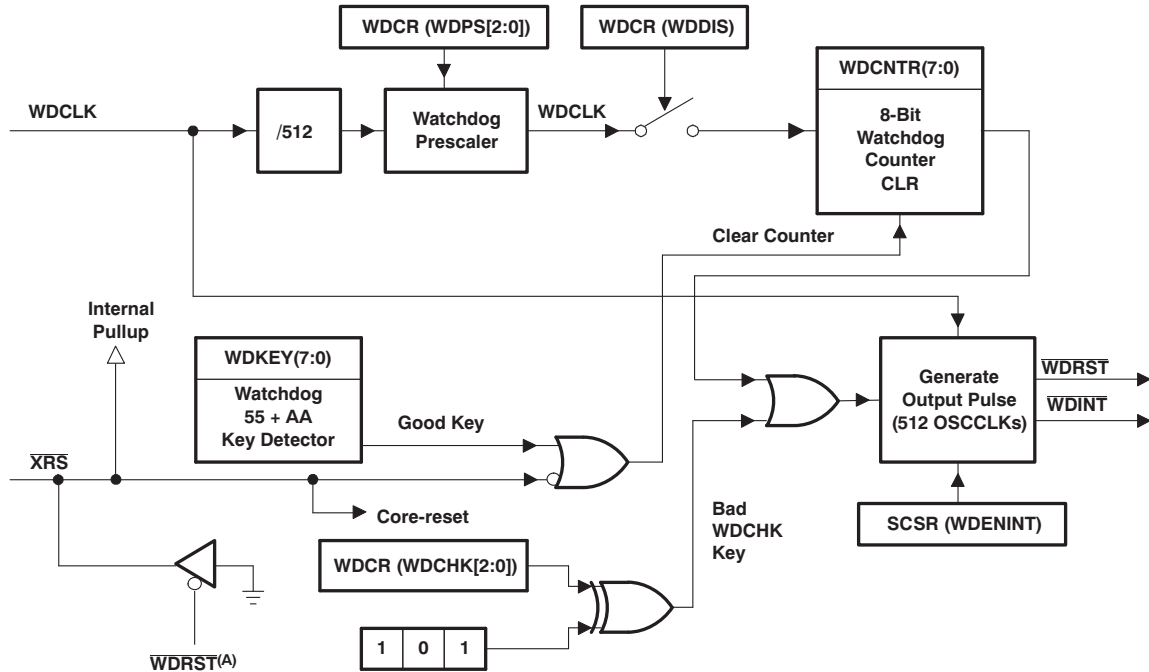
A. The $\overline{\text{WDRST}}$ signal is driven low for 512 OSCCLK cycles.

Figure 3-12. CPU-watchdog Module

The $\overline{\text{WDINT}}$ signal enables the watchdog to be used as a wakeup from IDLE/STANDBY mode.

In STANDBY mode, all peripherals are turned off on the device. The only peripheral that remains functional is the CPU-watchdog. This module will run off OSCCLK. The $\overline{\text{WDINT}}$ signal is fed to the LPM block so that it can wake the device from STANDBY (if enabled). See Section 3.9, Low-power Modes Block, for more details.

In IDLE mode, the $\overline{\text{WDINT}}$ signal can generate an interrupt to the CPU, via the PIE, to take the CPU out of IDLE mode.

In HALT mode, the CPU-watchdog can be used to wake up the device through a device reset.

3.9 Low-power Modes Block

Table 3-18 summarizes the various modes.

Table 3-18. Low-power Modes

MODE	LPMCR0(1:0)	OSCCLK	CLKIN	SYSCLKOUT	EXIT[1]
IDLE	00	On	On	On	$\overline{\text{XRS}}$, CPU-watchdog interrupt, any enabled interrupt
STANDBY	01	On (CPU-watchdog still running)	Off	Off	$\overline{\text{XRS}}$, CPU-watchdog interrupt, GPIO Port A signal, debugger[2]
HALT[3]	1X	Off (on-chip crystal oscillator and PLL turned off, zero-pin oscillator and CPU-watchdog state dependent on user code.)	Off	Off	$\overline{\text{XRS}}$, GPIO Port A signal, debugger[2], CPU-watchdog

(1) The Exit column lists which signals or under what conditions the low power mode is exited. A low signal, on any of the signals, exits the low power condition. This signal must be kept low long enough for an interrupt to be recognized by the device. Otherwise, the low-power mode will not be exited and the device will go back into the indicated low power mode.
(2) The JTAG port can still function even if the CPU clock (CLKIN) is turned off.
(3) The WDCLK must be active for the device to go into HALT mode.

The various low-power modes operate as follows:

IDLE Mode:	This mode is exited by any enabled interrupt that is recognized by the processor. The LPM block performs no tasks during this mode as long as the LPMCR0(LPM) bits are set to 0,0.
STANDBY Mode:	Any GPIO port A signal (GPIO[31:0]) can wake the device from STANDBY mode. The user must select which signal(s) will wake the device in the GPIOLPMSEL register. The selected signal(s) are also qualified by the OSCCLK before waking the device. The number of OSCCLKs is specified in the LPMCR0 register.
HALT Mode:	CPU-watchdog, $\overline{XRS}$, and any GPIO port A signal (GPIO[31:0]) can wake the device from HALT mode. The user selects the signal in the GPIOLPMSEL register.

NOTE

The low-power modes do not affect the state of the output pins (PWM pins included). They will be in whatever state the code left them in when the IDLE instruction was executed. See the *TMS320x2803x Piccolo System Control and Interrupts Reference Guide* (literature number SPRUGL8) for more details.

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4 Peripherals

4.1 Control Law Accelerator (CLA) Overview

The control law accelerator extends the capabilities of the C28x CPU by adding parallel processing. Time-critical control loops serviced by the CLA can achieve low ADC sample to output delay. Thus, the CLA enables faster system response and higher frequency control loops. Utilizing the CLA for time-critical tasks frees up the main CPU to perform other system and communication functions concurrently. The following is a list of major features of the CLA.

- Clocked at the same rate as the main CPU (SYSCLKOUT).
- An independent architecture allowing CLA algorithm execution independent of the main C28x CPU.
  - Complete bus architecture:
    - Program address bus and program data bus
    - Data address bus, data read bus, and data write bus
  - Independent eight-stage pipeline.
  - 12-bit program counter (MPC)
  - Four 32-bit result registers (MR0–MR3)
  - Two 16-bit auxillary registers (MAR0, MAR1)
  - Status register (MSTF)
- Instruction set includes:
  - IEEE single-precision (32-bit) floating-point math operations
  - Floating-point math with parallel load or store
  - Floating-point multiply with parallel add or subtract
  - 1/X and 1/sqrt(X) estimations
  - Data type conversions.
  - Conditional branch and call
  - Data load/store operations
- The CLA program code can consist of up to eight tasks or interrupt service routines.
  - The start address of each task is specified by the MVECT registers.
  - No limit on task size as long as the tasks fit within the CLA program memory space.
  - One task is serviced at a time through to completion. There is no nesting of tasks.
  - Upon task completion, a task-specific interrupt is flagged within the PIE.
  - When a task finishes, the next highest-priority pending task is automatically started.
- Task trigger mechanisms:
  - C28x CPU via the IACK instruction
  - Task1 to Task7: the corresponding ADC or ePWM module interrupt. For example:
    - Task1: ADCINT1 or EPWM1_INT
    - Task2: ADCINT2 or EPWM2_INT
    - Task7: ADCINT7 or EPWM7_INT
  - Task8: ADCINT8 or by CPU Timer 0.
- Memory and Shared Peripherals:
  - Two dedicated message RAMs for communication between the CLA and the main CPU.
  - The C28x CPU can map CLA program and data memory to the main CPU space or CLA space.
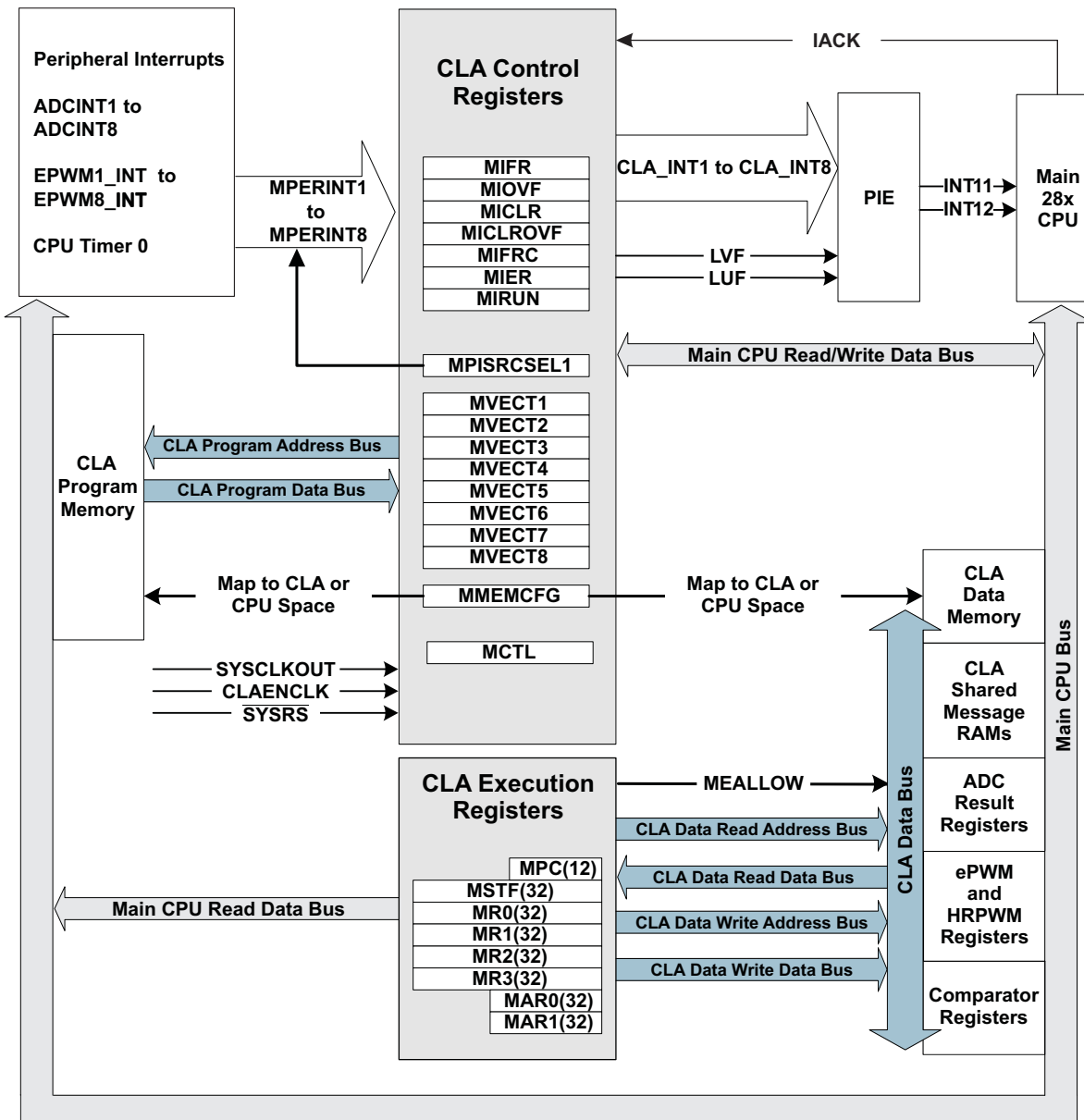 - The CLA has direct access to the ADC Result registers, comparator registers, and the ePWM+HRPWM registers.

Figure 4-1. CLA Block Diagram

Table 4-1. CLA Control Registers

REGISTER NAME	CLA1 ADDRESS	SIZE (x16)	EALLOW PROTECTED	DESCRIPTION[1]
MVECT1	0x1400	1	Yes	CLA Interrupt/Task 1 Start Address
MVECT2	0x1401	1	Yes	CLA Interrupt/Task 2 Start Address
MVECT3	0x1402	1	Yes	CLA Interrupt/Task 3 Start Address
MVECT4	0x1403	1	Yes	CLA Interrupt/Task 4 Start Address
MVECT5	0x1404	1	Yes	CLA Interrupt/Task 5 Start Address
MVECT6	0x1405	1	Yes	CLA Interrupt/Task 6 Start Address
MVECT7	0x1406	1	Yes	CLA Interrupt/Task 7 Start Address
MVECT8	0x1407	1	Yes	CLA Interrupt/Task 8 Start Address

(1)   All registers in this table are CSM protected

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Table 4-1. CLA Control Registers (continued)

REGISTER NAME	CLA1 ADDRESS	SIZE (x16)	EALLOW PROTECTED	DESCRIPTION[1]
MCTL	0x1410	1	Yes	CLA Control Register
MMEMCFG	0x1411	1	Yes	CLA Memory Configure Register
MPISRCSEL1	0x1414	2	Yes	Peripheral Interrupt Source Select Register 1
MIFR	0x1420	1	Yes	Interrupt Flag Register
MIOVF	0x1421	1	Yes	Interrupt Overflow Register
MIFRC	0x1422	1	Yes	Interrupt Force Register
MICLR	0x1423	1	Yes	Interrupt Clear Register
MICLROVF	0x1424	1	Yes	Interrupt Overflow Clear Register
MIER	0x1425	1	Yes	Interrupt Enable Register
MIRUN	0x1426	1	Yes	Interrupt RUN Register
MIPCTL	0x1427	1	Yes	Interrupt Priority Control Register
MPC[2]	0x1428	1	–	CLA Program Counter
MAR0[2]	0x142A	1	–	CLA Aux Register 0
MAR1[2]	0x142B	1	–	CLA Aux Register 1
MSTF[2]	0x142E	2	–	CLA STF Register
MR0[2]	0x1430	2	–	CLA R0H Register
MR1[2]	0x1434	2	–	CLA R1H Register
MR2[2]	0x1438	2	–	CLA R2H Register
MR3[2]	0x143C	2	–	CLA R3H Register

(2)   The main C28x CPU has read only access to this register for debug purposes. The main CPU cannot perform CPU or debugger writes to this register.

Table 4-2. CLA Message RAM

ADDRESS RANGE	SIZE (x16)	EALLOW PROTECTED	DESCRIPTION
0x1480 - 0x14FF	80	Yes	CLA to CPU Message RAM
0x1500 - 0x157F	80	Yes	CPU to CLA Message RAM

4.2 Analog Block

A 12-bit ADC core is implemented that has different timings than the 12-bit ADC used on F280x/F2833x. The ADC wrapper is modified to incorporate the new timings and also other enhancements to improve the timing control of start of conversions.
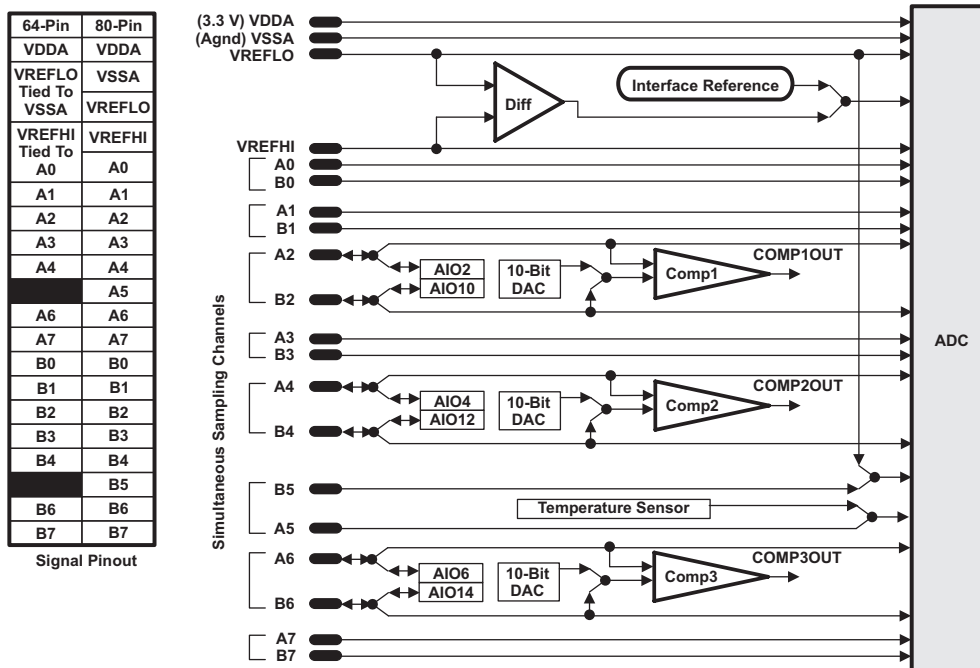

Figure 4-2. Analog Pin Configurations

Figure 4-3 shows the interaction of the analog module with the rest of the F2803x system.

4.2.1 ADC

Table 4-3. ADC Configuration and Control Registers

REGISTER NAME	ADDRESS	SIZE (x16)	EALLOW PROTECTED	DESCRIPTION
ADCCTL1	0x7100	1	Yes	Control 1 Register
ADCINTFLG	0x7104	1	No	Interrupt Flag Register
ADCINTFLGCLR	0x7105	1	No	Interrupt Flag Clear Register
ADCINTOVF	0x7106	1	No	Interrupt Overflow Register
ADCINTOVFCLR	0x7107	1	No	Interrupt Overflow Clear Register
ADCINTSEL1AND2	0x7108	1	Yes	Interrupt 1 and 2 Selection Register
ADCINTSEL3AND4	0x7109	1	Yes	Interrupt 3 and 4 Selection Register
ADCINTSEL5AND6	0x710A	1	Yes	Interrupt 5 and 6 Selection Register
ADCINTSEL7AND8	0x710B	1	Yes	Interrupt 7 and 8 Selection Register
ADCINTSEL9AND10	0x710C	1	Yes	Interrupt 9 Selection Register (reserved Interrupt 10 Selection)
ADCSOCPRIORITYCTL	0x7110	1	Yes	SOC Priority Control Register
ADCSAMPLEMODE	0x7112	1	Yes	Sampling Mode Register
ADCINTSOCSEL1	0x7114	1	Yes	Interrupt SOC Selection 1 Register (for 8 channels)
ADCINTSOCSEL2	0x7115	1	Yes	Interrupt SOC Selection 2 Register (for 8 channels)
ADCSOCFLG1	0x7118	1	No	SOC Flag 1 Register (for 16 channels)
ADCSOCFRC1	0x711A	1	No	SOC Force 1 Register (for 16 channels)

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Table 4-3. ADC Configuration and Control Registers (continued)

REGISTER NAME	ADDRESS	SIZE (x16)	EALLOW PROTECTED	DESCRIPTION
ADCSOCOVF1	0x711C	1	No	SOC Overflow 1 Register (for 16 channels)
ADCSOCOVFCLR1	0x711E	1	No	SOC Overflow Clear 1 Register (for 16 channels)
ADCSOC0CTL to ADCSOC15CTL	0x7120 - 0x712F	1	Yes	SOC0 Control Register to SOC15 Control Register
ADCREFTRIM	0x7140	1	Yes	Reference Trim Register
ADCOFFTRIM	0x7141	1	Yes	Offset Trim Register
ADCREV	0x714F	1	No	Revision Register

Table 4-4. ADC Result Registers (Mapped to PF0)

REGISTER NAME	ADDRESS	SIZE (x16)	EALLOW PROTECTED	DESCRIPTION
ADCRESULT0 to ADCRESULT15	0xB00 - 0xB0F	1	No	ADC Result 0 Register to ADC Result 15 Register

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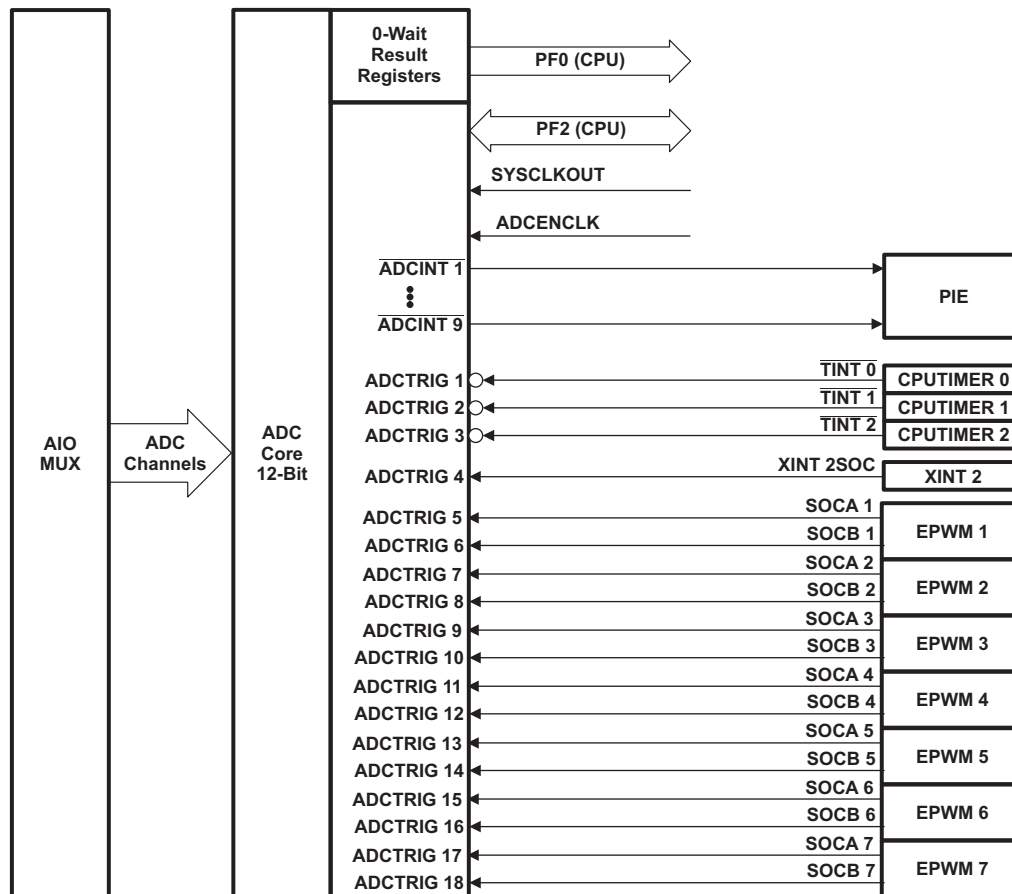
Figure 4-3. ADC Connections

4.2.2 ADC MUX
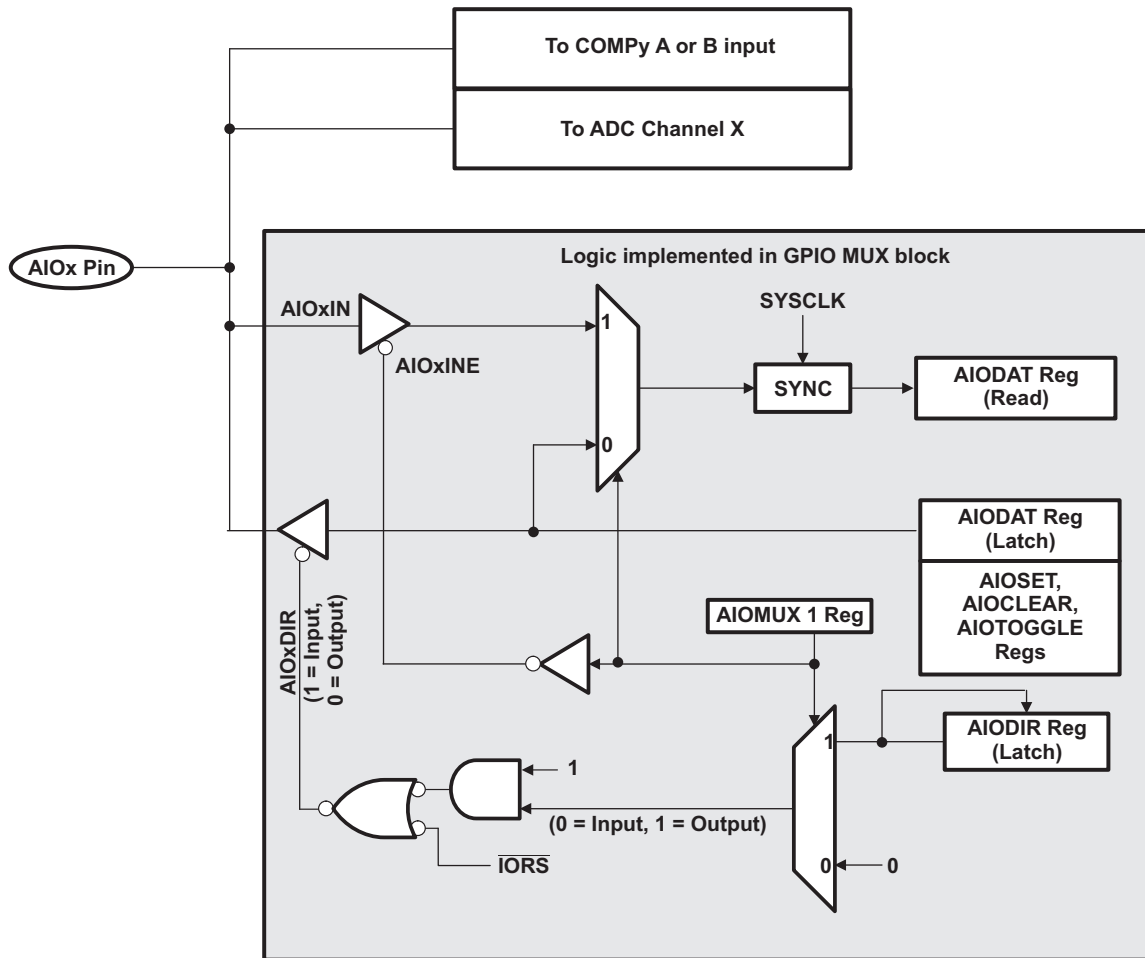
Figure 4-4. ADC MUX

The ADC channel and Comparator functions are always available. The digital I/O function is available only when the respective bit in the AIOMUX1 register is set to 1. In this mode, reading the AIODAT register reflects the actual pin state.

The digital I/O function is disabled when the respective bit in the AIOMUX1 register is cleared to 0. In this mode, reading the AIODAT register reflects the output latch of the AIODAT register and the input digital I/O buffer is disabled to prevent analog signals from generating noise.

On reset, the digital function is disabled. If the pin is used as an analog input, users should keep the AIO function disabled for that pin.

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4.2.3 Comparator Block

Figure 4-5 shows the interaction of the Comparator modules with the rest of the system.
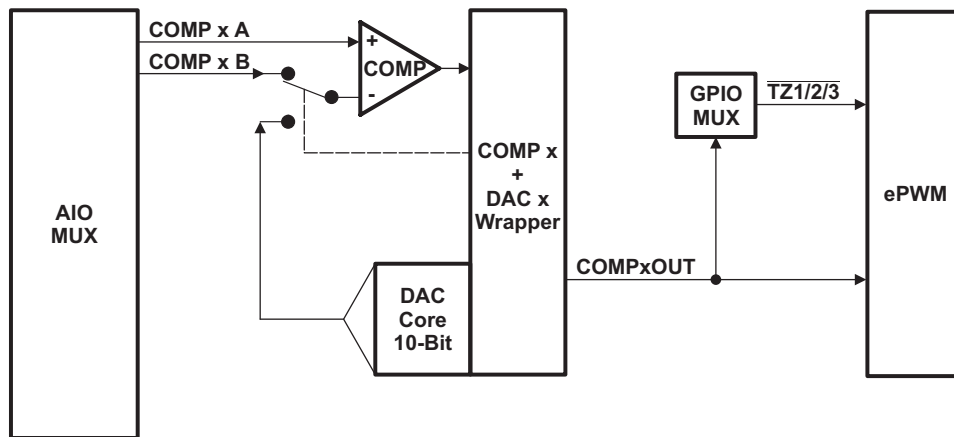
Figure 4-5. Comparator Block Diagram

Table 4-5. Comparator Control Registers

REGISTER NAME	COMP1 ADDRESS	COMP2 ADDRESS	COMP3 ADDRESS	SIZE (x16)	EALLOW PROTECTED	DESCRIPTION
COMPCTL	0x6400	0x6420	0x6440	1	Yes	Comparator Control Register
COMPSTS	0x6402	0x6422	0x6442	1	No	Comparator Status Register
DACVAL	0x6406	0x6426	0x6446	1	Yes	DAC Value Register

4.3 Serial Peripheral Interface (SPI) Module

The device includes the four-pin serial peripheral interface (SPI) module. One SPI module (SPI-A) is available. The SPI is a high-speed, synchronous serial I/O port that allows a serial bit stream of programmed length (one to sixteen bits) to be shifted into and out of the device at a programmable bit-transfer rate. Normally, the SPI is used for communications between the MCU and external peripherals or another processor. Typical applications include external I/O or peripheral expansion through devices such as shift registers, display drivers, and ADCs. Multidevice communications are supported by the master/slave operation of the SPI.

The SPI module features include:

- Four external pins:
  - SPISOMI: SPI slave-output/master-input pin
  - SPISIMO: SPI slave-input/master-output pin
  - $\overline{\text{SPISTE}}$: SPI slave transmit-enable pin
  - SPICLK: SPI serial-clock pin

NOTE: All four pins can be used as GPIO if the SPI module is not used.

- Two operational modes: master and slave

  Baud rate: 125 different programmable rates.

$$\text{Baud rate} = \frac{\text{LSPCLK}}{(\text{SPIBRR} + 1)} \qquad \text{when SPIBRR} = 3 \text{ to } 127$$

$$\text{Baud rate} = \frac{\text{LSPCLK}}{4} \qquad \text{when SPIBRR} = 0,1, 2$$

- Data word length: one to sixteen data bits
- Four clocking schemes (controlled by clock polarity and clock phase bits) include:
  - Falling edge without phase delay: SPICLK active-high. SPI transmits data on the falling edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
  - Falling edge with phase delay: SPICLK active-high. SPI transmits data one half-cycle ahead of the falling edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
  - Rising edge without phase delay: SPICLK inactive-low. SPI transmits data on the rising edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
  - Rising edge with phase delay: SPICLK inactive-low. SPI transmits data one half-cycle ahead of the falling edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
- Simultaneous receive and transmit operation (transmit function can be disabled in software)
- Transmitter and receiver operations are accomplished through either interrupt-driven or polled algorithms.
- Nine SPI module control registers: Located in control register frame beginning at address 7040h.

> **NOTE**
>
> All registers in this module are 16-bit registers that are connected to Peripheral Frame 2. When a register is accessed, the register data is in the lower byte (7-0), and the upper byte (15-8) is read as zeros. Writing to the upper byte has no effect.

Enhanced feature:

- 4-level transmit/receive FIFO
- Delayed transmit control
- Bi-directional 3 wire SPI mode support
- Audio data receive support via $\overline{\text{SPISTE}}$ inversion

The SPI port operation is configured and controlled by the registers listed in Table 4-6.

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Table 4-6. SPI-A Registers

NAME	ADDRESS	SIZE (x16)	EALLOW PROTECTED	DESCRIPTION[1]
SPICCR	0x7040	1	No	SPI-A Configuration Control Register
SPICTL	0x7041	1	No	SPI-A Operation Control Register
SPISTS	0x7042	1	No	SPI-A Status Register
SPIBRR	0x7044	1	No	SPI-A Baud Rate Register
SPIRXEMU	0x7046	1	No	SPI-A Receive Emulation Buffer Register
SPIRXBUF	0x7047	1	No	SPI-A Serial Input Buffer Register
SPITXBUF	0x7048	1	No	SPI-A Serial Output Buffer Register
SPIDAT	0x7049	1	No	SPI-A Serial Data Register
SPIFFTX	0x704A	1	No	SPI-A FIFO Transmit Register
SPIFFRX	0x704B	1	No	SPI-A FIFO Receive Register
SPIFFCT	0x704C	1	No	SPI-A FIFO Control Register
SPIPRI	0x704F	1	No	SPI-A Priority Control Register

(1) Registers in this table are mapped to Peripheral Frame 2. This space only allows 16-bit accesses. 32-bit accesses produce undefined results.

Table 4-7. SPI-B Registers

NAME	ADDRESS	SIZE (x16)	EALLOW PROTECTED	DESCRIPTION[1]
SPICCR	0x7740	1	No	SPI-B Configuration Control Register
SPICTL	0x7741	1	No	SPI-B Operation Control Register
SPISTS	0x7742	1	No	SPI-B Status Register
SPIBRR	0x7744	1	No	SPI-B Baud Rate Register
SPIRXEMU	0x7746	1	No	SPI-B Receive Emulation Buffer Register
SPIRXBUF	0x7747	1	No	SPI-B Serial Input Buffer Register
SPITXBUF	0x7748	1	No	SPI-B Serial Output Buffer Register
SPIDAT	0x7749	1	No	SPI-B Serial Data Register
SPIFFTX	0x774A	1	No	SPI-B FIFO Transmit Register
SPIFFRX	0x774B	1	No	SPI-B FIFO Receive Register
SPIFFCT	0x774C	1	No	SPI-B FIFO Control Register
SPIPRI	0x774F	1	No	SPI-B Priority Control Register

(1) Registers in this table are mapped to Peripheral Frame 2. This space only allows 16-bit accesses. 32-bit accesses produce undefined results.

Figure 4-6 is a block diagram of the SPI in slave mode.
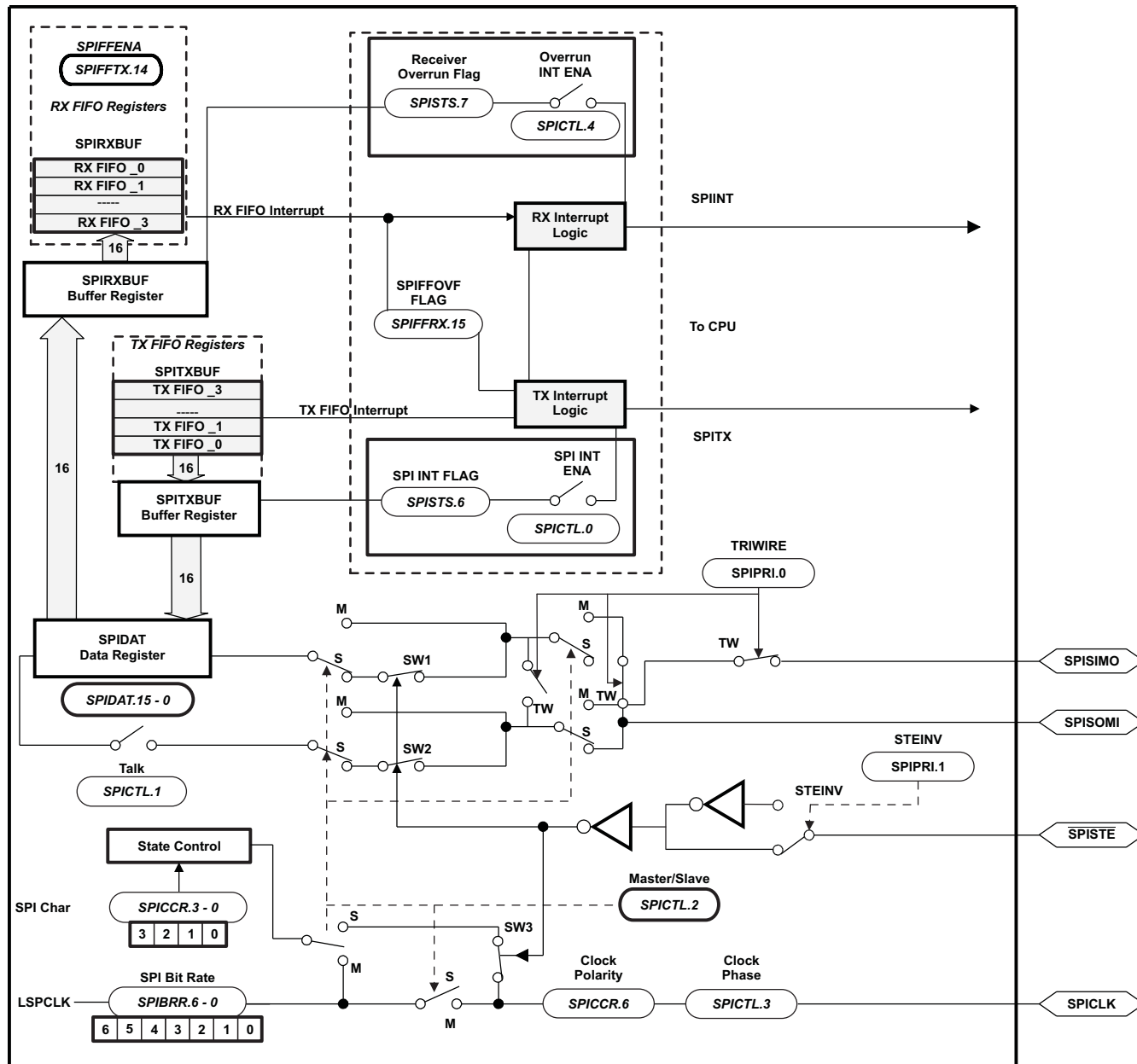
A.   SPISTE is driven low by the master for a slave device.

Figure 4-6. SPI Module Block Diagram (Slave Mode)

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4.4 Serial Communications Interface (SCI) Module

The devices include one serial communications interface (SCI) module (SCI-A). The SCI module supports digital communications between the CPU and other asynchronous peripherals that use the standard non-return-to-zero (NRZ) format. The SCI receiver and transmitter are double-buffered, and each has its own separate enable and interrupt bits. Both can be operated independently or simultaneously in the full-duplex mode. To ensure data integrity, the SCI checks received data for break detection, parity, overrun, and framing errors. The bit rate is programmable to over 65000 different speeds through a 16-bit baud-select register.

Features of each SCI module include:

- Two external pins:
  - SCITXD: SCI transmit-output pin
  - SCIRXD: SCI receive-input pin
    NOTE: Both pins can be used as GPIO if not used for SCI.
  - Baud rate programmable to 64K different rates:

$$\text{Baud rate} = \frac{\text{LSPCLK}}{(\text{BRR} + 1) * 8} \qquad \text{when BRR} \neq 0$$

$$\text{Baud rate} = \frac{\text{LSPCLK}}{16} \qquad \text{when BRR} = 0$$

- Data-word format
  - One start bit
  - Data-word length programmable from one to eight bits
  - Optional even/odd/no parity bit
  - One or two stop bits
- Four error-detection flags: parity, overrun, framing, and break detection
- Two wake-up multiprocessor modes: idle-line and address bit
- Half- or full-duplex operation
- Double-buffered receive and transmit functions
- Transmitter and receiver operations can be accomplished through interrupt-driven or polled algorithms with status flags.
  - Transmitter: TXRDY flag (transmitter-buffer register is ready to receive another character) and TX EMPTY flag (transmitter-shift register is empty)
  - Receiver: RXRDY flag (receiver-buffer register is ready to receive another character), BRKDT flag (break condition occurred), and RX ERROR flag (monitoring four interrupt conditions)
- Separate enable bits for transmitter and receiver interrupts (except BRKDT)
- NRZ (non-return-to-zero) format

NOTE

All registers in this module are 8-bit registers that are connected to Peripheral Frame 2. When a register is accessed, the register data is in the lower byte (7-0), and the upper byte (15-8) is read as zeros. Writing to the upper byte has no effect.

Enhanced features:
- Auto baud-detect hardware logic
- 4-level transmit/receive FIFO

The SCI port operation is configured and controlled by the registers listed in Table 4-8.

Table 4-8. SCI-A Registers[1]

NAME	ADDRESS	SIZE (x16)	EALLOW PROTECTED	DESCRIPTION
SCICCRA	0x7050	1	No	SCI-A Communications Control Register
SCICTL1A	0x7051	1	No	SCI-A Control Register 1
SCIHBAUDA	0x7052	1	No	SCI-A Baud Register, High Bits
SCILBAUDA	0x7053	1	No	SCI-A Baud Register, Low Bits
SCICTL2A	0x7054	1	No	SCI-A Control Register 2
SCIRXSTA	0x7055	1	No	SCI-A Receive Status Register
SCIRXEMUA	0x7056	1	No	SCI-A Receive Emulation Data Buffer Register
SCIRXBUFA	0x7057	1	No	SCI-A Receive Data Buffer Register
SCITXBUFA	0x7059	1	No	SCI-A Transmit Data Buffer Register
SCIFFTXA[2]	0x705A	1	No	SCI-A FIFO Transmit Register
SCIFFRXA[2]	0x705B	1	No	SCI-A FIFO Receive Register
SCIFFCTA[2]	0x705C	1	No	SCI-A FIFO Control Register
SCIPRIA	0x705F	1	No	SCI-A Priority Control Register

(1)   Registers in this table are mapped to Peripheral Frame 2 space. This space only allows 16-bit accesses. 32-bit accesses produce undefined results.
(2)   These registers are new registers for the FIFO mode.

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Figure 4-7 shows the SCI module block diagram.
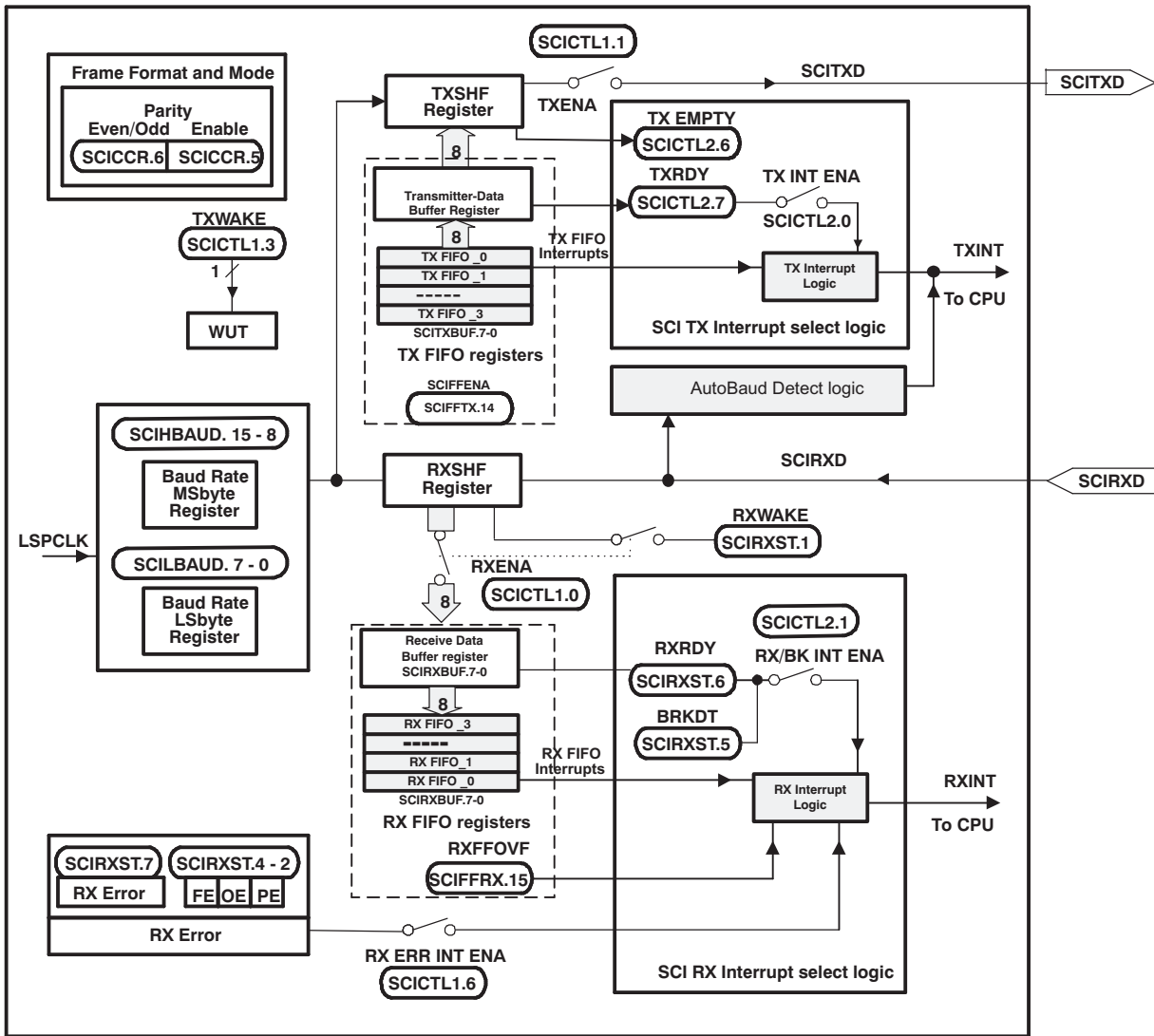
Figure 4-7. Serial Communications Interface (SCI) Module Block Diagram

4.5 Local Interconnect Network (LIN)

The device contains one LIN controller. The LIN standard is based on the SCI (UART) serial data link format. The LIN module can be configured to work as a SCI as well.

The LIN module has the following features:

- Compatible to LIN 1.3 or 2.0 protocols
- Two external pins: LINRX and LINTX
- Multi-buffered receive and transmit units
- Identification masks for message filtering
- Automatic master header generation
    - Programmable sync break field
    - Sync field
    - Identifier field
- Slave automatic synchronization
    - Sync break detection
    - Optional baudrate update
    - Synchronization validation
- 2^{31} programmable transmission rates with 7 fractional bits
- Wakeup on LINRX dominant level from transceiver
- Automatic wakeup support
    - Wakeup signal generation
    - Expiration times on wakeup signals
- Automatic bus idle detection
- Error detection
    - Bit error
    - Bus error
    - No-response error
    - Checksum error
    - Sync field error
    - Parity error
- 2 Interrupt lines with priority encoding for:
    - Receive
    - Transmit
    - ID, error and status

The registers in Table 4-9 configure and control the operation of the LIN module.

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Table 4-9. LIN-A Registers[1]

NAME	ADDRESS	SIZE (x16)	DESCRIPTION
SCIGCR0	0x6C00	2	Global Control Register 0
SCIGCR1	0x6C02	2	Global Control Register 1
SCIGCR2	0x6C04	2	Global Control Register 2
SCISETINT	0x6C06	2	Interrupt Enable Register
SCICLEARINT	0x6C08	2	Interrupt Disable Register
SCISETINTLVL	0x6C0A	2	Set Interrupt Level Register
SCICLEARINTLVL	0x6C0C	2	Clear Interrupt Level Register
SCIFLR	0x6C0E	2	Flag Register
SCIINTVECT0	0x6C10	2	Interrupt Vector Offset Register 0
SCIINTVECT1	0x6C12	2	Interrupt Vector Offset Register 1
SCIFORMAT	0x6C14	2	Length Control register
BRSR	0x6C16	2	Baud Rate Selection Register
SCIED	0x6C18	2	Emulation buffer register
SCIRD	0x6C1A	2	Receiver data buffer register
SCITD	0x6C1C	2	Transmit data buffer register
Reserved	0x6C1E	4	RSVD
SIPIO2	0x6C22	2	Pin control register 2
Reserved	0x6C24	10	RSVD
LINCOMP	0x6C30	2	Compare register
LINRD0	0x6C32	2	Receive data register 0
LINRD1	0x6C34	2	Receive data register 1
LINMASK	0x6C36	2	Acceptance mask register
LINID	0x6C38	2	Register containing ID- byte, ID-SlaveTask byte, and ID received fields.
LINTD0	0x6C3A	2	Transmit Data Register 0
LINTD1	0x6C3C	2	Transmit Data Register 1
MBRSR	0x6C3E	2	Baud Rate Selection Register
Reserved	0x6C40	8	RSVD
IODFTCTRL	0x6C48	2	IODFT for BLIN

(1) Some registers and some bits in other registers are EALLOW-protected. See the *TMS320x2803x Piccolo Local Interconnect Network (LIN) Module Reference Guide* (literature number SPRUGE2) for more details.

Figure 4-8 shows the LIN module block diagram.
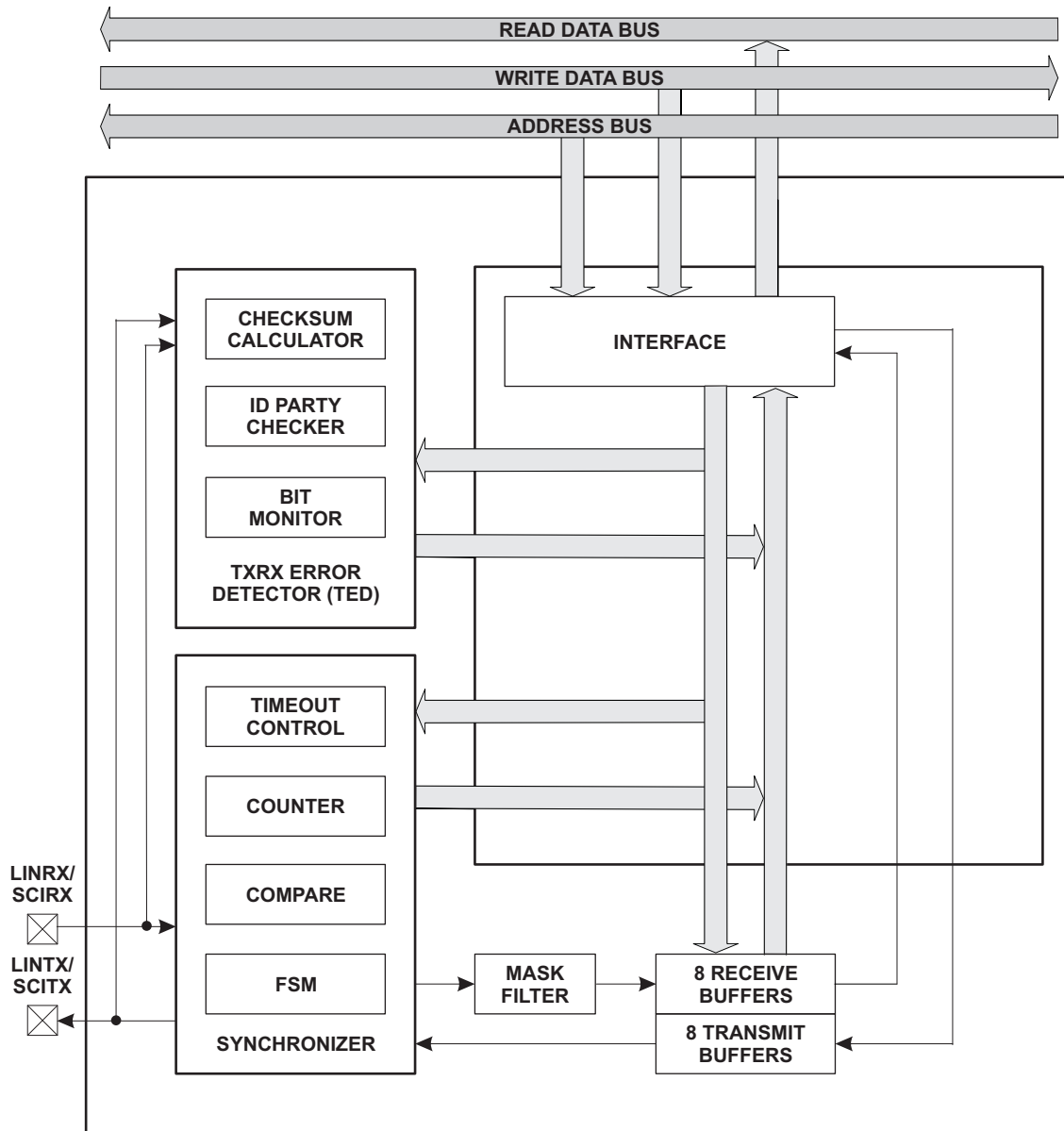
Figure 4-8. LIN Block Diagram

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4.6 Enhanced Controller Area Network (eCAN) Module

The CAN module (eCAN-A) has the following features:

- Fully compliant with CAN protocol, version 2.0B
- Supports data rates up to 1 Mbps
- Thirty-two mailboxes, each with the following properties:
  - Configurable as receive or transmit
  - Configurable with standard or extended identifier
  - Has a programmable receive mask
  - Supports data and remote frame
  - Composed of 0 to 8 bytes of data
  - Uses a 32-bit time stamp on receive and transmit message
  - Protects against reception of new message
  - Holds the dynamically programmable priority of transmit message
  - Employs a programmable interrupt scheme with two interrupt levels
  - Employs a programmable alarm on transmission or reception time-out
- Low-power mode
- Programmable wake-up on bus activity
- Automatic reply to a remote request message
- Automatic retransmission of a frame in case of loss of arbitration or error
- 32-bit local network time counter synchronized by a specific message (communication in conjunction with mailbox 16)
- Self-test mode
  - Operates in a loopback mode receiving its own message. A "dummy" acknowledge is provided, thereby eliminating the need for another node to provide the acknowledge bit.

NOTE

For a SYSCLKOUT of 60 MHz, the smallest bit rate possible is 9.375 kbps.

The F2803x CAN has passed the conformance test per ISO/DIS 16845. Contact TI for test report and exceptions.
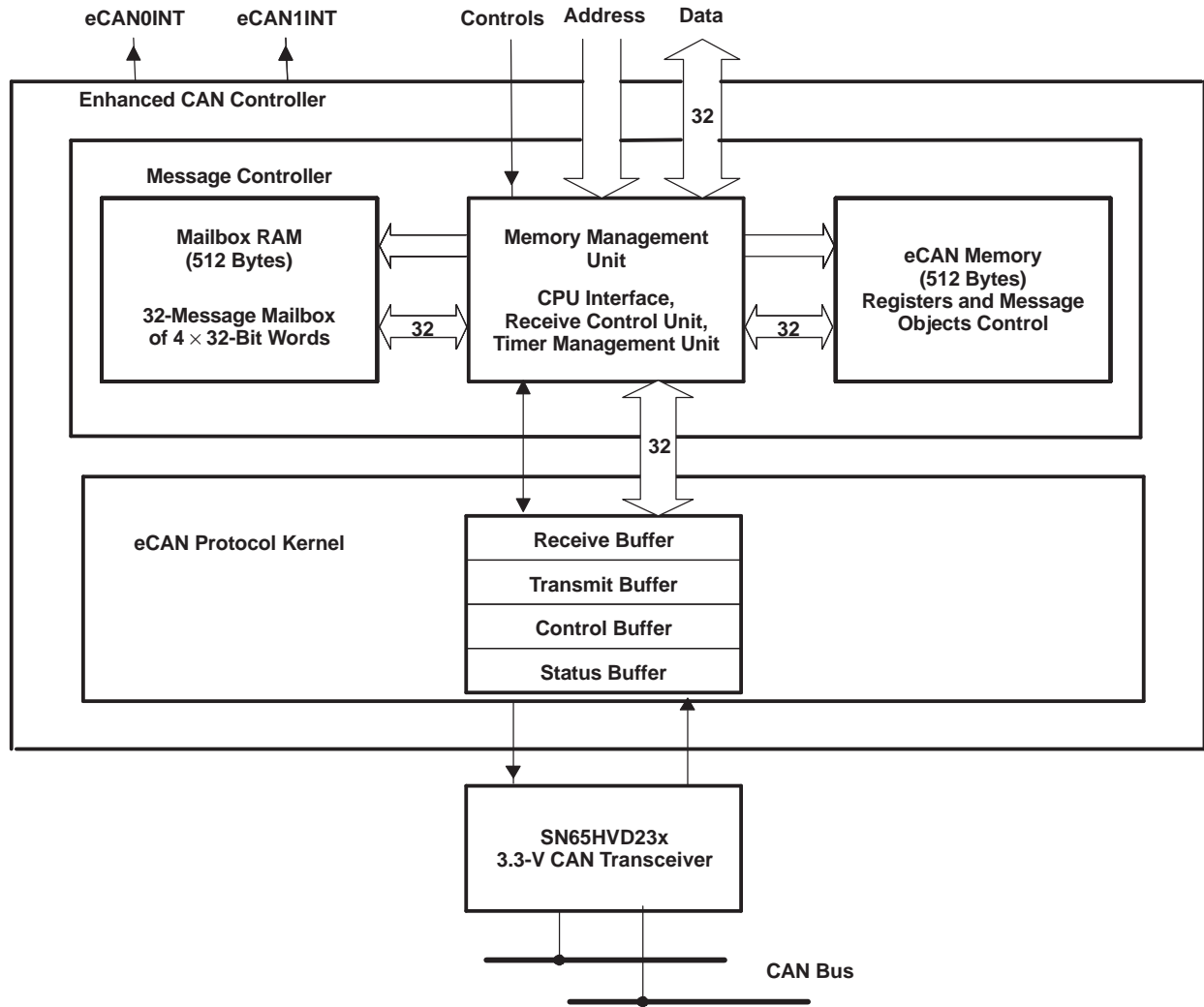
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Figure 4-9. eCAN Block Diagram and Interface Circuit

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Table 4-10. 3.3-V eCAN Transceivers

PART NUMBER	SUPPLY VOLTAGE	LOW-POWER MODE	SLOPE CONTROL	VREF	OTHER	T$_A$
SN65HVD230	3.3 V	Standby	Adjustable	Yes	–	-40°C to 85°C
SN65HVD230Q	3.3 V	Standby	Adjustable	Yes	–	-40°C to 125°C
SN65HVD231	3.3 V	Sleep	Adjustable	Yes	–	-40°C to 85°C
SN65HVD231Q	3.3 V	Sleep	Adjustable	Yes	–	-40°C to 125°C
SN65HVD232	3.3 V	None	None	None	–	-40°C to 85°C
SN65HVD232Q	3.3 V	None	None	None	–	-40°C to 125°C
SN65HVD233	3.3 V	Standby	Adjustable	None	Diagnostic Loopback	-40°C to 125°C
SN65HVD234	3.3 V	Standby and Sleep	Adjustable	None	–	-40°C to 125°C
SN65HVD235	3.3 V	Standby	Adjustable	None	Autobaud Loopback	-40°C to 125°C

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eCAN-A Control and Status Registers

Mailbox Enable – CANME
Mailbox Direction – CANMD
Transmission Request Set – CANTRS
Transmission Request Reset – CANTRR
Transmission Acknowledge – CANTA
Abort Acknowledge – CANAA
Received Message Pending – CANRMP
Received Message Lost – CANRML
Remote Frame Pending – CANRFP
Global Acceptance Mask – CANGAM
Master Control – CANMC
Bit-Timing Configuration – CANBTC
Error and Status – CANES
Transmit Error Counter – CANTEC
Receive Error Counter – CANREC
Global Interrupt Flag 0 – CANGIF0
Global Interrupt Mask – CANGIM
Global Interrupt Flag 1 – CANGIF1
Mailbox Interrupt Mask – CANMIM
Mailbox Interrupt Level – CANMIL
Overwrite Protection Control – CANOPC
TX I/O Control – CANTIOC
RX I/O Control – CANRIOC
Time Stamp Counter – CANTSC
Time-Out Control – CANTOC
Time-Out Status – CANTOS
Reserved

eCAN-A Memory (512 Bytes)

6000h	Control and Status Registers
603Fh	
6040h	Local Acceptance Masks (LAM)
607Fh	(32 × 32-Bit RAM)
6080h	Message Object Time Stamps (MOTS)
60BFh	(32 × 32-Bit RAM)
60C0h	Message Object Time-Out (MOTO)
60FFh	(32 × 32-Bit RAM)

eCAN-A Memory RAM (512 Bytes)

6100h–6107h	Mailbox 0
6108h–610Fh	Mailbox 1
6110h–6117h	Mailbox 2
6118h–611Fh	Mailbox 3
6120h–6127h	Mailbox 4
61E0h–61E7h	Mailbox 28
61E8h–61EFh	Mailbox 29
61F0h–61F7h	Mailbox 30
61F8h–61FFh	Mailbox 31

Message Mailbox (16 Bytes)

61E8h–61E9h	Message Identifier – MSGID
61EAh–61EBh	Message Control – MSGCTRL
61ECh–61EDh	Message Data Low – MDL
61EEh–61EFh	Message Data High – MDH

Figure 4-10. eCAN-A Memory Map

NOTE
If the eCAN module is not used in an application, the RAM available (LAM, MOTS, MOTO, and mailbox RAM) can be used as general-purpose RAM. The CAN module clock should be enabled for this.

The CAN registers listed in Table 4-11 are used by the CPU to configure and control the CAN controller and the message objects. eCAN control registers only support 32-bit read/write operations. Mailbox RAM can be accessed as 16 bits or 32 bits. 32-bit accesses are aligned to an even boundary.

Table 4-11. CAN Register Map[1]

REGISTER NAME	ECAN-A ADDRESS	SIZE (x32)	DESCRIPTION
CANME	0x6000	1	Mailbox enable
CANMD	0x6002	1	Mailbox direction
CANTRS	0x6004	1	Transmit request set
CANTRR	0x6006	1	Transmit request reset
CANTA	0x6008	1	Transmission acknowledge
CANAA	0x600A	1	Abort acknowledge
CANRMP	0x600C	1	Receive message pending
CANRML	0x600E	1	Receive message lost
CANRFP	0x6010	1	Remote frame pending
CANGAM	0x6012	1	Global acceptance mask
CANMC	0x6014	1	Master control
CANBTC	0x6016	1	Bit-timing configuration
CANES	0x6018	1	Error and status
CANTEC	0x601A	1	Transmit error counter
CANREC	0x601C	1	Receive error counter
CANGIF0	0x601E	1	Global interrupt flag 0
CANGIM	0x6020	1	Global interrupt mask
CANGIF1	0x6022	1	Global interrupt flag 1
CANMIM	0x6024	1	Mailbox interrupt mask
CANMIL	0x6026	1	Mailbox interrupt level
CANOPC	0x6028	1	Overwrite protection control
CANTIOC	0x602A	1	TX I/O control
CANRIOC	0x602C	1	RX I/O control
CANTSC	0x602E	1	Time stamp counter (Reserved in SCC mode)
CANTOC	0x6030	1	Time-out control (Reserved in SCC mode)
CANTOS	0x6032	1	Time-out status (Reserved in SCC mode)

(1)   These registers are mapped to Peripheral Frame 1.

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4.7 Inter-Integrated Circuit (I2C)

The device contains one I2C Serial Port. Figure 4-11 shows how the I2C peripheral module interfaces within the device.

The I2C module has the following features:

- Compliance with the Philips Semiconductors I2C-bus specification (version 2.1):
  – Support for 1-bit to 8-bit format transfers
  – 7-bit and 10-bit addressing modes
  – General call
  – START byte mode
  – Support for multiple master-transmitters and slave-receivers
  – Support for multiple slave-transmitters and master-receivers
  – Combined master transmit/receive and receive/transmit mode
  – Data transfer rate of from 10 kbps up to 400 kbps (I2C Fast-mode rate)
- One 4-word receive FIFO and one 4-word transmit FIFO
- One interrupt that can be used by the CPU. This interrupt can be generated as a result of one of the following conditions:
  – Transmit-data ready
  – Receive-data ready
  – Register-access ready
  – No-acknowledgment received
  – Arbitration lost
  – Stop condition detected
  – Addressed as slave
- An additional interrupt that can be used by the CPU when in FIFO mode
- Module enable/disable capability
- Free data format mode

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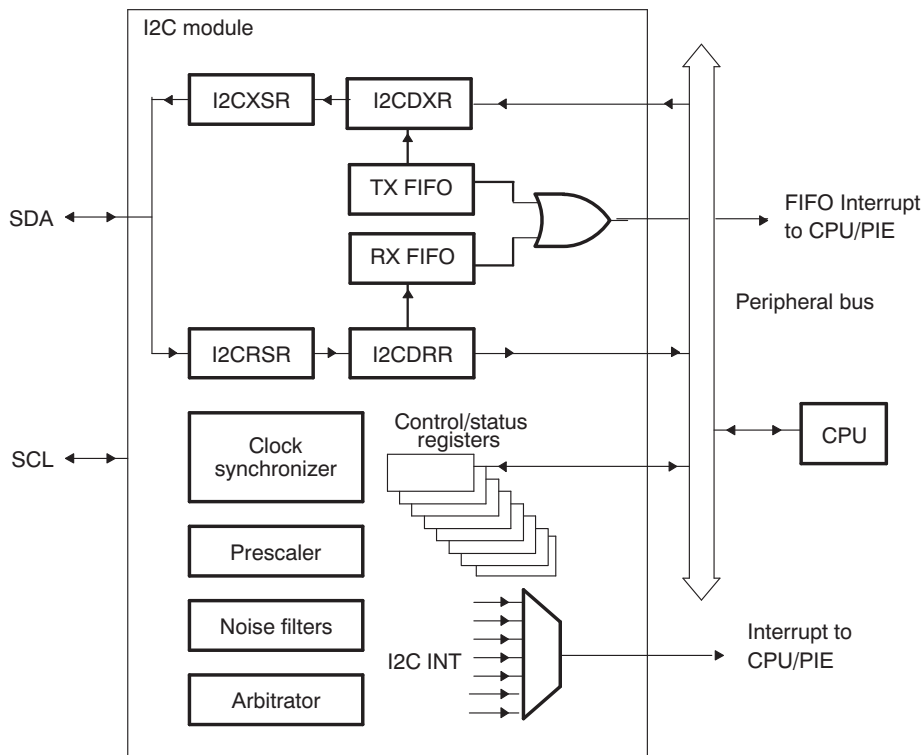
A. The I2C registers are accessed at the SYSCLKOUT rate. The internal timing and signal waveforms of the I2C port are also at the SYSCLKOUT rate.

B. The clock enable bit (I2CAENCLK) in the PCLKCRO register turns off the clock to the I2C port for low power operation. Upon reset, I2CAENCLK is clear, which indicates the peripheral internal clocks are off.

Figure 4-11. I2C Peripheral Module Interfaces

The registers in Table 4-12 configure and control the I2C port operation.

Table 4-12. I2C-A Registers

NAME	ADDRESS	EALLOW PROTECTED	DESCRIPTION
I2COAR	0x7900	No	I2C own address register
I2CIER	0x7901	No	I2C interrupt enable register
I2CSTR	0x7902	No	I2C status register
I2CCLKL	0x7903	No	I2C clock low-time divider register
I2CCLKH	0x7904	No	I2C clock high-time divider register
I2CCNT	0x7905	No	I2C data count register
I2CDRR	0x7906	No	I2C data receive register
I2CSAR	0x7907	No	I2C slave address register
I2CDXR	0x7908	No	I2C data transmit register
I2CMDR	0x7909	No	I2C mode register
I2CISRC	0x790A	No	I2C interrupt source register
I2CPSC	0x790C	No	I2C prescaler register
I2CFFTX	0x7920	No	I2C FIFO transmit register
I2CFFRX	0x7921	No	I2C FIFO receive register
I2CRSR	–	No	I2C receive shift register (not accessible to the CPU)
I2CXSR	–	No	I2C transmit shift register (not accessible to the CPU)

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4.8 Enhanced PWM Modules (ePWM1/2/3/4/5/6/7)

The devices contain up to seven enhanced PWM Modules (ePWM). Figure 4-12 shows a block diagram of multiple ePWM modules. Figure 4-13 shows the signal interconnections with the ePWM. See the *TMS320x2802x, 2803x Piccolo Enhanced Pulse Width Modulator (ePWM) Module Reference Guide* (literature number SPRUGE9) for more details.

Table 4-13 and Table 4-14 show the complete ePWM register set per module.
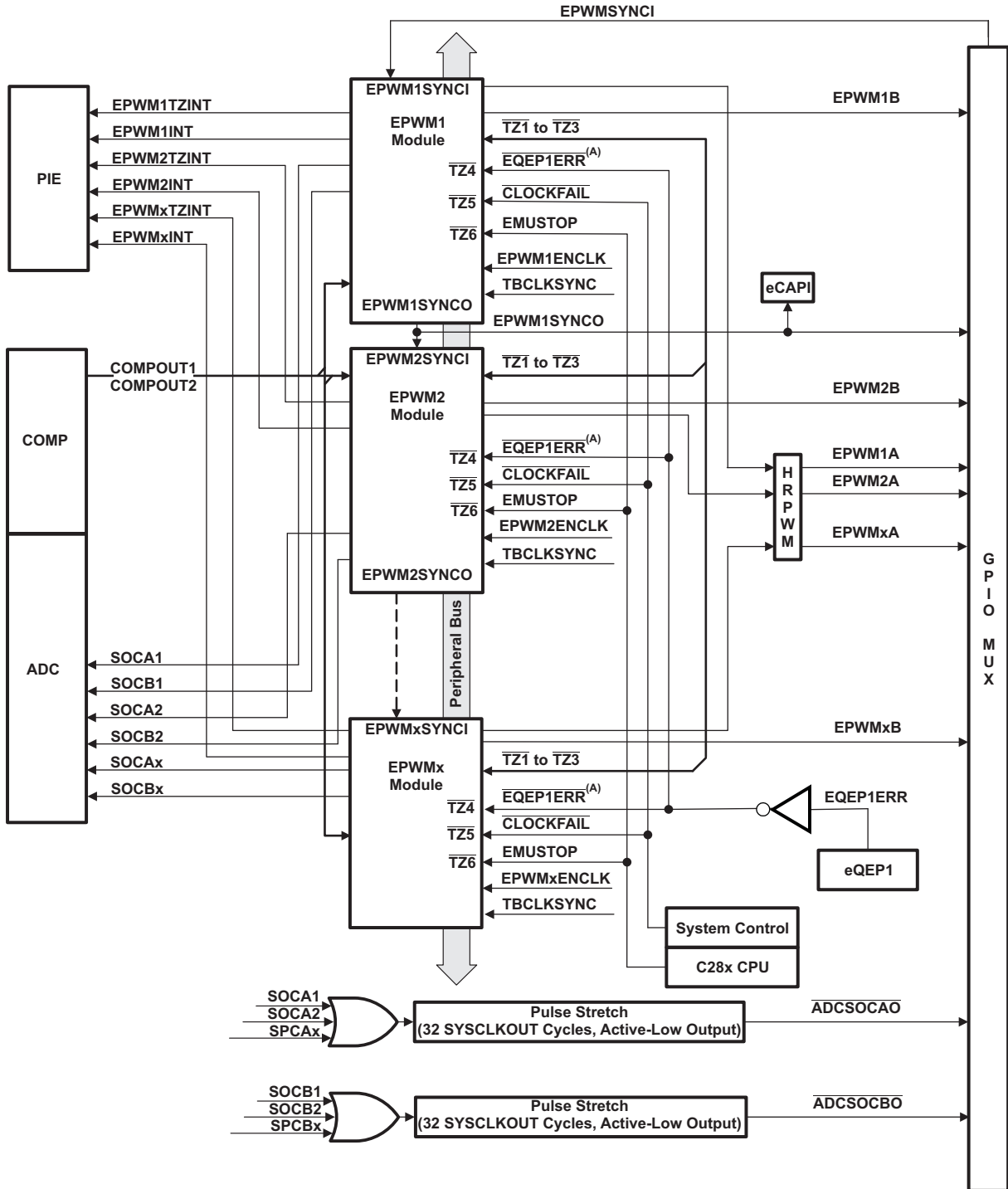
A.   This signal exists only on devices with an eQEP1 module.

Figure 4-12. ePWM

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Table 4-13. ePWM1–ePWM4 Control and Status Registers

NAME	ePWM1	ePWM2	ePWM3	ePWM4	SIZE (x16) / #SHADOW	DESCRIPTION
TBCTL	0x6800	0x6840	0x6880	0x68C0	1 / 0	Time Base Control Register
TBSTS	0x6801	0x6841	0x6881	0x68C1	1 / 0	Time Base Status Register
TBPHSHR	0x6802	0x6842	0x6882	0x68C2	1 / 0	Time Base Phase HRPWM Register
TBPHS	0x6803	0x6843	0x6883	0x68C3	1 / 0	Time Base Phase Register
TBCTR	0x6804	0x6844	0x6884	0x68C4	1 / 0	Time Base Counter Register
TBPRD	0x6805	0x6845	0x6885	0x68C5	1 / 1	Time Base Period Register Set
TBPRDHR	0x6806	0x6846	0x6886	0x68C6	1 / 1	Time Base Period High Resolution Register[1]
CMPCTL	0x6807	0x6847	0x6887	0x68C7	1 / 0	Counter Compare Control Register
CMPAHR	0x6808	0x6848	0x6888	0x68C8	1 / 1	Time Base Compare A HRPWM Register
CMPA	0x6809	0x6849	0x6889	0x68C9	1 / 1	Counter Compare A Register Set
CMPB	0x680A	0x684A	0x688A	0x68CA	1 / 1	Counter Compare B Register Set
AQCTLA	0x680B	0x684B	0x688B	0x68CB	1 / 0	Action Qualifier Control Register For Output A
AQCTLB	0x680C	0x684C	0x688C	0x68CC	1 / 0	Action Qualifier Control Register For Output B
AQSFRC	0x680D	0x684D	0x688D	0x68CD	1 / 0	Action Qualifier Software Force Register
AQCSFRC	0x680E	0x684E	0x688E	0x68CE	1 / 1	Action Qualifier Continuous S/W Force Register Set
DBCTL	0x680F	0x684F	0x688F	0x68CF	1 / 1	Dead-Band Generator Control Register
DBRED	0x6810	0x6850	0x6890	0x68D0	1 / 0	Dead-Band Generator Rising Edge Delay Count Register
DBFED	0x6811	0x6851	0x6891	0x68D1	1 / 0	Dead-Band Generator Falling Edge Delay Count Register
TZSEL	0x6812	0x6852	0x6892	0x68D2	1 / 0	Trip Zone Select Register[1]
TZDCSEL	0x6813	0x6853	0x6893	0x98D3	1 / 0	Trip Zone Digital Compare Register
TZCTL	0x6814	0x6854	0x6894	0x68D4	1 / 0	Trip Zone Control Register[1]
TZEINT	0x6815	0x6855	0x6895	0x68D5	1 / 0	Trip Zone Enable Interrupt Register[1]
TZFLG	0x6816	0x6856	0x6896	0x68D6	1 / 0	Trip Zone Flag Register [1]
TZCLR	0x6817	0x6857	0x6897	0x68D7	1 / 0	Trip Zone Clear Register[1]
TZFRC	0x6818	0x6858	0x6898	0x68D8	1 / 0	Trip Zone Force Register[1]
ETSEL	0x6819	0x6859	0x6899	0x68D9	1 / 0	Event Trigger Selection Register
ETPS	0x681A	0x685A	0x689A	0x68DA	1 / 0	Event Trigger Prescale Register
ETFLG	0x681B	0x685B	0x689B	0x68DB	1 / 0	Event Trigger Flag Register
ETCLR	0x681C	0x685C	0x689C	0x68DC	1 / 0	Event Trigger Clear Register
ETFRC	0x681D	0x685D	0x689D	0x68DD	1 / 0	Event Trigger Force Register
PCCTL	0x681E	0x685E	0x689E	0x68DE	1 / 0	PWM Chopper Control Register
HRCNFG	0x6820	0x6860	0x68A0	0x68E0	1 / 0	HRPWM Configuration Register[1]

(1)   Registers that are EALLOW protected.

NAME	ePWM1	ePWM2	ePWM3	ePWM4	SIZE (x16) / #SHADOW	DESCRIPTION
HRPWR	0x6821	-	-	-	1 / 0	HRPWM Power Register
HRMSTEP	0x6826	-	-	-	1 / 0	HRPWM MEP Step Register
HRPCTL	0x6828	0x6868	0x68A8	0x68E8	1 / 0	High resolution Period Control Register[1]
TBPRDHRM	0x682A	0x686A	0x68AA	0x68EA	1 / W[2]	Time Base Period HRPWM Register Mirror
TBPRDM	0x682B	0x686B	0x68AB	0x68EB	1 / W[2]	Time Base Period Register Mirror
CMPAHRM	0x682C	0x686C	0x68AC	0x68EC	1 / W[2]	Compare A HRPWM Register Mirror
CMPAM	0x682D	0x686D	0x68AD	0x68ED	1 / W[2]	Compare A Register Mirror
DCTRIPSEL	0x6830	0x6870	0x68B0	0x68F0	1 / 0	Digital Compare Trip Select Register [1]
DCACTL	0x6831	0x6871	0x68B1	0x68F1	1 / 0	Digital Compare A Control Register[1]
DCBCTL	0x6832	0x6872	0x68B2	0x68F2	1 / 0	Digital Compare B Control Register[1]
DCFCTL	0x6833	0x6873	0x68B3	0x68F3	1 / 0	Digital Compare Filter Control Register[1]
DCCAPCT	0x6834	0x6874	0x68B4	0x68F4	1 / 0	Digital Compare Capture Control Register[1]
DCFOFFSET	0x6835	0x6875	0x68B5	0x68F5	1 / 1	Digital Compare Filter Offset Register
DCFOFFSETCNT	0x6836	0x6876	0x68B6	0x68F6	1 / 0	Digital Compare Filter Offset Counter Register
DCFWINDOW	0x6837	0x6877	0x68B7	0x68F7	1 / 0	Digital Compare Filter Window Register
DCFWINDOWCNT	0x6838	0x6878	0x68B8	0x68F8	1 / 0	Digital Compare Filter Window Counter Register
DCCAP	0x6839	0x6879	0x68B9	0x68F9	1 / 1	Digital Compare Counter Capture Register

(2)   W = Write to shadow register

Table 4-14. ePWM5–ePWM7 Control and Status Registers

NAME	ePWM5	ePWM6	ePWM7	SIZE (x16) / #SHADOW	DESCRIPTION
TBCTL	0x6900	0x6940	0x6980	1 / 0	Time Base Control Register
TBSTS	0x6901	0x6941	0x6981	1 / 0	Time Base Status Register
TBPHSHR	0x6902	0x6942	0x6982	1 / 0	Time Base Phase HRPWM Register
TBPHS	0x6903	0x6943	0x6983	1 / 0	Time Base Phase Register
TBCTR	0x6904	0x6944	0x6984	1 / 0	Time Base Counter Register
TBPRD	0x6905	0x6945	0x6985	1 / 1	Time Base Period Register Set
TBPRDHR	0x6906	0x6946	0x6986	1 / 1	Time Base Period High Resolution Register[1]
CMPCTL	0x6907	0x6947	0x6987	1 / 0	Counter Compare Control Register
CMPAHR	0x6908	0x6948	0x6988	1 / 1	Time Base Compare A HRPWM Register
CMPA	0x6909	0x6949	0x6989	1 / 1	Counter Compare A Register Set
CMPB	0x690A	0x694A	0x698A	1 / 1	Counter Compare B Register Set
AQCTLA	0x690B	0x694B	0x698B	1 / 0	Action Qualifier Control Register For Output A
AQCTLB	0x690C	0x694C	0x698C	1 / 0	Action Qualifier Control Register For Output B
AQSFRC	0x690D	0x694D	0x698D	1 / 0	Action Qualifier Software Force Register
AQCSFRC	0x690E	0x694E	0x698E	1 / 1	Action Qualifier Continuous S/W Force Register Set
DBCTL	0x690F	0x694F	0x698F	1 / 1	Dead-Band Generator Control Register
DBRED	0x6910	0x6950	0x6990	1 / 0	Dead-Band Generator Rising Edge Delay Count Register
DBFED	0x6911	0x6951	0x6991	1 / 0	Dead-Band Generator Falling Edge Delay Count Register
TZSEL	0x6912	0x6952	0x6992	1 / 0	Trip Zone Select Register[1]
TZDCSEL	0x6913	0x6953	0x6993	1 / 0	Trip Zone Digital Compare Register
TZCTL	0x6914	0x6954	0x6994	1 / 0	Trip Zone Control Register[1]
TZEINT	0x6915	0x6955	0x6995	1 / 0	Trip Zone Enable Interrupt Register[1]
TZFLG	0x6916	0x6956	0x6996	1 / 0	Trip Zone Flag Register [1]
TZCLR	0x6917	0x6957	0x6997	1 / 0	Trip Zone Clear Register[1]
TZFRC	0x6918	0x6958	0x6998	1 / 0	Trip Zone Force Register[1]
ETSEL	0x6919	0x6959	0x6999	1 / 0	Event Trigger Selection Register
ETPS	0x691A	0x695A	0x699A	1 / 0	Event Trigger Prescale Register
ETFLG	0x691B	0x695B	0x699B	1 / 0	Event Trigger Flag Register
ETCLR	0x691C	0x695C	0x699C	1 / 0	Event Trigger Clear Register
ETFRC	0x691D	0x695D	0x699D	1 / 0	Event Trigger Force Register
PCCTL	0x691E	0x695E	0x699E	1 / 0	PWM Chopper Control Register
HRCNFG	0x6920	0x6960	0x69A0	1 / 0	HRPWM Configuration Register[1]

(1)   Registers that are EALLOW protected.

NAME	ePWM5	ePWM6	ePWM7	SIZE (x16) / #SHADOW	DESCRIPTION
HRPWR	-	-	-	1 / 0	HRPWM Power Register
HRMSTEP	-	-	-	1 / 0	HRPWM MEP Step Register
HRPCTL	0x6928	0x6968	0x69A8	1 / 0	High resolution Period Control Register[1]
TBPRDHRM	0x692A	0x696A	0x69AA	1 / W[2]	Time Base Period HRPWM Register Mirror
TBPRDM	0x692B	0x696B	0x69AB	1 / W[2]	Time Base Period Register Mirror
CMPAHRM	0x692C	0x696C	0x69AC	1 / W[2]	Compare A HRPWM Register Mirror
CMPAM	0x692D	0x696D	0x69AD	1 / W[2]	Compare A Register Mirror
DCTRIPSEL	0x6930	0x6970	0x69B0	1 / 0	Digital Compare Trip Select Register [1]
DCACTL	0x6931	0x6971	0x69B1	1 / 0	Digital Compare A Control Register[1]
DCBCTL	0x6932	0x6972	0x69B2	1 / 0	Digital Compare B Control Register[1]
DCFCTL	0x6933	0x6973	0x69B3	1 / 0	Digital Compare Filter Control Register[1]
DCCAPCT	0x6934	0x6974	0x69B4	1 / 0	Digital Compare Capture Control Register[1]
DCFOFFSET	0x6935	0x6975	0x69B5	1 / 1	Digital Compare Filter Offset Register
DCFOFFSETCNT	0x6936	0x6976	0x69B6	1 / 0	Digital Compare Filter Offset Counter Register
DCFWINDOW	0x6937	0x6977	0x69B7	1 / 0	Digital Compare Filter Window Register
DCFWINDOWCNT	0x6938	0x6978	0x69B8	1 / 0	Digital Compare Filter Window Counter Register
DCCAP	0x6939	0x6979	0x69B9	1 / 1	Digital Compare Counter Capture Register

(2)   W = Write to shadow register

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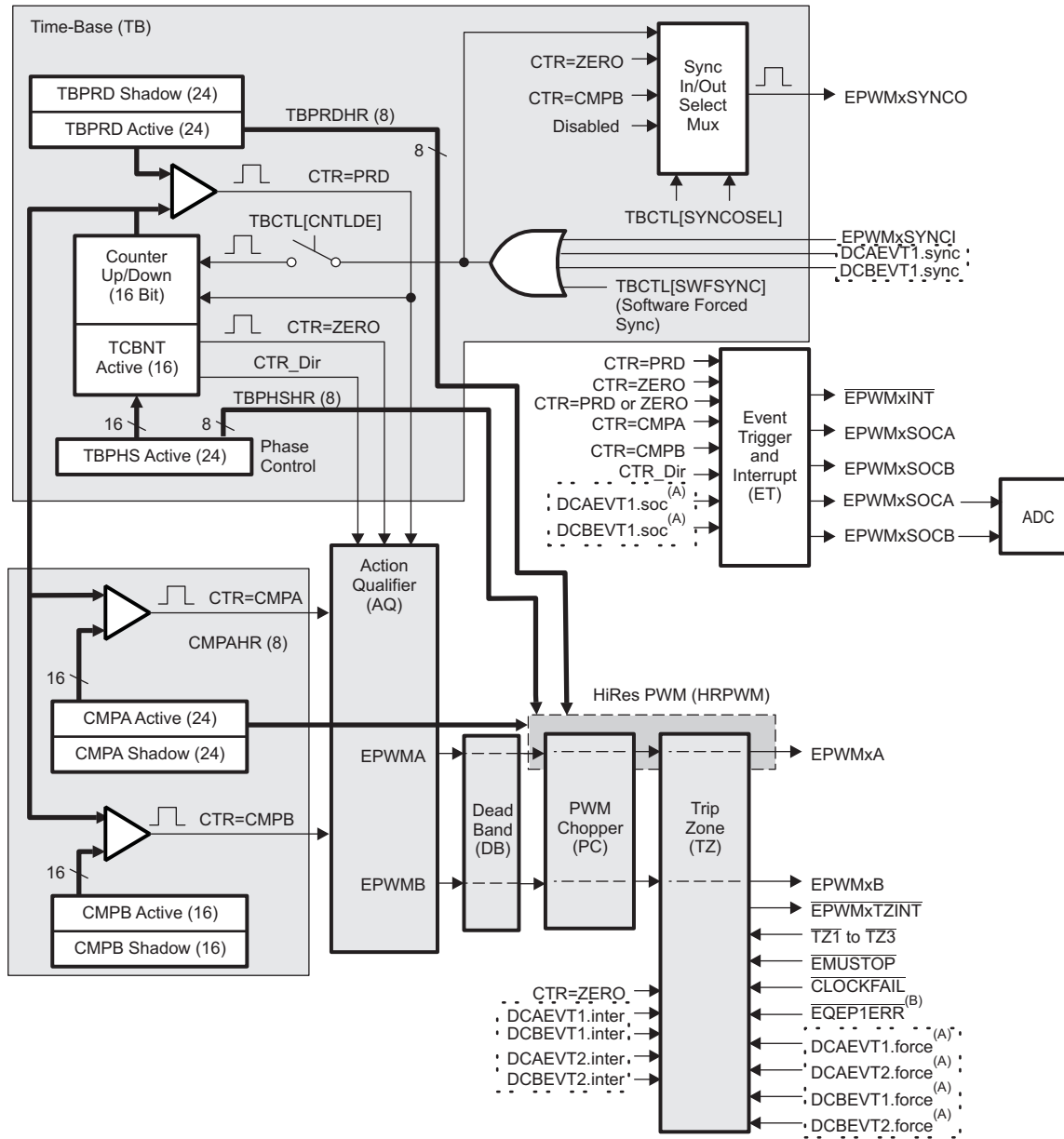
A.   These events are generated by the Type 1 ePWM digital compare (DC) submodule based on the levels of the COMPxOUT and $\overline{TZ}$ signals.

B.   This signal exists only on devices with an eQEP1 module.

Figure 4-13. ePWM Sub-Modules Showing Critical Internal Signal Interconnections

4.9 High-Resolution PWM (HRPWM)

This module combines multiple delay lines in a single module and a simplified calibration system by using a dedicated calibration delay line. For each ePWM module there is one HR delay line.

The HRPWM module offers PWM resolution (time granularity) that is significantly better than what can be achieved using conventionally derived digital PWM methods. The key points for the HRPWM module are:

- Significantly extends the time resolution capabilities of conventionally derived digital PWM
- This capability can be utilized in both single edge (duty cycle and phase-shift control) as well as dual edge control for frequency/period modulation.
- Finer time granularity control or edge positioning is controlled via extensions to the Compare A and Phase registers of the ePWM module.
- HRPWM capabilities, when available on a particular device, are offered only on the A signal path of an ePWM module (i.e., on the EPWMxA output). EPWMxB output has conventional PWM capabilities.

NOTE

At SYSCLKOUT frequencies below 50 MHz and under worst-case process, voltage, and temperature (maximum voltage and minimum temperature) conditions, the MEP step delay may decrease to a point such that the maximum of 254 MEP steps may not cover 1 full SYSCLKOUT cycle. In other words, high-resolution edge control will not be available for the full range of a SYSCLKOUT cycle. If running SFO calibration software, the SFO function will return an error code of "2" when this occurs. See the *TMS320x2802x, 2803x Piccolo High-Resolution Pulse Width Modulator (HRPWM) Reference Guide* (literature number SPRUGE8) for more information on this error condition.

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4.10 Enhanced Capture Module (eCAP1)

The device contains an enhanced capture (eCAP) module. Figure 4-14 shows a functional block diagram of a module.

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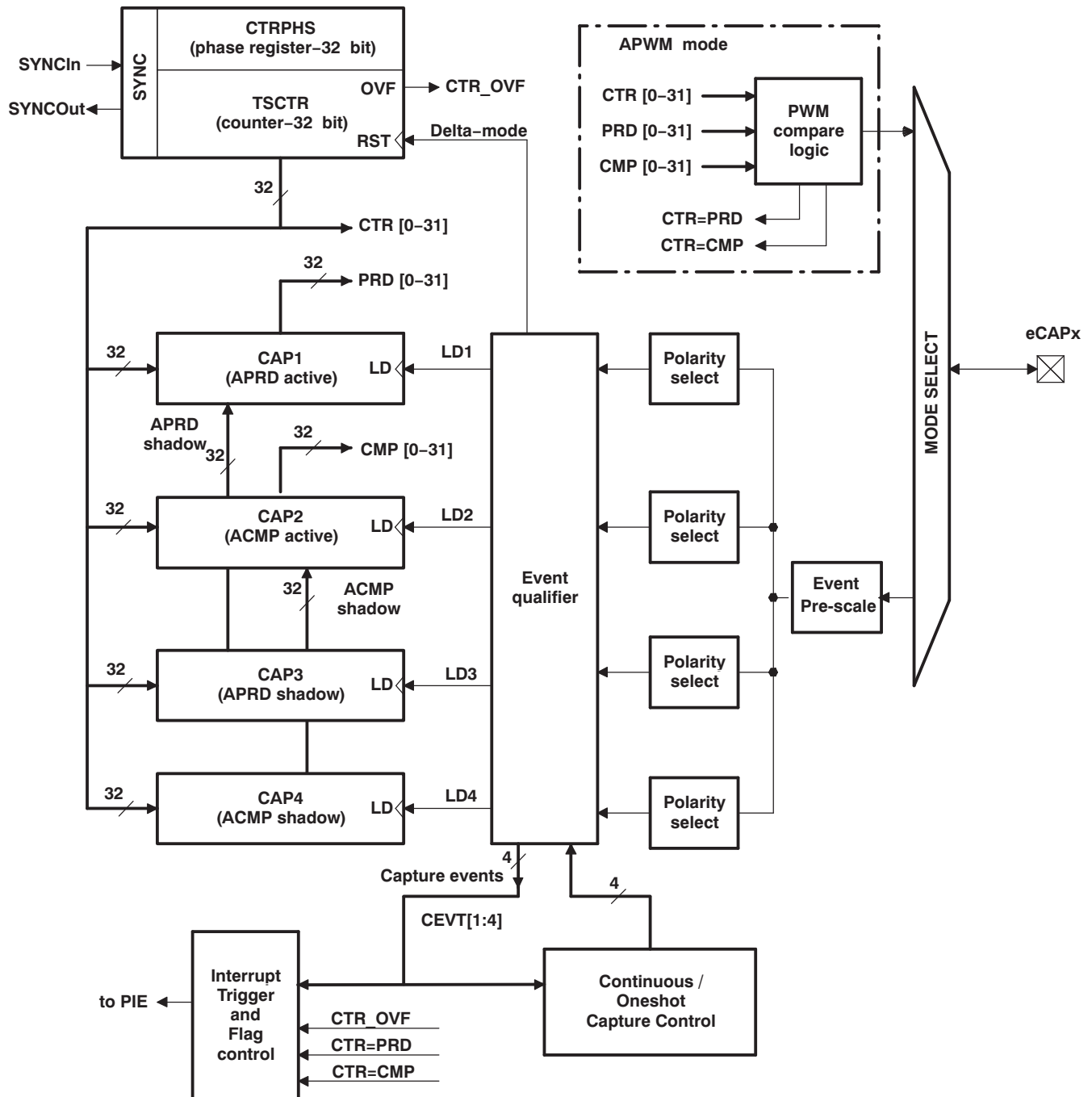
Figure 4-14. eCAP Functional Block Diagram

The eCAP module is clocked at the SYSCLKOUT rate.

The clock enable bits (ECAP1 ENCLK) in the PCLKCR1 register turn off the eCAP module individually (for low power operation). Upon reset, ECAP1ENCLK is set to low, indicating that the peripheral clock is off.

Table 4-15. eCAP Control and Status Registers

NAME	eCAP1	SIZE (x16)	EALLOW PROTECTED	DESCRIPTION
TSCTR	0x6A00	2		Time-Stamp Counter
CTRPHS	0x6A02	2		Counter Phase Offset Value Register
CAP1	0x6A04	2		Capture 1 Register
CAP2	0x6A06	2		Capture 2 Register
CAP3	0x6A08	2		Capture 3 Register
CAP4	0x6A0A	2		Capture 4 Register
Reserved	0x6A0C- 0x6A12	8		Reserved
ECCTL1	0x6A14	1		Capture Control Register 1
ECCTL2	0x6A15	1		Capture Control Register 2
ECEINT	0x6A16	1		Capture Interrupt Enable Register
ECFLG	0x6A17	1		Capture Interrupt Flag Register
ECCLR	0x6A18	1		Capture Interrupt Clear Register
ECFRC	0x6A19	1		Capture Interrupt Force Register
Reserved	0x6A1A- 0x6A1F	6		Reserved

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4.11 Enhanced Quadrature Encoder Pulse (eQEP)

The device contains one enhanced quadrature encoder pulse (eQEP) module.

Table 4-16. eQEP Control and Status Registers

NAME	eQEP1 ADDRESS	eQEP1 SIZE(x16)/ #SHADOW	REGISTER DESCRIPTION
QPOSCNT	0x6B00	2/0	eQEP Position Counter
QPOSINIT	0x6B02	2/0	eQEP Initialization Position Count
QPOSMAX	0x6B04	2/0	eQEP Maximum Position Count
QPOSCMP	0x6B06	2/1	eQEP Position-compare
QPOSILAT	0x6B08	2/0	eQEP Index Position Latch
QPOSSLAT	0x6B0A	2/0	eQEP Strobe Position Latch
QPOSLAT	0x6B0C	2/0	eQEP Position Latch
QUTMR	0x6B0E	2/0	eQEP Unit Timer
QUPRD	0x6B10	2/0	eQEP Unit Period Register
QWDTMR	0x6B12	1/0	eQEP Watchdog Timer
QWDPRD	0x6B13	1/0	eQEP Watchdog Period Register
QDECCTL	0x6B14	1/0	eQEP Decoder Control Register
QEPCTL	0x6B15	1/0	eQEP Control Register
QCAPCTL	0x6B16	1/0	eQEP Capture Control Register
QPOSCTL	0x6B17	1/0	eQEP Position-compare Control Register
QEINT	0x6B18	1/0	eQEP Interrupt Enable Register
QFLG	0x6B19	1/0	eQEP Interrupt Flag Register
QCLR	0x6B1A	1/0	eQEP Interrupt Clear Register
QFRC	0x6B1B	1/0	eQEP Interrupt Force Register
QEPSTS	0x6B1C	1/0	eQEP Status Register
QCTMR	0x6B1D	1/0	eQEP Capture Timer
QCPRD	0x6B1E	1/0	eQEP Capture Period Register
QCTMRLAT	0x6B1F	1/0	eQEP Capture Timer Latch
QCPRDLAT	0x6B20	1/0	eQEP Capture Period Latch
Reserved	0x6B21-0x6B3F	31/0	

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Figure 4-15 shows the eQEP functional block diagram.
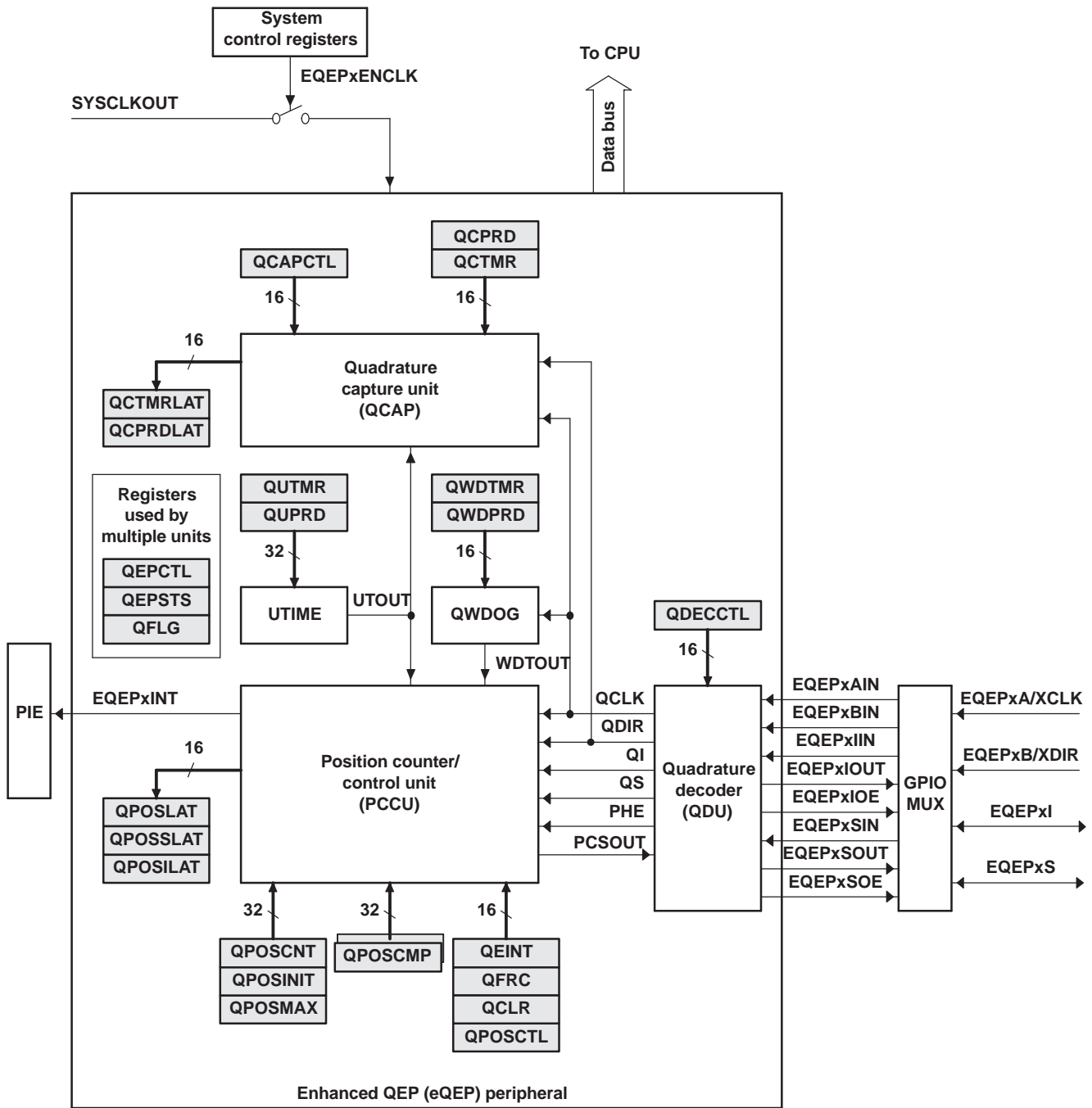
Figure 4-15. eQEP Functional Block Diagram

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4.12 JTAG Port

On the 2803x device, the JTAG port is reduced to 5 pins ($\overline{\text{TRST}}$, TCK, TDI, TMS, TDO). TCK, TDI, TMS and TDO pins are also GPIO pins. The $\overline{\text{TRST}}$ signal selects either JTAG or GPIO operating mode for the pins in Figure 4-16. During emulation/debug, the GPIO function of these pins are not available. If the GPIO38/TCK/XCLKIN pin is used to provide an external clock, an alternate clock source should be used to clock the device during emulation/debug since this pin will be needed for the TCK function.

NOTE

In 2803x devices, the JTAG pins may also be used as GPIO pins. Care should be taken in the board design to ensure that the circuitry connected to these pins do not affect the emulation capabilities of the JTAG pin function. Any circuitry connected to these pins should not prevent the emulator from driving (or being driven by) the JTAG pins for successful debug.
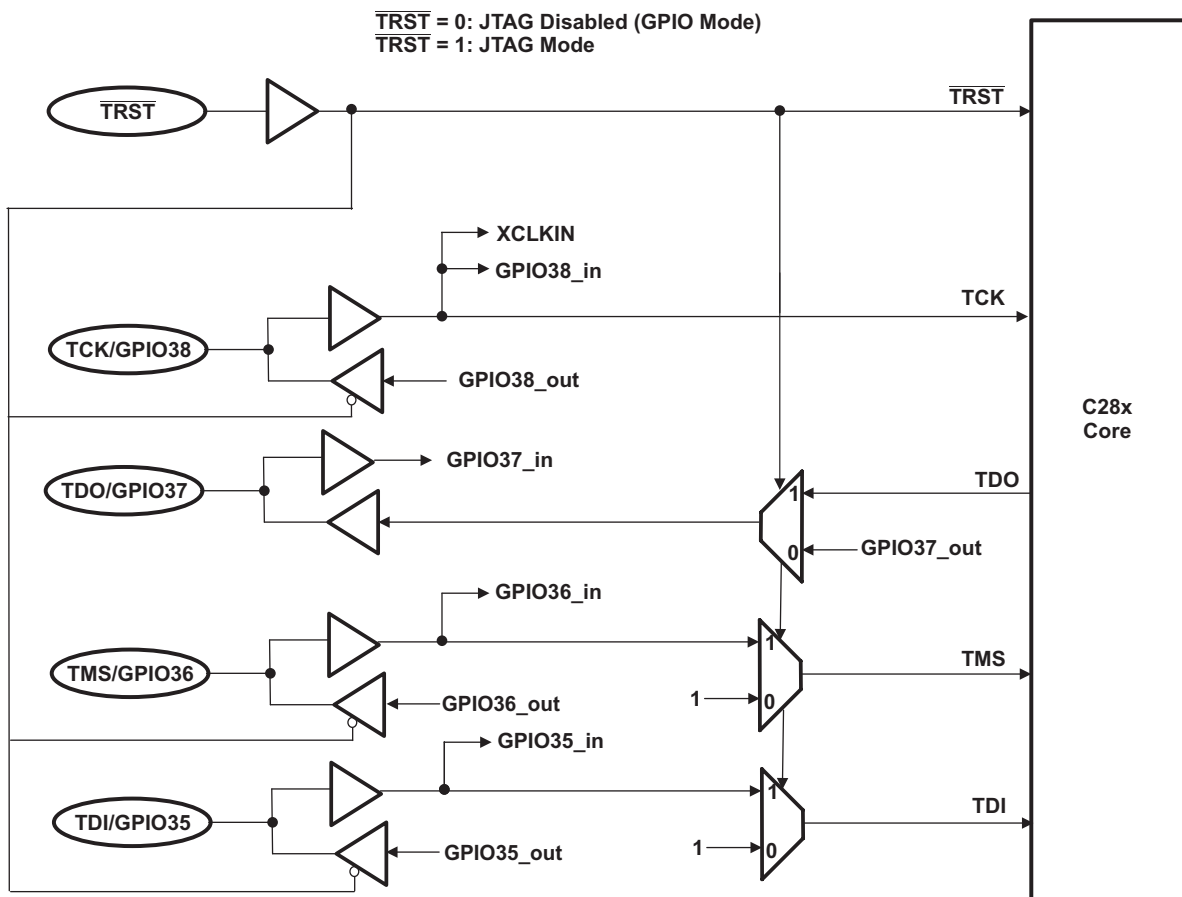
Figure 4-16. JTAG/GPIO Multiplexing

4.13 GPIO MUX

The GPIO MUX can multiplex up to three independent peripheral signals on a single GPIO pin in addition to providing individual pin bit-banging I/O capability.

The device supports 22 GPIO pins. The GPIO control and data registers are mapped to Peripheral Frame 1 to enable 32-bit operations on the registers (along with 16-bit operations). Table 4-17 shows the GPIO register mapping.

Table 4-17. GPIO Registers

NAME	ADDRESS	SIZE (x16)	DESCRIPTION
GPIO CONTROL REGISTERS (EALLOW PROTECTED)			
GPACTRL	0x6F80	2	GPIO A Control Register (GPIO0 to 31)
GPAQSEL1	0x6F82	2	GPIO A Qualifier Select 1 Register (GPIO0 to 15)
GPAQSEL2	0x6F84	2	GPIO A Qualifier Select 2 Register (GPIO16-31)
GPAMUX1	0x6F86	2	GPIO A MUX 1 Register (GPIO0 to 15)
GPAMUX2	0x6F88	2	GPIO A MUX 2 Register (GPIO16 to 31)
GPADIR	0x6F8A	2	GPIO A Direction Register (GPIO0 to 31)
GPAPUD	0x6F8C	2	GPIO A Pull Up Disable Register (GPIO0 to 31)
GPBCTRL	0x6F90	2	GPIO B Control Register (GPIO32 to 44)
GPBQSEL1	0x6F92	2	GPIO B Qualifier Select 1 Register (GPIO32 to 44)
GPBMUX1	0x6F96	2	GPIO B MUX 1 Register (GPIO32 to 44)
GPBDIR	0x6F9A	2	GPIO B Direction Register (GPIO32 to 44)
GPBPUD	0x6F9C	2	GPIO B Pull Up Disable Register (GPIO32 to 44)
AIOMUX1	0x6FB6	2	Analog, I/O mux 1 register (AIO0 - AIO15)
AIODIR	0x6FBA	2	Analog, I/O Direction Register (AIO0-AIO15)
GPIO DATA REGISTERS (NOT EALLOW PROTECTED)			
GPADAT	0x6FC0	2	GPIO A Data Register (GPIO0 to 31)
GPASET	0x6FC2	2	GPIO A Data Set Register (GPIO0 to 31)
GPACLEAR	0x6FC4	2	GPIO A Data Clear Register (GPIO0 to 31)
GPATOGGLE	0x6FC6	2	GPIO A Data Toggle Register (GPIO0 to 31)
GPBDAT	0x6FC8	2	GPIO B Data Register (GPIO32 to 44)
GPBSET	0x6FCA	2	GPIO B Data Set Register (GPIO32 to 44)
GPBCLEAR	0x6FCC	2	GPIO B Data Clear Register (GPIO32 to 44)
GPBTOGGLE	0x6FCE	2	GPIO B Data Toggle Register (GPIO32 to 44)
AIODAT	0x6FD8	2	Analog I/O Data Register (AIO0 - AIO15)
AIOSET	0x6FDA	2	Analog I/O Data Set Register (AIO0 - AIO15)
AIOCLEAR	0x6FDC	2	Analog I/O Data Clear Register (AIO0 - AIO15)
AIOTOGGLE	0x6FDE	2	Analog I/O Data Toggle Register (AIO0 - AIO15)
GPIO INTERRUPT AND LOW POWER MODES SELECT REGISTERS (EALLOW PROTECTED)			
GPIOXINT1SEL	0x6FE0	1	XINT1 GPIO Input Select Register (GPIO0 to 31)
GPIOXINT2SEL	0x6FE1	1	XINT2 GPIO Input Select Register (GPIO0 to 31)
GPIOXINT3SEL	0x6FE2	1	XINT3 GPIO Input Select Register (GPIO0 to 31)
GPIOLPMSEL	0x6FE8	2	LPM GPIO Select Register (GPIO0 to 31)

NOTE

There is a two-SYSCLKOUT cycle delay from when the write to the GPxMUXn/AIOMUXn and GPxQSELn registers occurs to when the action is valid.

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Table 4-18. GPIOA MUX[1]

GPAMUX1 REGISTER BITS	DEFAULT AT RESET PRIMARY I/O FUNCTION	PERIPHERAL SELECTION 1	PERIPHERAL SELECTION 2	PERIPHERAL SELECTION 3
	(GPAMUX1 BITS = 00)	(GPAMUX1 BITS = 01)	(GPAMUX1 BITS = 10)	(GPAMUX1 bits = 11)
1-0	GPIO0	EPWM1A (O)	Reserved	Reserved
3-2	GPIO1	EPWM1B (O)	Reserved	COMP1OUT (O)
5-4	GPIO2	EPWM2A (O)	Reserved	Reserved
7-6	GPIO3	EPWM2B (O)	SPISOMIA (I/O)	COMP2OUT (O)
9-8	GPIO4	EPWM3A (O)	Reserved	Reserved
11-10	GPIO5	EPWM3B (O)	SPISIMOA (I/O)	ECAP1 (I/O)
13-12	GPIO6	EPWM4A (O)	EPWMSYNCI (I)	EPWMSYNCO (O)
15-14	GPIO7	EPWM4B (O)	SCIRXDA (I)	Reserved
17-16	GPIO8	EPWM5A (O)	Reserved	$\overline{ADCSOCAO}$ (O)
19-18	GPIO9	EPWM5B (O)	LINTXA (O)	Reserved
21-20	GPIO10	EPWM6A (O)	Reserved	$\overline{ADCSOCBO}$ (O)
23-22	GPIO11	EPWM6B (O)	LINRXA (I)	Reserved
25-24	GPIO12	$\overline{TZ1}$ (I)	SCITXDA (O)	SPISIMOB (I/O)
27-26	GPIO13[2]	$\overline{TZ2}$ (I)	Reserved	SPISOMIB (I/O)
29-28	GPIO14[2]	$\overline{TZ3}$ (I)	LINTXA (O)	SPICLKB (I/O)
31-30	GPIO15[2]	$\overline{TZ1}$ (I)	LINRXA (I)	$\overline{SPISTEB}$ (I/O)
GPAMUX2 REGISTER BITS	**(GPAMUX2 BITS = 00)**	**(GPAMUX2 BITS = 01)**	**(GPAMUX2 BITS = 10)**	**(GPAMUX2 BITS = 11)**
1-0	GPIO16	SPISIMOA (I/O)	Reserved	$\overline{TZ2}$ (I)
3-2	GPIO17	SPISOMIA (I/O)	Reserved	$\overline{TZ3}$ (I)
5-4	GPIO18	SPICLKA (I/O)	LINTXA (O)	XCLKOUT (O)
7-6	GPIO19/XCLKIN	$\overline{SPISTEA}$ (I/O)	LINRXA (I)	ECAP1 (I/O)
9-8	GPIO20	EQEP1A (I)	Reserved	COMP1OUT (O)
11-10	GPIO21	EQEP1B (I)	Reserved	COMP2OUT (O)
13-12	GPIO22	EQEP1S (I/O)	Reserved	LINTXA (O)
15-14	GPIO23	EQEP1I (I/O)	Reserved	LINRXA (I)
17-16	GPIO24	ECAP1 (I/O)	Reserved	SPISIMOB (I/O)
19-18	GPIO25[2]	Reserved	Reserved	SPISOMIB (I/O)
21-20	GPIO26[2]	Reserved	Reserved	SPICLKB (I/O)
23-22	GPIO27[2]	Reserved	Reserved	$\overline{SPISTEB}$ (I/O)
25-24	GPIO28	SCIRXDA (I)	SDAA (I/OC)	$\overline{TZ2}$ (I)
27-26	GPIO29	SCITXDA (O)	SCLA (I/OC)	$\overline{TZ3}$ (I)
29-28	GPIO30	CANRXA (I)	Reserved	Reserved
31-30	GPIO31	CANTXA (O)	Reserved	Reserved

(1) The word reserved means that there is no peripheral assigned to this GPxMUX1/2 register setting. Should it be selected, the state of the pin will be undefined and the pin may be driven. This selection is a reserved configuration for future expansion.
(2) These pins are not available in the 64-pin package.

Table 4-19. GPIOB MUX

GPBMUX1 REGISTER BITS	DEFAULT AT RESET PRIMARY I/O FUNCTION (GPBMUX1 BITS = 00)	PERIPHERAL SELECTION 1 (GPBMUX1 BITS = 01)	PERIPHERAL SELECTION 2 (GPBMUX1 BITS = 10)	PERIPHERAL SELECTION 3 (GPBMUX1 BITS = 11)
1-0	GPIO32	SDAA (I/OC)	EPWMSYNCI (I)	$\overline{\text{ADCSOCAO}}$ (O)
3-2	GPIO33	SCLA (I/OC)	EPWMSYNCO (O)	$\overline{\text{ADCSOCBO}}$ (O)
5-4	GPIO34	COMP2OUT (O)	Reserved	COMP3OUT (O)
7-6	GPIO35 (TDI)	Reserved	Reserved	Reserved
9-8	GPIO36 (TMS)	Reserved	Reserved	Reserved
11-10	GPIO37 (TDO)	Reserved	Reserved	Reserved
13-12	GPIO38/XCLKIN (TCK)	Reserved	Reserved	Reserved
15-14	GPIO39[1]	Reserved	Reserved	Reserved
17-16	GPIO40[1]	EPWM7A (O)	Reserved	Reserved
19-18	GPIO41[1]	EPWM7B (O)	Reserved	Reserved
21-20	GPIO42[1]	Reserved	Reserved	COMP1OUT (O)
23-22	GPIO43[1]	Reserved	Reserved	COMP2OUT (O)
25-24	GPIO44[1]	Reserved	Reserved	Reserved
27-26	Reserved	Reserved	Reserved	Reserved
29-28	Reserved	Reserved	Reserved	Reserved
31-30	Reserved	Reserved	Reserved	Reserved

(1)   These pins are not available in the 64-pin package.

Table 4-20. Analog MUX

AIOMUX1 REGISTER BITS		DEFAULT AT RESET
	AIOx AND PERIPHERAL SELECTION 1	PERIPHERAL SELECTION 2 AND PERIPHERAL SELECTION 3
	AIOMUX1 BITS = 0,x	AIOMUX1 BITS = 1,x
1-0	ADCINA0 (I)	ADCINA0 (I)
3-2	ADCINA1 (I)	ADCINA1 (I)
5-4	AIO2 (I/O)	ADCINA2 (I), COMP1A (I)
7-6	ADCINA3 (I)	ADCINA3 (I)
9-8	AIO4 (I/O)	ADCINA4 (I), COMP2A (I)
11-10	ADCINA5[1] (I)	ADCINA5 (I)
13-12	AIO6 (I/O)	ADCINA6 (I)
15-14	ADCINA7 (I)	ADCINA7 (I)
17-16	ADCINB0 (I)	ADCINB0 (I)
19-18	ADCINB1 (I)	ADCINB1 (I)
21-20	AIO10 (I/O)	ADCINB2 (I), COMP1B (I)
23-22	ADCINB3 (I)	ADCINB3 (I)
25-24	AIO12 (I/O)	ADCINB4 (I), COMP2B (I)
27-26	ADCINB5[1] (I)	ADCINB5 (I)
29-28	AIO14 (I/O)	ADCINB6 (I)
31-30	ADCINB7 (I)	ADCINB7 (I)

(1)   These pins are not available in the 64-pin package.

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The user can select the type of input qualification for each GPIO pin via the GPxQSEL1/2 registers from four choices:

- Synchronization To SYSCLKOUT Only (GPxQSEL1/2=0, 0): This is the default mode of all GPIO pins at reset and it simply synchronizes the input signal to the system clock (SYSCLKOUT).

- Qualification Using Sampling Window (GPxQSEL1/2=0, 1 and 1, 0): In this mode the input signal, after synchronization to the system clock (SYSCLKOUT), is qualified by a specified number of cycles before the input is allowed to change.

- The sampling period is specified by the QUALPRD bits in the GPxCTRL register and is configurable in groups of 8 signals. It specifies a multiple of SYSCLKOUT cycles for sampling the input signal. The sampling window is either 3-samples or 6-samples wide and the output is only changed when ALL samples are the same (all 0s or all 1s) as shown in Figure 4-18 (for 6 sample mode).

- No Synchronization (GPxQSEL1/2=1,1): This mode is used for peripherals where synchronization is not required (synchronization is performed within the peripheral).

Due to the multi-level multiplexing that is required on the device, there may be cases where a peripheral input signal can be mapped to more then one GPIO pin. Also, when an input signal is not selected, the input signal will default to either a 0 or 1 state, depending on the peripheral.
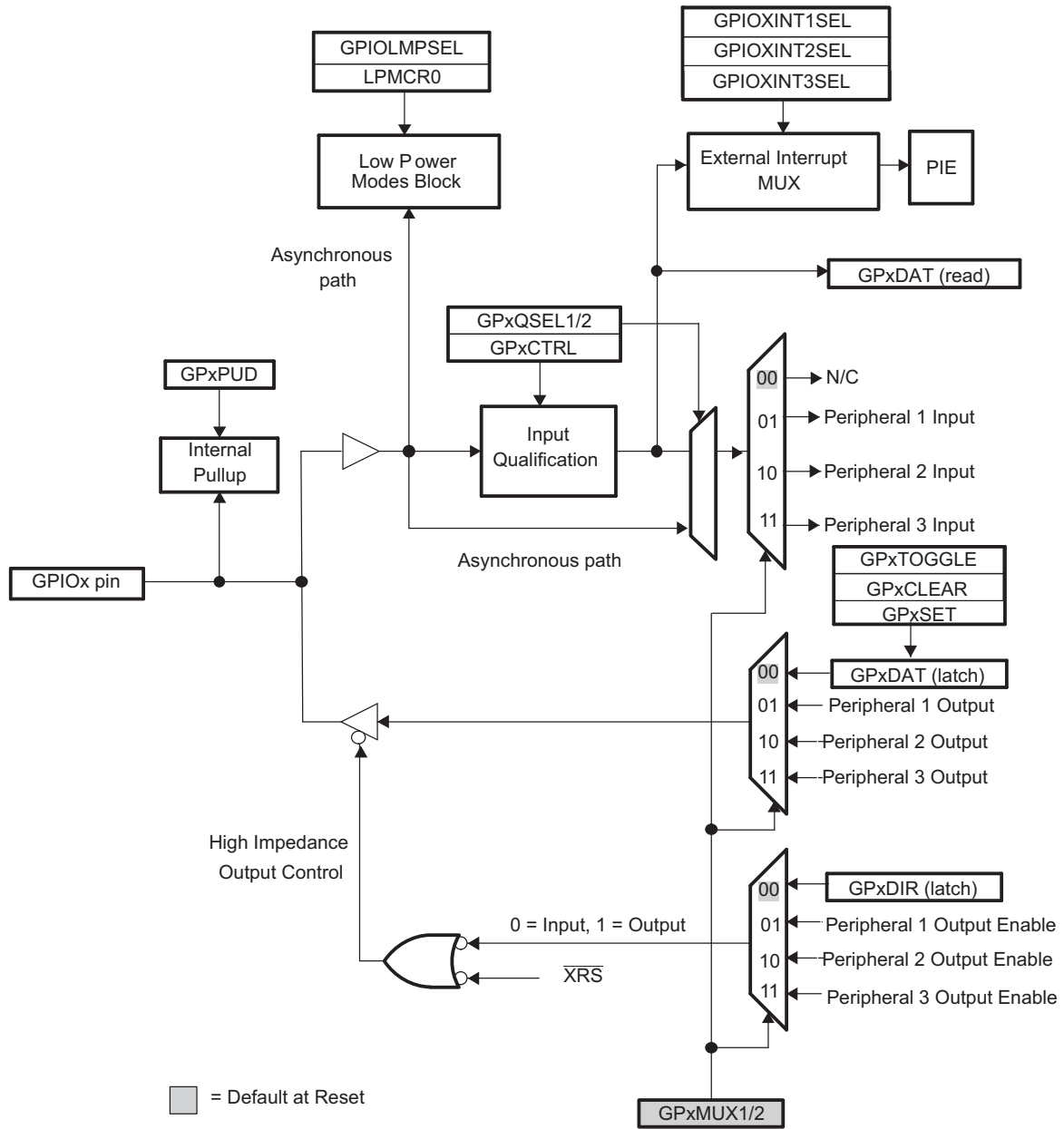
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Figure 4-17. GPIO Multiplexing

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5 Device Support

Texas Instruments (TI) offers an extensive line of development tools for the C28x™ generation of MCUs, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules.

The following products support development of 2803x-based applications:

Software Development Tools

- Code Composer Studio™ Integrated Development Environment (IDE)
  – C/C++ Compiler
  – Code generation tools
  – Assembler/Linker
  – Cycle Accurate Simulator
- Application algorithms
- Sample applications code

Hardware Development Tools

- Development and evaluation boards
- JTAG-based emulators - XDS510™ Class, XDS100
- Flash programming tools
- Power supply
- Documentation and cables

5.1 Device and Development Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all TMS320™ MCU devices and support tools. Each TMS320™ MCU commercial family member has one of three prefixes: TMX, TMP, or TMS (e.g., **TMX**320F28032). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX/TMDX) through fully qualified production devices/tools (TMS/TMDS).

Device development evolutionary flow:

TMX Experimental device that is not necessarily representative of the final device's electrical specifications

TMP Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification

TMS Fully qualified production device

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing

TMDS Fully qualified development-support product

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:
"Developmental product is intended for internal evaluation purposes."

TMS devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, PN) and temperature range (for example, T). Figure 5-1 provides a legend for reading the complete device name for any family member.

```
                    TMS  320   F  28032    PN    T

PREFIX                                            TEMPERATURE RANGE
 TMX = experimental device                         T = −40°C to 105°C
 TMP = prototype device                            S = −40°C to 125°C
 TMS = qualified device

                                            PACKAGE TYPE
DEVICE FAMILY                                80-Pin PN Plastic Quad Flatpack
 320 = TMS320 MCU Family                     64-Pin PAG Plastic Small-outline Package

                                      DEVICE
TECHNOLOGY                             28035
 F = Flash                             28034
                                       28033
                                       28032
```
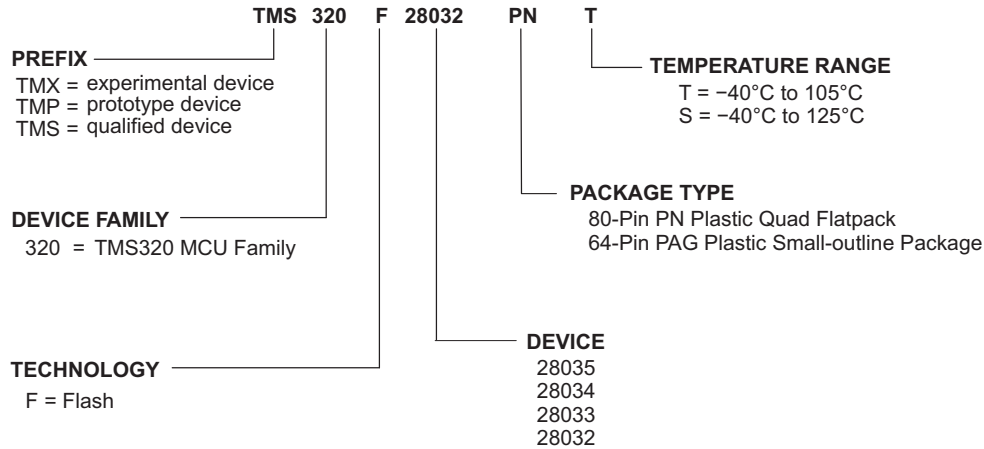
Figure 5-1. Device Nomenclature

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5.2 Related Documentation

Extensive documentation supports all of the TMS320™ MCU family generations of devices from product announcement through applications development. The types of documentation available include: data sheets and data manuals, with design specifications; and hardware and software applications.

Table 5-1 shows the peripheral reference guides appropriate for use with the devices in this data manual. See the *TMS320x28xx, 28xxx DSP Peripheral Reference Guide* (literature number SPRU566) for more information on types of peripherals.

Table 5-1. TMS320F2803x Peripheral Selection Guide

PERIPHERAL	LIT. NO.	TYPE[1]	28032, 28033, 28034, 28035
TMS320x2803x Piccolo System Control and Interrupts	SPRUGL8	–	X
TMS320x2802x, 2803x Piccolo Analog-to-Digital Converter (ADC) and Comparator	SPRUGE5	3/0[2]	X
TMS320x2802x, 2803x Piccolo Serial Communications Interface (SCI)	SPRUGH1	0	X
TMS320x2802x, 2803x Piccolo Serial Peripheral Interface (SPI)	SPRUG71	1	X
TMS320x2803x Piccolo Boot ROM	SPRUGO0	–	X
TMS320x2802x, 2803x Piccolo Enhanced Pulse Width Modulator (ePWM) Module	SPRUGE9	1	X
TMS320x2802x, 2803x Piccolo Enhanced Capture (eCAP) Module	SPRUFZ8	0	X
TMS320x2802x, 2803x Piccolo Inter-Integrated Circuit (I2C)	SPRUFZ9	0	X
TMS320x2802x, 2803x Piccolo High-Resolution Pulse-Width Modulator (HRPWM)	SPRUGE8	1	X
TMS320x2803x Piccolo Control Law Accelerator (CLA)	SPRUGE6	0	X
TMS320x2803x Piccolo Local Interconnect Network (LIN) Module	SPRUGE2	0	X
TMS320x2803x Piccolo Enhanced Quadrature Encoder Pulse (eQEP)	SPRUFK8	0	X
TMS320x2803x Piccolo Enhanced Controller Area Network (eCAN)	SPRUGL7	0	X

(1) A type change represents a major functional feature difference in a peripheral module. Within a peripheral type, there may be minor differences between devices that do not affect the basic functionality of the module. These device-specific differences are listed in the peripheral reference guides.
(2) The ADC module is Type 3 and the comparator module is Type 0.

The following documents can be downloaded from the TI website (www.ti.com):

Data Manual

SPRS584 **TMS320F28032, TMS320F28033, TMS320F28034, TMS320F28035 Piccolo Microcontrollers Data Manual** contains the pinout, signal descriptions, as well as electrical and timing specifications for the 2803x devices.

SPRZ295 **TMS320F28032, TMS320F28033, TMS320F28034, TMS320F28035 Piccolo MCU Silicon Errata** describes known advisories on silicon and provides workarounds.

CPU User's Guides

SPRU430 **TMS320C28x CPU and Instruction Set Reference Guide** describes the central processing unit (CPU) and the assembly language instructions of the TMS320C28x fixed-point digital signal processors (DSPs). It also describes emulation features available on these DSPs.

Peripheral Guides

SPRUGL8 **TMS320x2803x Piccolo System Control and Interrupts Reference Guide** describes the various interrupts and system control features of the 2803x microcontrollers (MCUs).

SPRU566 **TMS320x28xx, 28xxx DSP Peripheral Reference Guide** describes the peripheral reference guides of the 28x digital signal processors (DSPs).

SPRUGO0 **TMS320x2803x Piccolo Boot ROM Reference Guide** describes the purpose and features of the boot loader (factory-programmed boot-loading software) and provides examples of code. It also describes other contents of the device on-chip boot ROM and identifies where all of the information is located within that memory.

SPRUGE5   **TMS320x2802x, 2803x Piccolo Analog-to-Digital Converter (ADC) and Comparator Reference Guide** describes how to configure and use the on-chip ADC module, which is a 12-bit pipelined ADC.

SPRUGE9   **TMS320x2802x, 2803x Piccolo Enhanced Pulse Width Modulator (ePWM) Module Reference Guide** describes the main areas of the enhanced pulse width modulator that include digital motor control, switch mode power supply control, UPS (uninterruptible power supplies), and other forms of power conversion.

SPRUGE8   **TMS320x2802x, 2803x Piccolo High-Resolution Pulse Width Modulator (HRPWM)** describes the operation of the high-resolution extension to the pulse width modulator (HRPWM).

SPRUGH1   **TMS320x2802x, 2803x Piccolo Serial Communications Interface (SCI) Reference Guide** describes how to use the SCI.

SPRUFZ8   **TMS320x2802x, 2803x Piccolo Enhanced Capture (eCAP) Module Reference Guide** describes the enhanced capture module. It includes the module description and registers.

SPRUG71   **TMS320x2802x, 2803x Piccolo Serial Peripheral Interface (SPI) Reference Guide** describes the SPI - a high-speed synchronous serial input/output (I/O) port - that allows a serial bit stream of programmed length (one to sixteen bits) to be shifted into and out of the device at a programmed bit-transfer rate.

SPRUFZ9   **TMS320x2802x, 2803x Piccolo Inter-Integrated Circuit (I2C) Reference Guide** describes the features and operation of the inter-integrated circuit (I2C) module.

SPRUGE6   **TMS320x2803x Piccolo Control Law Accelerator (CLA) Reference Guide** describes the operation of the Control Law Accelerator (CLA).

SPRUGE2   **TMS320x2803x Piccolo Local Interconnect Network (LIN) Module Reference Guide** describes the operation of the Local Interconnect Network (LIN) Module.

SPRUFK8   **TMS320x2803x Piccolo Enhanced Quadrature Encoder Pulse (eQEP) Reference Guide** describes the operation of the Enhanced Quadrature Encoder Pulse (eQEP) .

SPRUGL7   **TMS320x2803x Piccolo Enhanced Controller Area Network (eCAN) Reference Guide** describes the operation of the Enhanced Controller Area Network (eCAN).

Tools Guides

SPRU513   **TMS320C28x Assembly Language Tools v5.0.0 User's Guide** describes the assembly language tools (assembler and other tools used to develop assembly language code), assembler directives, macros, common object file format, and symbolic debugging directives for the TMS320C28x device.

SPRU514   **TMS320C28x Optimizing C/C++ Compiler v5.0.0 User's Guide** describes the TMS320C28x™ C/C++ compiler. This compiler accepts ANSI standard C/C++ source code and produces TMS320 DSP assembly language source code for the TMS320C28x device.

SPRU608   **TMS320C28x Instruction Set Simulator Technical Overview** describes the simulator, available within the Code Composer Studio for TMS320C2000 IDE, that simulates the instruction set of the C28x™ core.

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6 Electrical Specifications

6.1 Absolute Maximum Ratings[(1)(2)]

Supply voltage range, V_{DDIO} (I/O and Flash)	with respect to V_{SS}	−0.3 V to 4.6 V
Supply voltage range, V_{DD}	with respect to V_{SS}	−0.3 V to 2.5 V
Analog voltage range, V_{DDA}	with respect to V_{SSA}	−0.3 V to 4.6 V
Input voltage range, V_{IN} (3.3 V)		−0.3 V to 4.6 V
Output voltage range, V_O		−0.3 V to 4.0 V
Input clamp current, I_{IK} (V_{IN} < 0 or V_{IN} > V_{DDIO})[(3)]		±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DDIO})		±20 mA
Junction temperature range, T_J[(4)]		−40°C to 150°C
Storage temperature range, T_{stg}[(4)]		−65°C to 150°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to V_{SS}, unless otherwise noted.
(3) Continuous clamp current per pin is ± 2 mA.
(4) Long-term high-temperature storage and/or extended use at maximum temperature conditions may result in a reduction of overall device life. For additional information, see *IC Package Thermal Metrics Application Report* (literature number SPRA953) and *Reliability Data for TMS320LF24xx and TMS320F28xx Devices Application Report* (literature number SPRA963).

6.2 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Device supply voltage, I/O, V_{DDIO}		2.97	3.3	3.63	V
Device supply voltage CPU, V_{DD} (When internal VREG is disabled and 1.8 V is supplied externally)		1.71	1.8	1.995	V
Supply ground, V_{SS}			0		V
Analog supply voltage, V_{DDA}		2.97	3.3	3.63	V
Analog ground, V_{SSA}			0		V
Device clock frequency (system clock)		2		60	MHz
High-level input voltage, V_{IH}(3.3 V)		2		V_{DDIO}	V
Low-level input voltage, V_{IL} (3.3 V)				0.8	V
High-level output source current, $V_{OH} = V_{OH(MIN)}$, I_{OH}	All GPIO pins		−4		mA
	Group 2[(1)]		−8		mA
Low-level output sink current, $V_{OL} = V_{OL(MAX)}$, I_{OL}	All GPIO pins		4		mA
	Group 2[(1)]		8		mA
Junction temperature, T_J[(2)]	T version	−40		105	°C
	S version	−40		125	

(1) Group 2 pins are as follows: GPIO16, GPIO17, GPIO18, GPIO19, GPIO28, GPIO29, GPIO36, GPIO37
(2) T_A (Ambient temperature) is product- and application-dependent and can go up to the specified T_J max of the device.

6.3 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = I_{OH}MAX$		2.4			V
		$I_{OH} = 50\ \mu A$		$V_{DDIO} - 0.2$			
V_{OL}	Low-level output voltage	$I_{OL} = I_{OL}MAX$				0.4	V
I_{IL}	Input current (low level)	Pin with pullup enabled	$V_{DDIO} = 3.3$ V, $V_{IN} = 0$ V	All I/Os (including $\overline{XRS}$)	−100		μA
		Pin with pulldown enabled	$V_{DDIO} = 3.3$ V, $V_{IN} = 0$ V			±2	
I_{IH}	Input current (high level)	Pin with pullup enabled	$V_{DDIO} = 3.3$ V, $V_{IN} = V_{DDIO}$			±2	μA
		Pin with pulldown enabled	$V_{DDIO} = 3.3$ V, $V_{IN} = V_{DDIO}$		100		
I_{OZ}	Output current, pullup or pulldown disabled	$V_O = V_{DDIO}$ or 0 V				±2	μA
C_I	Input capacitance				2		pF

6.4 Current Consumption

Table 6-1. TMS320F2803x Current Consumption at 60-MHz SYSCLKOUT

MODE	TEST CONDITIONS	VREG ENABLED				VREG DISABLED					
		I_{DDIO}		I_{DDA}		I_{DD}		I_{DDIO} [1]		I_{DDA} [2]	
		TYP [3]	MAX	TYP [3]	MAX	TYP [3]	MAX	TYP [3]	MAX	TYP	MAX
Operational (Flash)	The following peripheral clocks are enabled: • ePWM1/2/3/4/5/6/7 • eCAP1 • eQEP1 • SCI-A • SPI-A/B • ADC • I2C • COMP1/2/3 • CPU-TIMER0/1/2 All PWM pins are toggled at 60 kHz. All I/O pins are left unconnected. [4] [5] Code is running out of flash with 2 wait-states. XCLKOUT is turned off.	95 mA		13 mA		83 mA		15 mA		13 mA	
IDLE	Flash is powered down. XCLKOUT is turned off. All peripheral clocks are turned off.	20 mA		100 μA		20 mA		200 μA		100 μA	
STANDBY	Flash is powered down. Peripheral clocks are off.	5 mA		25 μA		4 mA		200 μA		25 μA	

(1) I_{DDIO} current is dependent on the electrical loading on the I/O pins.
(2) In order to realize the I_{DDA} currents shown for IDLE, STANDBY, and HALT, clock to the ADC module must be turned off explicitly by writing to the PCLKCR0 register.
(3) The TYP numbers are applicable over room temperature and nominal voltage.
(4) The following is done in a loop:
  • Data is continuously transmitted out of SPI-A and SCI-A ports.
  • The hardware multiplier is exercised.
  • Watchdog is reset.
  • ADC is performing coninuous conversion.
  • COMP1/2 are continuously switching voltages.
  • GPIO17 is toggled.
(5) If a quartz crystal or ceramic resonator is used as the clock source, the HALT mode shuts down the on-chip crystal oscillator.

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Table 6-1. TMS320F2803x Current Consumption at 60-MHz SYSCLKOUT (continued)

MODE	TEST CONDITIONS	VREG ENABLED				VREG DISABLED					
		I_{DDIO}		I_{DDA}		I_{DD}		I_{DDIO} [1]		I_{DDA} [2]	
		TYP [3]	MAX	TYP [3]	MAX	TYP [3]	MAX	TYP [3]	MAX	TYP	MAX
HALT	Flash is powered down. Peripheral clocks are off. Input clock is disabled.	100 µA		25 µA		50 µA		50 µA		25 µA	

<div style="text-align:center">

NOTE

</div>

The peripheral - I/O multiplexing implemented in the device prevents all available peripherals from being used at the same time. This is because more than one peripheral function may share an I/O pin. It is, however, possible to turn on the clocks to all the peripherals at the same time, although such a configuration is not useful. If this is done, the current drawn by the device will be more than the numbers specified in the current consumption tables.

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6.4.1 Reducing Current Consumption

The 2803x devices incorporate a method to reduce the device current consumption. Since each peripheral unit has an individual clock-enable bit, significant reduction in current consumption can be achieved by turning off the clock to any peripheral module that is not used in a given application. Furthermore, any one of the three low-power modes could be taken advantage of to reduce the current consumption even further. Table 6-2 indicates the typical reduction in current consumption achieved by turning off the clocks.

Table 6-2. Typical Current Consumption by Various Peripherals (at 60 MHz)[1]

PERIPHERAL MODULE[2]	I_{DD} CURRENT REDUCTION (mA)
ADC	2[3]
I2C	3
ePWM	2
eCAP	2
eQEP	2
SCI	2
SPI	2
COMP/DAC	1
HRPWM	3
CPU-TIMER	1
Internal zero-pin oscillator	0.5
CAN	2.5
LIN	1.5
CLA	20

(1) All peripheral clocks are disabled upon reset. Writing to/reading from peripheral registers is possible only after the peripheral clocks are turned on.

(2) For peripherals with multiple instances, the current quoted is per module. For example, the 2 mA value quoted for ePWM is for one ePWM module.

(3) This number represents the current drawn by the digital portion of the ADC module. Turning off the clock to the ADC module results in the elimination of the current drawn by the analog portion of the ADC (I_{DDA}) as well.

NOTE

I_{DDIO} current consumption is reduced by 15 mA (typical) when XCLKOUT is turned off.

NOTE

The baseline I_{DD} current (current when the core is executing a dummy loop with no peripherals enabled) is 45 mA, typical. To arrive at the I_{DD} current for a given application, the current-drawn by the peripherals (enabled by that application) must be added to the baseline I_{DD} current.

Following are other methods to reduce power consumption further:

- The flash module may be powered down if code is run off SARAM. This results in a current reduction of 18 mA (typical) in the V_{DD} rail and 13 mA (typical) in the V_{DDIO} rail.
- Savings in I_{DDIO} may be realized by disabling the pullups on pins that assume an output function.

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6.4.2 Current Consumption Graphs (VREG Enabled)
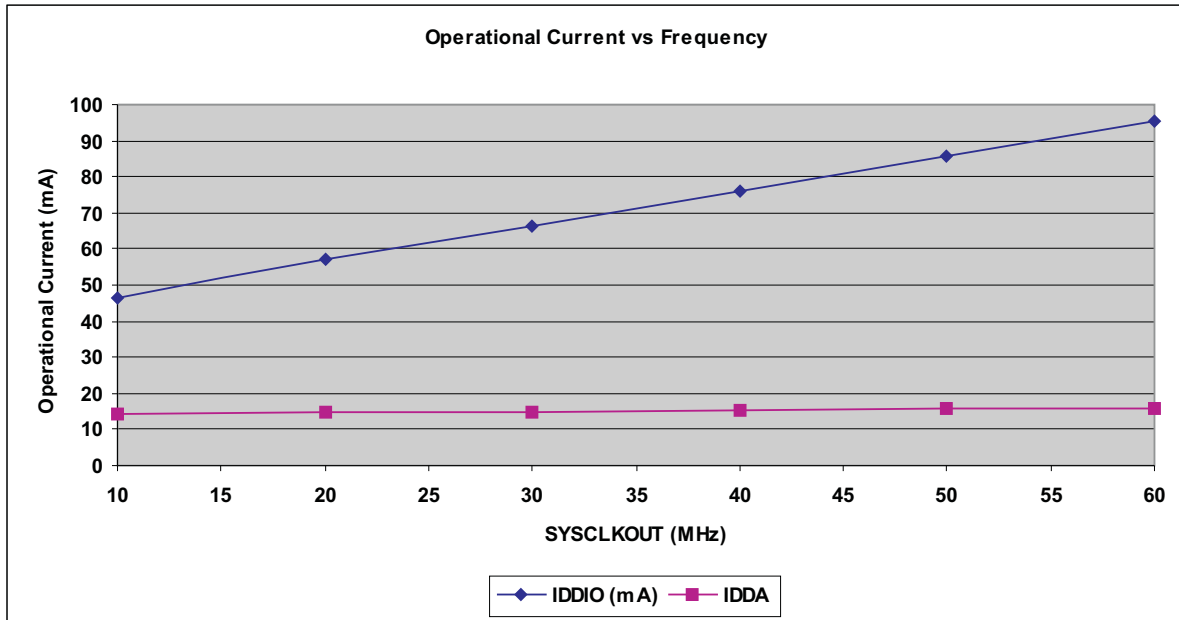
Figure 6-1. Typical Operational Current Versus Frequency (F2802x)
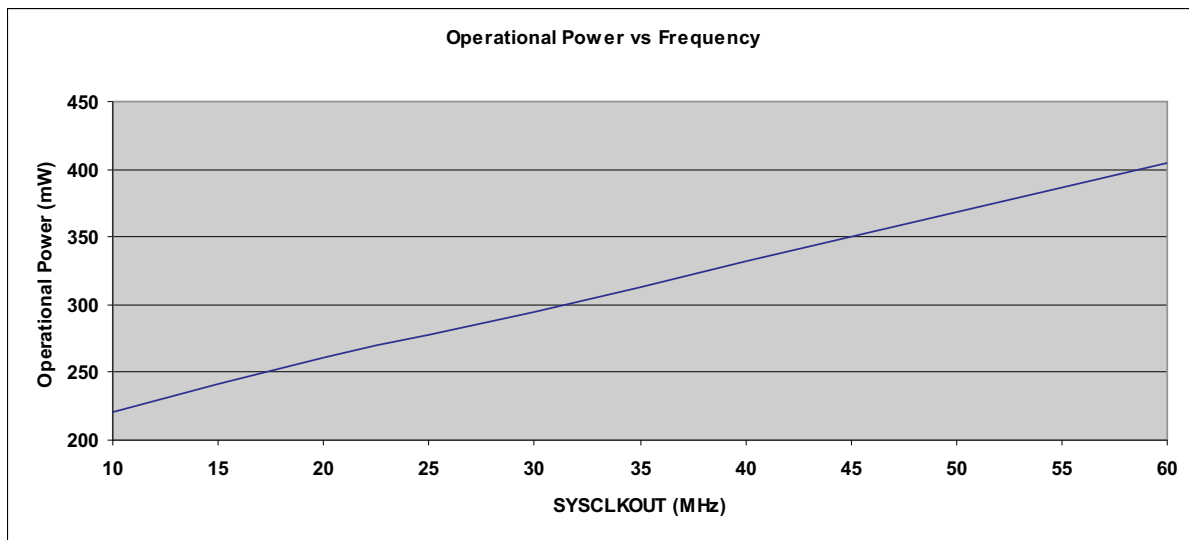
Figure 6-2. Typical Operational Power Versus Frequency (F2802x)

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6.5 Thermal Design Considerations

Based on the end application design and operational profile, the I_{DD} and I_{DDIO} currents could vary. Systems that exceed the recommended maximum power dissipation in the end product may require additional thermal enhancements. Ambient temperature (T_A) varies with the end application and product design. The critical factor that affects reliability and functionality is T_J, the junction temperature, not the ambient temperature. Hence, care should be taken to keep T_J within the specified limits. T_{case} should be measured to estimate the operating junction temperature T_J. T_{case} is normally measured at the center of the package top-side surface. The thermal application reports *IC Package Thermal Metrics* (literature number SPRA953) and *Reliability Data for TMS320LF24xx and TMS320F28xx Devices* (literature number SPRA963) help to understand the thermal metrics and definitions.

6.6 Emulator Connection Without Signal Buffering for the MCU

Figure 6-3 shows the connection between the MCU and JTAG header for a single-processor configuration. If the distance between the JTAG header and the MCU is greater than 6 inches, the emulation signals must be buffered. If the distance is less than 6 inches, buffering is typically not needed. Figure 6-3 shows the simpler, no-buffering situation. For the pullup/pulldown resistor values, see the pin description section.
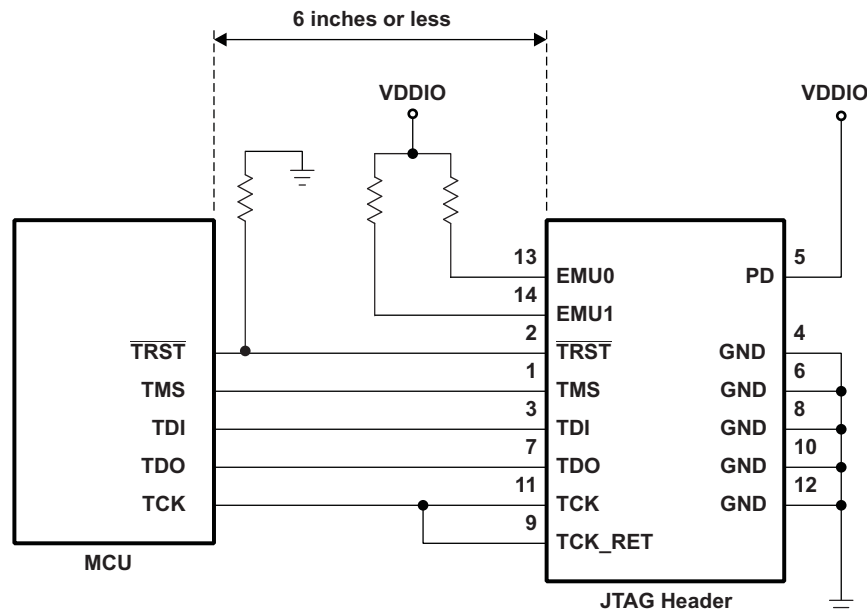
A.   See Figure 4-16 for JTAG/GPIO multiplexing.

Figure 6-3. Emulator Connection Without Signal Buffering for the MCU

> **NOTE**
>
> The 2802x devices do not have EMU0/EMU1 pins. For designs that have a JTAG Header on-board, the EMU0/EMU1 pins on the header must be tied to V_{DDIO} through a 4.7 kΩ (typical) resistor.

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6.7 Timing Parameter Symbology

Timing parameter symbols used are created in accordance with JEDEC Standard 100. To shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

Lowercase subscripts and their meanings:		**Letters and symbols and their meanings:**	
a	access time	H	High
c	cycle time (period)	L	Low
d	delay time	V	Valid
f	fall time	X	Unknown, changing, or don't care level
h	hold time	Z	High impedance
r	rise time		
su	setup time		
t	transition time		
v	valid time		
w	pulse duration (width)		

6.7.1 General Notes on Timing Parameters

All output signals from the 28x devices (including XCLKOUT) are derived from an internal clock such that all output transitions for a given half-cycle occur with a minimum of skewing relative to each other.

The signal combinations shown in the following timing diagrams may not necessarily represent actual cycles. For actual cycle examples, see the appropriate cycle description section of this document.

6.7.2 Test Load Circuit

This test load circuit is used to measure all switching characteristics provided in this document.
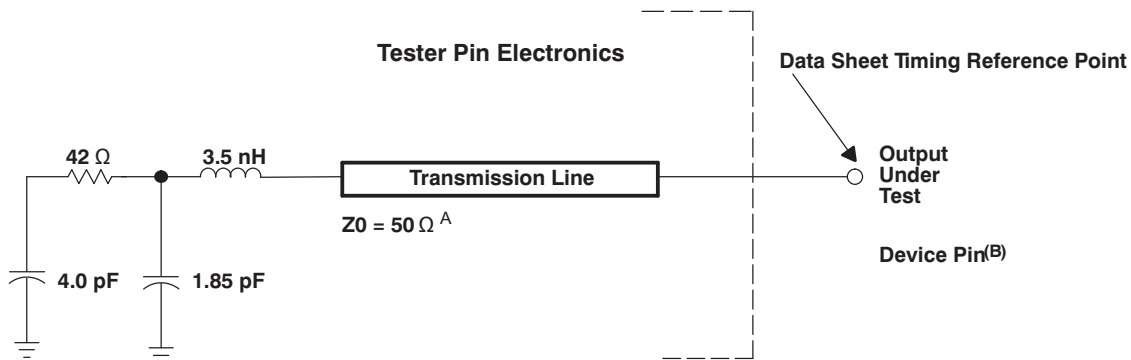
A. Input requirements in this data sheet are tested with an input slew rate of < 4 Volts per nanosecond (4 V/ns) at the device pin.

B. The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. A transmission line with a delay of 2 ns or longer can be used to produce the desired transmission line effect. The transmission line is intended as a load only. It is not necessary to add or subtract the transmission line delay (2 ns or longer) from the data sheet timing.

Figure 6-4. 3.3-V Test Load Circuit

6.7.3 Device Clock Table

This section provides the timing requirements and switching characteristics for the various clock options available on the 2803x MCUs. Table 6-3 lists the cycle times of various clocks.

Table 6-3. 2803x Clock Table and Nomenclature (60-MHz Devices)

		MIN	NOM	MAX	UNIT
Internal zero-pin oscillator 1 (INTOSC1)	$t_{c(ZPOSC1)}$, Cycle time		100		ns
	Frequency		10		MHz
Internal zero-pin oscillator 2 (INTOSC2)	$t_{c(ZPOSC2)}$, Cycle time		100		ns
	Frequency		10		MHz
On-chip crystal oscillator (X1/X2 pins)	$t_{c(OSC)}$, Cycle time	50		200	ns
	Frequency	5		20	MHz
XCLKIN	$t_{c(CI)}$, Cycle time	16.67		250	ns
	Frequency	4		60	MHz
SYSCLKOUT	$t_{c(SCO)}$, Cycle time	16.67		500	ns
	Frequency	2		60	MHz
XCLKOUT	$t_{c(XCO)}$, Cycle time	50		2000	ns
	Frequency	0.5		20	MHz
LSPCLK[1]	$t_{c(LCO)}$, Cycle time	16.67	66.7[2]		ns
	Frequency		15[2]	60	MHz
ADC clock	$t_{c(ADCCLK)}$, Cycle time	16.67			ns
	Frequency			60	MHz

(1)   Lower LSPCLK will reduce device power consumption.
(2)   This is the default reset value if SYSCLKOUT = 60 MHz.

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6.8 Clock Requirements and Characteristics

Table 6-4. Input Clock Frequency

PARAMETER		MIN	TYP	MAX	UNIT
f_x Input clock frequency	Resonator (X1/X2)	5		20	MHz
	Crystal (X1/X2)	5		20	
	External oscillator/clock source (XCLKIN pin)	4		60	
f_l Limp mode SYSCLKOUT frequency range (with /2 enabled)			1–5		MHz

Table 6-5. XCLKIN Timing Requirements - PLL Enabled

NO.			MIN	MAX	UNIT
C8	$t_{c(CI)}$	Cycle time, XCLKIN	33.3	200	ns
C9	$t_{f(CI)}$	Fall time, XCLKIN		6	ns
C10	$t_{r(CI)}$	Rise time, XCLKIN		6	ns
C11	$t_{w(CIL)}$	Pulse duration, XCLKIN low as a percentage of $t_{c(OSCCLK)}$	45	55	%
C12	$t_{w(CIH)}$	Pulse duration, XCLKIN high as a percentage of $t_{c(OSCCLK)}$	45	55	%

Table 6-6. XCLKIN Timing Requirements - PLL Disabled

NO.				MIN	MAX	UNIT
C8	$t_{c(CI)}$	Cycle time, XCLKIN		16.67	250	ns
C9	$t_{f(CI)}$	Fall time, XCLKIN	Up to 20 MHz		6	ns
			20 MHz to 60 MHz		2	
C10	$t_{r(CI)}$	Rise time, XCLKIN	Up to 20 MHz		6	ns
			20 MHz to 60 MHz		2	
C11	$t_{w(CIL)}$	Pulse duration, XCLKIN low as a percentage of $t_{c(OSCCLK)}$		45	55	%
C12	$t_{w(CIH)}$	Pulse duration, XCLKIN high as a percentage of $t_{c(OSCCLK)}$		45	55	%

The possible configuration modes are shown in Table 3-17.

Table 6-7. XCLKOUT Switching Characteristics (PLL Bypassed or Enabled)[1][2]

NO.		PARAMETER	MIN	TYP	MAX	UNIT
C1	$t_{c(XCO)}$	Cycle time, XCLKOUT	50			ns
C3	$t_{f(XCO)}$	Fall time, XCLKOUT		2		ns
C4	$t_{r(XCO)}$	Rise time, XCLKOUT		2		ns
C5	$t_{w(XCOL)}$	Pulse duration, XCLKOUT low	H – 2		H + 2	ns
C6	$t_{w(XCOH)}$	Pulse duration, XCLKOUT high	H – 2		H + 2	ns
	t_p	PLL lock time			1 [3]	ms

(1) A load of 40 pF is assumed for these parameters.
(2) H = 0.5$t_{c(XCO)}$
(3) The PLLLOCKPRD register must be updated based on the number of OSCCLK cycles.
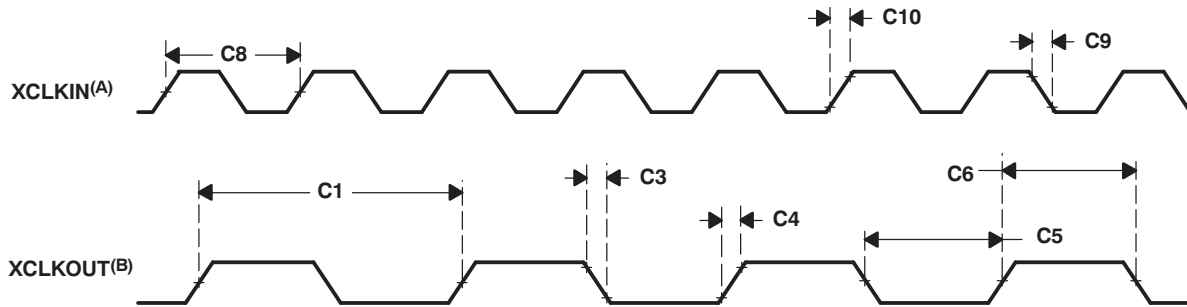
A. The relationship of XCLKIN to XCLKOUT depends on the divide factor chosen. The waveform relationship shown is intended to illustrate the timing parameters only and may differ based on actual configuration.

B. XCLKOUT configured to reflect SYSCLKOUT.

Figure 6-5. Clock Timing

6.9 Power Sequencing

There is no power sequencing requirement. However, it is recommended that no voltage larger than a diode drop (0.7 V) should be applied to any pin prior to powering up the device. Voltages applied to pins on an unpowered device can bias internal p-n junctions in unintended ways and produce unpredictable results.

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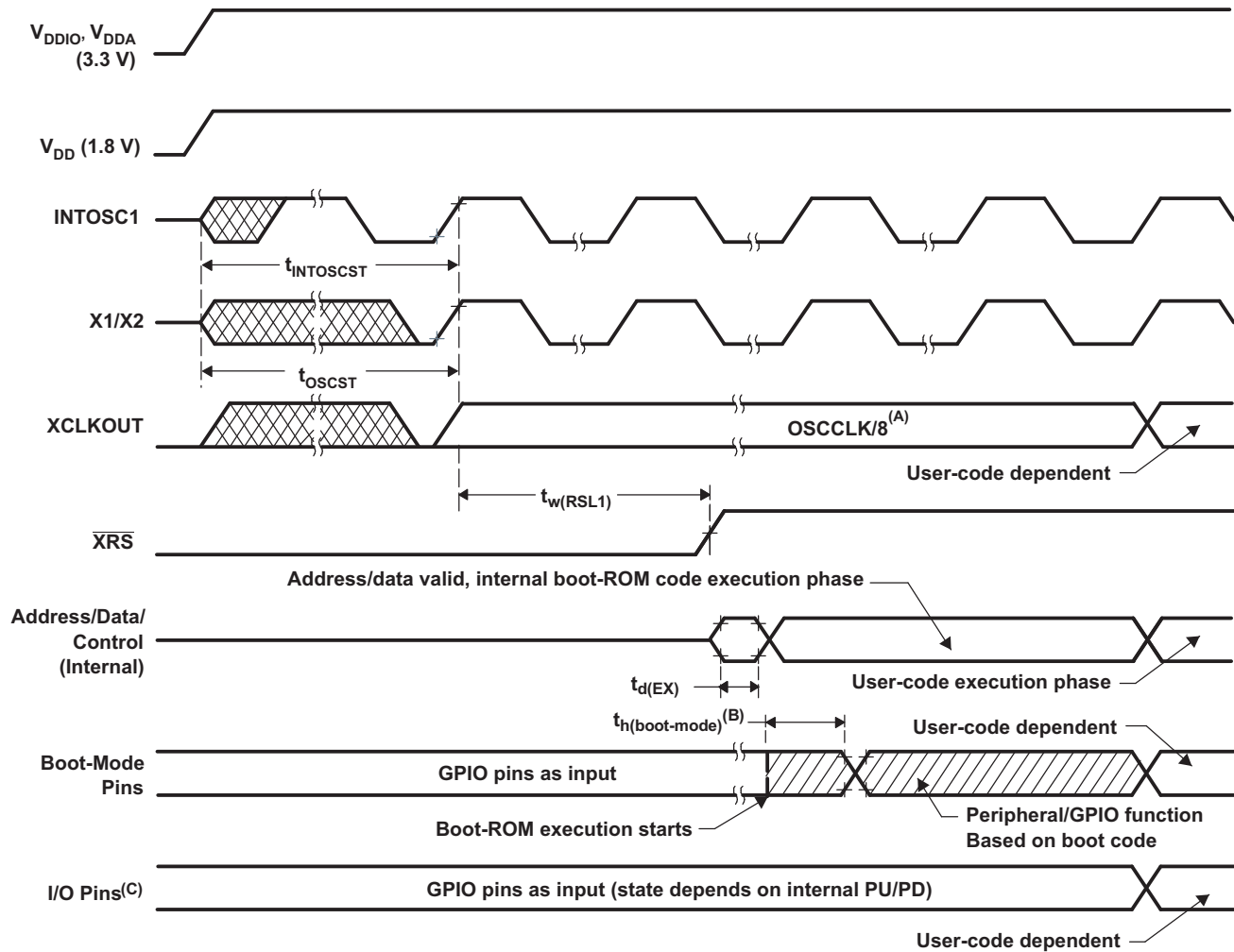
A. Upon power up, SYSCLKOUT is OSCCLK/2. Since the XCLKOUTDIV bits in the XCLK register come up with a reset state of 0, SYSCLKOUT is further divided by 4 before it appears at XCLKOUT. This explains why XCLKOUT = OSCCLK/8 during this phase.

B. After reset, the boot ROM code samples Boot Mode pins. Based on the status of the Boot Mode pin, the boot code branches to destination memory or boot code function. If boot ROM code executes after power-on conditions (in debugger environment), the boot code execution time is based on the current SYSCLKOUT speed. The SYSCLKOUT will be based on user environment and could be with or without PLL enabled.

C. See Section 6.9 for requirements to ensure a high-impedance state for GPIO pins during power-up.

D. Using the $\overline{\text{XRS}}$ pin is optional due to the on-chip power-on reset (POR) circuitry.

Figure 6-6. Power-on Reset

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Table 6-8. Reset ($\overline{XRS}$) Timing Requirements

		MIN	NOM	MAX	UNIT
$t_{h(boot-mode)}$	Hold time for boot-mode pins		TBD		cycles
$t_{w(RSL2)}$	Pulse duration, $\overline{XRS}$ low on warm reset		$8t_{c(OSCCLK)}$		cyclies

Table 6-9. Reset ($\overline{XRS}$) Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{w(RSL1)}$	Pulse duration, $\overline{XRS}$ driven by device			600		µs
$t_{w(WDRS)}$	Pulse duration, reset pulse generated by watchdog			$512t_{c(OSCCLK)}$		cycles
$t_{d(EX)}$	Delay time, address/data valid after $\overline{XRS}$ high			$32t_{c(OSCCLK)}$		cycles
$t_{INTOSCST}$	Start up time, internal zero-pin oscillator			3		µs
t_{OSCST}[1]	On-chip crystal, oscillator start-up time		1	10		ms

(1) Dependent on crystal/resonator and board design.

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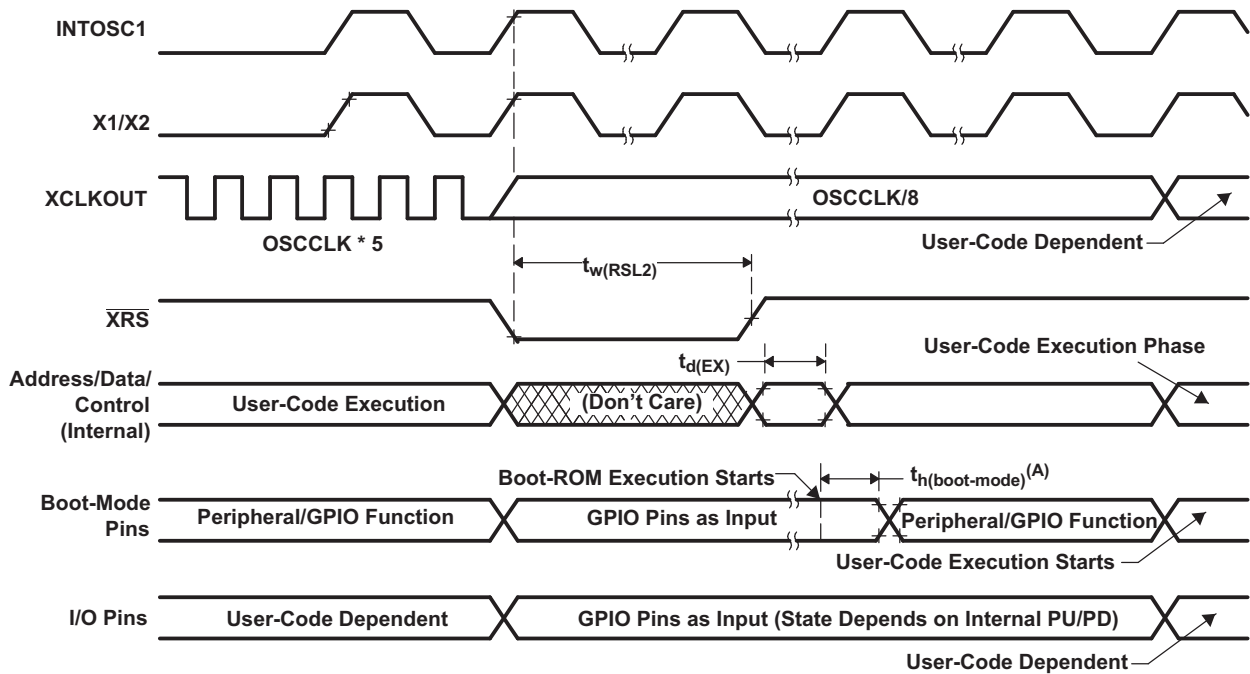
A. After reset, the Boot ROM code samples BOOT Mode pins. Based on the status of the Boot Mode pin, the boot code branches to destination memory or boot code function. If Boot ROM code executes after power-on conditions (in debugger environment), the Boot code execution time is based on the current SYSCLKOUT speed. The SYSCLKOUT will be based on user environment and could be with or without PLL enabled.

Figure 6-7. Warm Reset

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Figure 6-8 shows an example for the effect of writing into PLLCR register. In the first phase, PLLCR = 0x0004 and SYSCLKOUT = OSCCLK x 2. The PLLCR is then written with 0x0008. Right after the PLLCR register is written, the PLL lock-up phase begins. During this phase, SYSCLKOUT = OSCCLK/2. After the PLL lock-up is complete,SYSCLKOUT reflects the new operating frequency, OSCCLK x 4.

OSCCLK

Write to PLLCR

SYSCLKOUT

| OSCCLK * 2 | OSCCLK/2 | OSCCLK * 4 |

(Current CPU Frequency)

(CPU frequency while PLL is stabilizing with the desired frequency. This period (PLL lock-up time t_p) is 1 ms long.)

(Changed CPU frequency)
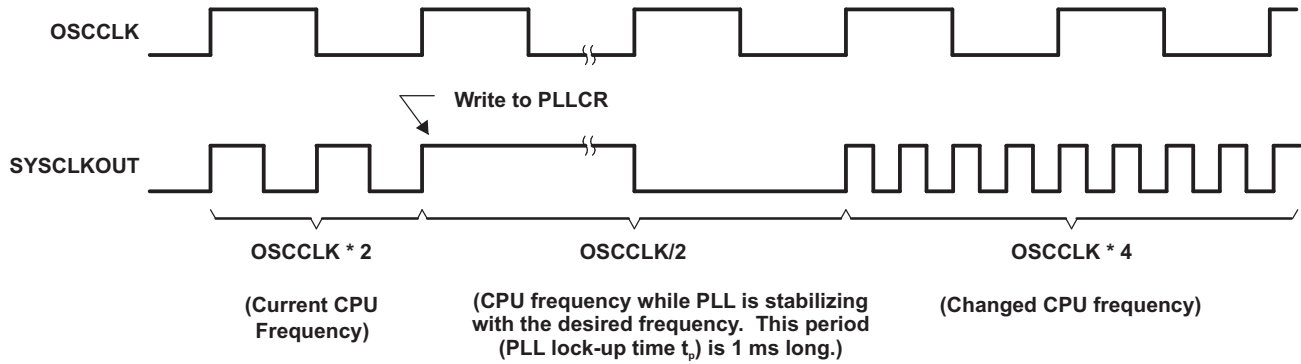
Figure 6-8. Example of Effect of Writing Into PLLCR Register

6.10 General-Purpose Input/Output (GPIO)

6.10.1 GPIO - Output Timing

Table 6-10. General-Purpose Output Switching Characteristics

PARAMETER			MIN	MAX	UNIT
$t_{r(GPO)}$	Rise time, GPIO switching low to high	All GPIOs		8	ns
$t_{f(GPO)}$	Fall time, GPIO switching high to low	All GPIOs		8	ns
t_{fGPO}	Toggling frequency			20	MHz

GPIO

$t_{f(GPO)}$ $t_{r(GPO)}$
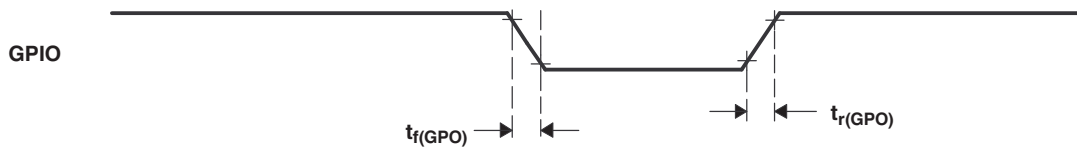
Figure 6-9. General-Purpose Output Timing

6.10.2 GPIO - Input Timing

Figure 6-10. Sampling Mode
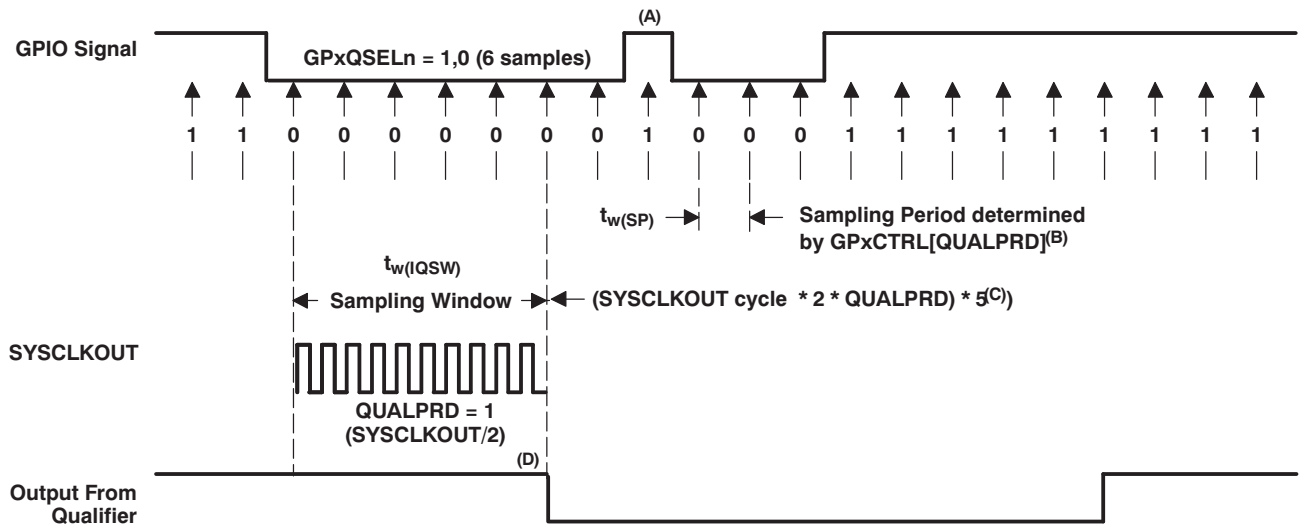
A. This glitch will be ignored by the input qualifier. The QUALPRD bit field specifies the qualification sampling period. It can vary from 00 to 0xFF. If QUALPRD = 00, then the sampling period is 1 SYSCLKOUT cycle. For any other value "n", the qualification sampling period in 2n SYSCLKOUT cycles (i.e., at every 2n SYSCLKOUT cycles, the GPIO pin will be sampled).

B. The qualification period selected via the GPxCTRL register applies to groups of 8 GPIO pins.

C. The qualification block can take either three or six samples. The GPxQSELn Register selects which sample mode is used.

D. In the example shown, for the qualifier to detect the change, the input should be stable for 10 SYSCLKOUT cycles or greater. In other words, the inputs should be stable for (5 x QUALPRD x 2) SYSCLKOUT cycles. This would ensure 5 sampling periods for detection to occur. Since external signals are driven asynchronously, an 13-SYSCLKOUT-wide pulse ensures reliable recognition.

Table 6-11. General-Purpose Input Timing Requirements

			MIN	MAX	UNIT
$t_{w(SP)}$	Sampling period	QUALPRD = 0	$1t_{c(SCO)}$		cycles
		QUALPRD ≠ 0	$2t_{c(SCO)}$ * QUALPRD		cycles
$t_{w(IQSW)}$	Input qualifier sampling window		$t_{w(SP)}$ * ($n^{(1)}$ − 1)		cycles
$t_{w(GPI)}$[(2)]	Pulse duration, GPIO low/high	Synchronous mode	$2t_{c(SCO)}$		cycles
		With input qualifier	$t_{w(IQSW)}$ + $t_{w(SP)}$ + $1t_{c(SCO)}$		cycles

(1) "n" represents the number of qualification samples as defined by GPxQSELn register.
(2) For $t_{w(GPI)}$, pulse width is measured from V_{IL} to V_{IL} for an active low signal and V_{IH} to V_{IH} for an active high signal.

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6.10.3 Sampling Window Width for Input Signals

The following section summarizes the sampling window width for input signals for various input qualifier configurations.

Sampling frequency denotes how often a signal is sampled with respect to SYSCLKOUT.

Sampling frequency = SYSCLKOUT/(2 * QUALPRD), if QUALPRD ≠ 0

Sampling frequency = SYSCLKOUT, if QUALPRD = 0

Sampling period = SYSCLKOUT cycle x 2 x QUALPRD, if QUALPRD ≠ 0

In the above equations, SYSCLKOUT cycle indicates the time period of SYSCLKOUT.

Sampling period = SYSCLKOUT cycle, if QUALPRD = 0

In a given sampling window, either 3 or 6 samples of the input signal are taken to determine the validity of the signal. This is determined by the value written to GPxQSELn register.

Case 1:

Qualification using 3 samples

Sampling window width = (SYSCLKOUT cycle x 2 x QUALPRD) x 2, if QUALPRD ≠ 0

Sampling window width = (SYSCLKOUT cycle) x 2, if QUALPRD = 0

Case 2:

Qualification using 6 samples

Sampling window width = (SYSCLKOUT cycle x 2 x QUALPRD) x 5, if QUALPRD ≠ 0

Sampling window width = (SYSCLKOUT cycle) x 5, if QUALPRD = 0
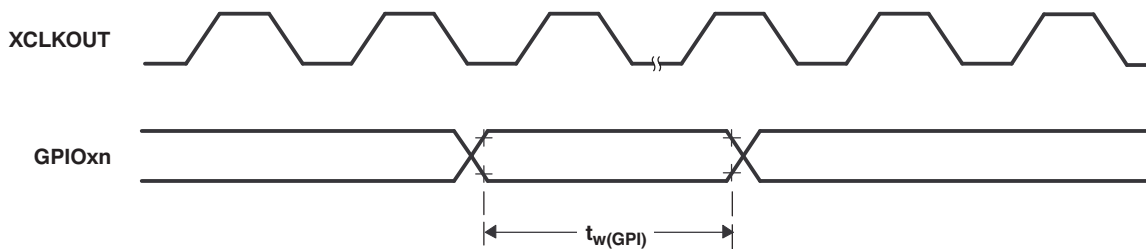
Figure 6-11. General-Purpose Input Timing

6.10.4 Low-Power Mode Wakeup Timing

Table 6-12 shows the timing requirements, Table 6-13 shows the switching characteristics, and Figure 6-12 shows the timing diagram for IDLE mode.

Table 6-12. IDLE Mode Timing Requirements[1]

			MIN	NOM	MAX	UNIT
$t_{w(WAKE-INT)}$	Pulse duration, external wake-up signal	Without input qualifier		$2t_{c(SCO)}$		cycles
		With input qualifier		$5t_{c(SCO)} + t_{w(IQSW)}$		

(1) For an explanation of the input qualifier parameters, see Table 6-11.

Table 6-13. IDLE Mode Switching Characteristics[1]

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(WAKE-IDLE)}$	Delay time, external wake signal to program execution resume [2]					cycles
	• Wake-up from Flash – Flash module in active state	Without input qualifier			$20t_{c(SCO)}$	cycles
		With input qualifier			$20t_{c(SCO)} + t_{w(IQSW)}$	
	• Wake-up from Flash – Flash module in sleep state	Without input qualifier			$1050t_{c(SCO)}$	cycles
		With input qualifier			$1050t_{c(SCO)} + t_{w(IQSW)}$	
	• Wake-up from SARAM	Without input qualifier			$20t_{c(SCO)}$	cycles
		With input qualifier			$20t_{c(SCO)} + t_{w(IQSW)}$	

(1) For an explanation of the input qualifier parameters, see Table 6-11.
(2) This is the time taken to begin execution of the instruction that immediately follows the IDLE instruction. execution of an ISR (triggered by the wake up) signal involves additional latency.
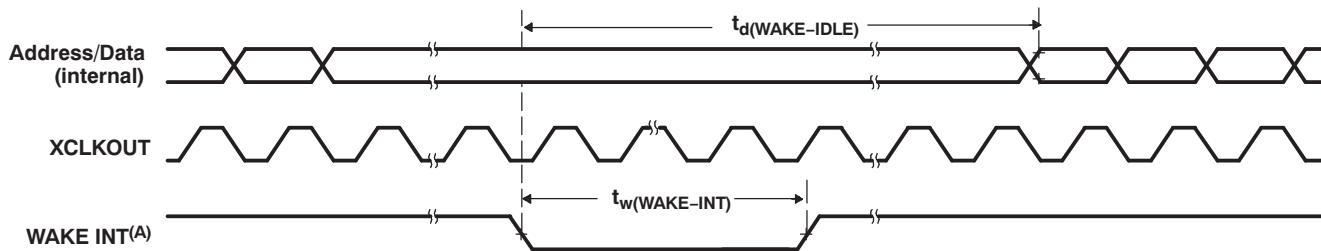
A. WAKE INT can be any enabled interrupt, $\overline{WDINT}$ or $\overline{XRS}$.

Figure 6-12. IDLE Entry and Exit Timing

Table 6-14. STANDBY Mode Timing Requirements

		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{w(WAKE-INT)}$	Pulse duration, external wake-up signal	Without input qualification		$3t_{c(OSCCLK)}$		cycles
		With input qualification[1]		$(2 + QUALSTDBY) * t_{c(OSCCLK)}$		

(1) QUALSTDBY is a 6-bit field in the LPMCR0 register.

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Table 6-15. STANDBY Mode Switching Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(IDLE-XCOL)}$	Delay time, IDLE instruction executed to XCLKOUT low		$32t_{c(SCO)}$		$45t_{c(SCO)}$	cycles
$t_{d(WAKE-STBY)}$	Delay time, external wake signal to program execution resume[1]					cycles
	• Wake up from flash – Flash module in active state	Without input qualifier			$100t_{c(SCO)}$	cycles
		With input qualifier			$100t_{c(SCO)} + t_{w(WAKE-INT)}$	
	• Wake up from flash – Flash module in sleep state	Without input qualifier			$1125t_{c(SCO)}$	cycles
		With input qualifier			$1125t_{c(SCO)} + t_{w(WAKE-INT)}$	
	• Wake up from SARAM	Without input qualifier			$100t_{c(SCO)}$	cycles
		With input qualifier			$100t_{c(SCO)} + t_{w(WAKE-INT)}$	

(1) This is the time taken to begin execution of the instruction that immediately follows the IDLE instruction. execution of an ISR (triggered by the wake up signal) involves additional latency.
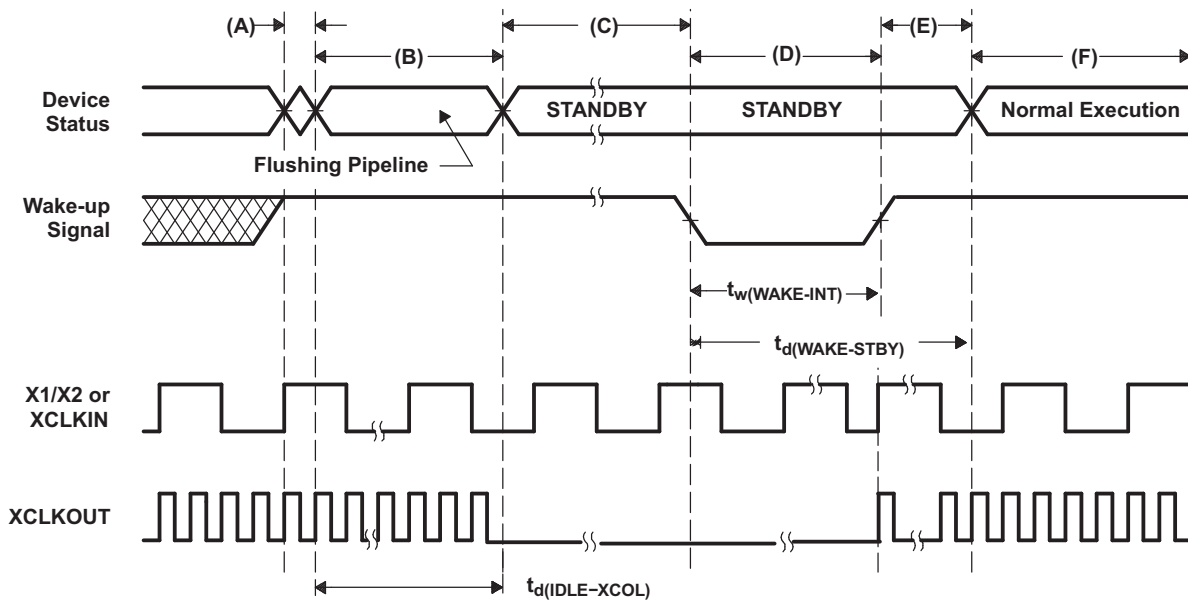
A. IDLE instruction is executed to put the device into STANDBY mode.
B. The PLL block responds to the STANDBY signal. SYSCLKOUT is held for approximately 32 cycles before being turned off. This 32-cycle delay enables the CPU pipe and any other pending operations to flush properly.
C. Clock to the peripherals are turned off. However, the PLL and watchdog are not shut down. The device is now in STANDBY mode.
D. The external wake-up signal is driven active.
E. After a latency period, the STANDBY mode is exited.
F. Normal execution resumes. The device will respond to the interrupt (if enabled).

Figure 6-13. STANDBY Entry and Exit Timing Diagram

Table 6-16. HALT Mode Timing Requirements

		MIN	NOM	MAX	UNIT
$t_{w(WAKE-GPIO)}$	Pulse duration, GPIO wake-up signal	$t_{oscst} + 2t_{c(OSCCLK)}$			cycles
$t_{w(WAKE-XRS)}$	Pulse duration, $\overline{XRS}$ wakeup signal	$t_{oscst} + 8t_{c(OSCCLK)}$			cycles

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Table 6-17. HALT Mode Switching Characteristics

PARAMETER		MIN	TYP	MAX	UNIT
$t_{d(IDLE-XCOL)}$	Delay time, IDLE instruction executed to XCLKOUT low	$32t_{c(SCO)}$		$45t_{c(SCO)}$	cycles
t_p	PLL lock-up time			1	ms
$t_{d(WAKE-HALT)}$	Delay time, PLL lock to program execution resume • Wake up from flash – Flash module in sleep state			$1125t_{c(SCO)}$	cycles
	• Wake up from SARAM			$35t_{c(SCO)}$	cycles
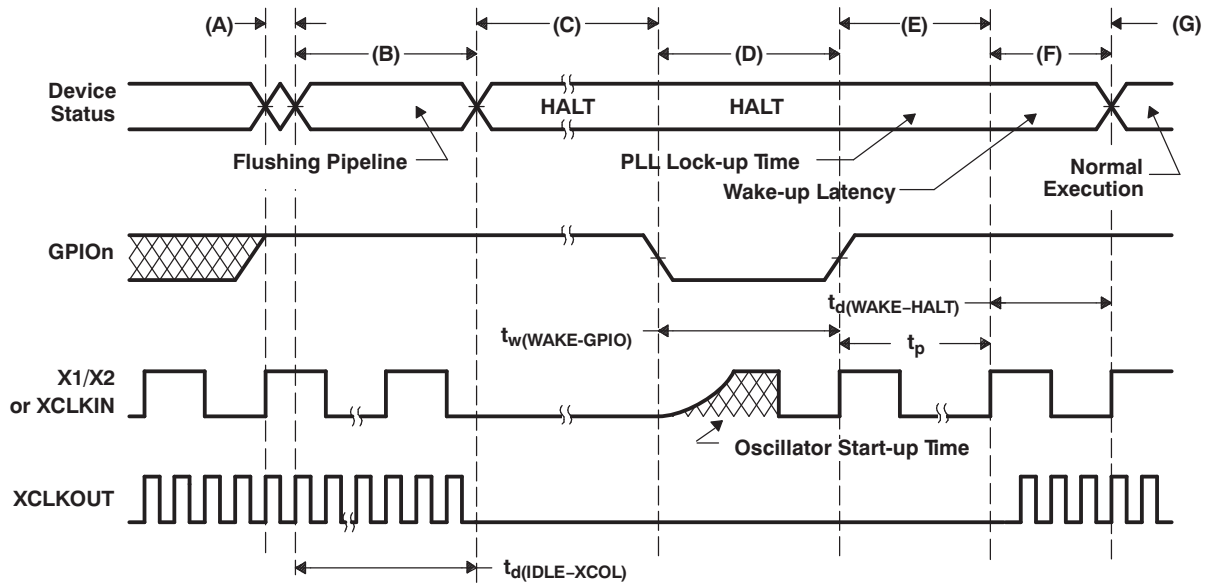
A. IDLE instruction is executed to put the device into HALT mode.

B. The PLL block responds to the HALT signal. SYSCLKOUT is held for approximately 32 cycles before the oscillator is turned off and the CLKIN to the core is stopped. This 32-cycle delay enables the CPU pipe and any other pending operations to flush properly.

C. Clocks to the peripherals are turned off and the PLL is shut down. If a quartz crystal or ceramic resonator is used as the clock source, the internal oscillator is shut down as well. The device is now in HALT mode and consumes absolute minimum power.

D. When the GPIOn pin is driven low, the oscillator is turned on and the oscillator wake-up sequence is initiated. The GPIO pin should be driven high only after the oscillator has stabilized. This enables the provision of a clean clock signal during the PLL lock sequence. Since the falling edge of the GPIO pin asynchronously begins the wakeup procedure, care should be taken to maintain a low noise environment prior to entering and during HALT mode.

E. When GPIOn is deactivated, it initiates the PLL lock sequence, which takes 131,072 OSCCLK (X1/X2 or X1 or XCLKIN) cycles.

F. When CLKIN to the core is enabled, the device will respond to the interrupt (if enabled), after a latency. The HALT mode is now exited.

G. Normal operation resumes.

Figure 6-14. HALT Wake-Up Using GPIOn

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6.11 Enhanced Control Peripherals

6.11.1 Enhanced Pulse Width Modulator (ePWM) Timing

PWM refers to PWM outputs on ePWM1–7. Table 6-18 shows the PWM timing requirements and Table 6-19, switching characteristics.

Table 6-18. ePWM Timing Requirements[1]

		TEST CONDITIONS	MIN	MAX	UNIT
$t_{w(SYCIN)}$	Sync input pulse width	Asynchronous	$2t_{c(SCO)}$		cycles
		Synchronous	$2t_{c(SCO)}$		cycles
		With input qualifier	$1t_{c(SCO)} + t_{w(IQSW)}$		cycles

(1) For an explanation of the input qualifier parameters, see Table 6-11.

Table 6-19. ePWM Switching Characteristics

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{w(PWM)}$	Pulse duration, PWMx output high/low		20		ns
$t_{w(SYNCOUT)}$	Sync output pulse width		$8t_{c(SCO)}$		cycles
$t_{d(PWM)tza}$	Delay time, trip input active to PWM forced high Delay time, trip input active to PWM forced low	no pin load		25	ns
$t_{d(TZ-PWM)HZ}$	Delay time, trip input active to PWM Hi-Z			20	ns

6.11.2 Trip-Zone Input Timing
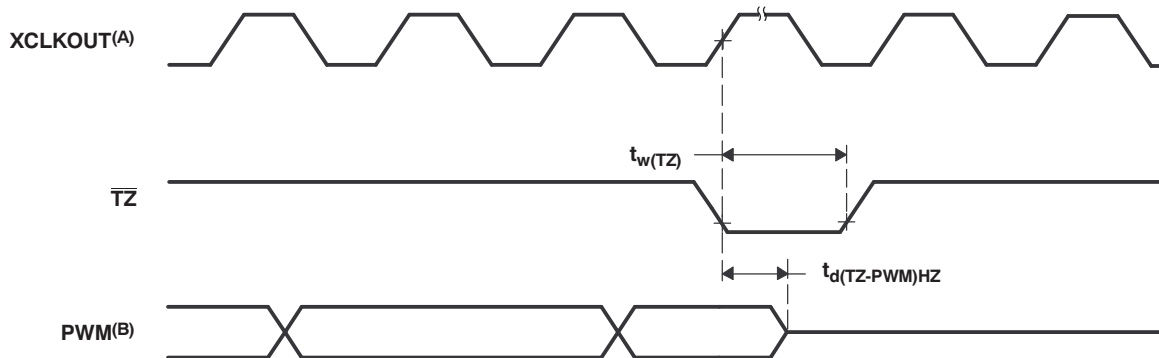
A. $\overline{TZ}$ - $\overline{TZ1}$, $\overline{TZ2}$, $\overline{TZ3}$, $\overline{TZ4}$, $\overline{TZ5}$, $\overline{TZ6}$

B. PWM refers to all the PWM pins in the device. The state of the PWM pins after $\overline{TZ}$ is taken high depends on the PWM recovery software.

Figure 6-15. PWM Hi-Z Characteristics

Table 6-20. Trip-Zone input Timing Requirements[1]

			MIN	MAX	UNIT
$t_{w(TZ)}$	Pulse duration, $\overline{TZx}$ input low	Asynchronous	$1t_{c(SCO)}$		cycles
		Synchronous	$2t_{c(SCO)}$		cycles
		With input qualifier	$1t_{c(SCO)} + t_{w(IQSW)}$		cycles

(1) For an explanation of the input qualifier parameters, see Table 6-11.

Table 6-21 shows the high-resolution PWM switching characteristics.

Table 6-21. High Resolution PWM Characteristics at SYSCLKOUT = (60 - 100 MHz)

	MIN	TYP	MAX	UNIT
Micro Edge Positioning (MEP) step size[1] [2]		150	310	ps

(1) Maximum MEP step size is based on worst-case process, maximum temperature and maximum voltage. MEP step size will increase with low voltage and high temperature and decrease with voltage and cold temperature.
Applications that use the HRPWM feature should use MEP Scale Factor Optimizer (SFO) estimation software functions. See the TI software libraries for details of using SFO function in end applications. SFO functions help to estimate the number of MEP steps per SYSCLKOUT period dynamically while the HRPWM is in operation.
(2) Between 40 to 50 MHz SYSCLKOUT under worst case process, voltage, and temperature (maximum voltage and minimum temperature) conditions, the MEP step delay may decrease to a point such that the maximum of 254 MEP steps may not cover 1 full SYSCLKOUT cycle. In other words, high-resolution edge control will not be available for the full range of a SYSCLKOUT cycle. If running SFO calibration software, the SFO function will return an error code of "2" when this occurs. See the *TMS320x2802x, 2803x Piccolo High-Resolution Pulse Width Modulator (HRPWM) Reference Guide* (literature number SPRUGE8) for more information on this error condition.

6.11.3 Enhanced Capture (eCAP) Timing

Table 6-22 shows the eCAP timing requirement and Table 6-23 shows the eCAP switching characteristics.

Table 6-22. Enhanced Capture (eCAP) Timing Requirement[1]

		TEST CONDITIONS	MIN	MAX	UNIT
$t_{w(CAP)}$	Capture input pulse width	Asynchronous	$2t_{c(SCO)}$		cycles
		Synchronous	$2t_{c(SCO)}$		cycles
		With input qualifier	$1t_{c(SCO)} + t_{w(IQSW)}$		cycles

(1) For an explanation of the input qualifier parameters, see Table 6-11.

Table 6-23. eCAP Switching Characteristics

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{w(APWM)}$	Pulse duration, APWMx output high/low		20		ns

6.11.4 Enhanced Quadrature Encoder Pulse (eQEP) Timing

Table 6-24 shows the eQEP timing requirement and Table 6-25 shows the eQEP switching characteristics.

Table 6-24. Enhanced Quadrature Encoder Pulse (eQEP) Timing Requirements[1]

		TEST CONDITIONS	MIN	MAX	UNIT
$t_{w(QEPP)}$	QEP input period	Asynchronous/synchronous	$2t_{c(SCO)}$		cycles
		With input qualifier	$2(1t_{c(SCO)} + t_{w(IQSW)})$		cycles
$t_{w(INDEXH)}$	QEP Index Input High time	Asynchronous/synchronous	$2t_{c(SCO)}$		cycles
		With input qualifier	$2t_{c(SCO)} + t_{w(IQSW)}$		cycles
$t_{w(INDEXL)}$	QEP Index Input Low time	Asynchronous/synchronous	$2t_{c(SCO)}$		cycles
		With input qualifier	$2t_{c(SCO)} + t_{w(IQSW)}$		cycles
$t_{w(STROBH)}$	QEP Strobe High time	Asynchronous/synchronous	$2t_{c(SCO)}$		cycles
		With input qualifier	$2t_{c(SCO)} + t_{w(IQSW)}$		cycles
$t_{w(STROBL)}$	QEP Strobe Input Low time	Asynchronous/synchronous	$2t_{c(SCO)}$		cycles
		With input qualifier	$2t_{c(SCO)} + t_{w(IQSW)}$		cycles

(1) For an explanation of the input qualifier parameters, see Table 6-11.

Table 6-25. eQEP Switching Characteristics

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{d(CNTR)xin}$	Delay time, external clock to counter increment			$4t_{c(SCO)}$	cycles
$t_{d(PCS-OUT)QEP}$	Delay time, QEP input edge to position compare sync output			$6t_{c(SCO)}$	cycles

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6.11.5 ADC Start-of-Conversion Timing

Table 6-26. External ADC Start-of-Conversion Switching Characteristics

PARAMETER		MIN	MAX	UNIT
$t_{w(ADCSOCL)}$	Pulse duration, $\overline{ADCSOCxO}$ low	$32t_{c(HCO)}$		cycles
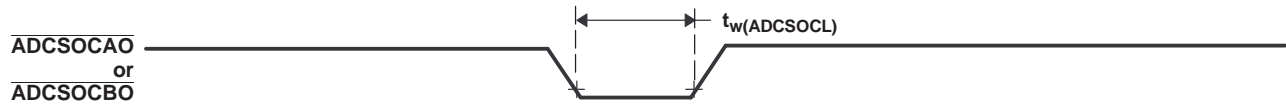
Figure 6-16. $\overline{ADCSOCAO}$ or $\overline{ADCSOCBO}$ Timing

6.11.6 External Interrupt Timing
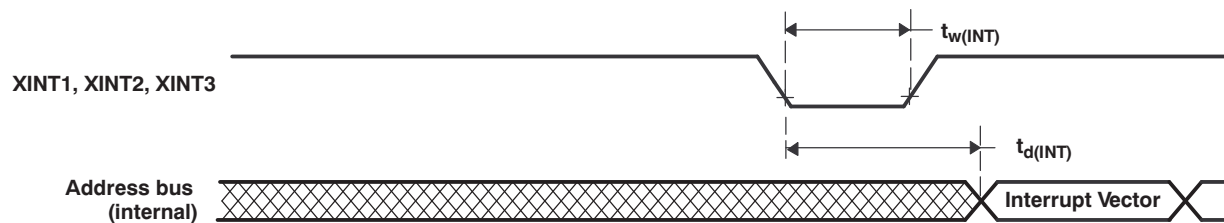
Figure 6-17. External Interrupt Timing

Table 6-27. External Interrupt Timing Requirements[1]

		TEST CONDITIONS	MIN	MAX	UNIT
$t_{w(INT)}$ [2]	Pulse duration, INT input low/high	Synchronous	$1t_{c(SCO)}$		cycles
		With qualifier	$1t_{c(SCO)} + t_{w(IQSW)}$		cycles

(1) For an explanation of the input qualifier parameters, see Table 6-11.
(2) This timing is applicable to any GPIO pin configured for ADCSOC functionality.

Table 6-28. External Interrupt Switching Characteristics[1]

PARAMETER		MIN	MAX	UNIT
$t_{d(INT)}$	Delay time, INT low/high to interrupt-vector fetch		$t_{w(IQSW)} + 12t_{c(SCO)}$	cycles

(1) For an explanation of the input qualifier parameters, see Table 6-11.

6.11.7 I2C Electrical Specification and Timing

Table 6-29. I2C Timing

		TEST CONDITIONS	MIN	MAX	UNIT
f_{SCL}	SCL clock frequency	I2C clock module frequency is between 7 MHz and 12 MHz and I2C prescaler and clock divider registers are configured appropriately		400	kHz
v_{il}	Low level input voltage			0.3 V_{DDIO}	V
V_{ih}	High level input voltage		0.7 V_{DDIO}		V
V_{hys}	Input hysteresis		0.05 V_{DDIO}		V
V_{ol}	Low level output voltage	3 mA sink current	0	0.4	V
t_{LOW}	Low period of SCL clock	I2C clock module frequency is between 7 MHz and 12 MHz and I2C prescaler and clock divider registers are configured appropriately	1.3		µs
t_{HIGH}	High period of SCL clock	I2C clock module frequency is between 7 MHz and 12 MHz and I2C prescaler and clock divider registers are configured appropriately	0.6		µs
I_I	Input current with an input voltage between 0.1 V_{DDIO} and 0.9 V_{DDIO} MAX		−10	10	µA

6.11.8 Serial Peripheral Interface (SPI) Master Mode Timing

Table 6-30 lists the master mode timing (clock phase = 0) and Table 6-31 lists the timing (clock phase = 1). Figure 6-18 and Figure 6-19 show the timing waveforms.

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Table 6-30. SPI Master Mode External Timing (Clock Phase = 0)[1][2][3][4][5]

NO.			SPI WHEN (SPIBRR + 1) IS EVEN OR SPIBRR = 0 OR 2		SPI WHEN (SPIBRR + 1) IS ODD AND SPIBRR > 3		UNIT
			MIN	MAX	MIN	MAX	
1	$t_{c(SPC)M}$	Cycle time, SPICLK	$4t_{c(LCO)}$	$128t_{c(LCO)}$	$5t_{c(LCO)}$	$127t_{c(LCO)}$	ns
2	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)M} - 10$	$0.5t_{c(SPC)M}$	$0.5t_{c(SPC)M} - 0.5t_{c(LCO)} - 10$	$0.5t_{c(SPC)M} - 0.5t_{c(LCO)}$	ns
	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)M} - 10$	$0.5t_{c(SPC)M}$	$0.5t_{c(SPC)M} - 0.5t_{c(LCO)} - 10$	$0.5t_{c(SPC)M} - 0.5t_{c(LCO)}$	
3	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)M} - 10$	$0.5t_{c(SPC)M}$	$0.5t_{c(SPC)M} + 0.5t_{c(LCO)} - 10$	$0.5t_{c(SPC)M} + 0.5t_{c(LCO)}$	ns
	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 1)	$0.5t_{c(SPC)M} - 10$	$0.5t_{c(SPC)M}$	$0.5t_{c(SPC)M} + 0.5t_{c(LCO)} - 10$	$0.5t_{c(SPC)M} + 0.5t_{c(LCO)}$	
4	$t_{d(SPCH-SIMO)M}$	Delay time, SPICLK high to SPISIMO valid (clock polarity = 0)		10		10	ns
	$t_{d(SPCL-SIMO)M}$	Delay time, SPICLK low to SPISIMO valid (clock polarity = 1)		10		10	
5	$t_{v(SPCL-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)M} - 10$		$0.5t_{c(SPC)M} + 0.5t_{c(LCO)} - 10$		ns
	$t_{v(SPCH-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK high (clock polarity = 1)	$0.5t_{c(SPC)M} - 10$		$0.5t_{c(SPC)M} + 0.5t_{c(LCO)} - 10$		
8	$t_{su(SOMI-SPCL)M}$	Setup time, SPISOMI before SPICLK low (clock polarity = 0)	35		35		ns
	$t_{su(SOMI-SPCH)M}$	Setup time, SPISOMI before SPICLK high (clock polarity = 1)	35		35		
9	$t_{v(SPCL-SOMI)M}$	Valid time, SPISOMI data valid after SPICLK low (clock polarity = 0)	$0.25t_{c(SPC)M} - 10$		$0.5t_{c(SPC)M} - 0.5t_{c(LCO)} - 10$		ns
	$t_{v(SPCH-SOMI)M}$	Valid time, SPISOMI data valid after SPICLK high (clock polarity = 1)	$0.25t_{c(SPC)M} - 10$		$0.5t_{c(SPC)M} - 0.5t_{c(LCO)} - 10$		

(1) The MASTER / SLAVE bit (SPICTL.2) is set and the CLOCK PHASE bit (SPICTL.3) is cleared.
(2) $t_{c(SPC)}$ = SPI clock cycle time = LSPCLK/4 or LSPCLK/(SPIBRR +1)
(3) $t_{c(LCO)}$ = LSPCLK cycle time
(4) Internal clock prescalers must be adjusted such that the SPI clock speed is limited to the following SPI clock rate:
    Master mode transmit 20-MHz MAX, master mode receive 10-MHz MAX
    Slave mode transmit 10-MAX, slave mode receive 10-MHz MAX.
(5) The active edge of the SPICLK signal referenced is controlled by the clock polarity bit (SPICCR.6).
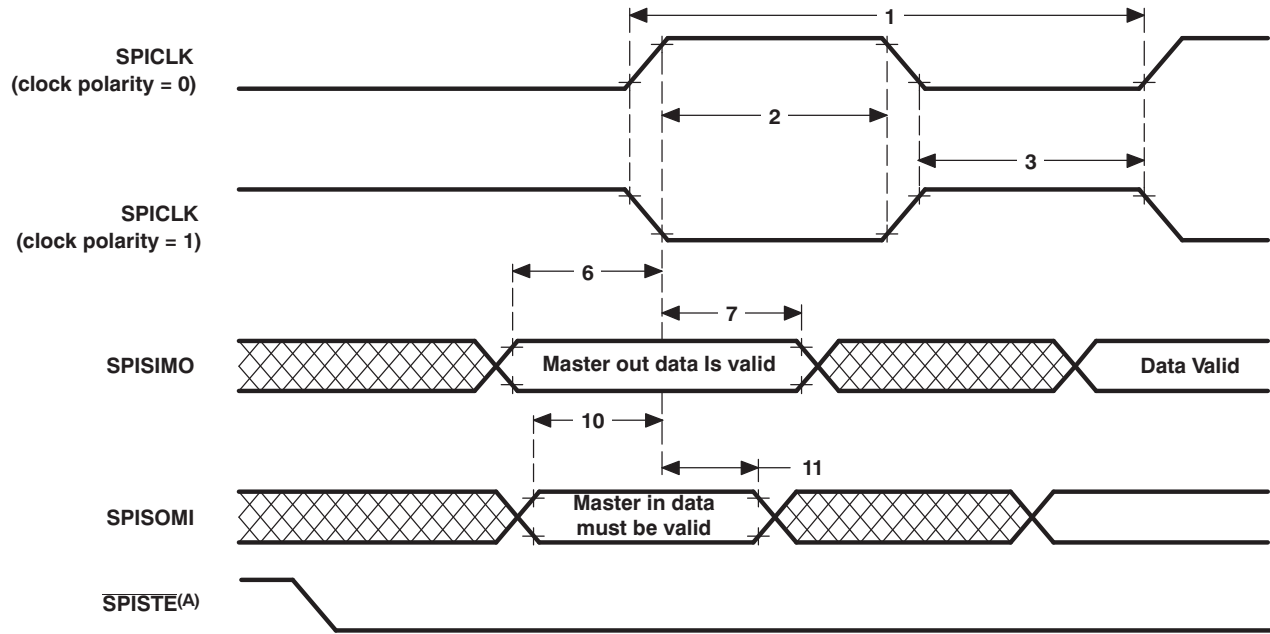
A. In the master mode, $\overline{\text{SPISTE}}$ goes active $0.5t_{c(SPC)}$ (minimum) before valid SPI clock edge. On the trailing end of the word, the $\overline{\text{SPISTE}}$ will go inactive $0.5t_{c(SPC)}$ after the receiving edge (SPICLK) of the last data bit, except that $\overline{\text{SPISTE}}$ stays active between back-to-back transmit words in both FIFO and nonFIFO modes.

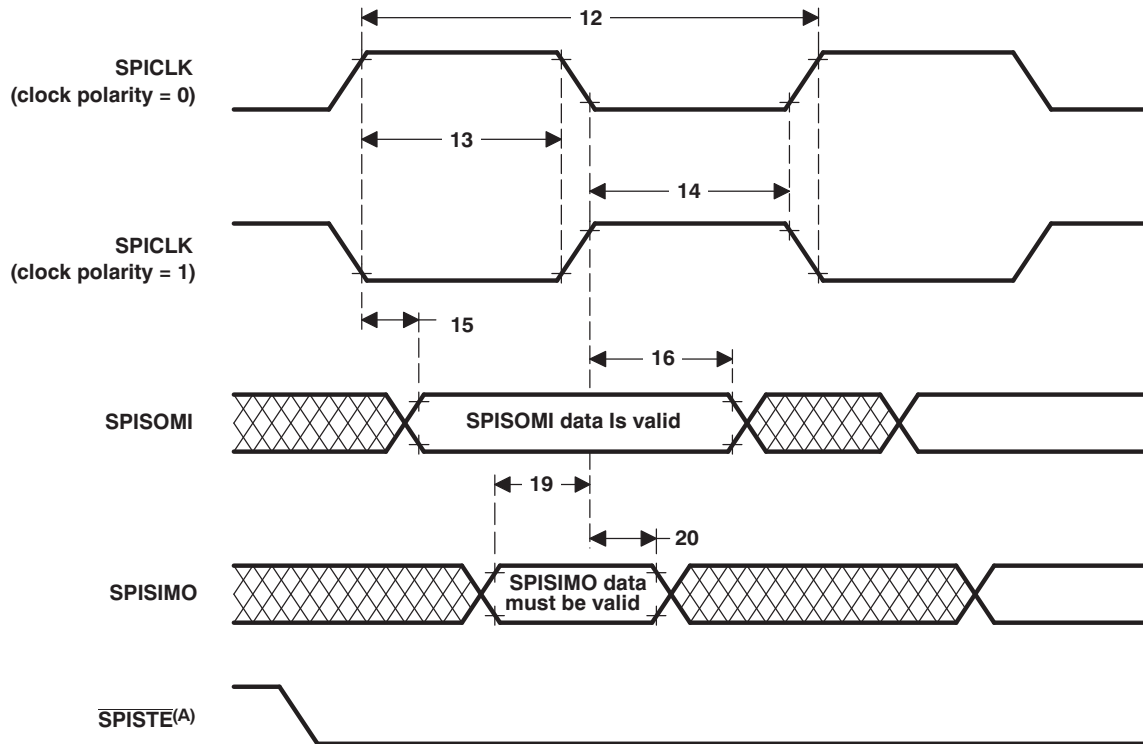**Figure 6-18. SPI Master Mode External Timing (Clock Phase = 0)**

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Table 6-31. SPI Master Mode External Timing (Clock Phase = 1)[1][2][3][4][5]

NO.			SPI WHEN (SPIBRR + 1) IS EVEN OR SPIBRR = 0 OR 2		SPI WHEN (SPIBRR + 1) IS ODD AND SPIBRR > 3		UNIT
			MIN	MAX	MIN	MAX	
1	$t_{c(SPC)M}$	Cycle time, SPICLK	$4t_{c(LCO)}$	$128t_{c(LCO)}$	$5t_{c(LCO)}$	$127t_{c(LCO)}$	ns
2	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)M} - 10$	$0.5t_{c(SPC)M}$	$0.5t_{c(SPC)M} - 0.5t_{c\ (LCO)} - 10$	$0.5t_{c(SPC)M} - 0.5t_{c(LCO)}$	ns
	$t_{w(SPCL))M}$	Pulse duration, SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)M} - 10$	$0.5t_{c(SPC)M}$	$0.5t_{c(SPC)M} - 0.5t_{c\ (LCO)} - 10$	$0.5t_{c(SPC)M} - 0.5t_{c(LCO}$	
3	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)M} - 10$	$0.5t_{c(SPC)M}$	$0.5t_{c(SPC)M} + 0.5t_{c(LCO)} - 10$	$0.5t_{c(SPC)M} + 0.5t_{c(LCO)}$	ns
	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 1)	$0.5t_{c(SPC)M} - 10$	$0.5t_{c(SPC)M}$	$0.5t_{c(SPC)M} + 0.5t_{c(LCO)} - 10$	$0.5t_{c(SPC)M} + 0.5t_{c(LCO)}$	
6	$t_{su(SIMO-SPCH)M}$	Setup time, SPISIMO data valid before SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)M} - 10$		$0.5t_{c(SPC)M} - 10$		ns
	$t_{su(SIMO-SPCL)M}$	Setup time, SPISIMO data valid before SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)M} - 10$		$0.5t_{c(SPC)M} - 10$		
7	$t_{v(SPCH-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)M} - 10$		$0.5t_{c(SPC)M} - 10$		ns
	$t_{v(SPCL-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)M} - 10$		$0.5t_{c(SPC)M} - 10$		
10	$t_{su(SOMI-SPCH)M}$	Setup time, SPISOMI before SPICLK high (clock polarity = 0)	35		35		ns
	$t_{su(SOMI-SPCL)M}$	Setup time, SPISOMI before SPICLK low (clock polarity = 1)	35		35		
11	$t_{v(SPCH-SOMI)M}$	Valid time, SPISOMI data valid after SPICLK high (clock polarity = 0)	$0.25t_{c(SPC)M} - 10$		$0.5t_{c(SPC)M} - 10$		ns
	$t_{v(SPCL-SOMI)M}$	Valid time, SPISOMI data valid after SPICLK low (clock polarity = 1)	$0.25t_{c(SPC)M} - 10$		$0.5t_{c(SPC)M} - 10$		

(1) The MASTER/SLAVE bit (SPICTL.2) is set and the CLOCK PHASE bit (SPICTL.3) is set.
(2) $t_{c(SPC)}$ = SPI clock cycle time = LSPCLK/4 or LSPCLK/(SPIBRR + 1)
(3) Internal clock prescalers must be adjusted such that the SPI clock speed is limited to the following SPI clock rate:
     Master mode transmit 20 MHz MAX, master mode receive 10 MHz MAX
     Slave mode transmit 10 MHz MAX, slave mode receive 10 MHz MAX.
(4) $t_{c(LCO)}$ = LSPCLK cycle time
(5) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPICCR.6).

A. In the master mode, $\overline{\text{SPISTE}}$ goes active $0.5t_{c(SPC)}$ (minimum) before valid SPI clock edge. On the trailing end of the word, the $\overline{\text{SPISTE}}$ will go inactive $0.5t_{c(SPC)}$ after the receiving edge (SPICLK) of the last data bit, except that $\overline{\text{SPISTE}}$ stays active between back-to-back transmit words in both FIFO and nonFIFO modes.

Figure 6-19. SPI Master Mode External Timing (Clock Phase = 1)

6.11.9 SPI Slave Mode Timing

Table 6-32 lists the slave mode external timing (clock phase = 0) and Table 6-33 (clock phase = 1). Figure 6-20 and Figure 6-21 show the timing waveforms.

Table 6-32. SPI Slave Mode External Timing (Clock Phase = 0)[1][2][3][4][5]

NO.			MIN	MAX	UNIT
12	$t_{c(SPC)S}$	Cycle time, SPICLK	$4t_{c(LCO)}$		ns
13	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)S} - 10$	$0.5t_{c(SPC)S}$	ns
	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)S} - 10$	$0.5t_{c(SPC)S}$	
14	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)S} - 10$	$0.5t_{c(SPC)S}$	ns
	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 1)	$0.5t_{c(SPC)S} - 10$	$0.5t_{c(SPC)S}$	
15	$t_{d(SPCH-SOMI)S}$	Delay time, SPICLK high to SPISOMI valid (clock polarity = 0)		35	ns
	$t_{d(SPCL-SOMI)S}$	Delay time, SPICLK low to SPISOMI valid (clock polarity = 1)		35	
16	$t_{v(SPCL-SOMI)S}$	Valid time, SPISOMI data valid after SPICLK low (clock polarity = 0)	$0.75t_{c(SPC)S}$		ns
	$t_{v(SPCH-SOMI)S}$	Valid time, SPISOMI data valid after SPICLK high (clock polarity = 1)	$0.75t_{c(SPC)S}$		
19	$t_{su(SIMO-SPCL)S}$	Setup time, SPISIMO before SPICLK low (clock polarity = 0)	35		ns
	$t_{su(SIMO-SPCH)S}$	Setup time, SPISIMO before SPICLK high (clock polarity = 1)	35		
20	$t_{v(SPCL-SIMO)S}$	Valid time, SPISIMO data valid after SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)S} - 10$		ns
	$t_{v(SPCH-SIMO)S}$	Valid time, SPISIMO data valid after SPICLK high (clock polarity = 1)	$0.5t_{c(SPC)S} - 10$		

(1) The MASTER / SLAVE bit (SPICTL.2) is cleared and the CLOCK PHASE bit (SPICTL.3) is cleared.
(2) $t_{c(SPC)}$ = SPI clock cycle time = LSPCLK/4 or LSPCLK/(SPIBRR + 1)
(3) Internal clock prescalers must be adjusted such that the SPI clock speed is limited to the following SPI clock rate:
    Master mode transmit 20-MHz MAX, master mode receive 10-MHz MAX
    Slave mode transmit 10-MHz MAX, slave mode receive 10-MHz MAX.
(4) $t_{c(LCO)}$ = LSPCLK cycle time
(5) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPICCR.6).

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A. In the slave mode, the $\overline{\text{SPISTE}}$ signal should be asserted low at least $0.5t_{c(SPC)}$ (minimum) before the valid SPI clock edge and remain low for at least $0.5t_{c(SPC)}$ after the receiving edge (SPICLK) of the last data bit.

Figure 6-20. SPI Slave Mode External Timing (Clock Phase = 0)

Table 6-33. SPI Slave Mode External Timing (Clock Phase = 1)[1][2][3][4]

NO.			MIN	MAX	UNIT
12	$t_{c(SPC)S}$	Cycle time, SPICLK	$8t_{c(LCO)}$		ns
13	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)S} - 10$	$0.5t_{c(SPC)S}$	ns
	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)S} - 10$	$0.5t_{c(SPC)S}$	
14	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)S} - 10$	$0.5t_{c(SPC)S}$	ns
	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 1)	$0.5t_{c(SPC)S} - 10$	$0.5t_{c(SPC)S}$	
17	$t_{su(SOMI-SPCH)S}$	Setup time, SPISOMI before SPICLK high (clock polarity = 0)	$0.125t_{c(SPC)S}$		ns
	$t_{su(SOMI-SPCL)S}$	Setup time, SPISOMI before SPICLK low (clock polarity = 1)	$0.125t_{c(SPC)S}$		
18	$t_{v(SPCH-SOMI)S}$	Valid time, SPISOMI data valid after SPICLK low (clock polarity = 0)	$0.75t_{c(SPC)S}$		ns
	$t_{v(SPCL-SOMI)S}$	Valid time, SPISOMI data valid after SPICLK high (clock polarity = 1)	$0.75t_{c(SPC)S}$		
21	$t_{su(SIMO-SPCH)S}$	Setup time, SPISIMO before SPICLK high (clock polarity = 0)	35		ns
	$t_{su(SIMO-SPCL)S}$	Setup time, SPISIMO before SPICLK low (clock polarity = 1)	35		
22	$t_{v(SPCH-SIMO)S}$	Valid time, SPISIMO data valid after SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)S} - 10$		ns
	$t_{v(SPCL-SIMO)S}$	Valid time, SPISIMO data valid after SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)S} - 10$		

(1) The MASTER / SLAVE bit (SPICTL.2) is cleared and the CLOCK PHASE bit (SPICTL.3) is cleared.
(2) $t_{c(SPC)}$ = SPI clock cycle time = LSPCLK/4 or LSPCLK/(SPIBRR + 1)
(3) Internal clock prescalers must be adjusted such that the SPI clock speed is limited to the following SPI clock rate:
     Master mode transmit 20-MHz MAX, master mode receive 10-MHz MAX
     Slave mode transmit 10-MHz MAX, slave mode receive 10-MHz MAX.
(4) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPICCR.6).

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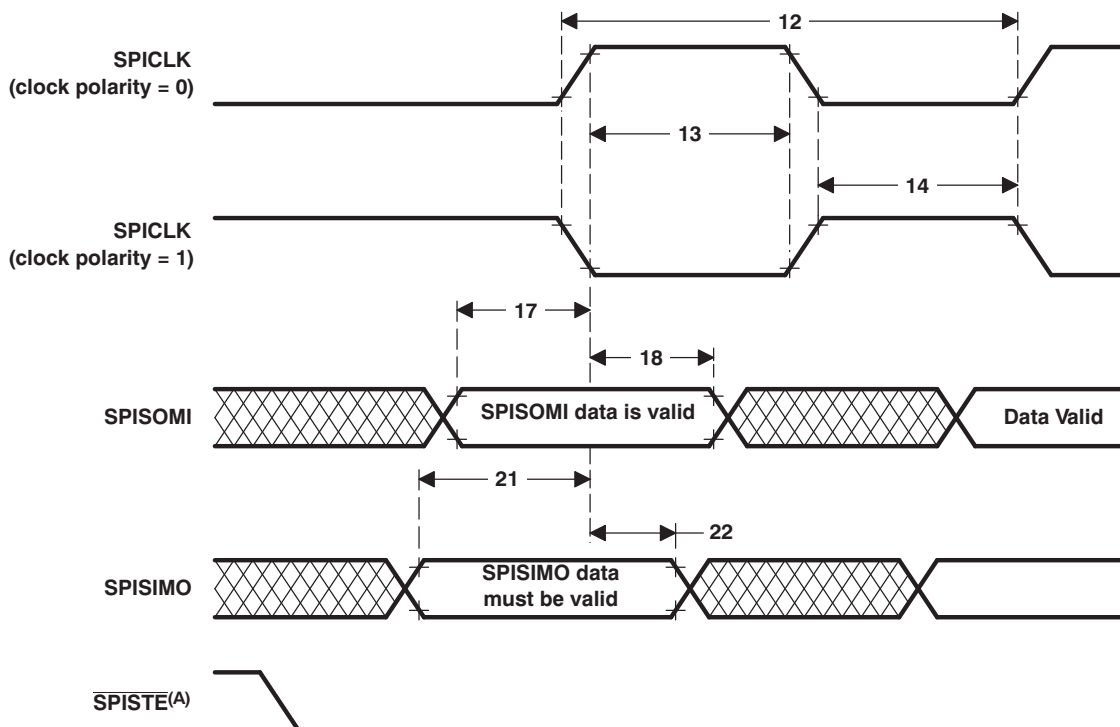
A. In the slave mode, the $\overline{SPISTE}$ signal should be asserted low at least $0.5t_{c(SPC)}$ before the valid SPI clock edge and remain low for at least $0.5t_{c(SPC)}$ after the receiving edge (SPICLK) of the last data bit.

Figure 6-21. SPI Slave Mode External Timing (Clock Phase = 1)

6.11.9.1 On-chip Comparator/DAC

Table 6-34. Electrical Characteristics of the Comparator/DAC

CHARACTERISTIC	MIN	TYP	MAX	UNITS
Comparator				
Comparator Input Range		$V_{SSA} - V_{DDA}$		V
Comparator response time to PWM Trip Zone (Async)		30		ns
Input Offset		±5		mV
Input Hysteresis		35		mV
DAC				
DAC Output Range		$V_{SSA} - V_{DDA}$		V
DAC resolution		10		bits
DAC settling time		2		us
DAC Gain		−1.5		%
DAC Offset		10		mV
No Missing Codes		Yes		
INL		±3		LSB

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6.11.10 On-Chip Analog-to-Digital Converter

Table 6-35. ADC Electrical Characteristics (over recommended operating conditions)

PARAMETER		MIN	TYP	MAX	UNIT
DC SPECIFICATIONS					
Resolution			12		Bits
ADC clock	60-MHz device	0.001		60	MHz
ACCURACY					
INL (Integral nonlinearity)	60-MHz clock (4.62 MSPS)		±2		LSB
DNL (Differential nonlinearity)			±1		LSB
Offset error [1]			±10		LSB
Overall gain error with internal reference			±10		LSB
Overall gain error with external reference			±10		LSB
Channel-to-channel offset variation			±4		LSB
Channel-to-channel gain variation			±4		LSB
ANALOG INPUT					
Analog input voltage [2] with internal reference		0		3.3	V
Analog input voltage [2] with external reference		V_{REFLO}		V_{REFHI}	V
V_{REFLO} input voltage		V_{SSA}	[3]	0.66	V
V_{REFHI} input voltage		2.64		V_{DDA}	V
	with $V_{REFLO} = V_{SSA}$	1.98		V_{DDA}	V
Temperature coefficient			50		PPM/°C
Input capacitance			10		pF
Input leakage current			±5		µA

(1) 1 LSB has the weighted value of full-scale range (FSR)/4096. FSR is 3.3 V with internal reference and V_{REFHI} - V_{REFLO} for external reference.
(2) Voltages above V_{DDA} + 0.3 V or below V_{SS} - 0.3 V applied to an analog input pin may temporarily affect the conversion of another pin. To avoid this, the analog inputs should be kept within these limits.
(3) VREFLO is always connected to V_{SSA} on the 64-pin PAG device.

6.11.10.1 Internal Temperature Sensor

Table 6-36. Temperature Sensor Coefficient

PARAMETER[1]		MIN	TYP	MAX	UNIT
T_Δ	Degrees C of temperature movement per measured ADC LSB change of the temperature sensor		0.18[2][3]		°C/LSB

(1) Temperature Coefficient given in terms of ADC LSB using the internal reference of the ADC.
(2) ADC temperature coeffieicient is accounted for in this specification
(3) Output of the temperature sensor (in terms of LSBs) is sign-consistent with the direction of the temperature movement. Increasing temperatures will give increasing ADC values relative to an initial value; decreasing temperatures will give decreasing ADC values relative to an initial value.

6.11.10.2 ADC Power-Up Control Bit Timing

Table 6-37. ADC Power-Up Delays

PARAMETER[1]		MIN	TYP	MAX	UNIT
$t_{d(PWD)}$	Delay time for the ADC to be stable after power up			1	ms

(1) Timings maintain compatibility to the ADC module. The 2802x ADC supports driving all 3 bits at the same time $t_{d(PWD)}$ ms before first conversion.
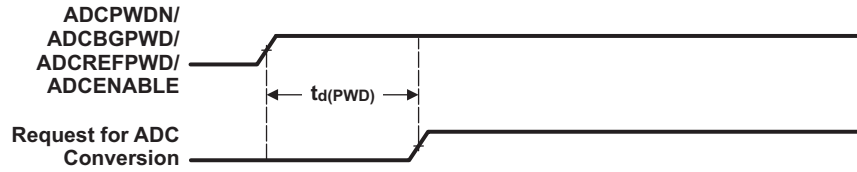
Figure 6-22. ADC Conversion Timing

6.11.10.2.1 ADC Sequential and Simultaneous Timings
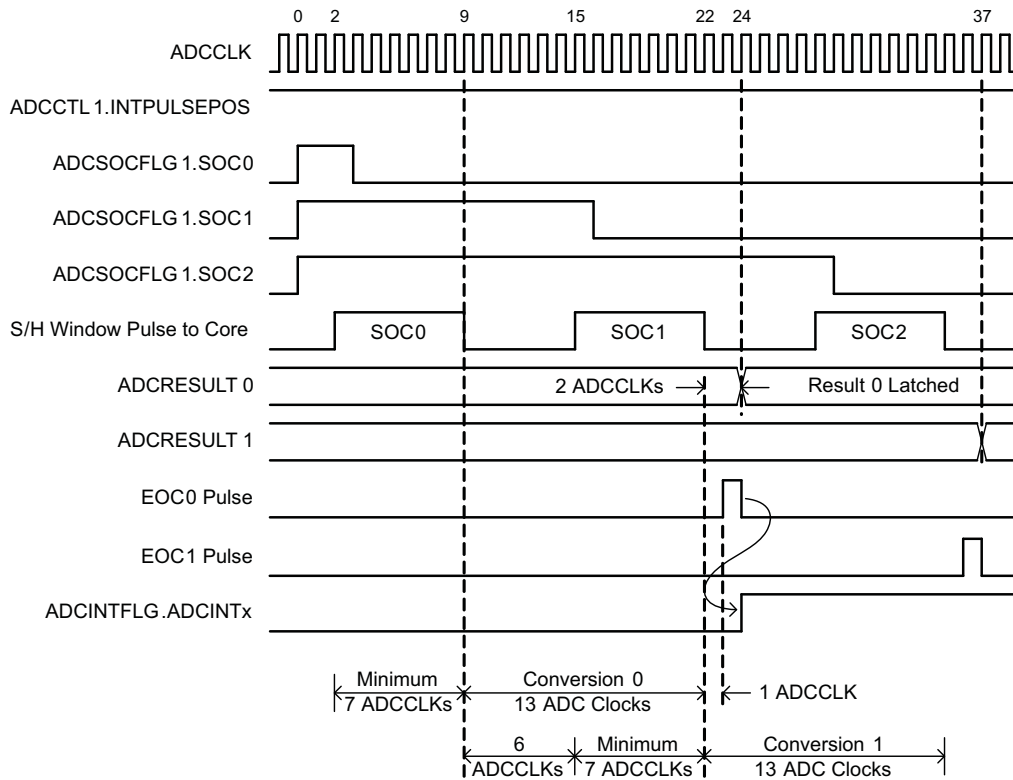
Figure 6-23. Timing Example For Sequential Mode / Late Interrupt Pulse

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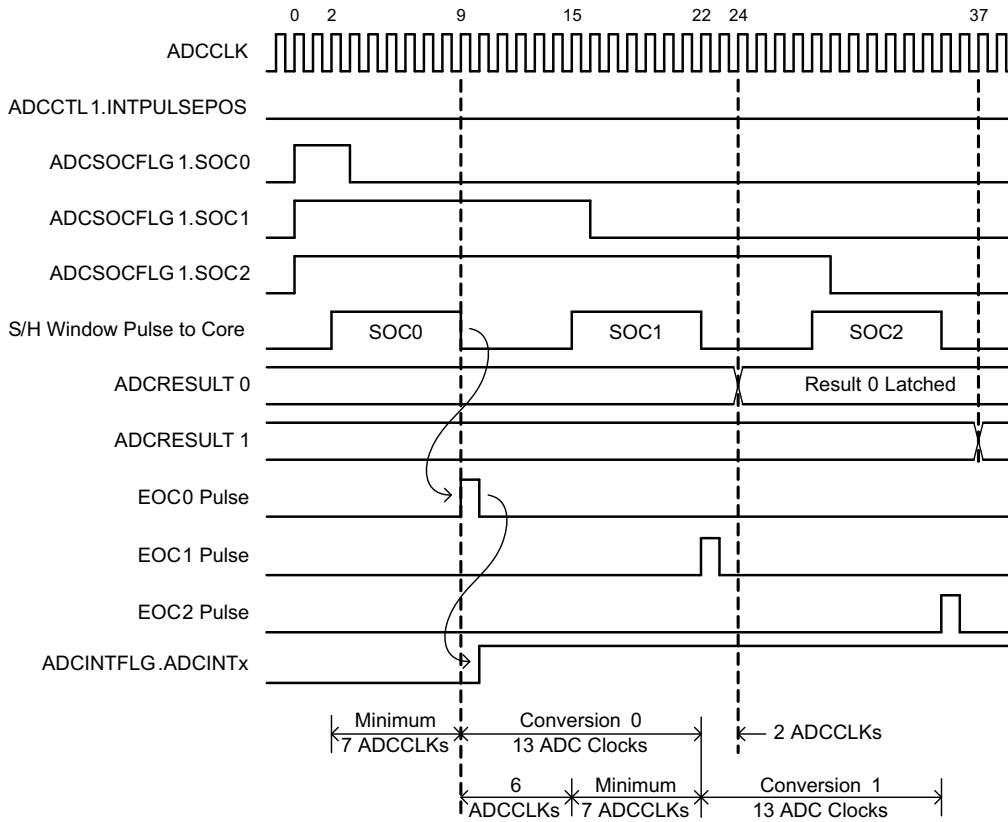
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Figure 6-24. Timing Example For Sequential Mode / Early Interrupt Pulse
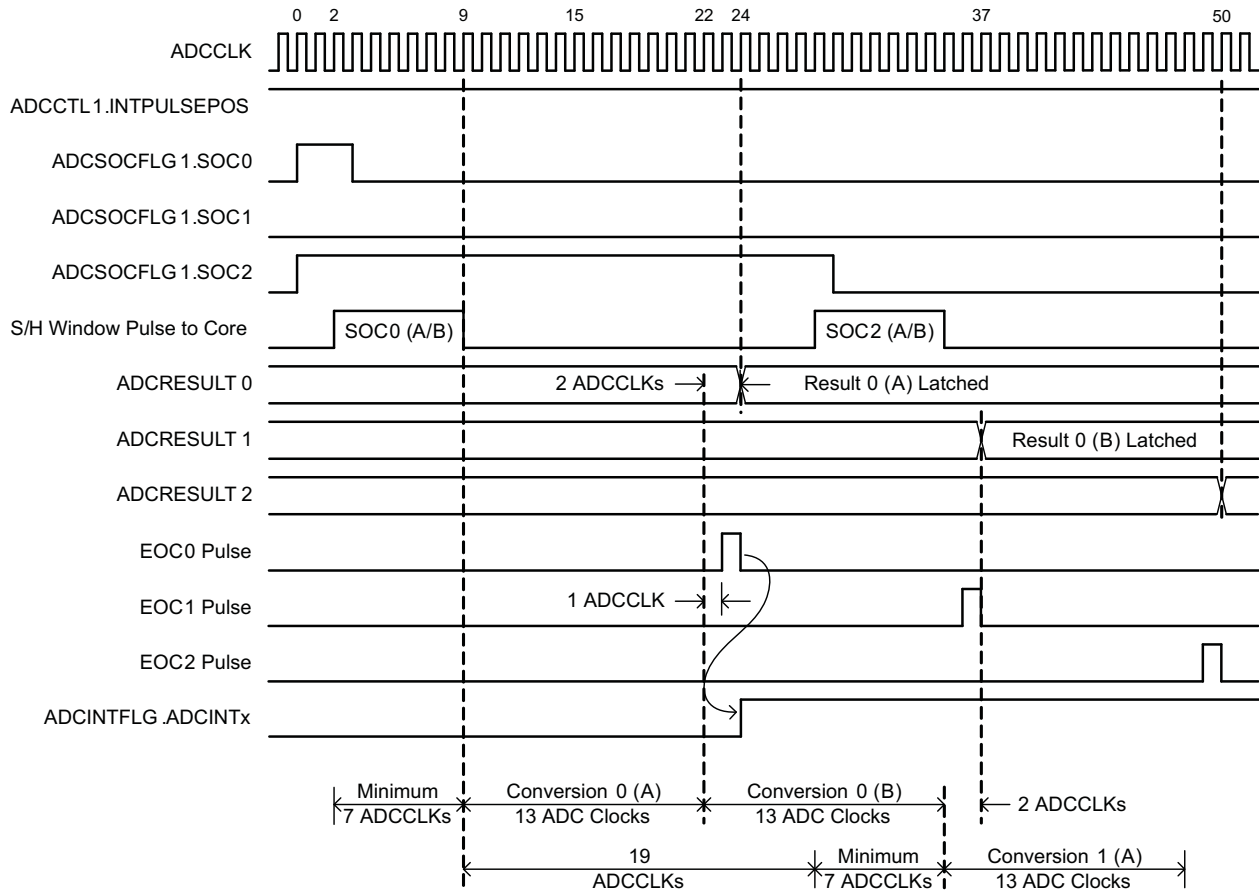
Figure 6-25. Timing Example For Simultaneous Mode / Late Interrupt Pulse

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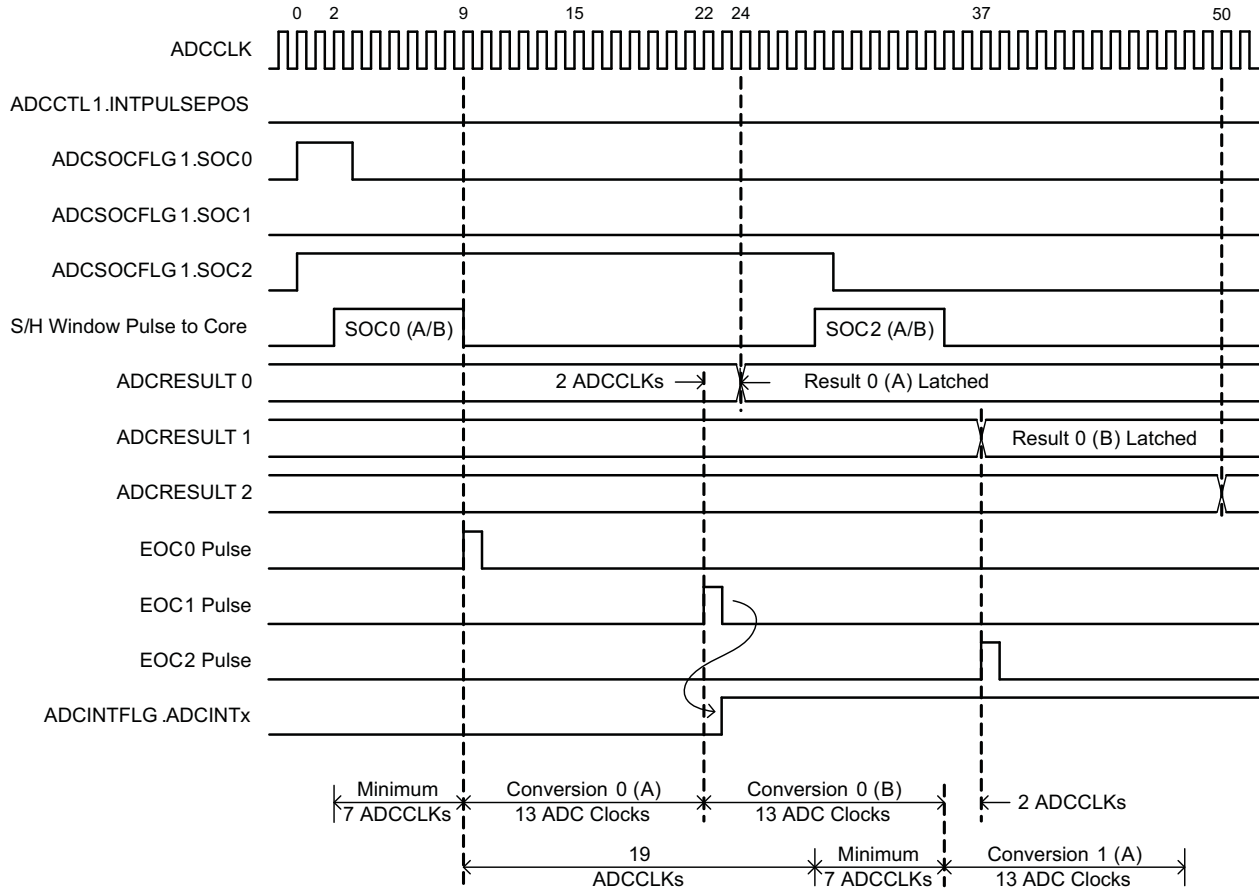
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Figure 6-26. Timing Example For Simultaneous Mode/Early Interrupt Pulse

6.12 Detailed Descriptions

Integral Nonlinearity

Integral nonlinearity refers to the deviation of each individual code from a line drawn from zero through full scale. The point used as zero occurs one-half LSB before the first code transition. The full-scale point is defined as level one-half LSB beyond the last code transition. The deviation is measured from the center of each particular code to the true straight line between these two points.

Differential Nonlinearity

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. A differential nonlinearity error of less than ±1 LSB ensures no missing codes.

Zero Offset

The major carry transition should occur when the analog input is at zero volts. Zero error is defined as the deviation of the actual transition from that point.

Gain Error

The first code transition should occur at an analog value one-half LSB above negative full scale. The last transition should occur at an analog value one and one-half LSB below the nominal full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

Signal-to-Noise Ratio + Distortion (SINAD)

SINAD is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

Effective Number of Bits (ENOB)

For a sine wave, SINAD can be expressed in terms of the number of bits. Using the following formula, $N = \dfrac{(\text{SINAD} - 1.76)}{6.02}$ it is possible to get a measure of performance expressed as N, the effective number of bits. Thus, effective number of bits for a device for sine wave inputs at a given input frequency can be calculated directly from its measured SINAD.

Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of the first nine harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

Spurious Free Dynamic Range (SFDR)

SFDR is the difference in dB between the rms amplitude of the input signal and the peak spurious signal.

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7 Revision History

This data sheet revision history highlights the technical changes made to the SPRS584 device-specific data sheet to make it an SPRS584A revision.

Scope: Added Section 6.11.5, ADC Start-of-Conversion Timing.

Added Section 6.11.10.1, Internal Temperature Sensor.

See table below.

LOCATION	ADDITIONS, DELETIONS, AND MODIFICATIONS
Section 1.1	Features: • Added "On-Chip Temperature Sensor" feature
Table 2-1	Hardware Features: • Added "Temperature Sensor" row to "12-Bit ADC" FEATURE
Figure 3-2	28034/28035 Memory Map: • Updated memory map from 0x3D 7C80 to 0x3D 8000
Figure 3-3	28032/28033 Memory Map: • Updated memory map from 0x3D 7C80 to 0x3D 8000
Table 3-9	Device Emulation Registers: • PARTID: Changed ADDRESS RANGE from 0x3D 7FFF to 0x3D 7E80 • Added footnote
Section 5.1	Device and Development Support Tool Nomenclature: • Changed example of temperature range from "S" to "T"
Figure 5-1	Device Nomenclature: • Changed example of temperature range from "S" to "T"
Section 6.11	Enhanced Control Peripherals: • Added Section 6.11.5, ADC Start-of-Conversion Timing

Table 6-35	ADC Electrical Characteristics (over recommended operating conditions):
	• V_{REFLO} input voltage:
	   – Changed MIN value from 0 V to V_{SSA}
	   – Changed MAX value from 0.6 V to 0.66 V
	• V_{REFHI} input voltage:
	   – Added MIN value of 2.64 V
	   – Added MAX value of V_{DDA}

Section 6.11.10.1	Added "Internal Temperature Sensor" section

PRODUCT PREVIEW

8 Mechanicals

The mechanical package diagram(s) that follow the tables reflect the most current released mechanical data available for the designated device(s).

PRODUCT PREVIEW

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TMX320F28035PAGT	ACTIVE	TQFP	PAG	64	1	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TMX320F28035PNT	ACTIVE	LQFP	PN	80	1	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PN (S-PQFP-G80)   **PLASTIC QUAD FLATPACK**

0,50

0,27
0,17

$\oplus$ | 0,08 Ⓜ

60   41

61   40

80   21

1   20

9,50 TYP

12,20
11,80 SQ

14,20
13,80 SQ

1,45
1,35

1,60 MAX

0,13 NOM

Gage Plane

0,25

0,05 MIN

0°−7°

0,75
0,45

Seating Plane

0,08

4040135 / B 11/96

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Falls within JEDEC MS-026

PAG (S-PQFP-G64)   **PLASTIC QUAD FLATPACK**

0,50

$\dfrac{0,27}{0,17}$

⊕ | 0,08 Ⓜ

48   33

49   32

64   17

1   16

7,50 TYP

$\dfrac{10,20}{9,80}$ SQ

$\dfrac{12,20}{11,80}$ SQ

$\dfrac{1,05}{0,95}$

1,20 MAX

Seating Plane

⌒ | 0,08

0,13 NOM

Gage Plane

0,25

0,05 MIN

0°–7°

$\dfrac{0,75}{0,45}$

4040282/C 11/96

NOTES: A. All linear dimensions are in millimeters.
          B. This drawing is subject to change without notice.
          C. Falls within JEDEC MS-026

IMPORTANT NOTICE