2-Line BUS-Port ESD-Protection - Flow Through Design

Features

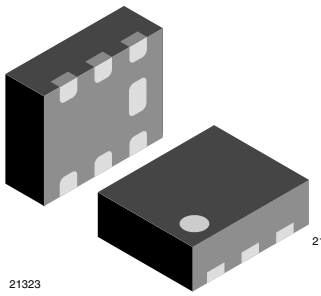
- Compact LLP1713-7L package
- Low package height < 0.6 mm
- 2-line ESD-protection
- Low leakage current I_R < 0.1 µA
- Low load capacitance C_D = 0.8 pF
- Ideal for high speed data line like
  - HDMI, DisplayPort, eSATA
  - USB, 1394/firewire
- ESD-protection acc. IEC 61000-4-2
  - ± 15 kV contact discharge
  - ± 15 kV air discharge
- Soldering can be checked by standard vision inspection. No X-ray necessary
- Lead (Pb)-free component
- Pin plating SN (e3) = pure tin
- Component in accordance to RoHS 2002/95/EC and WEEE 2002/96/EC

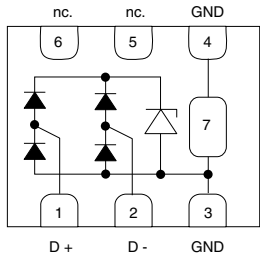
Pb-free

e3

RoHS COMPLIANT

GREEN (5-2008)**





Marking (example only)

20719

Dot = Pin 1 marking
Y = Type code (see table below)
XX = Date code

Ordering Information

Device name	Ordering code	Taped units per reel (8 mm tape on 7" reel)	Minimum order quantity
VBUS052CD-FAH	VBUS052CD-FAH-GS08	3000	15 000

Package Data

Device name	Package name	Type code	Weight	Molding compound flammability rating	Moisture sensitivity level	Soldering conditions
VBUS052CD-FAH	LLP1713-7L	G	3.7 mg	UL 94 V-0	MSL level 1 (according J-STD-020)	260 °C/10 s at terminals

Absolute Maximum Ratings

Rating	Test conditions	Symbol	Value	Unit
Peak pulse current	Acc. IEC 61000-4-5; t_p = 8/20 µs; single shot	I_{PPM}	3.5	A
Peak pulse power	Acc. IEC 61000-4-5; t_p = 8/20 µs; single shot	P_{PP}	63	W
ESD immunity	Contact discharge acc. IEC 61000-4-2; 10 pulses	V_{ESD}	± 15	kV
	Air discharge acc. IEC 61000-4-2; 10 pulses	V_{ESD}	± 15	kV
Operating temperature	Junction temperature	T_J	- 40 to + 125	°C
Storage temperature	Storage temperature	T_{STG}	- 55 to + 150	°C

** Please see document “Vishay Green and Halogen-Free Definitions (5-2008)” www.vishay.com/doc?99902

Electrical Characteristics

Ratings at 25 °C, ambient temperature unless otherwise specified

VBUS052CD-FAH

Pin 1 or 2 to pin 3

Parameter	Test conditions/remarks	Symbol	Min.	Typ.	Max.	Unit
Protection paths	Number of lines which can be protected	N_{lines}			2	lines
Reverse working voltage	at I_R = 0.1 µA	V_{RWM}	5			V
Reverse current	at $V_R = V_{RWM}$ = 5 V	I_R		< 0.01	0.1	µA
Reverse break down voltage	at I_R = 1 mA	V_{BR}	6.9	7.9	8.7	V
Clamping voltage	at I_{PP} = 1 A; acc. IEC 61000-4-5	V_C		10	12	V
	at I_{PP} = 3.5 A; acc. IEC 61000-4-5	V_C		15	18	V
Forward clamping voltage	at I_F = 1 A; acc. IEC 61000-4-5	V_F		1.9	2.4	V
	at I_F = 3.5 A; acc. IEC 61000-4-5	V_F		4	5	V
Line capacitance	at V_R = 0 V; f = 1 MHz	C_D		0.8	1	pF

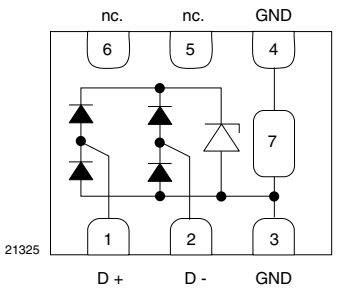
Application Note:

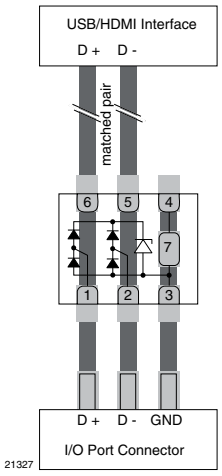
The **VBUS052CD-FAH** is a two-line ESD-protection device with the characteristic of a Z-diode with a high ESD-immunity and a very low capacitance which makes it usable for high frequency applications like USB2.0 or HDMI.

With the **VBUS052CD-FAH** two high speed data lines can be protected against transient voltage signals like ESD (Electro Static Discharge). Connected to the data line (pin 1 and pin 2) and to ground (pin 3) negative transients will be clamped close below the ground level while positive transients will be clamped close above the 5 V working range. The clamping behaviour of the **VBUS052CD-FAH** is bidirectional but asymmetrical (**BiAs**) and so it offers the best protection for applications running up to 5 V.

Pin configuration:

- Pin 3, 4 and 7 are internally shorted and have to be connected to ground
- Pin 1 and 2 are the inputs for the data lines D + and D -
- Pin 5 and 6 are not connected internally





Flow Through Design

Modern digital transmission lines can be clocked up to 480 Mbit/s (USB2.0) or 1.65 Gbit/s (HDMI).

At such high data rates the transmission lines like cables or the line traces on the PCBs have to be very homogeneous regarding their surge impedance. This requires well defined trace dimensions as trace width and distance which have to be calculated depending on the requested surge impedance (e.g. 50 Ω) and the PCB material and layer dimensions. Any device connected to the data lines - like ESD-protection devices - have to be connected with minimal changes in these trace dimensions and distances.

With the package in the so called "Flow Through Design" this is possible. The lines are running straight along the PCB while the VBUS052CD-FAH is placed on top without any vias or loops.

Typical Characteristics

T_{amb} = 25 °C, unless otherwise specified

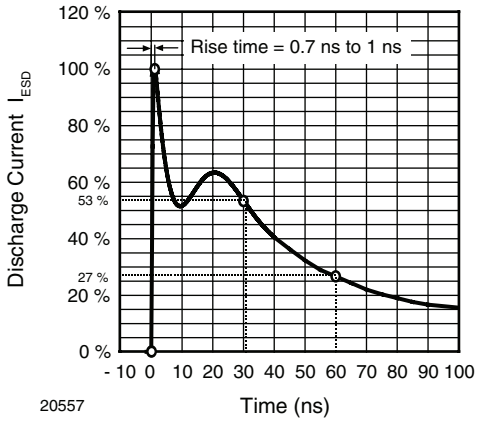


Figure 1. ESD Discharge Current Wave Form acc. IEC 61000-4-2 (330 Ω/150 pF)

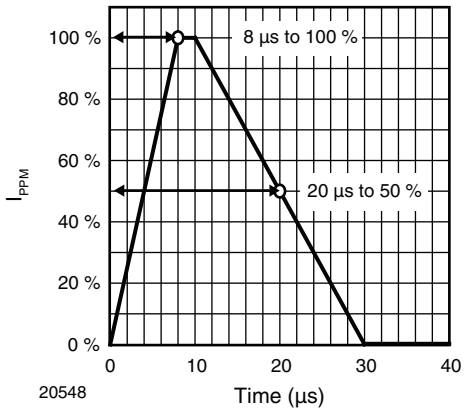


Figure 2. 8/20 µs Peak Pulse Current Wave Form acc. IEC 61000-4-5

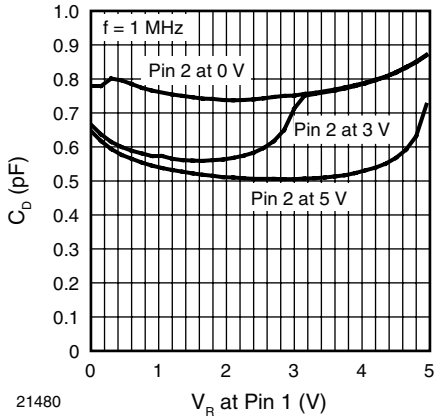


Figure 3. Typical Capacitance C_D vs. Reverse Voltage V_R

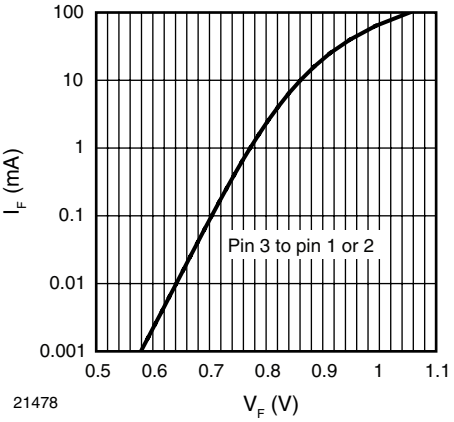


Figure 4. Typical Forward Current I_F vs. Forward Voltage V_F

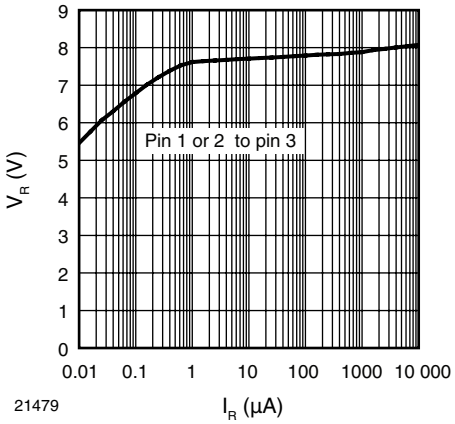


Figure 5. Typical Reverse Voltage V_R vs. Reverse Current I_R

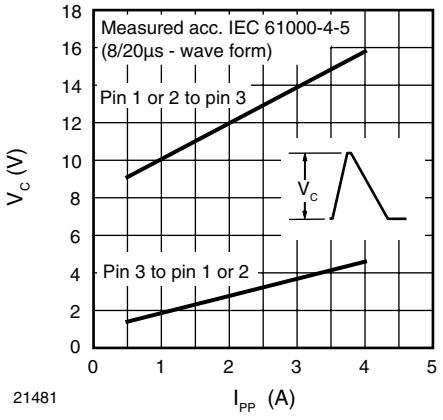


Figure 6. Typical Peak Clamping Voltage vs. Peak Pulse Current I_{PP}

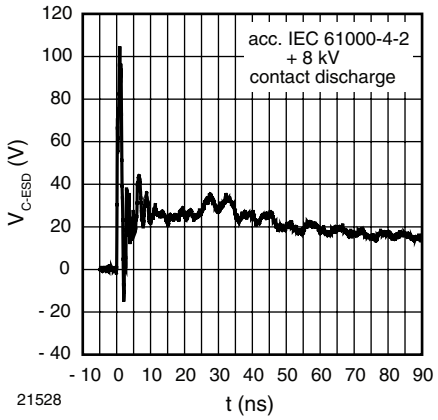


Figure 7. Typical Clamping Performance at + 8 kV Contact Discharge (acc. IEC 61000-4-2)

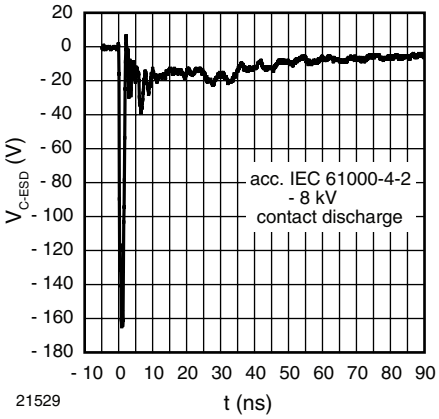


Figure 8. Typical Clamping Performance at - 8 kV Contact Discharge (acc. IEC 61000-4-2)

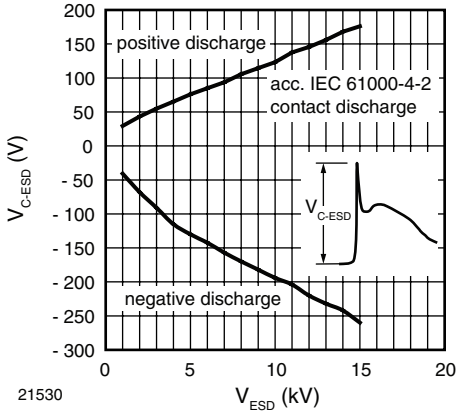
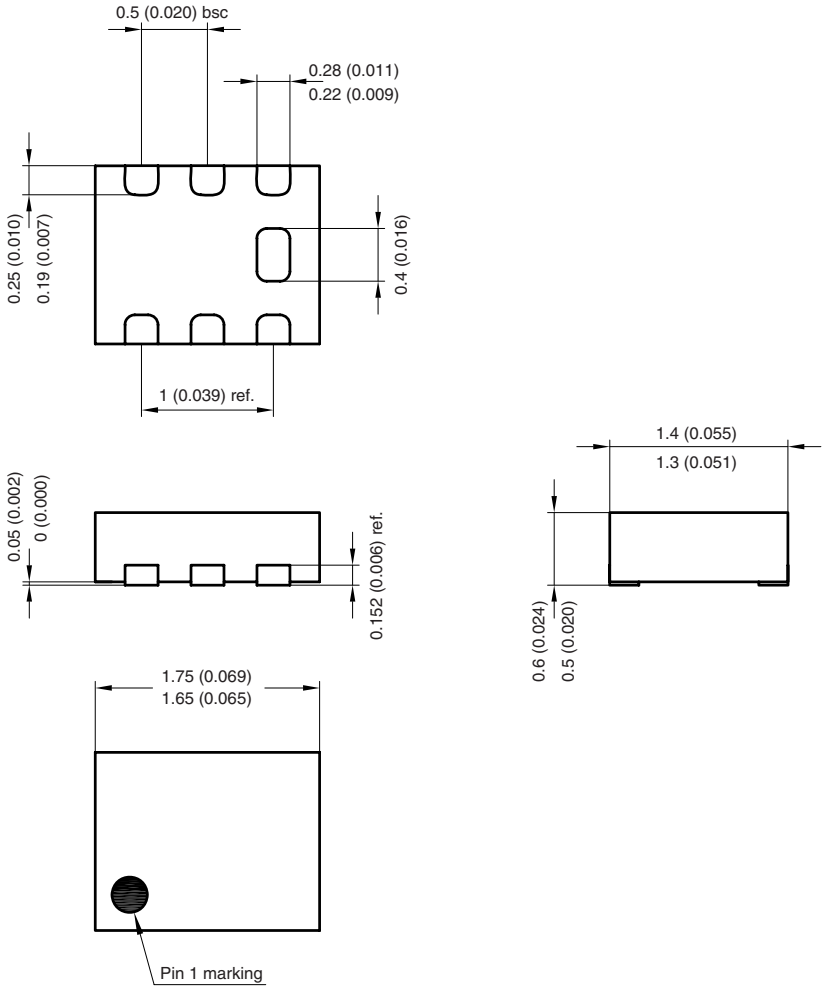
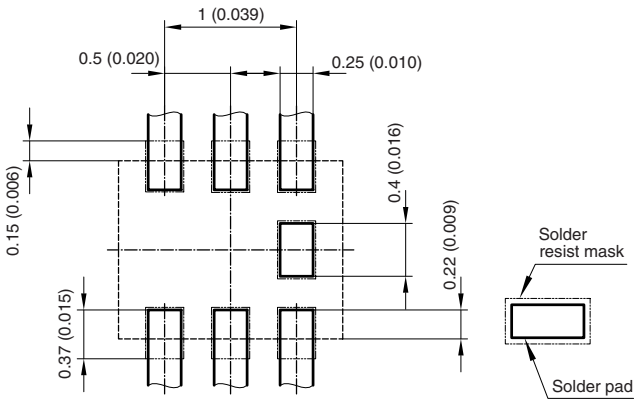


Figure 9. Typical Peak Clamping Voltage at ESD Contact Discharge (acc. IEC 61000-4-2)

Package Dimensions in millimeters (inches): **LLP1713-7L**



Foot print recommendation:



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