CYF1018V
CYF1036V
CYF1072V

18/36/72-Mbit Programmable 2-Queue FIFOs

Features

- Memory organization
  - Industry's largest first in first out (FIFO) memory densities: 18-Mbit, 36-Mbit, 72-Mbit
  - Selectable memory organization: × 9, × 12, × 16, × 18, × 20, × 24, × 32, × 36
- Up to 100-MHz clock operation
- Unidirectional operation
- Independent read and write ports
  - Supports simultaneous read and write operations
  - Reads and writes operate on independent clocks upto a maximum clock ratio of 2, enabling data buffering across clock domains
  - Supports multiple I/O voltage standard: Low voltage complementary metal oxide semiconductor (LVCMOS) 3.3 V and 1.8 V voltage standards.
- Output enable control for read skip operations
- User configured two-Queue operating mode
- Mark and retransmit: resets read pointer to user marked position
- Empty and full status flags
- Flow-through mailbox register to send data from input to output port, bypassing the FIFO sequence
- Configure programmable flags and registers through serial or parallel modes
- Separate serial clock (SCLK) input for serial programming
- Master reset to clear entire FIFO
- Joint test action group (JTAG) port provided for boundary scan function
- Industrial temperature range: –40 °C to +85 °C

Functional Description

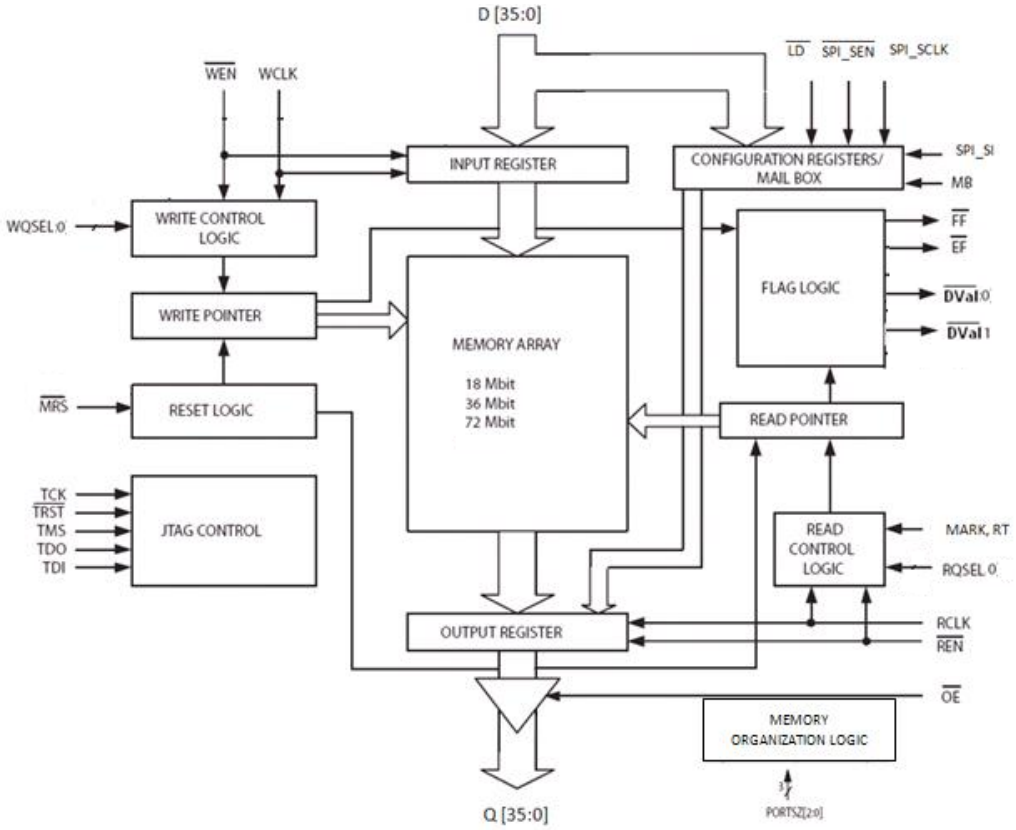
The Cypress programmable FIFO family offers the industry's highest-density programmable FIFO memory device. It has independent read and write ports, which can be clocked up to 100 MHz. User can configure input and output bus sizes. The maximum bus size of 36 bits enables a maximum data throughput of 3.6 Gbps. The read and write ports can support multiple I/O voltage standards. The user-programmable registers enable user to configure the device operation as desired. The device also offers a simple and easy-to-use interface to reduce implementation and debugging efforts, improve time-to-market, and reduce engineering costs. This makes it an ideal memory choice for a wide range of applications including multiprocessor interfaces, video and image processing, networking and telecommunications, high-speed data acquisition, or any system that needs buffering at very high speeds across different domains.

As implied by the name, the functionality of the FIFO is such that the data is read out of the read port in the same sequence in which it was written into the write port. The data is sequentially written into the FIFO from the write port. If the writes and inputs are enabled, the data on the write port gets written into the device at the rising edge of the write clock. Enabling the reads and outputs fetches data on the read port at every rising edge of the read clock. Both reads and writes can occur simultaneously at different speeds provided the ratio of read to write clock is between 0.5 and 2. Appropriate flags are set whenever the FIFO is empty or full.

The device also supports two-Queue operation, mark and retransmit of data, and a flow-through mailbox register.

All product features and specs are common to all densities (CYF1072V, CYF1036V, and CYF1018V) unless otherwise specified. All descriptions are given assuming the device is CYF1072V operated in × 36 mode. They hold good for other densities (CYF1036V, and CYF1018V) and all port sizes × 9, ×12, × 16, × 18, × 20, × 24 and × 32 unless otherwise specified. the only difference will be in the input and output bus width. Table 1 on page 8 shows the part of bus with valid data from D[35:0] and Q[35:0] in × 9, × 12, × 16, × 18, × 20, × 24, × 32 and × 36 modes.

Logic Block Diagram



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Pin Diagram for CYF1XXXV

Figure 1. 209-ball FBGA (Top View)

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{FF}$	D0	D1	WQSEL0	PORTSZ0	PORTSZ1	DNU	RQSEL0	RT	Q0	Q1
B	$\overline{EF}$	D2	D3	DNU	DNU	PORTSZ2	DNU	DNU	$\overline{REN}$	Q2	Q3
C	D4	D5	$\overline{WEN}$	DNU	VCC1	DNU	VCC1	DNU	RCLK	Q4	Q5
D	D6	D7	VSS	VCC1	DNU	$\overline{LD}$	DNU	VCC1	VSS	Q6	Q7
E	D8	D9	VCC2	VCC2	VCCIO	VCCIO	VCCIO	VCC2	VCC2	Q8	Q9
F	D10	D11	VSS	VSS	VSS	DNU	VSS	VSS	VSS	Q10	Q11
G	D12	D13	VCC2	VCC2	VCCIO	VCC1	VCCIO	VCC2	VCC2	Q12	Q13
H	D14	D15	VSS	VSS	VSS	VCC1	VSS	VSS	VSS	Q14	Q15
J	D16	D17	VCC2	VCC2	VCCIO	VCC1	VCCIO	VCC2	VCC2	Q16	Q17
K	DNU	DNU	WCLK	DNU	VSS	DNU	VSS	DNU	VCCIO	VCCIO	VCCIO
L	D18	D19	VCC2	VCC2	VCCIO	VCC1	VCCIO	VCC2	VCC2	Q18	Q19
M	D20	D21	VSS	VSS	VSS	VCC1	VSS	VSS	VSS	Q20	Q21
N	D22	D23	VCC2	VCC2	VCCIO	VCC1	VCCIO	VCC2	VCC2	Q22	Q23
P	D24	D25	VSS	VSS	VSS	$\overline{SPI\_SEN}$	VSS	VSS	VSS	Q24	Q25
R	D26	D27	VCC2	VCC2	VCCIO	VCCIO	VCCIO	VCC2	VCC2	Q26	Q27
T	D28	D29	VSS	VCC1	VCC1	SPI_SI	VCC1	VCC1	VSS	Q28	Q29
U	$\overline{DVal0}$	DNU	D30	D31	DNU	DNU [1]	SPI_SCLK	Vref	$\overline{OE}$	Q30	Q31
V	DNU	DNU	D32	D33	DNU	$\overline{MRS}$	MB	DNU	MARK	Q32	Q33
W	TDO	$\overline{DVal1}$	D34	D35	TDI	$\overline{TRST}$	TMS	TCK	Vref	Q34	Q35

Note
1. This pin should be tied to V_{SS} preferably or can be left floating to ensure normal operation.

Pin Definitions

Pin Name	I/O	Pin Description
D[35:0]	Input	Data inputs: Data inputs for a 36-bit bus.
Q[35:0]	Output	Data outputs: Data outputs for a 36-bit bus.
$\overline{WEN}$	Input	Write enable: $\overline{WEN}$ enables WCLK to write data into the FIFO memory and configuration registers.
$\overline{REN}$	Input	Read enable: $\overline{REN}$ enables RCLK to read data from the FIFO memory and configuration registers.
$\overline{OE}$	Input	Output enable: When $\overline{OE}$ is LOW, FIFO data outputs are enabled; when $\overline{OE}$ is HIGH, the FIFO's outputs are in High Z (high impedance) state.
WCLK	Input	Write clock: When enabled by $\overline{WEN}$, the rising edge of WCLK writes data into the FIFO if $\overline{LD}$ is high and into the configuration registers if $\overline{LD}$ is low.
RCLK	Input	Read clock: When enabled by $\overline{REN}$, the rising edge of RCLK reads data from the FIFO memory if $\overline{LD}$ is high and from the configuration registers if $\overline{LD}$ is low.
$\overline{DVal0}$	Output	Data valid for Queue-0: Active low signal indicating valid data read for Queue-0 from Q[35:0].
$\overline{DVal1}$	Output	Data valid for Queue-1: Active low signal indicating valid data read for Queue-1 from Q[35:0].
$\overline{EF}$	Output	Empty flag: When $\overline{EF}$ is LOW, the Queue is empty. $\overline{EF}$ is synchronized to RCLK.
$\overline{FF}$	Output	Full flag: When $\overline{FF}$ is LOW, the Queue is full. $\overline{FF}$ is synchronized to WCLK.
$\overline{LD}$	Input	Load: When $\overline{LD}$ is LOW, D[7:0] (Q[7:0]) are written (read) into (from) the configuration registers. When $\overline{LD}$ is HIGH, D[35:0] (Q[35:0]) are written (read) into (from) the FIFO.
RT	Input	Retransmit: A HIGH pulse on RT resets the internal read pointer to a physical location of the FIFO which is marked by the user (using MARK pin). With every valid read cycle after retransmit, previously accessed data is read and the read pointer is incremented until it is equal to the write pointer.
$\overline{MRS}$	Input	Master reset: $\overline{MRS}$ initializes the read and write pointers to zero and sets the output register to all zeroes. During Master Reset, the configuration registers are all set to default values and flags are reset.
SPI_SCLK	Input	Serial clock: A rising edge on SPI_SCLK clocks the serial data present on the SPI_SI input into the offset registers if $\overline{SPI\_SEN}$ is enabled.
SPI_SI	Input	Serial input: Serial input when $\overline{SPI\_SEN}$ is enabled.
$\overline{SPI\_SEN}$	Input	Serial enable: Enables serial loading of programmable flag offsets and configuration registers.
MARK	Input	Mark for retransmit: When this pin is asserted the current location of the read pointer is marked. Any subsequent retransmit operation resets the read pointer to this position.
MB	Input	Mailbox: When asserted the reads and writes happen to flow-through mailbox register.
WQSEL0	Input	Write Queue select: select Queue-0 when low and Queue-1 when high.
RQSEL0	Input	Read Queue select: select Queue-0 when low and Queue-1 when high.
TCK	Input	Test clock (TCK) pin for JTAG.
$\overline{TRST}$	Input	Reset pin for JTAG.
TMS	Input	Test mode select (TMS) pin for JTAG.
TDI	Input	Test data in (TDI) pin for JTAG.
TDO	Output	Test data out (TDO) for JTAG.
PORTSZ [2:0]	Input	Port word size select: Port word width select pins (common for read and write ports).
V_{CC1}	Power Supply	Core voltage supply 1: 1.8 V supply voltage
V_{CC2}	Power Supply	Core voltage supply 2: 1.5 V supply voltage

Pin Definitions (continued)

Pin Name	I/O	Pin Description
V_{CCIO}	Power Supply	Supply for I/Os.
Vref	Input Reference	Reference voltage: Reference voltage (regardless of I/O standard used)
V_{SS}	Ground	Ground
DNU	–	Do not use: These pins need to be left floating.

Architecture

The CYF1072V, CYF1036V, and CYF1018V are of memory arrays of 72-Mbit, 36-Mbit, and 18-Mbit respectively. The memory organization is user configurable and word sizes can be selected as × 9, × 12, × 16, × 18, × 20, × 24, × 32, or × 36. The logic blocks to implement FIFO functionality and the associated features are built around these memory arrays.

The input and output data buses have a maximum width of 36 bits configurable through PORTSZ[2:0]. The input data bus goes to an input register and the data flow from the input register to the memory is controlled by the write logic block. The inputs to the write logic block are WCLK, WEN and WQSEL0. When the writes are enabled through WEN, the data on the input bus is written into the memory array at the rising edge of WCLK. This also increments the write pointer. WQSEL0 selects the Queue for write operation.

Similarly, the output register is connected to the data output bus. Transfer of contents from the memory to the output register is controlled by the read control logic. The inputs to the read control logic include RCLK, REN, OE, RQSEL0, RT and MARK. When reads are enabled by REN and outputs are enabled through OE, the data from the memory pointed by the read pointer is transferred to the output data bus at the rising edge of RCLK along with active low Dval0 or Dval1 based on the Queue number selected using RQSEL0. If the outputs are disabled through OE but the reads enabled, the outputs are in high impedance state, but internally the read pointer is incremented. The MARK signal is used to ‘mark’ the location from which data is retransmitted when requested.

During write operation, the number of writes performed is always a even number (i.e., minimum write burst length is two and number of writes always a multiple of two), whereas during read operation, the number of reads performed can be even or odd (i.e., minimum read burst length is one).

By default, the FIFO is accessed as a single Queue device. It is possible to divide the whole memory space into 2 equal sized array, and each array can be independently accessed as an independent FIFO. This is like having two independent Queues inside the FIFO instead of entire memory space acting as single Queue FIFO. User can configure the number of Queues by setting the value of D0 of configuration register 3(refer Table 3 on page 9). Table 2 on page 8 shows the value to be set in D0 of configuration register 3 to configure the device in single-Queue or two-Queue mode.

Reset Logic

The Master Reset ($\overline{MRS}$) initializes the read and write pointers to zero, sets the output registers to all zeros and sets the status of the flags to $\overline{FF}$ deasserted and $\overline{EF}$ asserted. $\overline{MRS}$ also resets the configuration register and the mark address to their default values. $\overline{MRS}$ affects all the Queues in the FIFO. A $\overline{MRS}$ is required after power up before accessing the FIFO. After $\overline{MRS}$, a minimum latency of 1024 clocks is necessary before the first access. The word size is configured through pins; values of the three PORTSZ pins are latched during rising edge of $\overline{MRS}$. After $\overline{MRS}$, the device is configured in single Queue mode by default.

Flag Operation

This device provides two flag pins to indicate the condition of the FIFO contents.

Full Flag

The Full Flag ($\overline{FF}$) goes LOW when the device is full. All write operations are ignored whenever $\overline{FF}$ is LOW regardless of the state of $\overline{WEN}$. $\overline{FF}$ is synchronized to WCLK, that is, it is exclusively updated by each rising edge of WCLK. In 2Q mode, $\overline{FF}$ indicates the status of the Queue selected by WQSEL0.The worst case assertion latency for Full Flag is four. As the user cannot know that the FIFO is full for four clock cycles, it is possible that user continues writing data during this time. In this case, the four data word written will be stored to prevent data loss and these words have to be read back in order for full flag to get de-asserted. The minimum number of reads required to de-assert full-flag is two and the maximum number of reads required to de-assert full flag is six. The assertion and de-assertion of full flag with associated latencies is explained in Latency Table on page 14.

Empty Flag

The Empty Flag ($\overline{EF}$) goes LOW when the device is empty. Read operations are ignored whenever $\overline{EF}$ is LOW, regardless of the state of REN. $\overline{EF}$ is synchronized to RCLK, i.e., it is exclusively updated by each rising edge of RCLK. In 2Q mode, $\overline{EF}$ indicates the status of the Queue selected by RQSEL0. The assertion and de-assertion of empty flag with associated latencies is explained in Latency Table on page 14.

Retransmit from Mark Operation

The retransmit feature is useful for transferring packets of data repeatedly. It enables the receipt of data to be acknowledged by the receiver and retransmitted if necessary. The retransmit feature is used when the number of writes equal to or less than the depth of the FIFO has occurred – and at least one word has been read since the last reset cycle. A HIGH pulse on RT resets the internal read pointer to a physical location of the FIFO that is marked by the user (using the MARK pin). In 2-Queue mode the MARK and RT signals are validated with RQSEL0, i.e., Mark or Retransmit function will be performed for the Queue that is selected by RQSEL0. With every valid read cycle after retransmit, previously accessed data is read and the read pointer is incremented until it is equal to the write pointer. Flags are governed by the relative locations of the read and write pointers and are updated during a retransmit cycle. Data written to FIFO after activation of RT are also transmitted. The full depth of the FIFO can be repeatedly retransmitted. To mark a location, the Mark pin is asserted when reading that particular location.

Flow-through mailbox Register

This feature transfers data from input to output directly by bypassing the FIFO sequence. When MB signal is asserted the data present in D[35:0] will be available at Q[35:0] after two WCLK cycles. Normal read and write operations are not allowed during flow-through mailbox operation. Before starting Flow-through mailbox operation FIFO read should be completed to make data valid (DVal0/DVal1) high in order to avoid data loss from FIFO. The width of flow-through mailbox register always corresponds to port size.

Selecting Word Sizes

The word sizes are configured based on the logic levels on the PORTSZ pins during the master reset (MRS) cycle only (latched on low to high edge). The port size cannot be changed during normal mode of operation and these pins are ignored. Table 1. explains the pins of D[35:0] and Q[35:0] that will have valid data in modes where the word size is less than × 36. If word size is less than × 36, the unused output pins are tri-stated by the device and unused input pins will be ignored by the internal logic. The pins with valid data input D[N:0] and output Q[N:0] is given in Table 1.

Data Valid Signal

Data valid ($\overline{Dval0}$, $\overline{Dval1}$) are active low signals provided for easy capture of output data. When a read operation is performed, the DVal0/DVal1 signal goes low along with output data indicating valid data on Q bus for either Queue-0 or Queue-1. This helps to capture the data without keeping track of $\overline{REN}$ and RQSEL0 to data output latency. These signals also help to capture the output data when write and read operations are performed continuously at different frequencies by indicating when valid data is read out at the output port Q[35:0].

Power Up

The device becomes functional after V_{CC1}, V_{CC2}, V_{CCIO}, and Vref attain minimum stable voltage required as given in Recommended DC Operating Conditions on page 13. The device can be accessed t_{PU} time after these supplies attain the minimum required level
(see Switching Characteristics on page 15). There is no power sequencing requirement for the device.

Table 1. Word Size Selection

PORTSZ[2:0]	Word Size	Active input data pins D[X:0]	Active output data pins Q[X:0]
000	× 9	D[8:0]	Q[8:0]
001	× 12	D[11:0]	Q[11:0]
010	× 16	D[15:0]	Q[15:0]
011	× 18	D[17:0]	Q[17:0]
100	× 20	D[19:0]	Q[19:0]
101	× 24	D[23:0]	Q[23:0]
110	× 32	D[31:0]	Q[31:0]
111	× 36	D[35:0]	Q[35:0]

Table 2. Multi-Queue Configuration

operating mode	RQSEL0/WQSEL0	Queue Number Selected
1Q mode register 0x3[0] = 0	0	0
	1	invalid
2Q mode register 0x3[0] = 1	0	0
	1	1

Read Skip Operation

As mentioned in Architecture on page 7, during a read operation, if the outputs are disabled by having the $\overline{OE}$ high, the read data does not appear on the output bus; however, the read pointer is incremented.

Multi-Queue Operation

In general, the entire memory space is accessed as a First In First Out (FIFO) order for the write and read operation. In this case, the entire memory space is called a single Queue. For example, for 72M device, the entire memory space is available as a single Queue FIFO operation.

In multi Queue mode, the entire memory space is divided into equal sized memory array and each individual memory array can be accessed as an independent FIFO based on additional control signals. These independent memory arrays are called as Queues. For example, when 72M device, is configured into two Queue mode, the entire memory space of 72M is divided into two 36M memory array called as Queue-0 and Queue-1. These Queues can be accessed independently as a FIFO by selecting the Queue select signals WQSEL0 and RQSEL0. In this way, two Queues can be created for a given device where data can be stored independently and read out independently.

Table 3. Configuration Registers

ADDR	Configuration Register	Default	Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
0x1	Reserved	0x00	X	X	X	X	X	X	X	X
0x2	Reserved	0x00	X	X	X	X	X	X	X	X
0x3	Number of Queues	0x00	X	X	X	X	X	X	X	D0
0x4	Reserved	0x7F	X	X	X	X	X	X	X	X
0x5	Reserved	0x00	X	X	X	X	X	X	X	X
0x6	Reserved	0x00	X	X	X	X	X	X	X	X
0x7	Reserved	0x7F	X	X	X	X	X	X	X	X
0x8	Reserved	0x00	X	X	X	X	X	X	X	X
0x9	Reserved	0x00	X	X	X	X	X	X	X	X
0xA	Fast CLK Bit Register	1XXXXXXXb	Fast CLK bit	X	X	X	X	X	X	X

Table 4. Writing and Reading Configuration Registers in Parallel Mode

$\overline{\text{SPI\_SEN}}$	$\overline{\text{LD}}$	$\overline{\text{WEN}}$	$\overline{\text{REN}}$	WCLK	RCLK	SPI_SCLK	Operation
1	0	0	1	↑ First rising edge because both LD and $\overline{\text{WEN}}$ are low	X	X	Parallel write to first register
1	0	0	1	↑ Second rising edge	X	X	Parallel write to second register
1	0	0	1	↑ Third rising edge	X	X	Parallel write to third register
1	0	0	1	↑ Fourth rising edge	X	X	Parallel write to fourth register
1	0	0	1	•	X	X	•
1	0	0	1	•	X	X	•
1	0	0	1	•	X	X	•
1	0	0	1	↑ Tenth rising edge	X	X	Parallel write to tenth register
1	0	0	1	↑ Eleventh rising edge	X	X	Parallel write to first register (roll back)
1	0	1	0	X	↑ First rising edge since both LD and $\overline{\text{REN}}$ are low	X	Parallel read from first register
1	0	1	0	X	↑ Second rising edge	X	Parallel read from second register
1	0	1	0	X	↑ Third rising edge	X	Parallel read from third register
1	0	1	0	X	↑ Fourth rising edge	X	Parallel read from fourth register
1	0	1	0	X	•	X	•
1	0	1	0	X	•	X	•
1	0	1	0	X	•	X	•
1	0	1	0	X	↑ Tenth rising edge	X	Parallel read from tenth register
1	0	1	0	X	↑ Eleventh rising edge	X	Parallel read from first register (roll back)
1	X	1	1	X	X	X	No operation

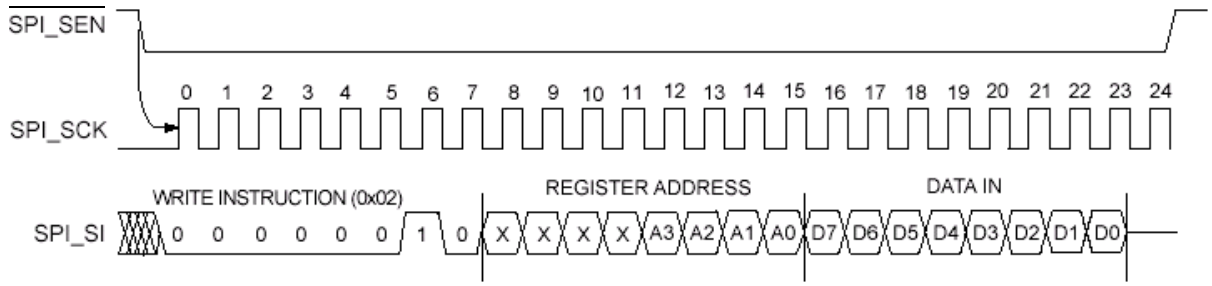
Table 4. Writing and Reading Configuration Registers in Parallel Mode (continued)

SPI_SEN	LD	WEN	REN	WCLK	RCLK	SPI_SCLK	Operation
X	1	0	X	↑ Rising edge	X	X	Write to FIFO memory
X	1	X	0	X	↑ Rising edge	X	Read from FIFO memory
0	0	X	1	X	X	X	Illegal operation

Table 5. Writing into Configuration Registers in Serial Mode

SPI_SEN	LD	WEN	REN	WCLK	RCLK	SCLK	Operation
0	1	X	X	X	X	↑ Rising edge	Each rising of the SCLK clocks in one bit from the SI (Serial In). Any of the 10 registers can be addressed and written to, following the SPI protocol.
X	1	0	X	↑ Rising edge	X	X	Parallel write to FIFO memory.
X	1	X	0	X	↑ Rising edge	X	Parallel read from FIFO memory.
1	0	1	1	X	X	X	This corresponds to parallel mode (refer to Table 4).

Figure 2. Serial WRITE to Configuration Register

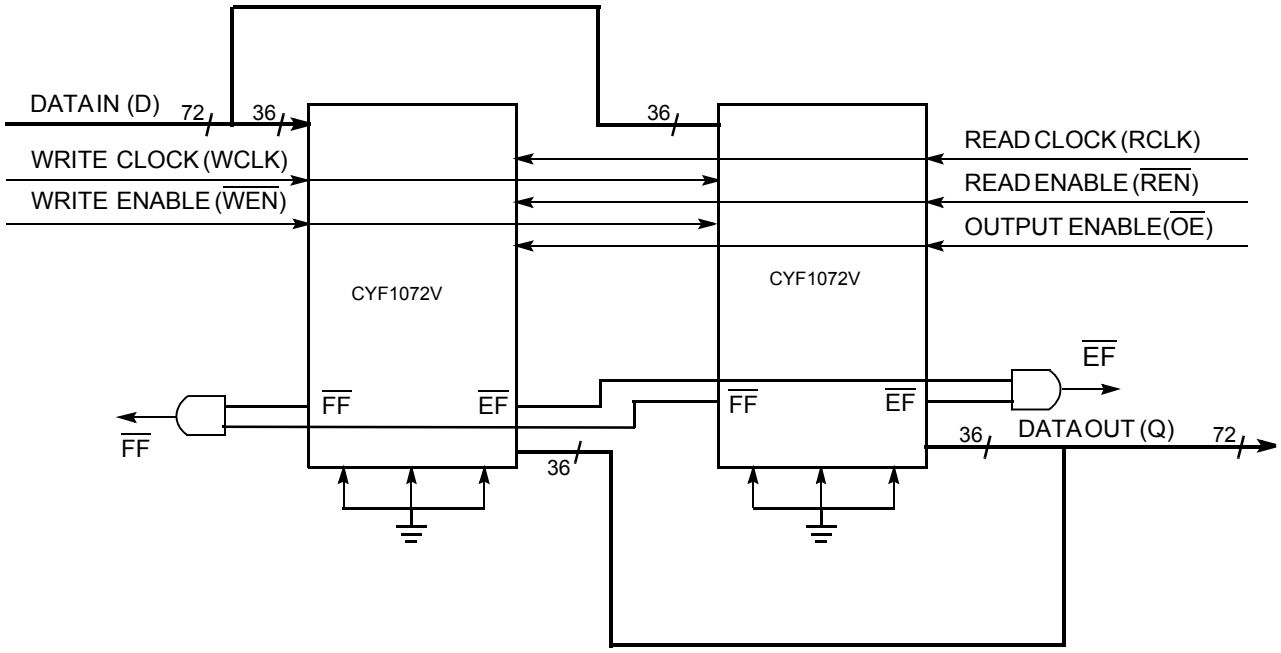


Width Expansion Configuration

The width of CYF1072V can be expanded to provide word widths greater than 36 bits. During width expansion mode, all control line inputs are common and all flags are available. Empty (Full) flags are created by ANDing the Empty (Full) flags of every FIFO.

This technique avoids reading data from or writing data to the FIFO that is “staggered” by one clock cycle due to the variations in skew between RCLK and WCLK. Figure 3 on page 11 demonstrates a 72 bit-word width by using two 36-bit word CYF1072Vs.

Figure 3. Using Two CYF1072V for Width Expansion



Memory Organization for Different Port Sizes

The 72-Mbit memory has different organization for different port sizes. Table 6 shows the depth of the FIFO for all port sizes.

Note that for all port sizes, four to eight locations are not available for writing the data and are used to safeguard against false synchronization of empty and full flags.

Table 6. Word Size Selection

PORTSZ[2:0]	Word Size	FIFO Depth	Memory Size
000	× 9	8 Meg	72 Mbit
001	× 12	4 Meg	48 Mbit
010	× 16	4 Meg	64 Mbit
011	× 18	4 Meg	72 Mbit
100	× 20	2 Meg	40 Mbit
101	× 24	2 Meg	48 Mbit
110	× 32	2 Meg	64 Mbit
111	× 36	2 Meg	72 Mbit

The memory size mentioned is when the device is configured in single-Queue mode.

Read/Write Clock Requirements

The read and write clocks must satisfy the following requirements:

- Both read (RCLK) and write (WCLK) clocks should be free-running.
- The clock frequency for both clocks should be between the minimum and maximum range given in Switching Characteristics on page 15.
- The ratio of RCLK to WCLK must be in the range of 0.5 to 2.

The device uses internal PLL to achieve high performance. Whenever there is change in the frequency of the clock, the device takes t_{PLL} time to synchronize with the input clock. (see Switching Characteristics on page 15). The PLL requires re-synchronization when there is change in the frequency of either WCLK or RCLK or when master reset is asserted.

For proper FIFO operation, the device must determine which of the input clocks – RCLK or WCLK – is faster. This is evaluated by using counters after the MRS cycle. The device uses two 10-bit counters inside (one running on RCLK and other on WCLK), which count 1,024 cycles of read and write clock after MRS. The clock of the counter which reaches its terminal count first is used as master clock inside the FIFO.

When there is change in the relative frequency of RCLK and WCLK during normal operation of FIFO, user can specify it by using “Fast CLK bit” in the configuration register (0xA).

“1” - indicates f_{req} (WCLK) > f_{req} (RCLK)

“0” - indicates f_{req} (WCLK) < f_{req} (RCLK)

The result of counter evaluated frequency is available in this register bit. User can override the counter evaluated frequency for faster clock by changing this bit.

Whenever there is a change in this bit value, user must wait t_{PLL} time before issuing the next read or write to FIFO.

JTAG operation

CYF1072V has two devices connected internally in a JTAG chain as shown in Figure 4 on page 12.

Figure 4. JTAG Operation

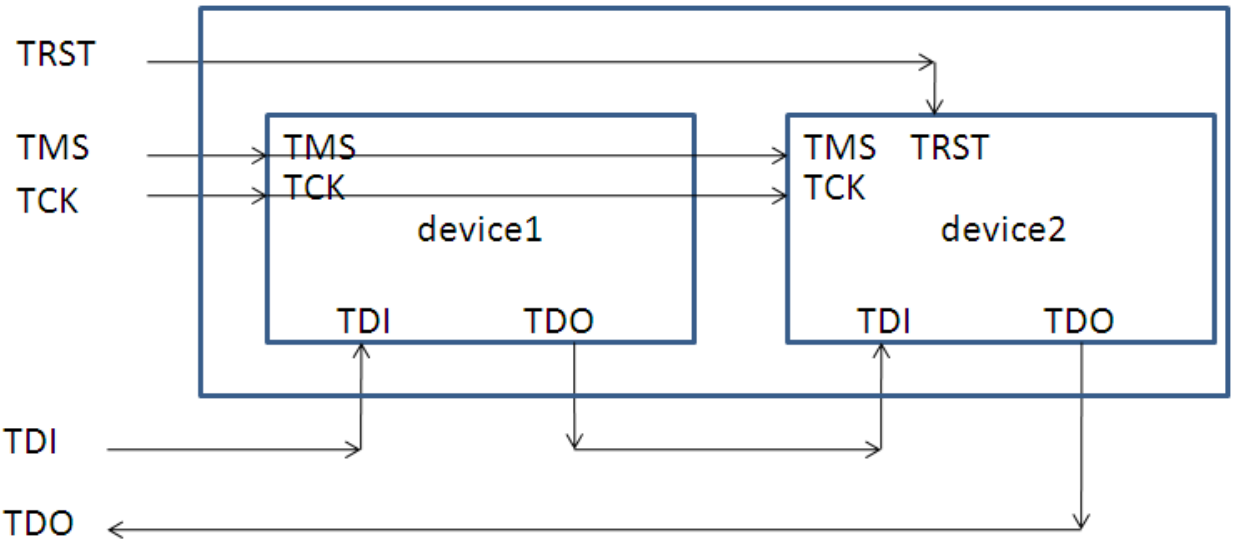


Table 7 shows the IR register length and device ID.

Table 7. JTAG IDCODES

	IR Register length	Device ID (HEX)	Bypass register length
Device-1	3	“Ignore”	1
Device-2	8	1E3261CF	1

For boundary scan, device-1 should be in bypass mode.

Table 8 and Table 9 shows the JTAG instruction set for devices 1 and 2.

Table 8. JTAG Instructions

Device-1	Opcode (Binary)
BYPASS	111

Table 9. JTAG Instructions

Device-2	Opcode (HEX)
EXTEST	00
HIGHZ	07
SAMPLE/PRELOAD	01
BYPASS	FF
IDCODE	0F

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature (without bias) ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Core supply voltage 1 (V_{CC1}) to ground potential .....–0.3 V to 2.5 V

Core supply voltage 2 (V_{CC2}) to ground potential .....–0.3 V to 1.65 V

Latch-up current ..... >100mA

I/O port supply voltage (V_{CCIO}) .....–0.3 V to 3.7 V

Voltage applied to I/O pins .....–0.3 V to 3.75 V

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage (per MIL–STD–883, Method 3015) ..... > 2001 V

Operating Range

Range	Ambient Temperature
Industrial	–40 °C to +85 °C

Recommended DC Operating Conditions

Parameter [2]	Description		Min	Typ	Max	Unit
V_{CC1}	Core supply voltage 1		1.70	1.80	1.90	V
V_{CC2}	Core supply voltage 2		1.425	1.5	1.575	V
V_{REF}	Reference voltage (irrespective of I/O standard used)		0.7	0.75	0.8	V
V_{CCIO}	I/O supply voltage, read and write banks.	LVCMOS33	3.00	3.30	3.60	V
		LVCMOS18	1.70	1.8	1.90	V

Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_{cc}	Active current	$V_{CC1} = V_{CC1MAX}$	–	–	300	mA
		$V_{CC2} = V_{CC2MAX}$, All I/O switching, 100 MHz	–	–	500	mA
		$V_{CCIO} = V_{CCIOMAX}$ (All outputs disabled)	–	–	100	mA
I_I	Input pin leakage current	$V_{IN} = V_{CCIOmax}$ to 0 V	–15	–	15	µA
I_{OZ}	I/O pin leakage current	$V_O = V_{CCIOmax}$ to 0 V	–15	–	15	µA
C_P	Capacitance for TMS and TCK	–	–	–	16	pF
C_{PIO}	Capacitance for all I/Os apart from TMS and TCK	–	–	–	8	pF

Note
2. Device operation guaranteed for a supply rate > 1 V / µs.

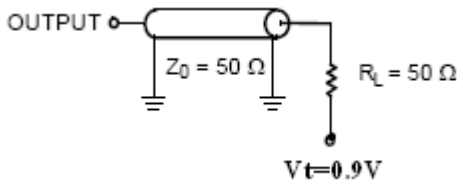
I/O Characteristics

I/O standard	Nominal I/O supply voltage	Input Voltage (V)		Output voltage (V)		Output Current (mA)	
		V_{IL}(max)	V_{IH}(min)	V_{OL}(max)	V_{OH}(min)	I_{OL}(max)	I_{OH}(max)
LVCMOS33	3.3 V	0.80	2.20	0.45	2.40	24	24
LVCMOS18	1.8 V	30% V_{CCIO}	65% V_{CCIO}	0.45	V_{CCIO} – 0.45	16	16

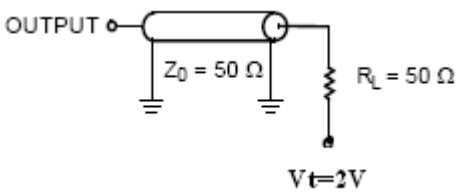
Latency Table

Latency Parameter	Number of cycles	Details
$L_{\overline{FF}\_ASSERT}$	Min = 0 Max = 4	Last data write to $\overline{FF}$ going low
$L_{\overline{EF}\_ASSERT}$	0	Last data read to $\overline{EF}$ going low
L_{RQSEL_CHANGE}	1	Minimum RCLK cycles before RQSEL0 can change
L_{WQSEL_CHANGE}	2	Minimum WCLK cycles before WQSEL0 can change
$L_{MAILBOX}$	2	Latency from write port to read port when MB = 1 (w.r.t WCLK)
$L_{\overline{REN}\_TO\_DATA}$	4	Latency when $\overline{REN}$ is asserted low to first data output from FIFO
$L_{\overline{REN}\_TO\_CONFIG}$	4	Latency when $\overline{REN}$ is asserted along with $\overline{LD}$ to first data read from configuration registers
$L_{\overline{FF}\_DEASSERT}$	7	Read to $\overline{FF}$ going high
$L_{RT\_TO\_\overline{REN}}$	9	RT 5th cycle to $\overline{REN}$ going low for read
$L_{RT\_TO\_DATA}$	Min = 20 Max = 23	RT 5th cycle to valid data on Q[35:0]
L_{IN}	Min = 8 Max = 29	Initial latency for data read after FIFO goes empty during simultaneous read/write
$L_{\overline{EF}\_DEASSERT}$	Min = 6 Max = 27	Write to $\overline{EF}$ going high

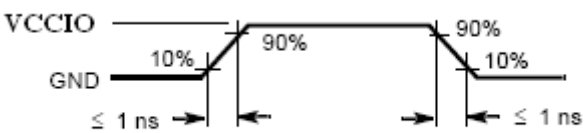
Figure 5. AC Test Load Conditions



(a) V_{CCIO} = 1.8 Volt



(b) V_{CCIO} = 3.3 Volt



(c) All Input Pulses

Switching Characteristics

Over the operating Range

Parameter	Description		-100		Unit
			Min	Max	
t_{PU}	Power-up time after all supplies reach minimum value		–	2	ms
t_S	Clock cycle frequency	3.3 V LVCMOS	24	100	MHz
t_S	Clock cycle frequency	1.8 V LVCMOS	24	100	MHz
t_A	Data access time		–	10	ns
t_{CLK}	Clock cycle time		10	41.67	ns
t_{CLKH}	Clock high time		4.5	–	ns
t_{CLKL}	Clock low time		4.5	–	ns
t_{DS}	Data setup time		3	–	ns
t_{DH}	Data hold time		3	–	ns
t_{QS}	RQSEL0 and WQSEL0 setup time		3	–	ns
t_{QH}	RQSEL0 and WQSEL0 hold time		3	–	ns
t_{ENS}	Enable setup time		3	–	ns
t_{ENH}	Enable hold time		3	–	ns
t_{ENS_SI}	Setup time for SPI_SI and $\overline{\text{SPI\_SEN}}$ pin		5	–	ns
t_{ENH_SI}	Hold time for SPI_SI and $\overline{\text{SPI\_SEN}}$ pin		5	–	ns
t_{RATE_SPI}	Frequency of SPI_SCLK		–	25	MHz
t_{RS}	Reset pulse width		100	–	ns
t_{PZS}	Port size select to MRS setup time		25	–	ns
t_{PZH}	MRS to port size select hold time		25	–	ns
t_{RSF}	Reset to flag output time		–	50	ns
t_{PRT}	Retransmit pulse width		5	–	RCLK cycles
t_{OLZ}	Output enable to output in Low Z		4	15	ns
t_{OE}	Output enable to output valid		–	15	ns
t_{OHZ}	Output enable to output in High Z		–	15	ns
t_{WFF}	Write clock to $\overline{\text{FF}}$		–	9	ns
t_{REF}	Read clock to $\overline{\text{EF}}$		–	9	ns
t_{PLL}	Time required to synchronize PLL		–	1024	cycles
t_{RATE_JTAG}	JTAG TCK cycle time		100	–	ns
t_{S_JTAG}	Setup time for JTAG TMS,TDI		8	–	ns
t_{H_JTAG}	Hold time for JTAG TMS,TDI		8	–	ns
t_{CO_JTAG}	JTAG TCK low to TDO valid		–	20	ns

Switching Waveforms

Figure 6. Write Cycle Timing

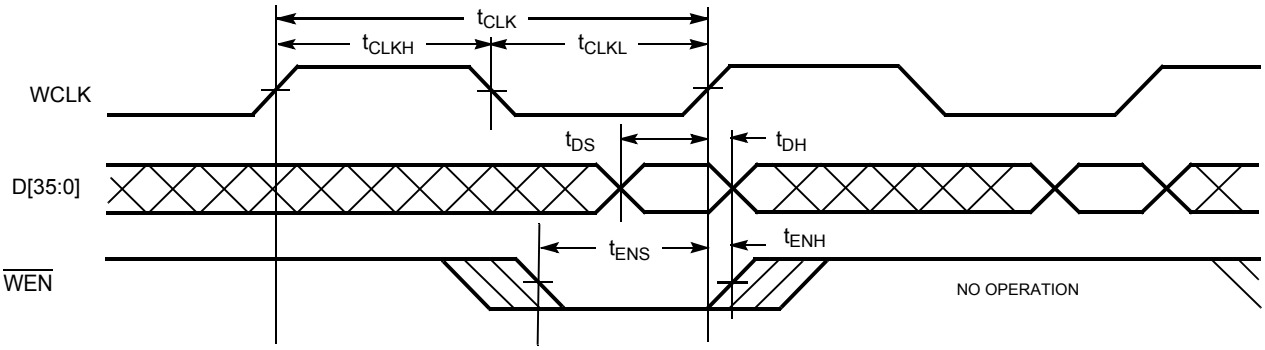


Figure 7. Read Cycle Timing

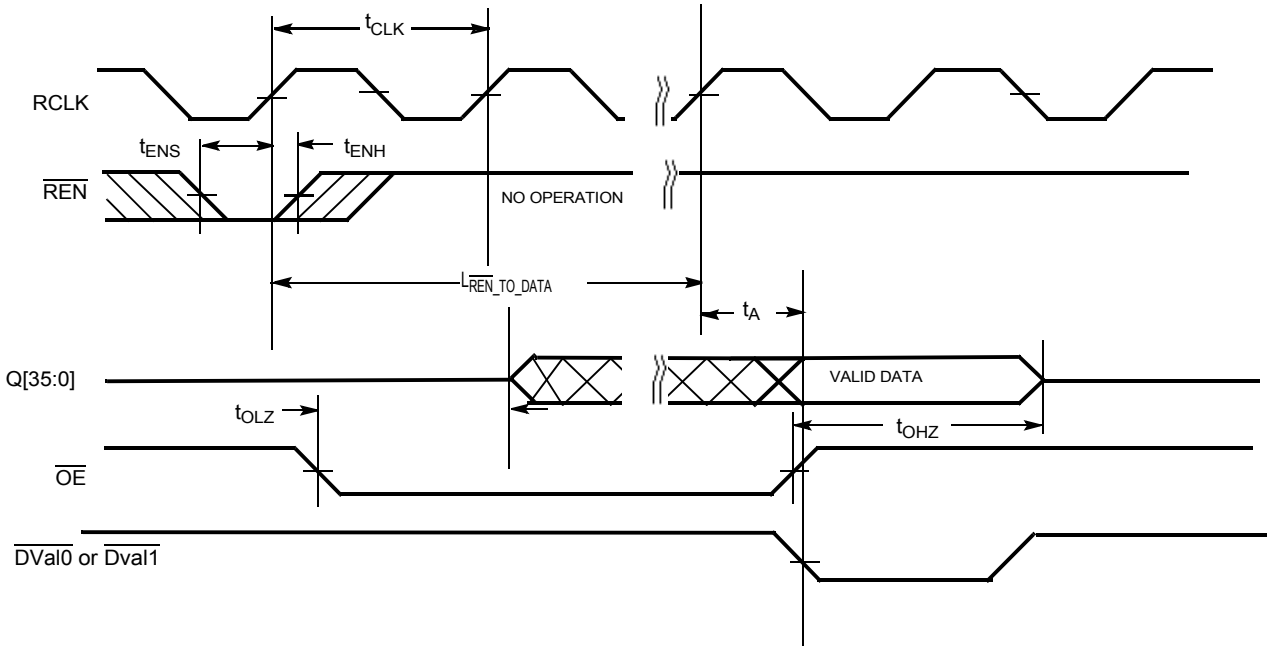
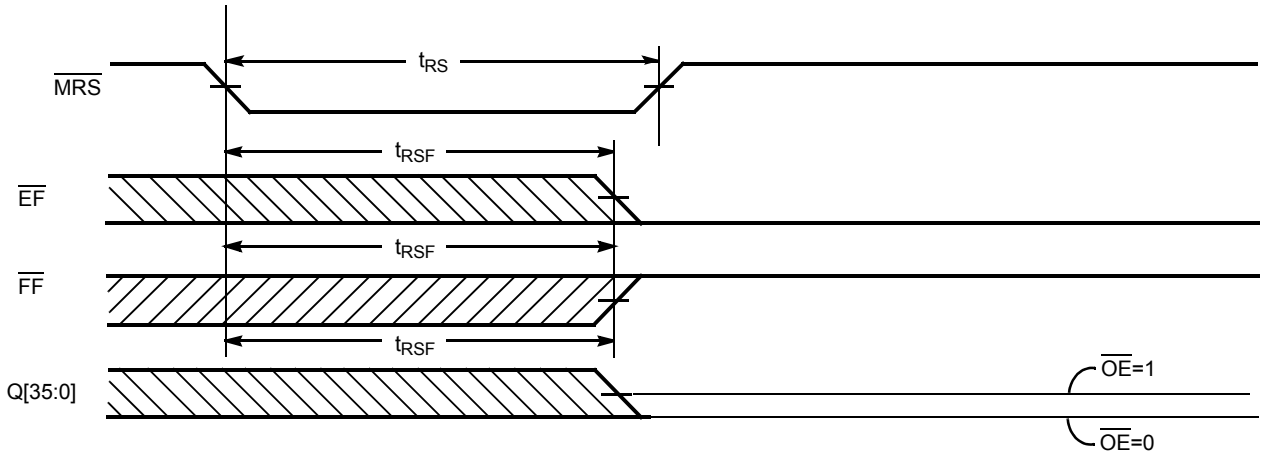


Figure 8. Reset Timing



Switching Waveforms (continued)

Figure 9. $\overline{MRS}$ to PORTSZ [2:0]

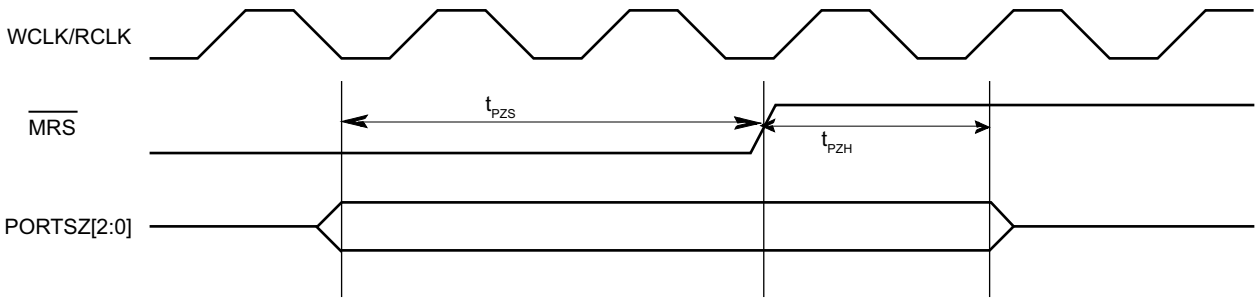
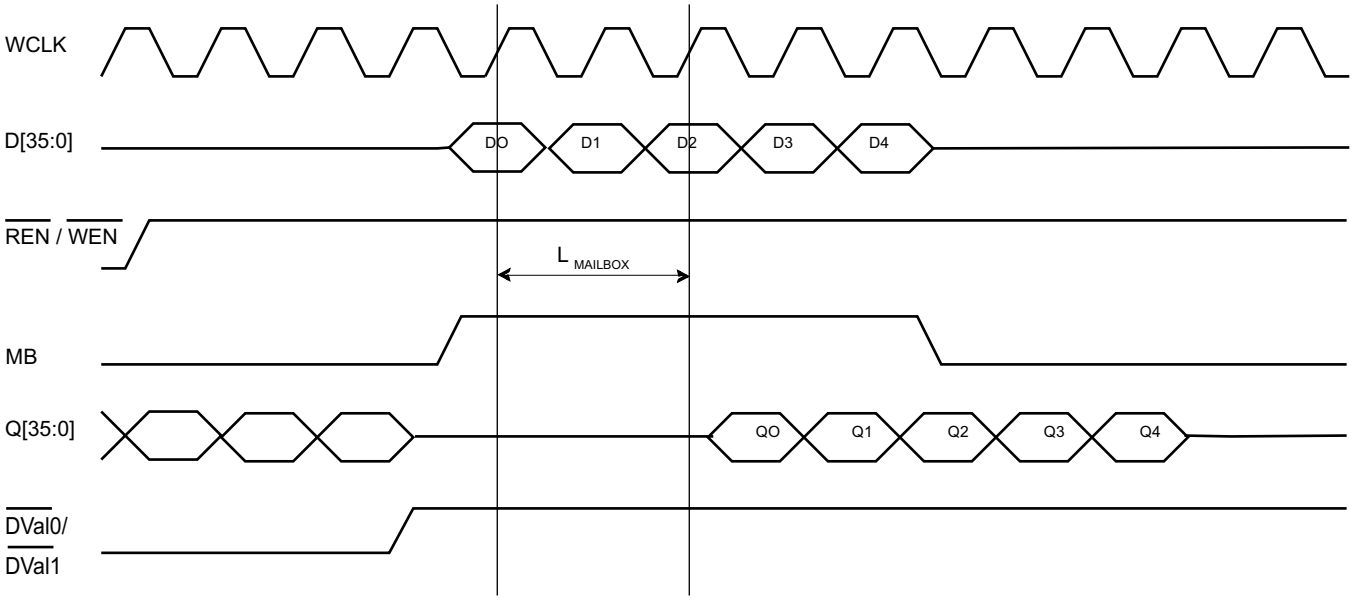


Figure 10. Flow-through mailbox Operation



Switching Waveforms (continued)

Figure 11. Configuration Register Write

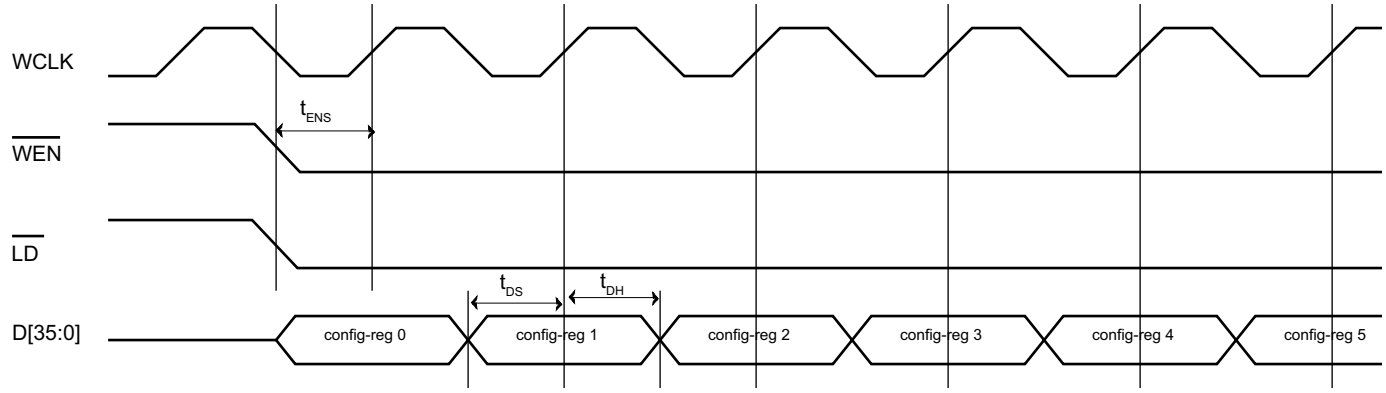


Figure 12. Configuration Register Read

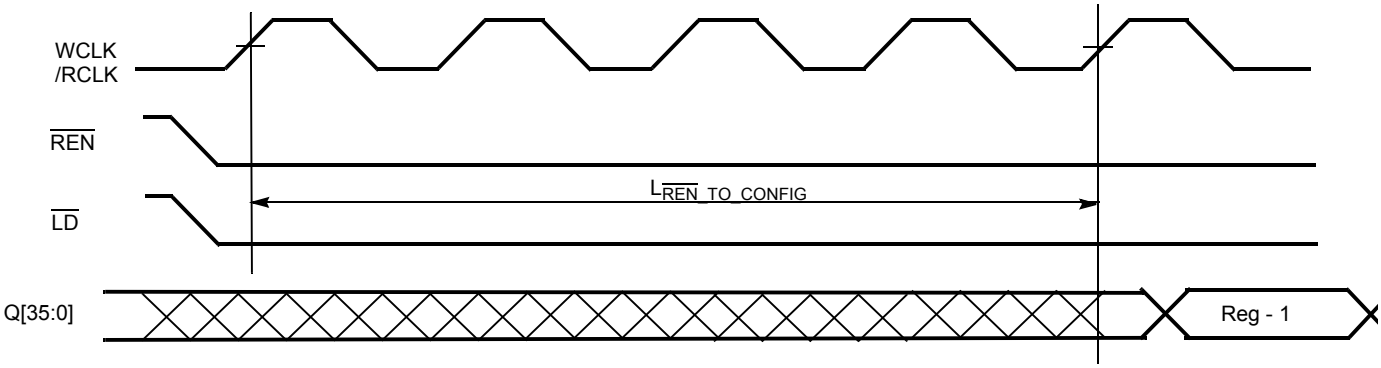
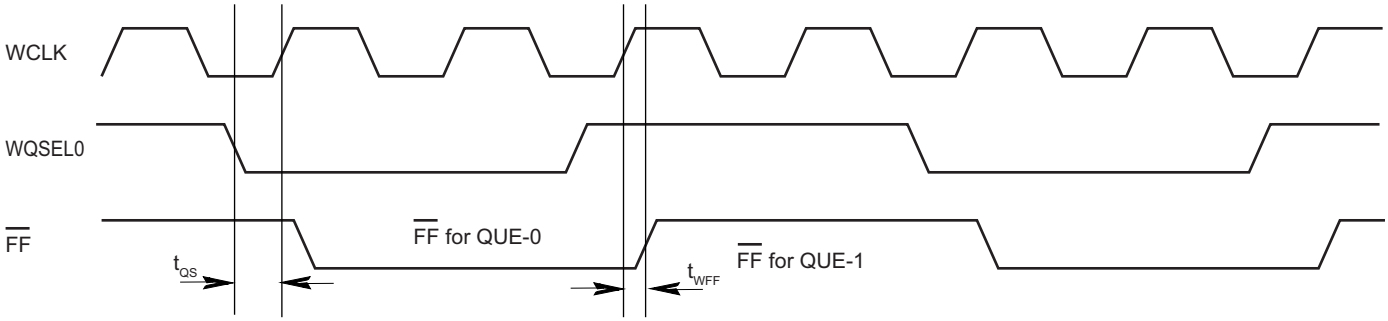


Figure 13. WQSEL to $\overline{FF}$



Switching Waveforms (continued)

Figure 14. RQSEL0 to $\overline{EF}$

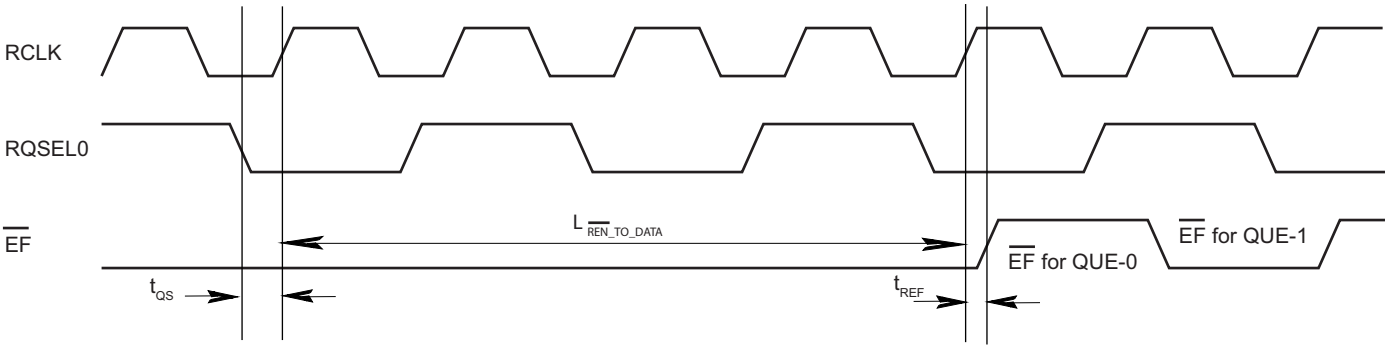
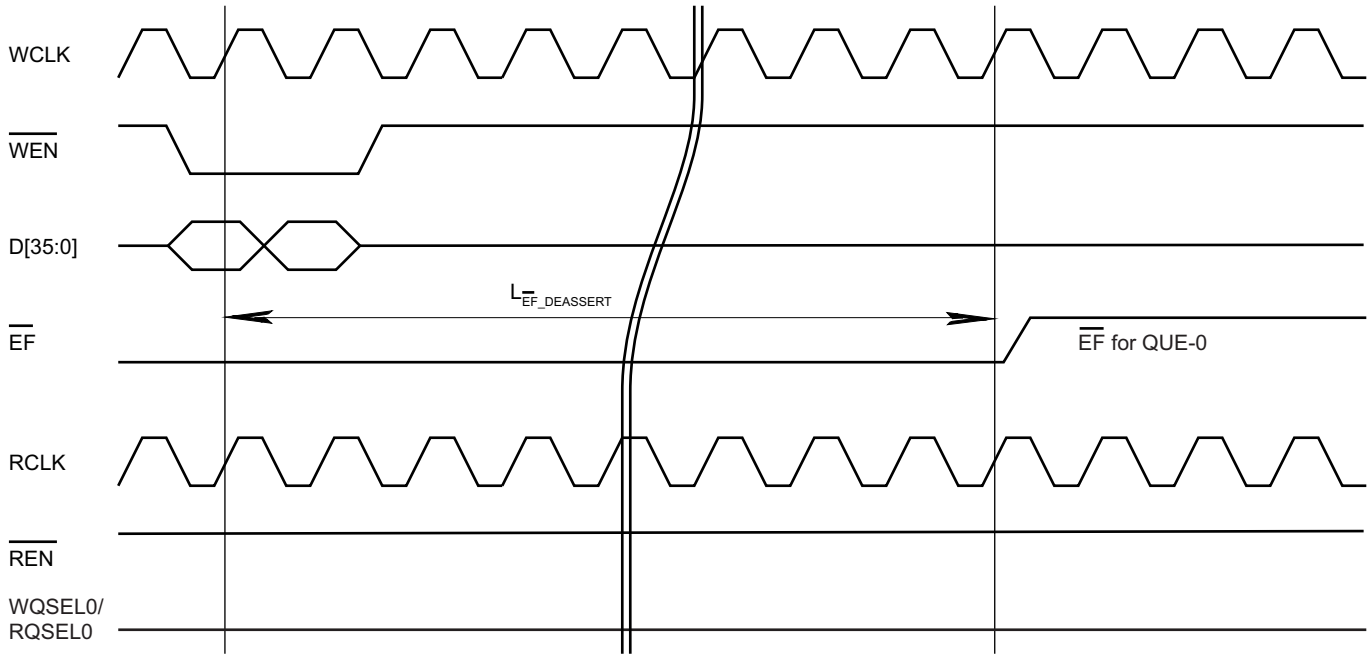


Figure 15. Write to Empty Flag De-assertion



Switching Waveforms (continued)

Figure 16. Read to Empty Flag Assertion

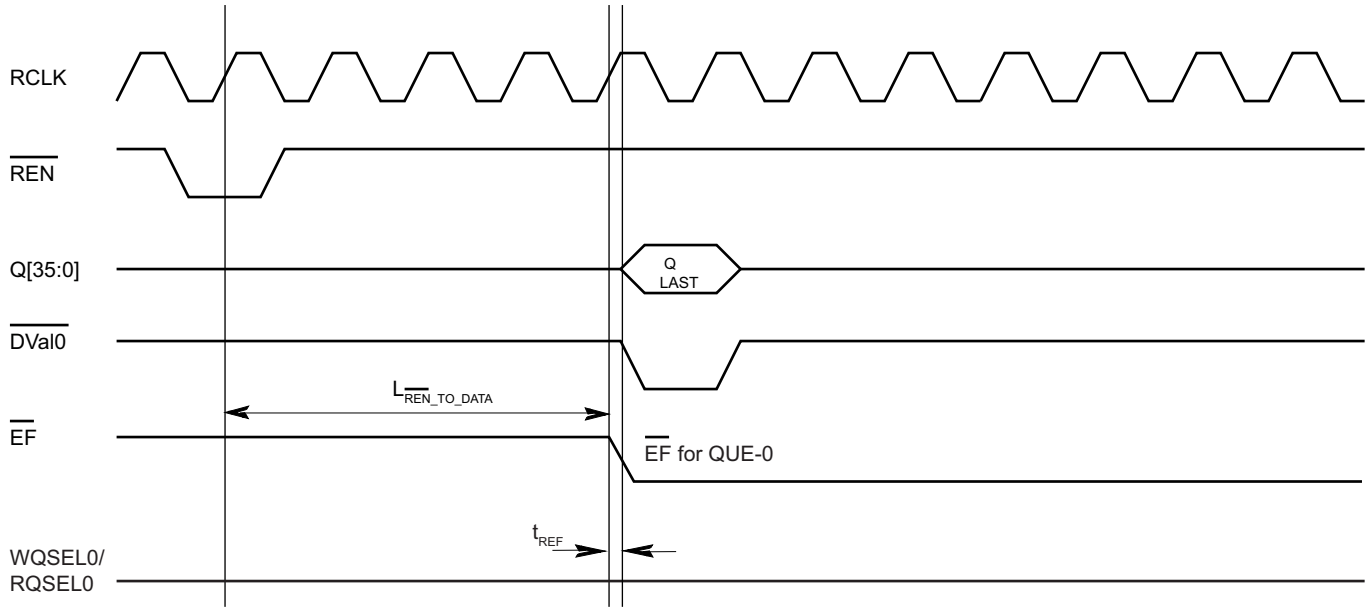
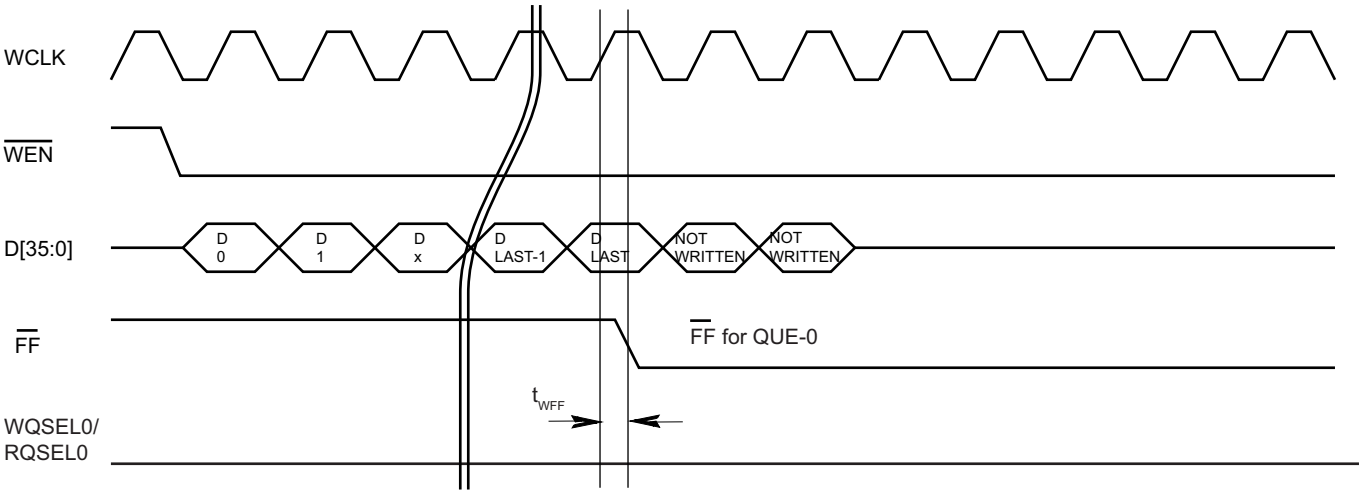


Figure 17. Full Flag Assertion



Switching Waveforms (continued)

Figure 18. Full Flag De-assertion

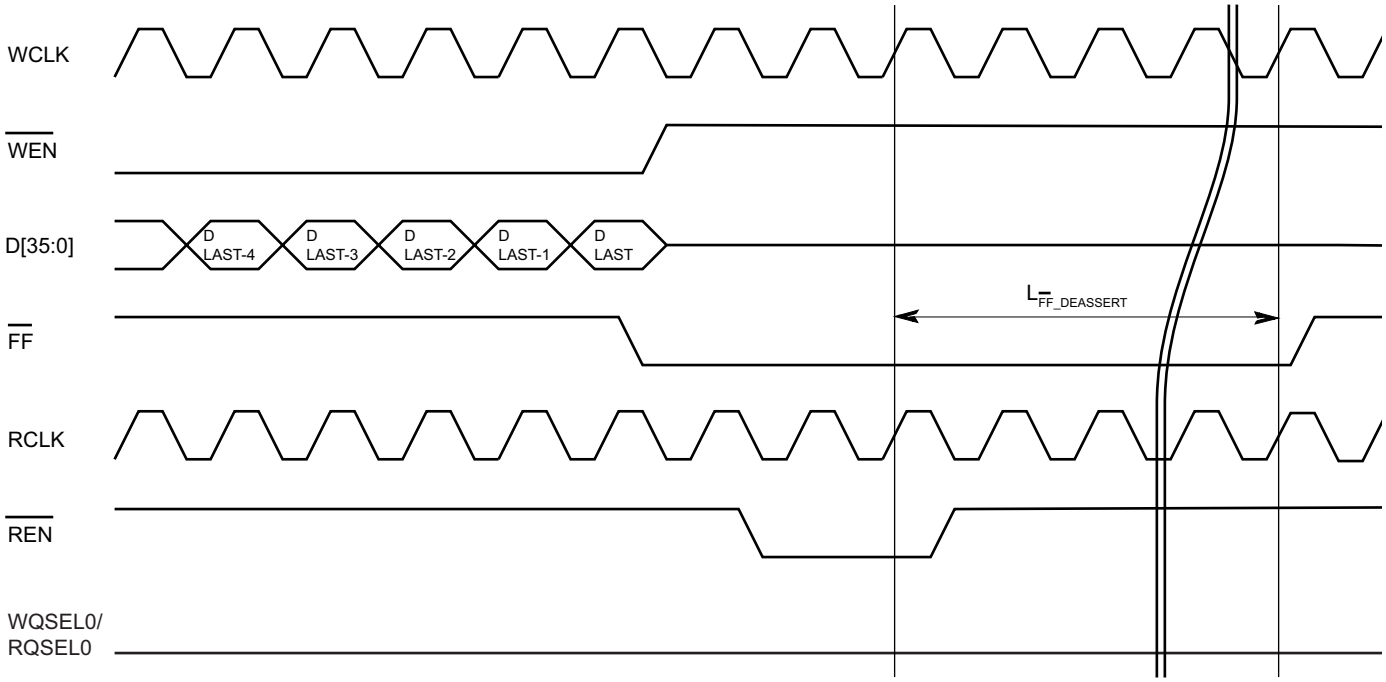
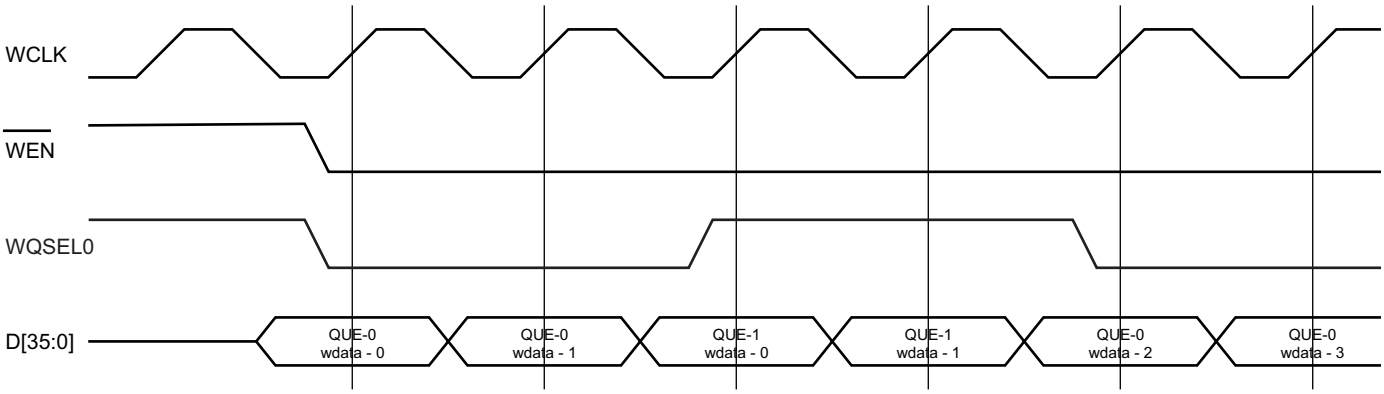


Figure 19. Switching between Queues - Write



Switching Waveforms (continued)

Figure 20. Switching between Queues - Read

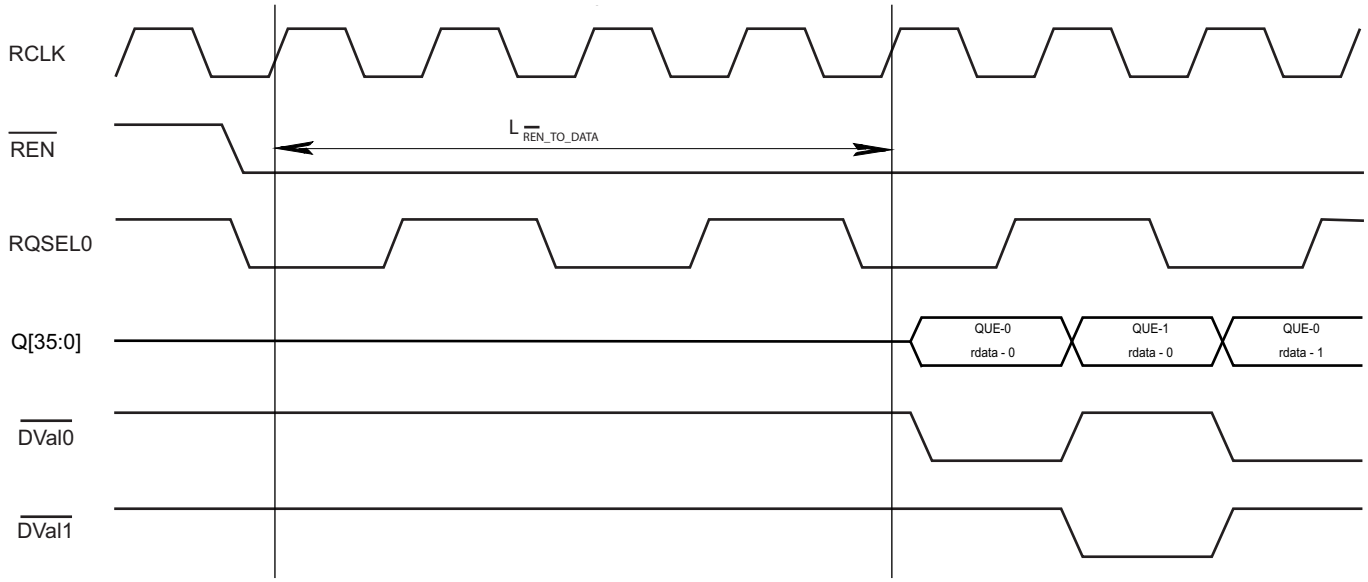
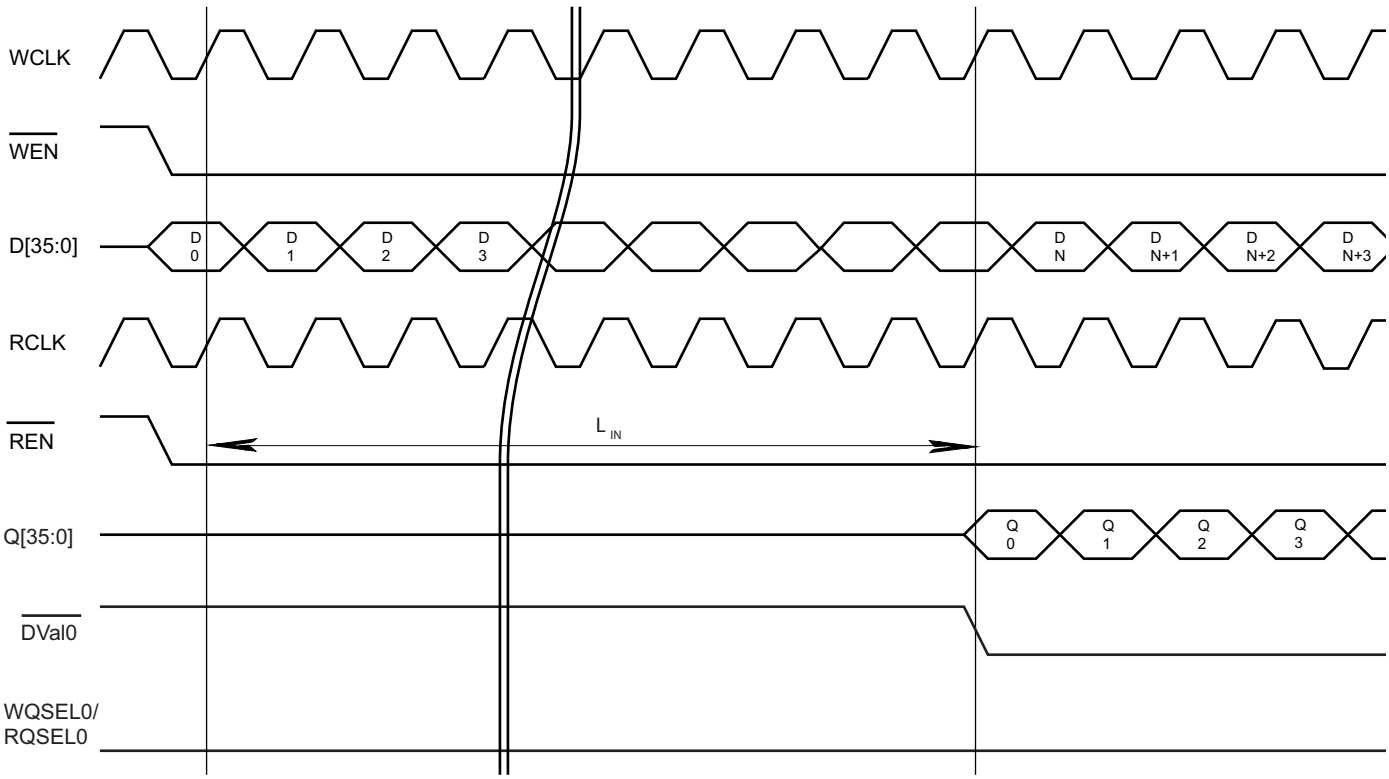


Figure 21. Simultaneous Write & Read QUE - 0



Switching Waveforms (continued)

Figure 22. Mark

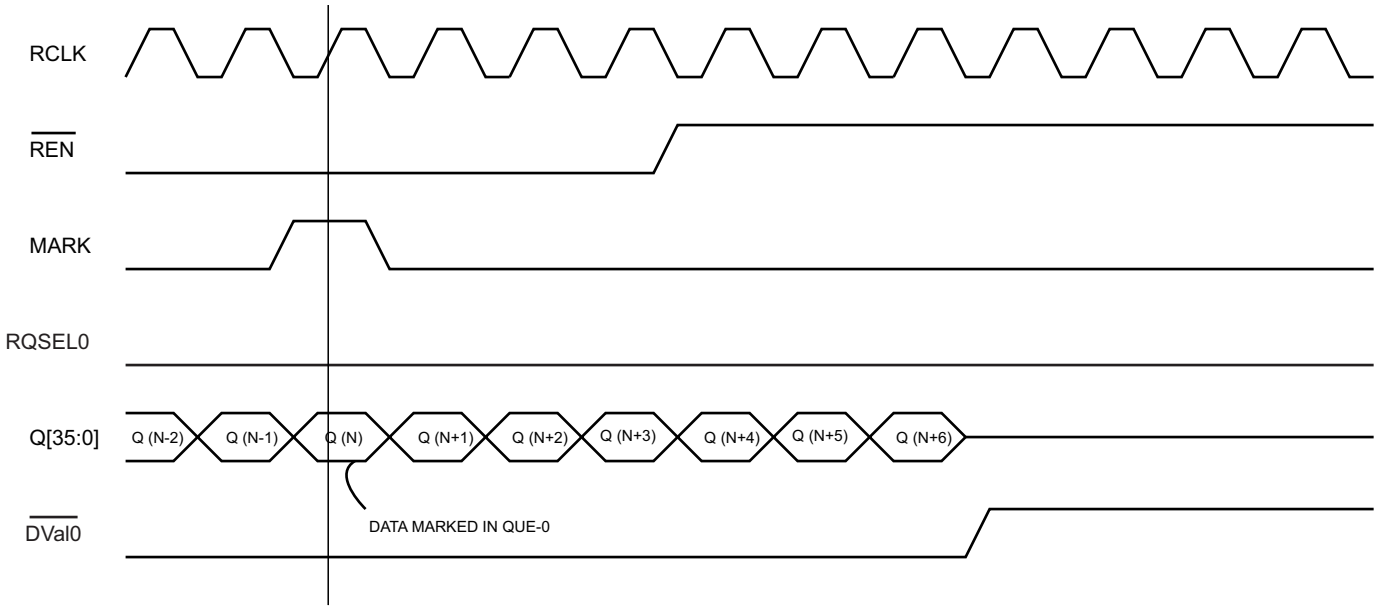
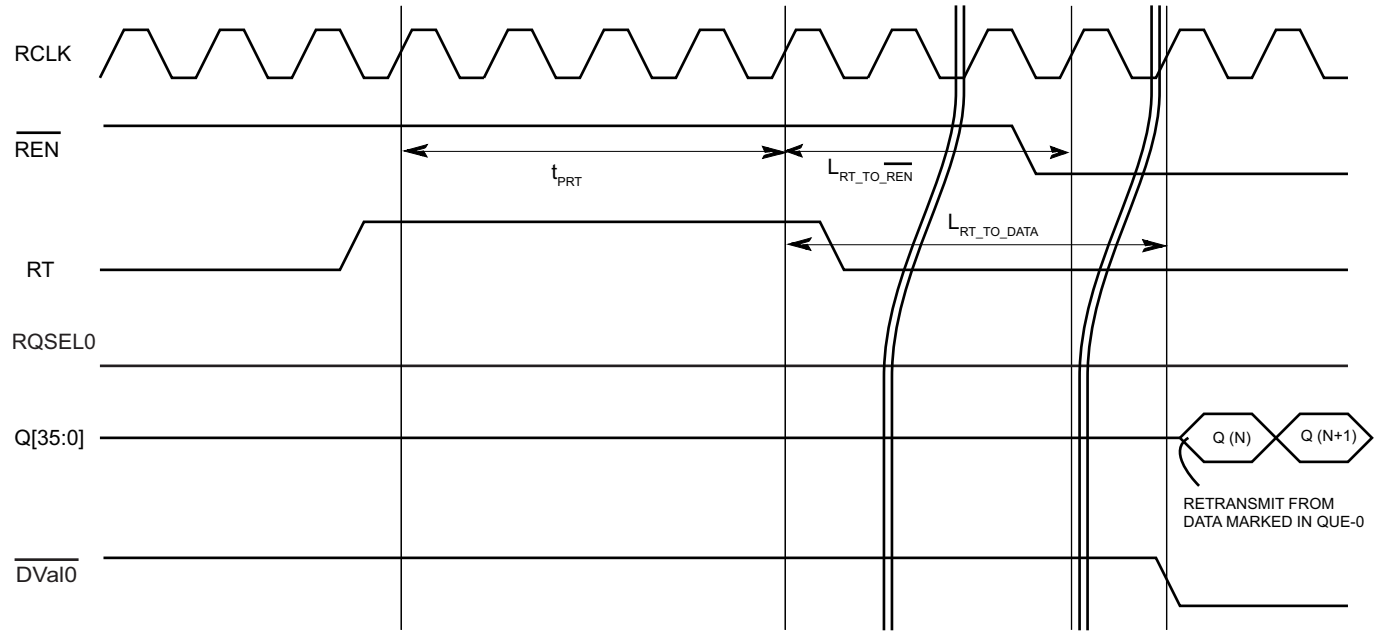


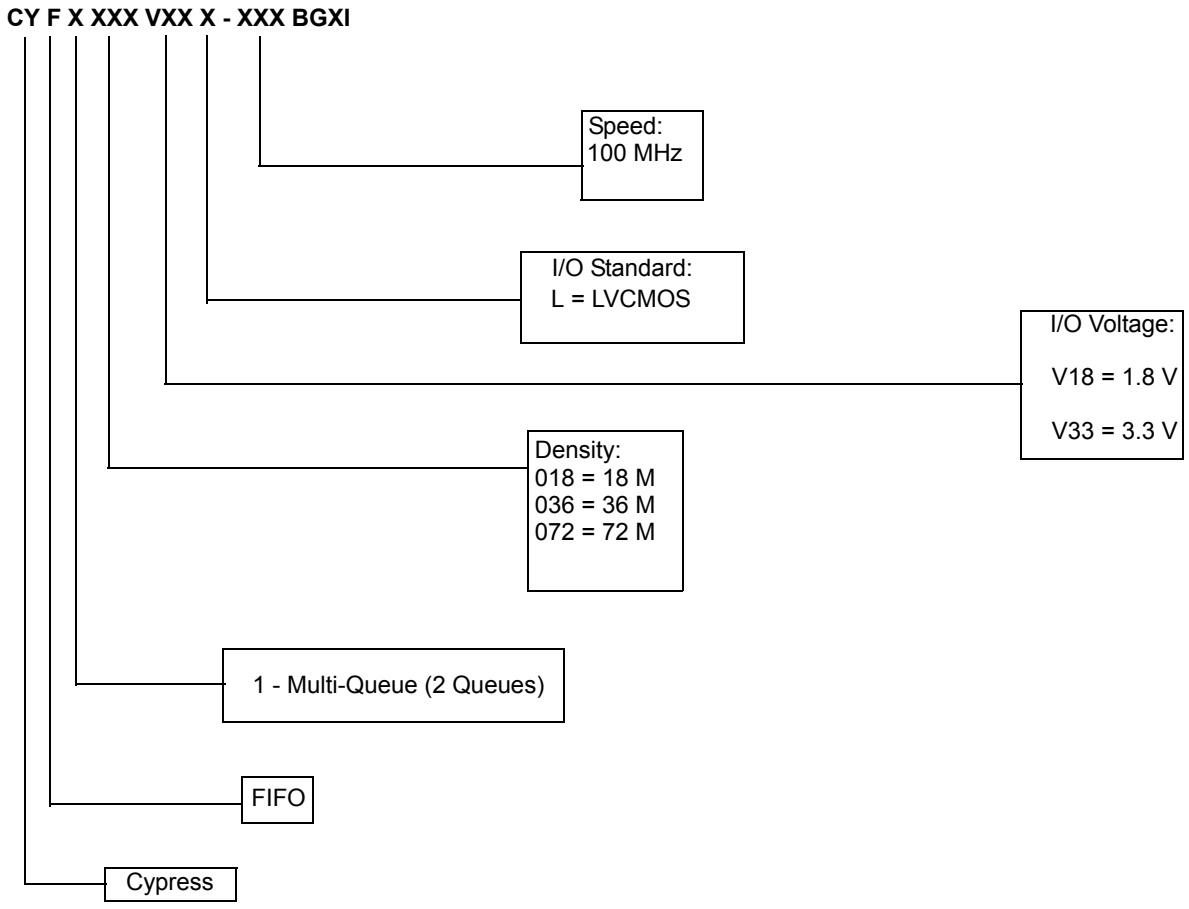
Figure 23. Retransmit



Ordering Information

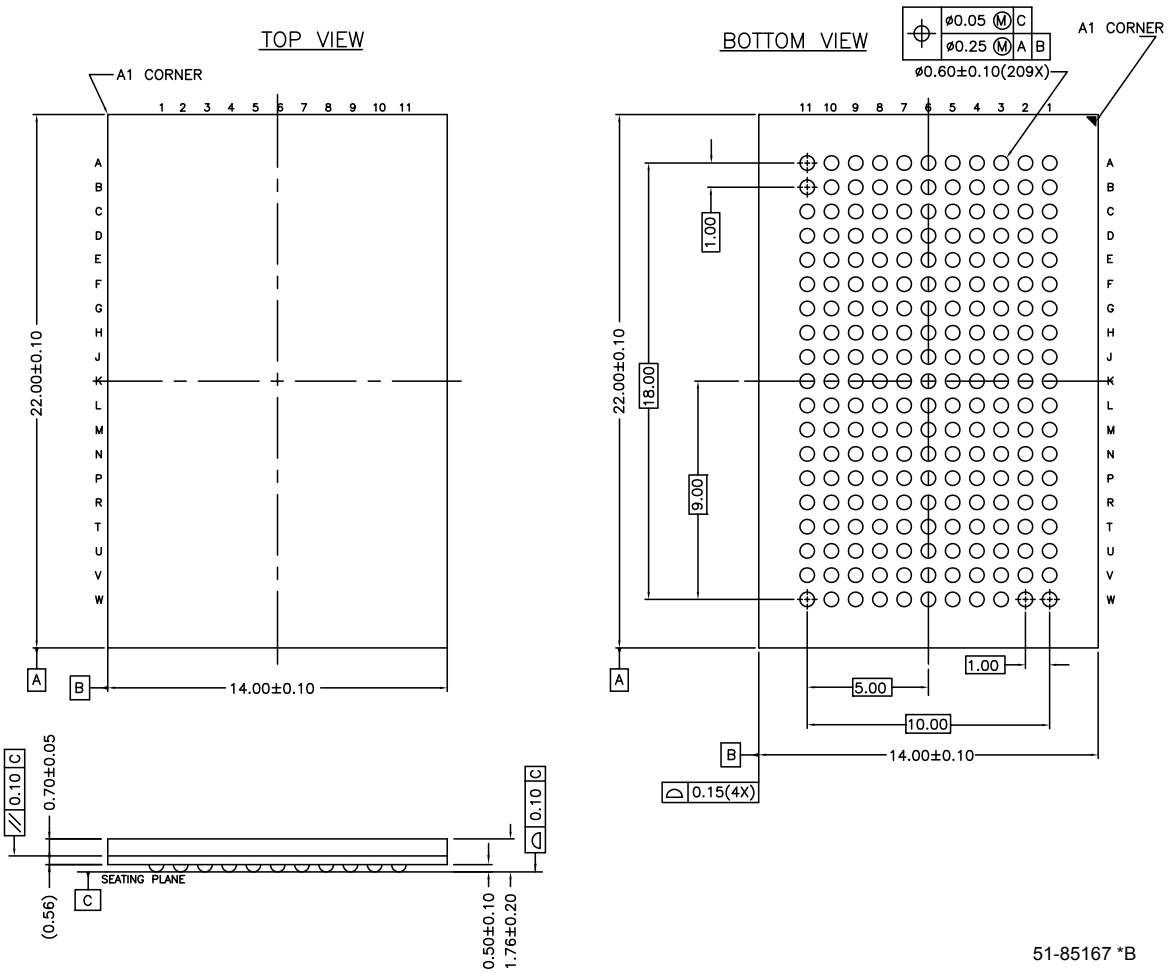
Speed (MHz)	Ordering Code	Package Diagram	Package Type	Operating Range
100	CYF1018V33L-100BGXI	51-85167	209-ball fine-pitch ball grid array (FBGA) (14 × 22 × 1.76 mm)	Industrial
	CYF1036V33L-100BGXI			
	CYF1072V33L-100BGXI			
	CYF1018V18L-100BGXI			
	CYF1036V18L-100BGXI			
	CYF1072V18L-100BGXI			

Ordering Code Definitions



Package Diagram

Figure 24. 209-ball FBGA (14 × 22 × 1.76 mm) BB209A, 51-85167



Acronyms

Acronym	Description
$\overline{EF}$	empty flag
$\overline{FF}$	full flag
FIFO	first in first out
I/O	input/output
FBGA	fine-pitch ball grid array
JTAG	joint test action group
LVCMOS	low voltage complementary metal oxide semiconductor
MB	mailbox
$\overline{MRS}$	master reset
$\overline{OE}$	output enable
RCLK	read clock
$\overline{REN}$	read enable
RQSEL0	read queue select
SCLK	serial clock
TDI	test data in
TDO	test data out
TCK	test clock
TMS	test mode select
WCLK	write clock
$\overline{WEN}$	write enable
WQSEL0	write queue select
QUE-0	queue number 0
QUE-1	queue number 1

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
mm	millimeter
ms	millisecond
ns	nanosecond
Ω	ohm
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CYF1018V/CYF1036V/CYF1072V, 18/36/72-Mbit Programmable 2-Queue FIFOs Document Number: 001-68321				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	3209860	SIVS	03/30/2011	New data sheet
*A	3353401	AJU	08/26/2011	Updated Package Diagram.
*B	3387127	AJU	09/28/2011	Updated Pin Diagram for CYF1XXXV (Added Note 1 and referred the same note in DNU in ball U6). Updated Multi-Queue Operation (Updated Table 4 (WCLK column in first row)). Updated Recommended DC Operating Conditions (Added Note 2 and referred the same note in Parameter column). Updated Switching Waveforms (Removed the numbers in Figure 10, Figure 14, Figure 16, and Figure 20).

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