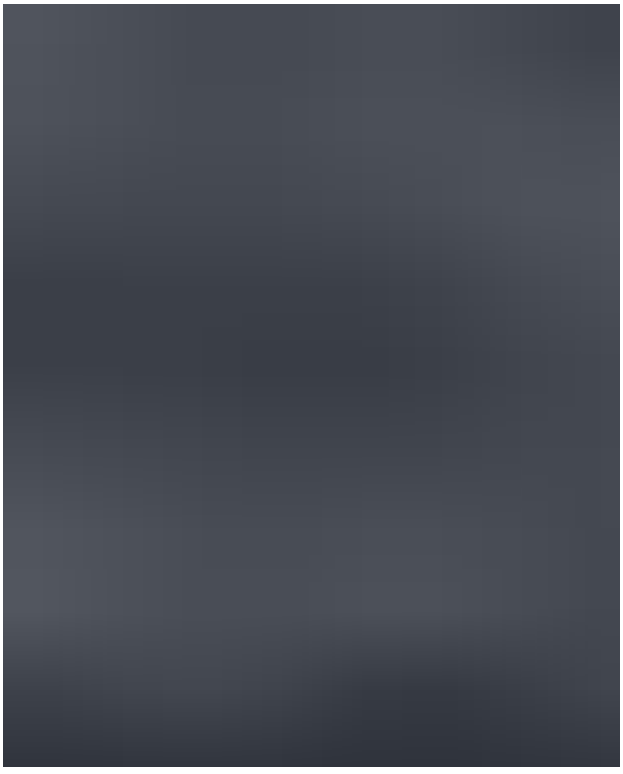
Datasheet

DB4CGX15

Cyclone IV GX Development Board



www.devboards.de

Contents

Revisions

Revision	Remark	Date
1.00	Initial Version	26.02.2010
1.01	Changes in the DDR2 VREF generation, programming Adapter for EPM240,	19.05.2010
1.10	The MSEL PINS on Board Revision 1.0 are selected for an IO voltage of 3.3V. MSEL[2..0]= “101”. Due to the used IO Voltage of 3.0V the MSEL[2..0] Signals will be changed to “011” for Board Revision 1.1	22.07.2010
1.11	Issue in documentation: 32Mbyte DDR2 memory on board. 128Mbyte device mounted, but A13 and BA2 not connected due to lack of I/O-Pins of FPGA.	16.08.2010
1.12	Added Documentation for ADD-On Boards	03.09.2010
1.13	Some minor changes in documentation	02.11.2010

Package contents

DB4CGX15

- DB4CGX15 Development Board
- Mini USB to USB Cable
- Reference Designs can be downloaded from www.devboards.de

Introduction

The DB4CGX15 is a Cyclone IV Development Board for PCIexpress applications with embedded USB-Blaster, Memory and IO Pins

The following features are integrated:

- EP4CGX15F14C6N
- EPCS16 configuration device
- 32 Mbyte DDR2 Memory
- 19 I/O Pins
- 6x Input Pins
- 2x User LEDs
- JTAG interface
- Crystal Oscillator

- Embedded USB Blaster on Board

- Power Supply via PCIexpress or USB-Blaster

- on board power supplies for 3.3V / 1.8V / 1.2V

- dimension : 70x68mm²

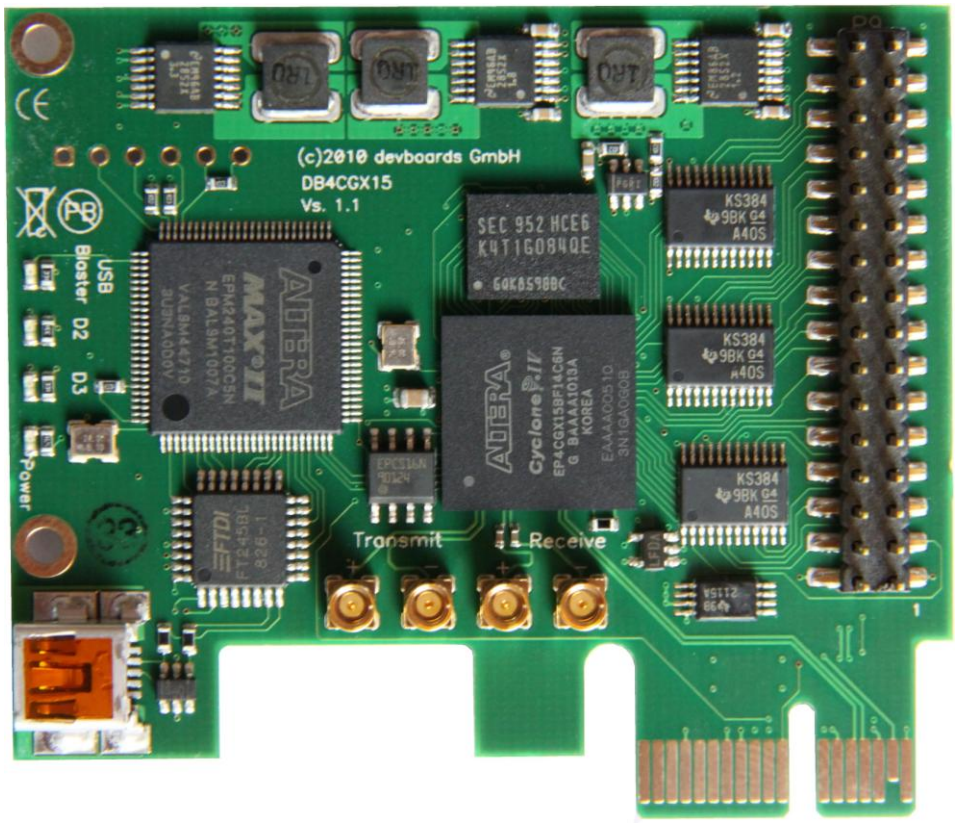


Figure 1

Installation

Download and execute the DB4CGX15_Setup.Exe file from www.devboards.de to install the Reference Designs and documentation. The Free Quartus Software and NIOS IDE can be downloaded from www.altera.com/download

Please install the applications in the following sequence:

- install the Quartus® 9.1SP2 Web Edition
- install Nios®II 9.1SP2 Version
- install the reference designs.

Getting started

Documentation

The complete documentation of the board, the reference designs, IP functions and the on-board devices are stored in the documentation directory of the Altera® Nios®II directory e.g. C:\Altera\91SP1\nios2eds\documents\DB4CGX15.

Setting up the board

Standalone usage :
Connect the DB4CGX15 Board via the USB Cable to the PC. The Power LED should lit and the board should be registered as an Altera USB-Blaster on your PC. After that you can work with the board. The board can also be powered via the expansion connector P9 – the board requires 3.3V

Using as add-on Board via PCIexpress

Power down the motherboard. Plug the DB4CGX15 development board in a PCIexpress slot on the motherboard. Connect the DB4CGX15 board via the USB cable to the PC. The DB4CGX15 development boards come with a PCIexpress application programmed in the configuration device. After Powering up the PC, the DB4CGX15 boards should be recognised as PCIexpress device and registered.

Flashing the board

Programming the configuration device

To program the EPCS16 configuration device on the DB4CGX15 Development Board, a JTAG indirect programming file (.jic) is used. In the file / convert programming file menu in Quartus®II a .SOF file can be converted into a .jic file. The .jic file can be selected in the Quartus®II programmer (in JTAG mode). Make sure that both configure / program lines are selected to download the loader into the FPGA and the SOF file into the configuration device.
The Nios®II IDE flash programmer can also be used to program a SOF file into the configuration device.

Reference designs

The Reference Designs are located in the \Altera\91SP2\nios2eds\examples\vhdl\DB4CGX15 folder.

Standard NIOS Application

This application can be used for running this board without PCIexpress. A NIOS, DDR2 Controller and PIOs for the LEDs and I/O Signals are included.

PCIexpress Reference Design

A PCIe Reference Design is available from www.logicandmore.com.

Board Description

FPGA Configuration

The DB4CGX15 Development Board includes an on-board USB Blaster that can be used to configure the FPGA, program the EPCS Configuration device, use the Signal-Tap Logic Analyser and together with the NIOS IDE to download and debug software.

Clocking

The DB4CGX15 Development Board includes a free running 25MHz Crystal Oscillator. The Crystal Oscillator drives the FPGA directly. Table 1 show the clock distribution on the DB4CGX15 board. The Crystal Oscillator is a ±50ppm Clock source. The DDR2 memory requires a differential clock, which is generated from a PLL inside the FPGA.

Clock Distribution

Function	FPGA Pin	Signal Name
25MHz	A10	Clk25
DDR1clk_p	E10	DDR1_clk
DDR1clk_n	D10	DDR1_clkn
PCIE_refclk_p	J6	PCI_REFCLKP
PCIE_refclk_n	J7	PCI_REFCLKN

Table 1

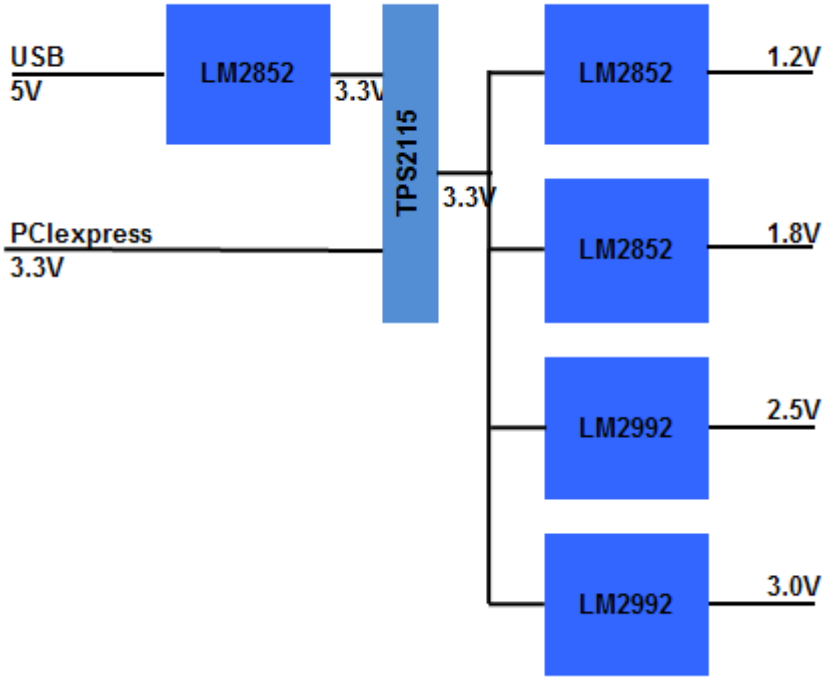
Power Supply

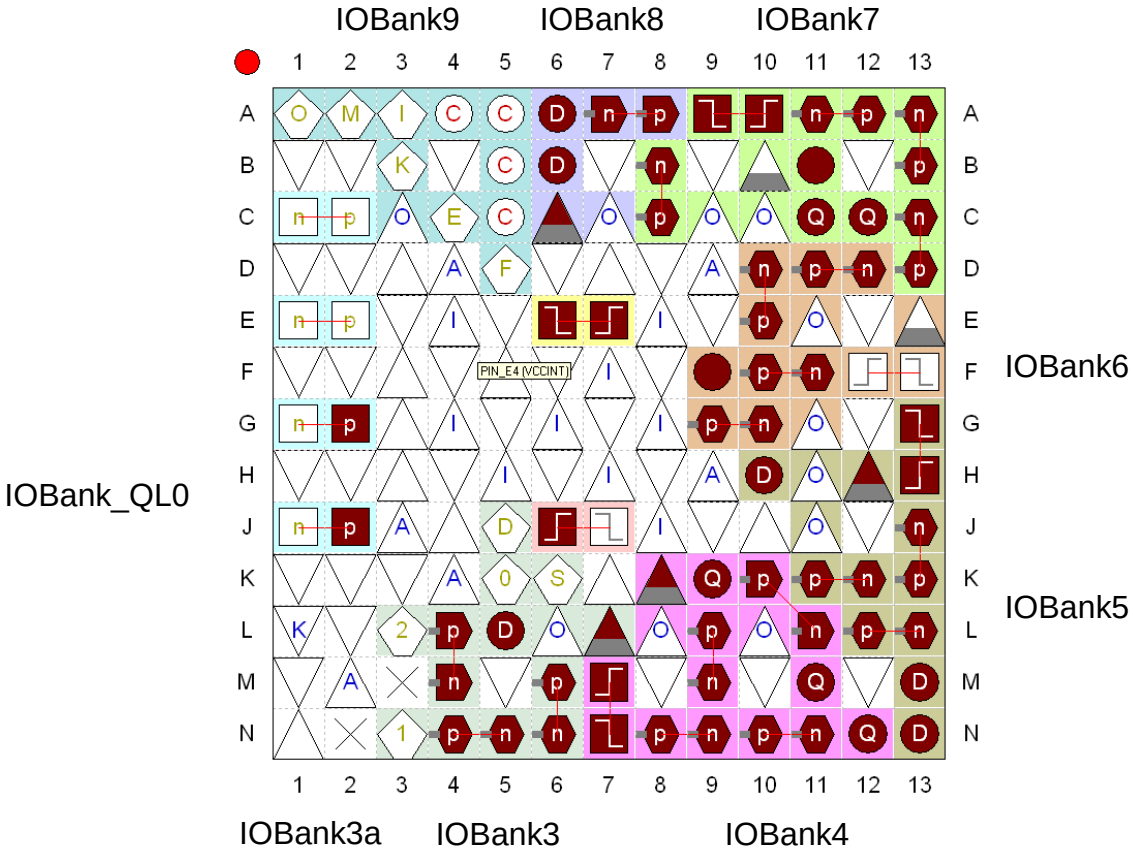
The DB4CGX15 Development Board can be supplied either via the USB Connection to the PC or via the PCIe slot

Figure 4 shows the Power distribution on the DB4CGX15 board.
For details of the power supply refer to the schematic on the end of the document.

- 1.2V Core Voltage
- 1.8V DDR2 memory supply
- 2.5V Analog Supply for FPGA
- 3.0V FPGA I/O Bank Supply
- 3.3V I/O Voltage and supply for the other components

A Power Good signal is generated monitoring the 1.2V and 3.3V.


USB
5V
LM2852
3.3V
TPS2115
PCIexpress
3.3V
3.3V
LM2852
1.2V
LM2852
1.8V
LM2992
2.5V
LM2992
3.0V


IOBank9
IOBank8
IOBank7
IOBank6
IOBank5
IOBank4
IOBank3
IOBank3a
IOBank_QL0
PIN_E4 (VCCINT)

IO-Bank	Used for	Supply
QL0	Transceiver	
3	I/O	3.0V
4	I/O	3.0V
5	DDR2	1.8V
6	DDR2	1.8V
7	DDR2	1.8V
8	DDR2, LED	1.8V
9	Config	3.0V

Reset Signal

Function	Pin	Signal Name
Power Good	G13	RSTn

Table 2

I/O Connections

DDR2 RAM

A 1Gbit DDR2 Memory is used on the DB4CGX15 development Board. Due to the lack of I/O_pins of the FPGA only 256Mbit are available. The memory is organized 64Mx8. Table 3 shows the wiring between the FPGA and the SDRAM.

FPGA Connection

Function	Pin	FPGA Pin
DDR1CLKp	E8	E10
DDR1CLKn	F8	D10
DDR1_CSn	G8	B6
DDR1_CKE	F2	F11
DDR1_RASn	F7	B11
DDR1_CASn	G7	D11
DDR1_WEn	F3	D12
DDR1_DM	B3	C11
DDR1_A0	H8	C6
DDR1_A1	H3	K12
DDR1_A2	H7	N13
DDR1_A3	J2	K13
DDR1_A4	J8	F9
DDR1_A5	J3	K11
DDR1_A6	J7	F10
DDR1_A7	K2	L13
DDR1_A8	K8	H10
DDR1_A9	K3	M13
DDR1_A10	H2	J13
DDR1_A11	K7	G9
DDR1_A12	L2	L12
DDR1_A13	L8	--
DDR1_BA0	G2	H12
DDR1_BA1	G3	G10
DDR1_BA2	G1	--
DDR1_DQ0	C8	C8
DDR1_DQ1	C2	C13
DDR1_DQ2	D7	A12
DDR1_DQ3	D3	B13
DDR1_DQ4	D1	D13
DDR1_DQ5	D9	B8
DDR1_DQ6	B1	C12
DDR1_DQ7	B9	A11
DDR1_DQS	B7	A13
DDR1_ODT	F9	A8

Table 3

Pin Header

A Pin header with 20 IO signals and 4 inputs are connected to the FPGA via analog switches. Table 4
shows the pinning and the FPGA connection for Pin Header P9.

Make sure that only 3.3V signals are connected to the Pin Headers P9.

I/O Connector P9

Function	FPGA	Pin	Pin	FPGA	Function
GND		1	2		GND
IO1	L4	3	4	M4	IO2
IO3	N4	5	6	N5	IO4
IO5	L5	7	8	N6	IO6
IO7	M6	9	10	E6	IN1
VCC33		11	12		VCC33
IO8	L7	13	14	N7	IN2
IN3	M7	15	16	N8	IO9
IO10	M9	17	18	E7	IN4
IO11	K8	19	20	N9	IO12
GND		21	22		GND
IO13	L9	23	24	K9	IO14
IO15	N10	25	26	M11	IO16
IO17	N11	27	28	L11	IO18
IO19	N12	29	30	K10	IO20
VCC33		31	31		VCC33

Table 4

PCIexpress connector

Table 6 shows the connection between FPGA and PCIexpress slot.

PCI express connector

Function	FPGA	Pin	Pin	FPGA	Function
		B1	A1		PRSNT
		B2	A2		
		B3	A3		
GND		B4	A4		GND
		B5	A5		
		B6	A6		
GND		B7	A7		
3.3V		B8	A8		
		B9	A9		3.3V
		B10	A10		3.3V
PCI_Wake	H13	B11	A11	A9	PCI_PWRGD
		B12	A12		GND
GND		B13	A13	J6	PCIREFCLKp
PCI_RX0p	J2	B14	A14	J7	PCIREFCLKn
PCI_RX0n	J1	B15	A15		GND
GND		B16	A16	G2	PCI_TX0p
PRSNT		B17	A17	G1	PCI_TX0n
GND		B18	A18		GND

Table 5

LEDs

2 LEDs are available on the DB4CGX15 Development Board. The LEDs are connected to 3.3V. To light the LED the FPGA must drive a Low signal.. Table 6 shows the FPGA connection of the Buttons and LEDs. The LED outputs must be used as Open Drain signals.

FPGA Connection

Function	Device	Pin	FPGA Pin
LED0	D2	1	A7
LED1	D3	1	A6

Table 6

Transceiver

The second High Speed transceiver is available via MMCX connectors. Information on the MMCX connectors can be found at www.samtec.com. Adapter cables from mmcx to SMA are available from samtec,too.

Bill of Material

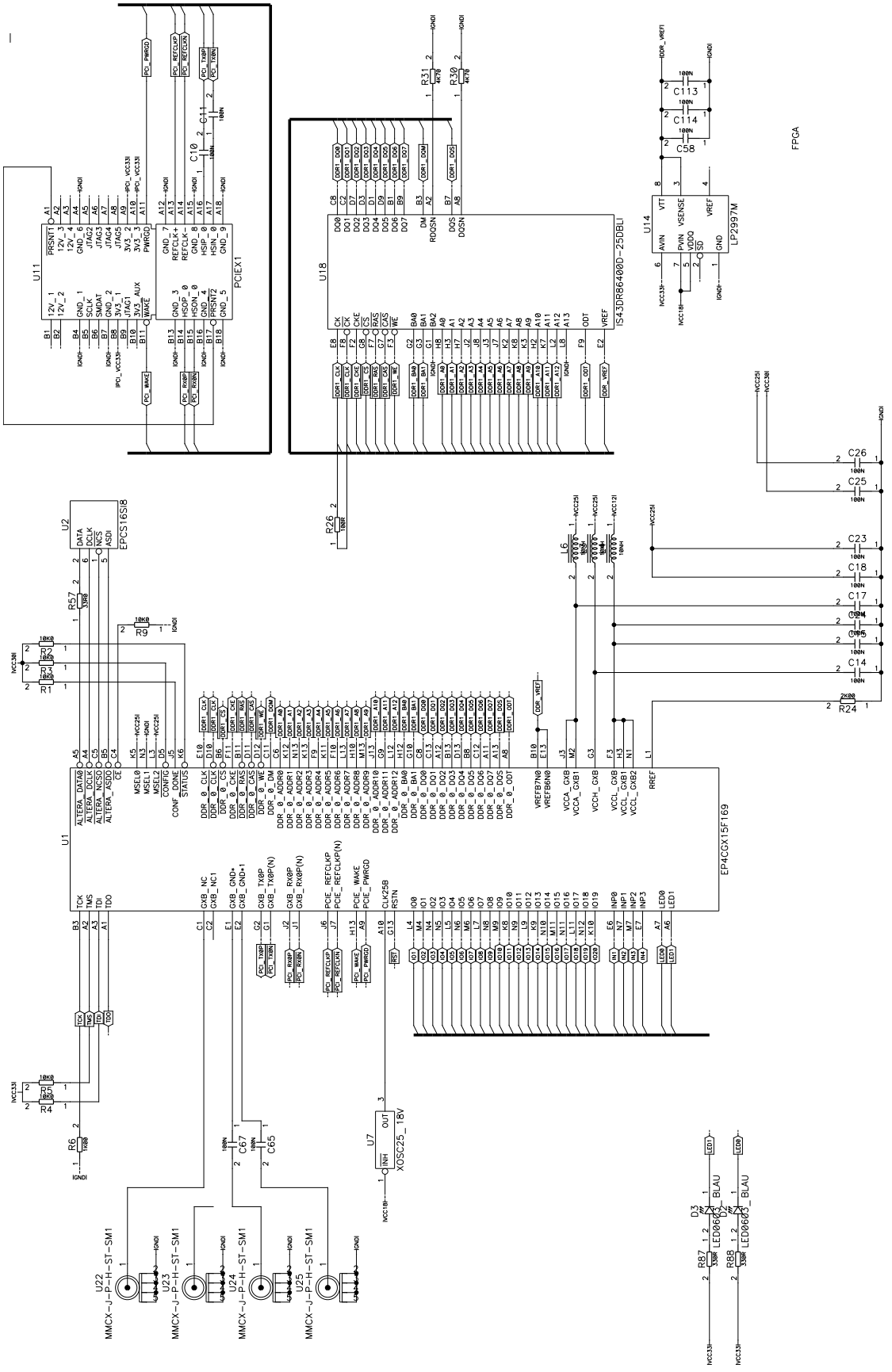
Description	Count	SMD	Package	Reference Designator
AT93C46-DN-SH-B	1	Y	SO8	U4
BC850B	1	Y	SOT23	U13
C0402_100NA25V	27	Y	C0402	C10 C11 C14 C15 C17 C18 C23 C24 C25 C26 C57 C58 C59 C60 C61 C62 C63 C64 C110 C111 C112 C113 C114 C117 C119 C173 C176
C0603_100N0A50V	23	Y	C0603	C1 C3 C4 C5 C13 C16 C19 C22 C30 C34 C35 C36 C37 C38 C39 C40 C41 C42 C50 C66 C91 C92 C93
C0603_10N0A50V	3	Y	C0603	C6 C174 C175
C0603_2N20A50V	3	Y	C0603	C20 C29 C44
C0805_10UFA10V	8	Y	C0805	C2 C8 C9 C12 C45 C46 C49 C52
C1206_1N00A2KV	1	Y	C1206	C7
C1210_100UA6V3	5	Y	C1210	C33 C43 C51 C53 C54
C1210_47U0A6V3	1	Y	C1210	C68
EP4CGX15BF14C7N	1	Y	FBGA169	U1
EPCS16SI8N	1	Y	SO8	U2
EPM240T100C5N	1	Y	TQ100	U5
FT245BL	1	Y	LQFP32	U10
IS43DR86400D-25DBLI	1	Y	BGA60	U18
L0603_10NHA0A4 EPCOS B82496C3100J	3	Y	S0603BR	L3 L4 L6
L0805_330RA2A0 Würth 742792037	1	Y	L0805	L1
LED 0603_Blau	4	Y	0603	D1 D2 D3 D15
LM2852XMXA-1.2	1	Y	TSSOP14	U9
LM2852XMXA-1.8	1	Y	TSSOP14	U15
LM2852XMXA-3.3	1	Y	TSSOP14	U16
LP2992AIM5-2.5	1	Y	SOT23-5	U12
LP2992AIM5-3.0	1	Y	SOT23-5	U32
LP2997	1	Y	SO8	U14
LWE-T_1U0A2A7 Würth 744042001	3	Y	WE-TPC-M	L2 L7 L9
MMCX-J-P-H-ST-SM1	4	Y		U22 U23 U24 U25

Description	Count	SMD	Package	Reference Designator
R0402_100RA1%	2	Y	R0402	R15 R26
R0402_4K70A1%	2	Y	R0402	R30 R31
R0603_100KA1%0	1	Y	R0603	R22
R0603_10K0A1%0	11	Y	R0603	R1 R2 R3 R4 R5 R9 R11 R17 R18 R19 R25
R0603_10RA1%0	1	Y	R0603	R139
R0603_1K00A1%0	5	Y	R0603	R6 R16 R20 R27 R33
R0603_1K50A1%0	1	Y	R0603	R12
R0603_22R0A1%0	2	Y	R0603	R7 R8
R0603_2K00A1%0	1	Y	R0603	R24
R0603_2K20A1%0	1	Y	R0603	R10
R0603_330RA1%0	3	Y	R0603	R21 R87 R88
R0603_33R0A1%0	1	Y	R0603	R57
R0603_470RA1%0	2	Y	R0603	R14 R23
R0603_680RA1%0	1	Y	R0603	R13
SN65220DBVT	1	Y	SO8	U3
SN74CB3T3384	3	Y	TSSOP24	U19 U20 U21
TPS2115APW	1	Y	TSSOP8	U8
TPS3103K33DVBR	1	Y	SOT23-5	U17
TSM-116-01-L-DV-A	1	Y		P9
USB_MINI_AB	1	Y	MOLEX	P2
Crystal Oscillator 24Mhz O 24-JO32-B-3,3-1-L	1	Y	JO32	U6
Crystal Oscillator 25Mhz 1.8V O 50-JO32-B-1,8-1-L	1	Ja	JO32	U7

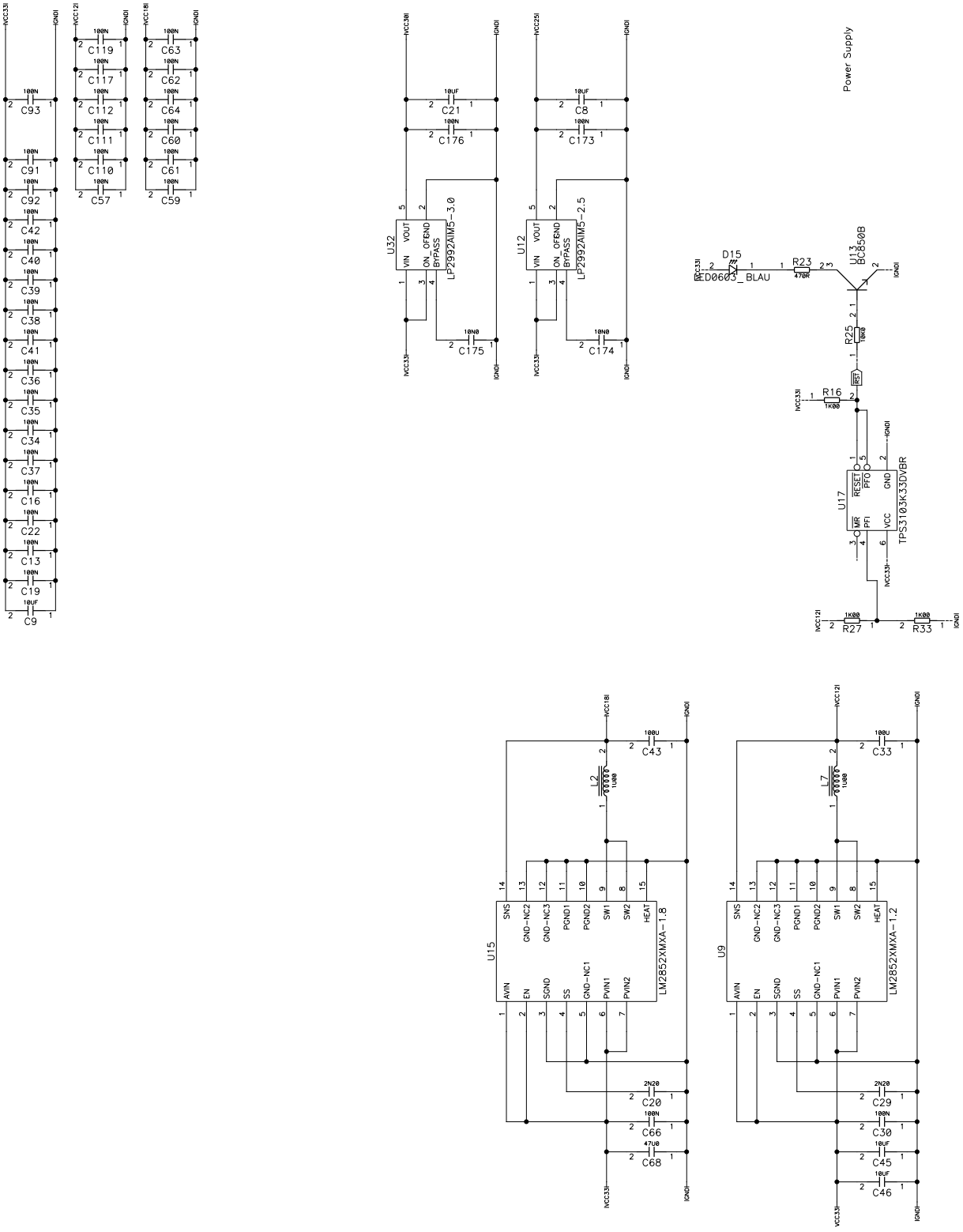
Table 7

Schematics

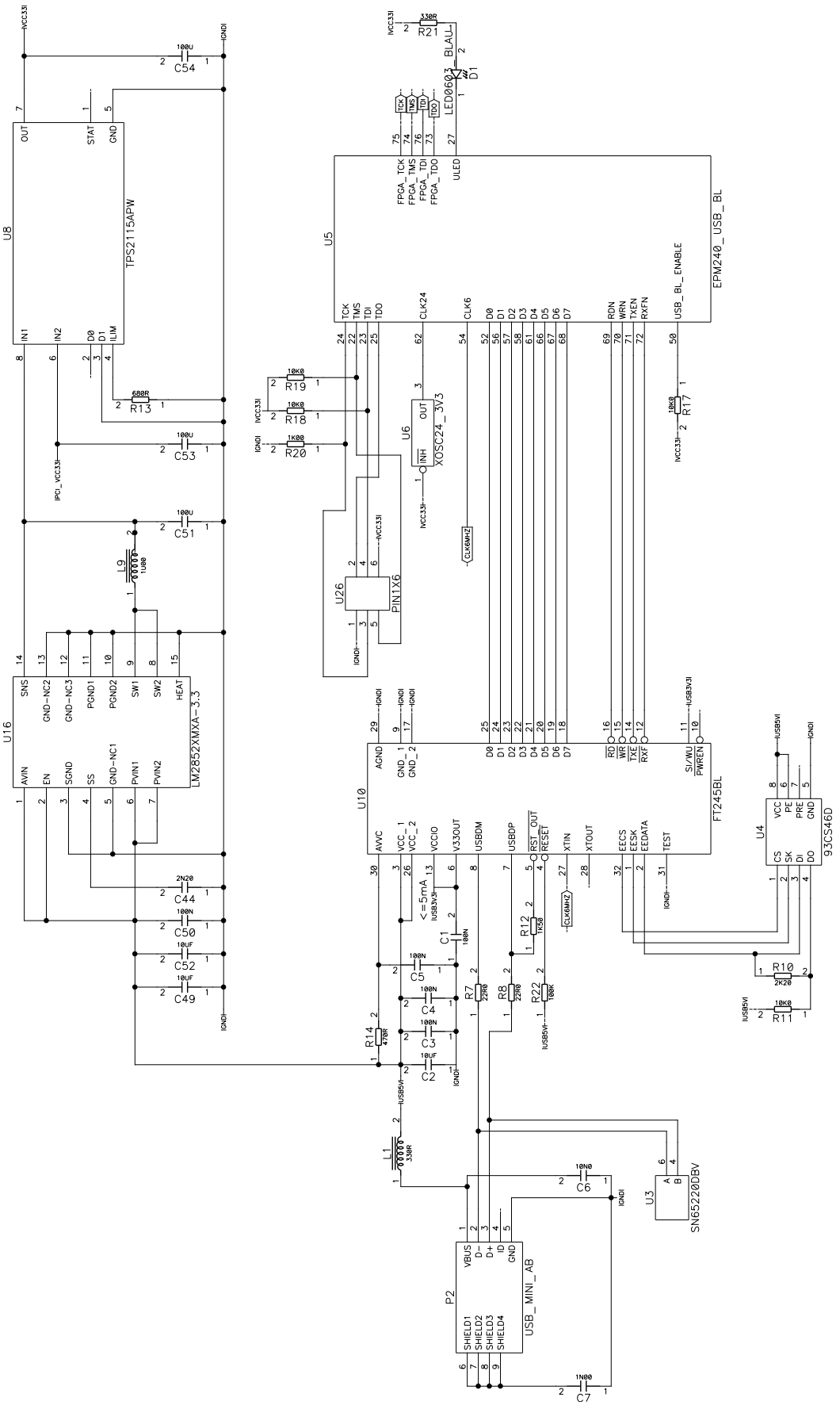
FPGA, Memory, IO



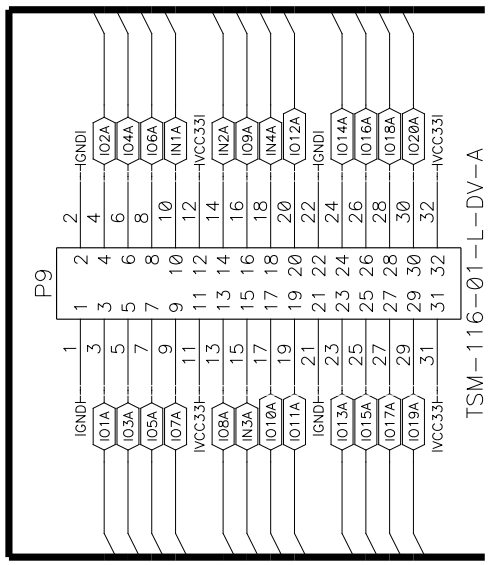
Power Supply



Embedded USB Blaster



IO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TSM-116-01-L-DV-A
IGND
IO1A
IO2A
IO3A
IO4A
IO5A
IO6A
IO7A
IN1A
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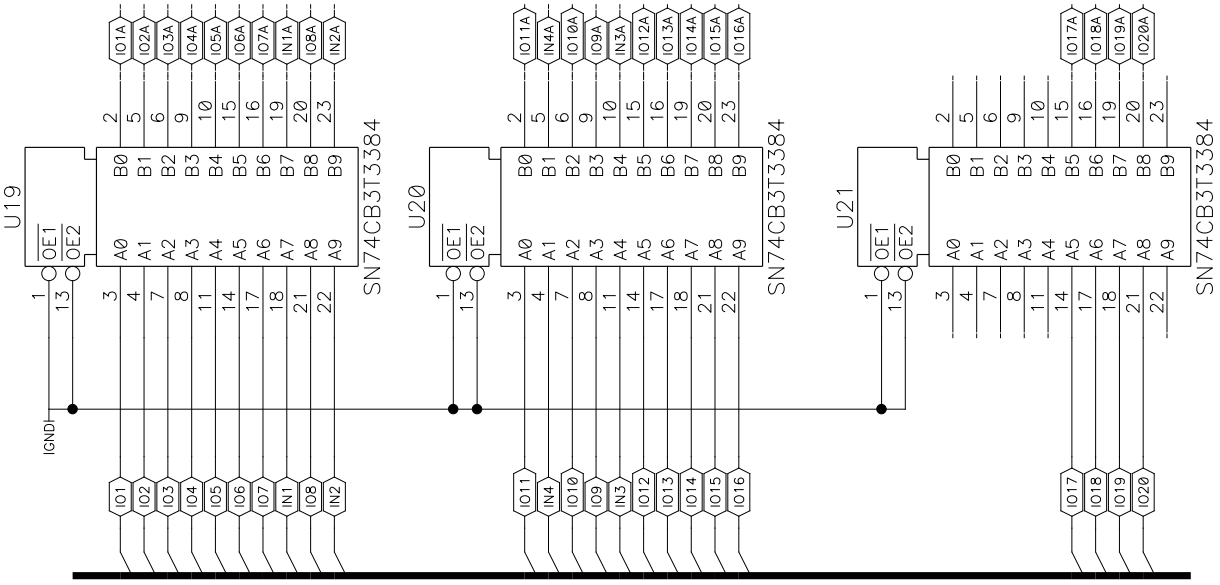
IN2A
IO8A
IO9A
IN3A
IO10A
IN4A
IO11A
IO12A
IO13A
IO14A
IO15A
IO16A
IO17A
IO18A
IO19A
IO20A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U20
U21
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OE2
A0
A1
A2
A3
A4
A5
A6
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A9
B0
B1
B2
B3
B4
B5
B6
B7
B8
B9
IGND
IO1
IO2
IO3
IO4
IO5
IO6
IO7
IN1
IO8
IN2
IO9
IN3
IO10
IN4
IO11
IO12
IO13
IO14
IO15
IO16
IO17
IO18
IO19
IO20

Board Top View

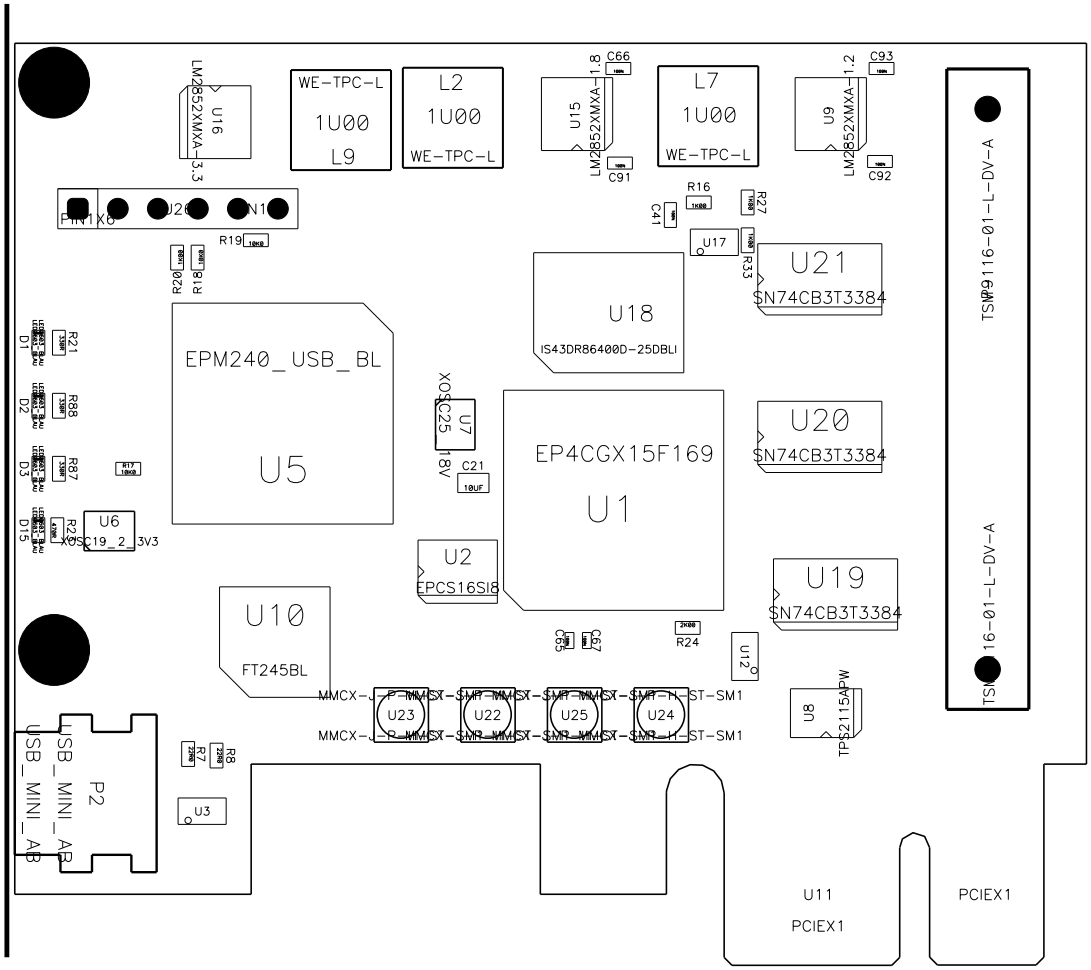


Figure 2

Board Bottom View

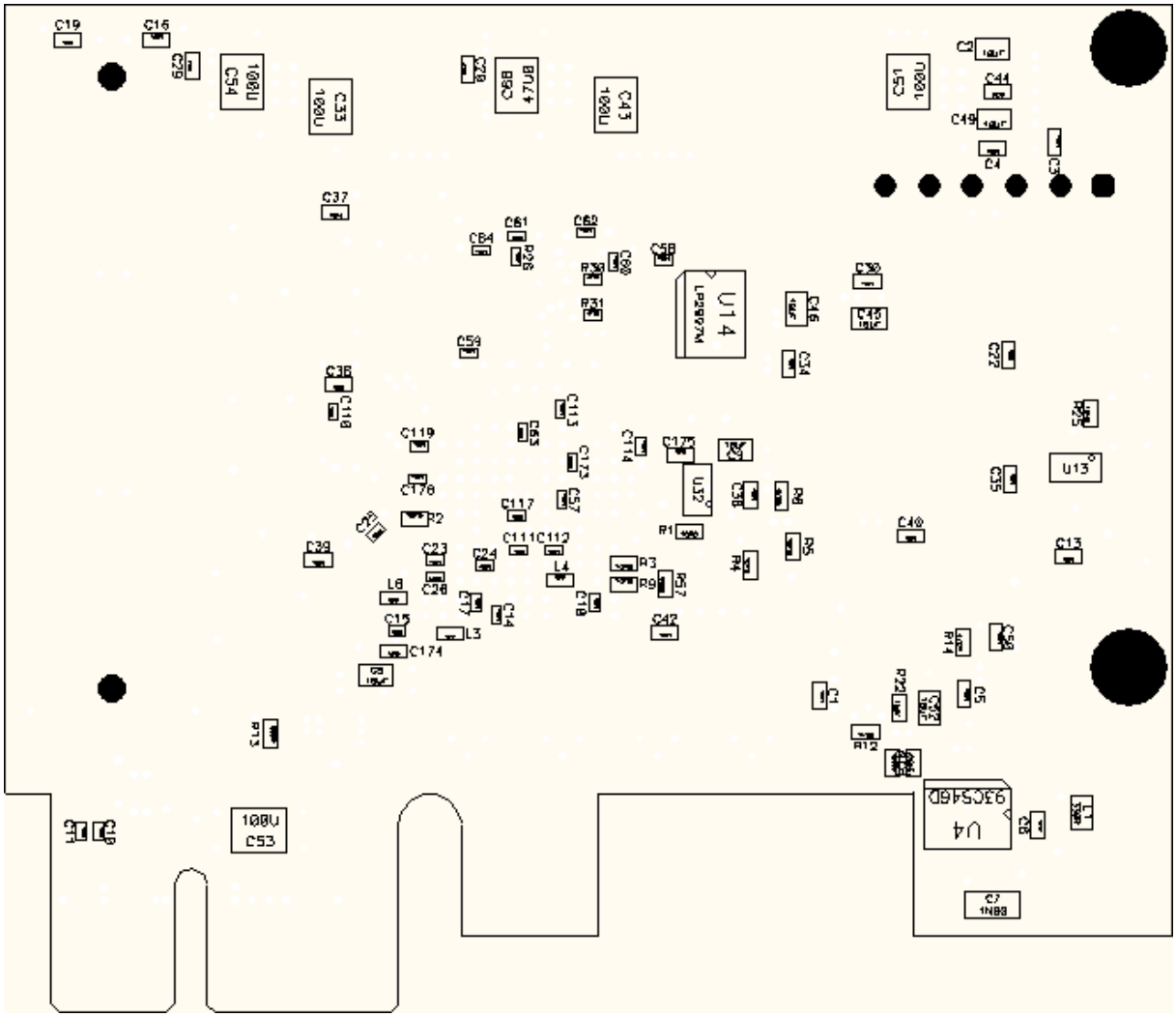


Figure 3

DB4CGX Add-On Boards

DB4CGX-COM1

The DB4CGX-COM1 Add-on Module contains two CAN driver, four RS485 driver and one RS232 Transceiver. All Signals are routed to a D-SUB26 connector.

CAN

The module contains 2 CAN driver SN75HVD233D. Table 8 shows the Pinning of D-SUB connector, Table 9 shows the routing to the FPGA: P19 and P21 can be used for CAN Termination.

Function	SUB-D Pin
CAN1-L	19
CAN1-H	10
CAN2-L	20
CAN2-H	11

Table 8

Function	P2 pinning	FPGA Signal	FPGA Pin
C1D	29	IO20	K10
C1R	30	IO19	N12
C2D	27	IO18	L11
C2R	28	IO17	N11

Table 9

RS285

Four RS485 drivers are implemented based on TI SN75HVD11D devices. Table 10 shows the Pinning of D-SUB connector,

R3R	17	IN4	E7
R3DE	19	IO12	N9
R3D	16	IN3	M7
R4R	13	IN2	N7
R4DE	14	IO8	L7
R4D	15	IO9	N8

Table 11 shows the routing to the FPGA:

ATTENTION : There is an error in the pinning of R3D This pin is routed to an input pin, instead of on output pin. This requires that we will change the pinout of the module!

Function	SUB-D Pin
RS485-1A	12
RS485-1B	21
RS485-2A	13
RS485-2B	22
RS485-3A	14

Function	SUB-D Pin
RS485-3B	23
RS485-4A	15
RS485-4B	24

Table 10

Function	P2 pinning	FPGA Signal	FPGA Pin
R1R	23	IO14	K9
R1DE	25	IO16	M11
R1D	26	IO15	N10
R2R	18	IO10	M9
R2DE	24	IO13	L9
R2D	20	IO11	K8
R3R	17	IN4	E7
R3DE	19	IO12	N9
R3D	16	IN3	M7
R4R	13	IN2	N7
R4DE	14	IO8	L7
R4D	15	IO9	N8

Table 11

RS232

The module contains RS232 driver. Table 8 shows the Pinning of D-SUB connector, Table 9 shows the routing to the FPGA:

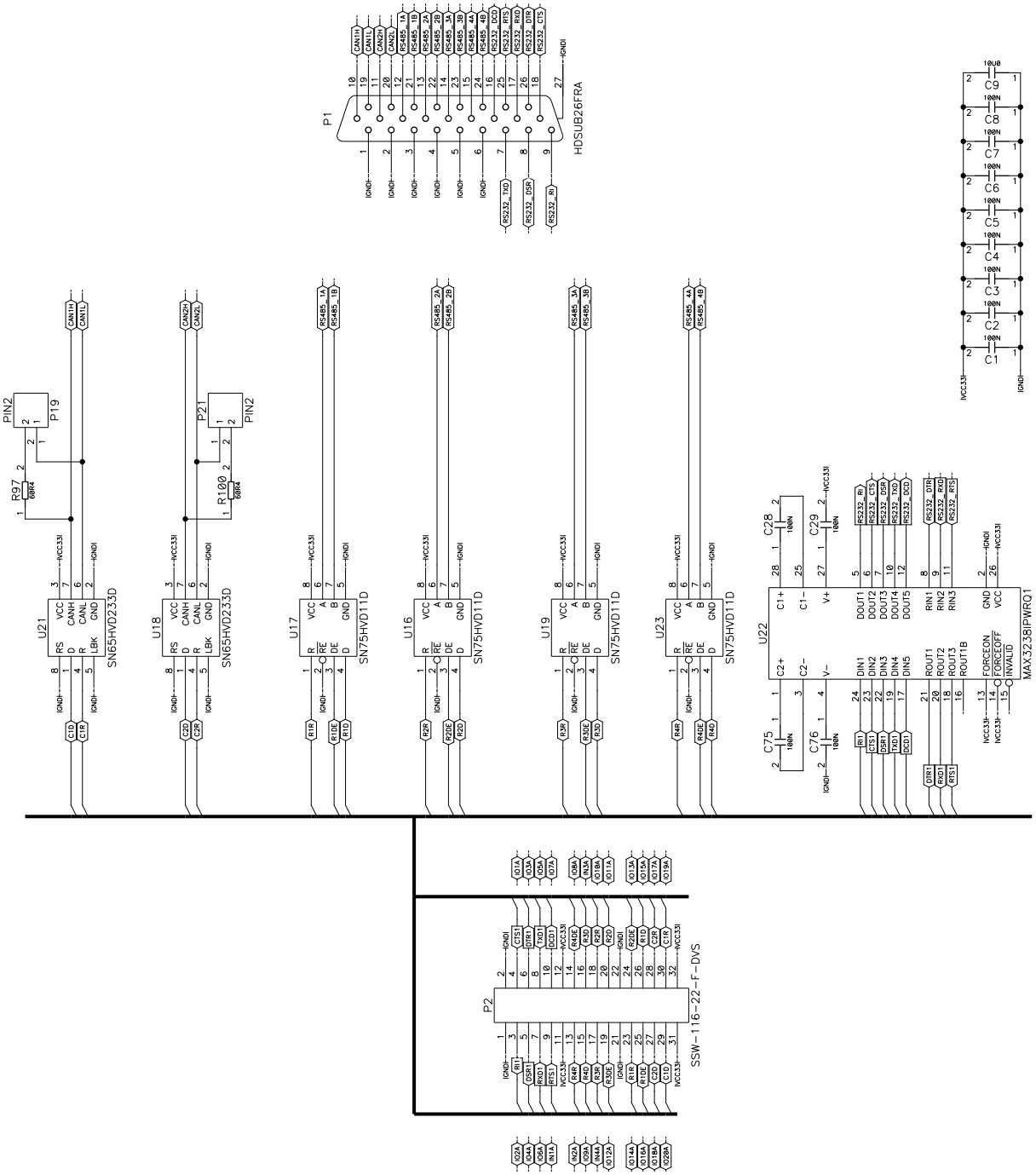
Function	SUB-D Pin
RS232-RI	9
RS232-CTS	18
RS232-DSR	8
RS232-TXD	7
RS232-DCD	16
RS232-DTR	26
RS232-RXD	17
RS232-RTS	25

Table 12

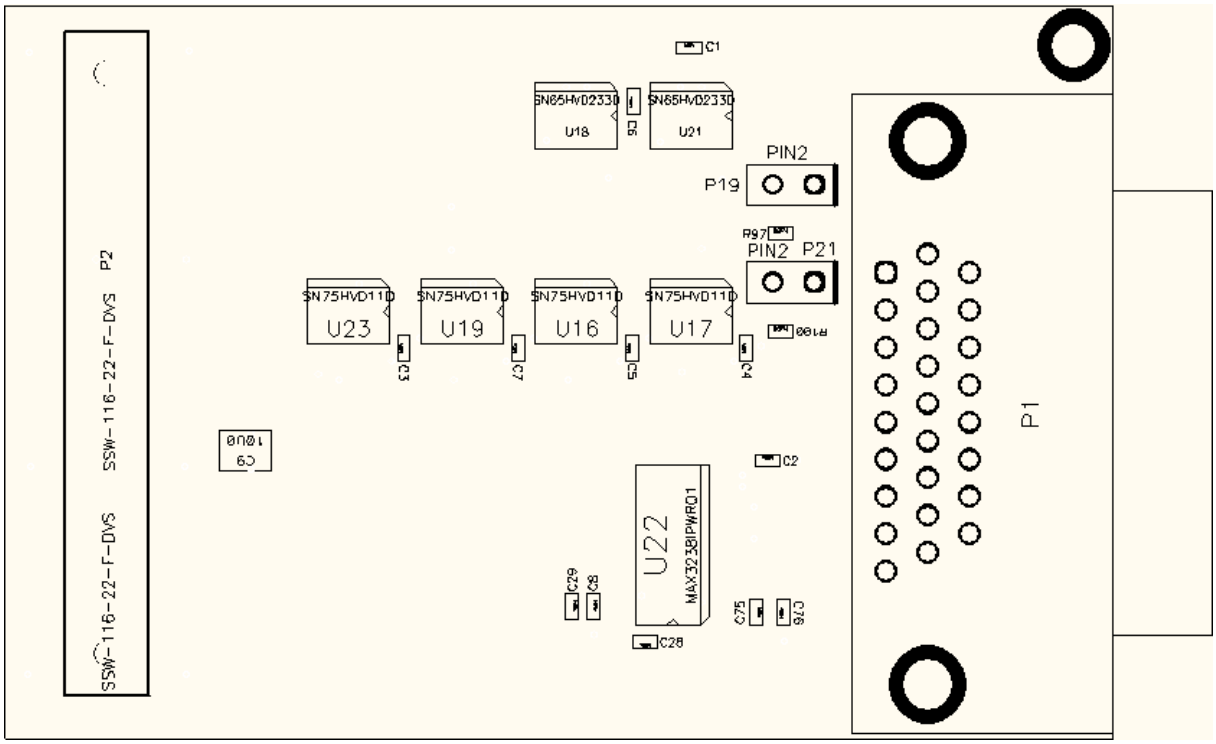
Function	P2 pinning	FPGA Signal	FPGA Pin
RI	3	IO2	M4
CTS	4	IO1	L4
DSR	5	IO4	N5
TXD	8	IO5	L5
DCD	10	IO7	M6
DTR	6	IO3	N4
RXD	7	IO6	N6
RTS	9	IN1	E6

Table 13

Schematic



Top View

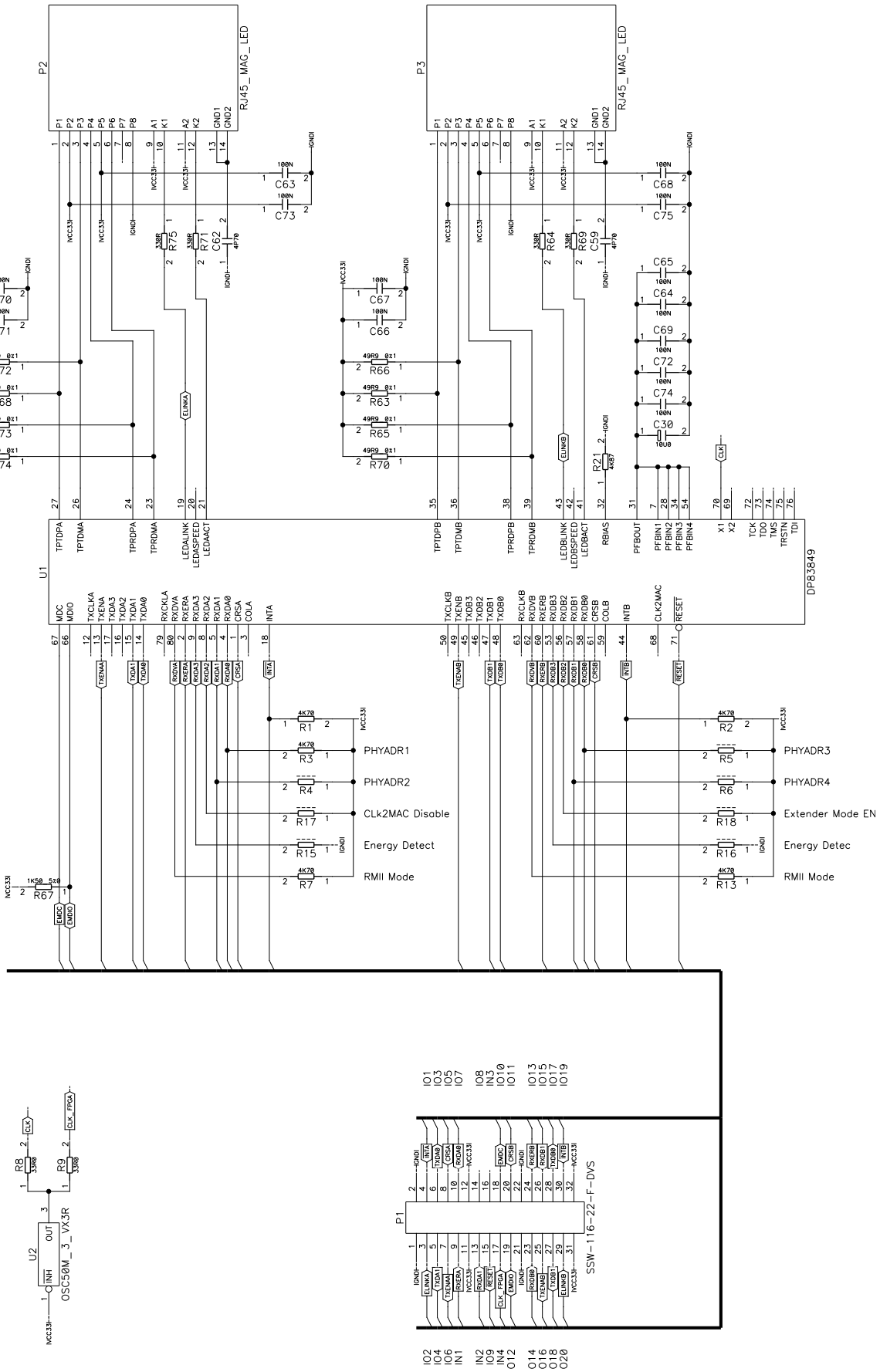

C1
SN65HVD233D
U18
C6
SN65HVD233D
U21
PIN2
P19
R97
PIN2
P21
SN75HVD11D
U23
SN75HVD11D
U19
SN75HVD11D
U16
SN75HVD11D
U17
C3
C7
C5
C4
C9
C2
U22
MAX3238IPWR01
C29
C8
C28
C75
C76
P1
SSW-116-22-F-DVS
P2
SSW-116-22-F-DVS

DB4CGX-PHY2

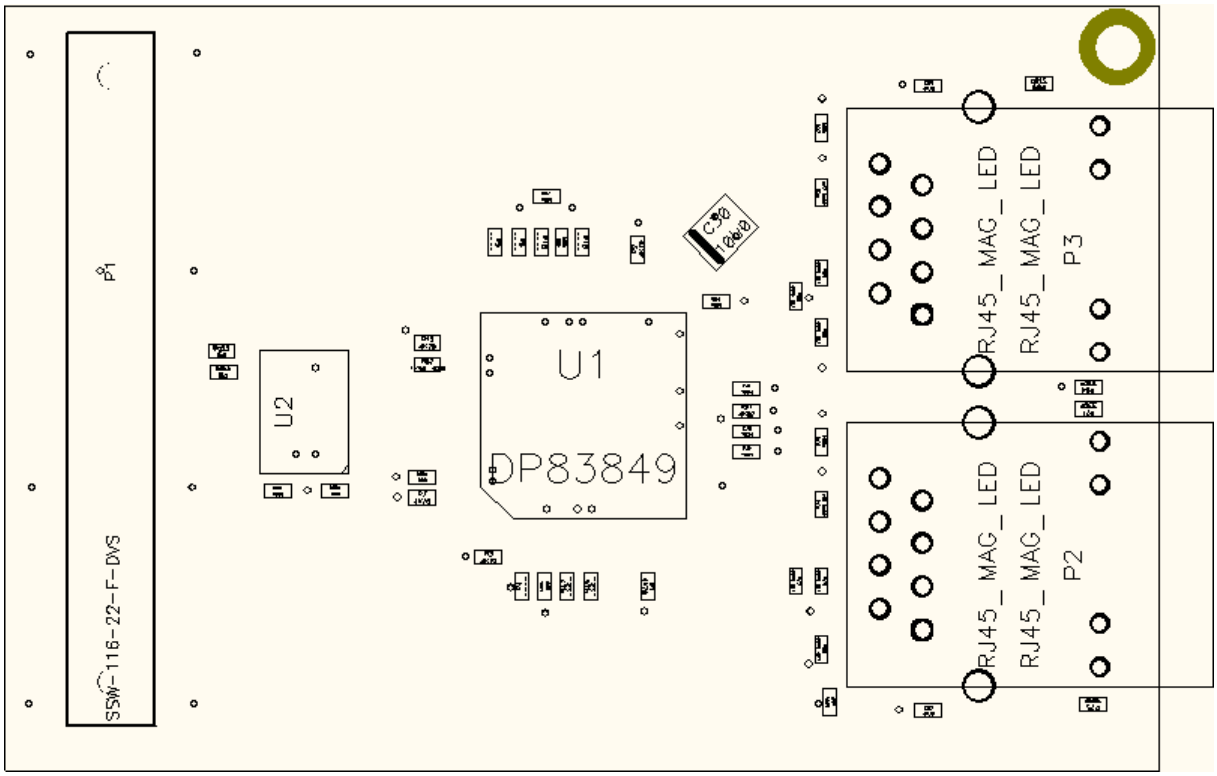
The DB4CGX-PHY2 add-on board contains a two 10/100 Ethernet Phys connected via RMII Interface to the base board.Datasheet is available at http://www.national.com/ds/DP/DP83849I.pdf
A 25Mhz crystal is implemented on the board that feeds the PHY and the FPGA.

Function	FPGA	P1 pinning		FPGA	Function
GND		1	2		GND
ELINKA	M4	3	4	L4	INTAn
TXDA1	N5	5	6	N4	TXDA0
TXENAA	N6	7	8	L5	CRSA
RXERA	E6	9	10	M6	RXDA0
VCC33		11	12		VCC33
RXDA1	N7	13	14	L7	
RESETn	N8	15	16	M7	
CLK_FPGA	E7	17	18	M9	EMDC
EMDIO	N9	19	20	K8	CRSB
GND		21	22		GND
RXDB0	K9	23	24	L9	RXERB
TXENAB	M11	25	26	N10	RXDB1
TXDB1	L11	27	28	N11	TXDB0
ELINKB	K10	29	30	N12	INTBn
VCC33		31	32		

Schematic


P2
RJ45_MAG_LED
P3
RJ45_MAG_LED
U1
DP83849
PHYADR1
PHYADR2
CLk2MAC Disable
Energy Detect
RMII Mode
PHYADR3
PHYADR4
Extender Mode EN
Energy Detec
RMII Mode
U2
OSC50M_3_VX3R
P1
SSW-116-22-F-DVS

Top View


P1
SSW-116-22-F-DVS
U2
U1
DP83849
RJ45_MAG_LED
RJ45_MAG_LED
P3
RJ45_MAG_LED
RJ45_MAG_LED
P2