National Semiconductor

May 6, 2011

LMP90100

Sensor AFE System: Multi-Channel, Low Power 24-Bit Sensor AFE with True Continuous Background Calibration

1.0 General Description

The LMP90100 is a highly integrated, multi-channel, low power 24-bit Sensor AFE. The device features a precision, 24-bit Sigma Delta Analog-to-Digital Converter (ADC) with a low-noise programmable gain amplifier and a fully differential high impedance analog input multiplexer. A true continuous background calibration feature allows calibration at all gains and output data rates without interrupting the signal path. The background calibration feature essentially eliminates gain and offset errors across temperature and time, providing measurement accuracy without sacrificing speed and power consumption.

Another feature of the LMP90100 is continuous background sensor diagnostics, allowing the detection of open and short circuit conditions and out-of-range signals, without requiring user intervention, resulting in enhanced system reliability.

Two sets of independent external reference voltage pins allow multiple ratiometric measurements. In addition, two matched programmable current sources are available to excite external sensors such as resistive temperature detectors and bridge sensors. Furthermore, seven GPIO pins are provided for interfacing to external LEDs and switches to simplify control across an isolation barrier.

Collectively, these features make the LMP90100 a complete analog front-end for low power, precision sensor applications such as temperature, pressure, strain gauge, and industrial process control. The LMP90100 is guaranteed over the extended temperature range of -40°C to +105°C and is available in a 28-pin TSSOP package.

2.0 Features

- 24-Bit Low Power Sigma Delta ADC
- True Continuous Background Calibration at all gains
- Low-Noise programmable gain (1x - 128x)
- Continuous background open/short and out of range sensor diagnostics
- 8 selectable output data rates (ODR) with single-cycle settling
- 2 matched excitation current sources from 100 µA to 1000 µA
- 4-DIFF / 7-SE flexible and programmable MUX channels
- 7 General Purpose Input/Output pins
- Chopper-stabilized buffer for low offset
- SPI 4 wire serial interface with CRC data link error correction
- Simultaneous 50 Hz & 60 Hz line rejection at ODR ≤13.42 SPS
- Independent gain and ODR selection per channel
- Supported by Webench Sensor AFE Designer
- Automatic Channel Sequencer

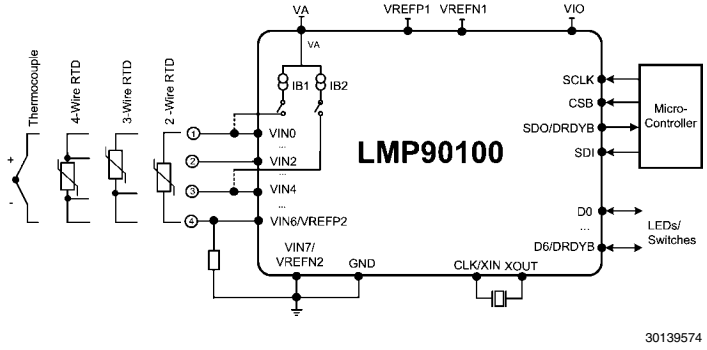
3.0 Key Specifications

ENOB/NFR	Up to 21.5/19 bits
Offset Error (typ)	8.4 nV
Gain Error (typ)	7 ppm
Total Noise	< 10 µV-rms
Integral Non-Linearity (INL max)	±15 ppm of FSR
Output Data Rates (ODR)	1.6775 SPS - 214.65 SPS
Analog Voltage, VA	+2.85V to +5.5V
Digital Input/Output Voltage, VIO	+2.7V to +5.5V
Operating Temp Range	-40°C to 105°C
Package	28-Pin TSSOP

4.0 Applications

- Temperature and Pressure Transmitters
- Strain Gauge Interface
- Industrial Process Control

5.0 Typical Application



TRI-STATE® is a registered trademark of National Semiconductor Corporation.

6.0 Block Diagram

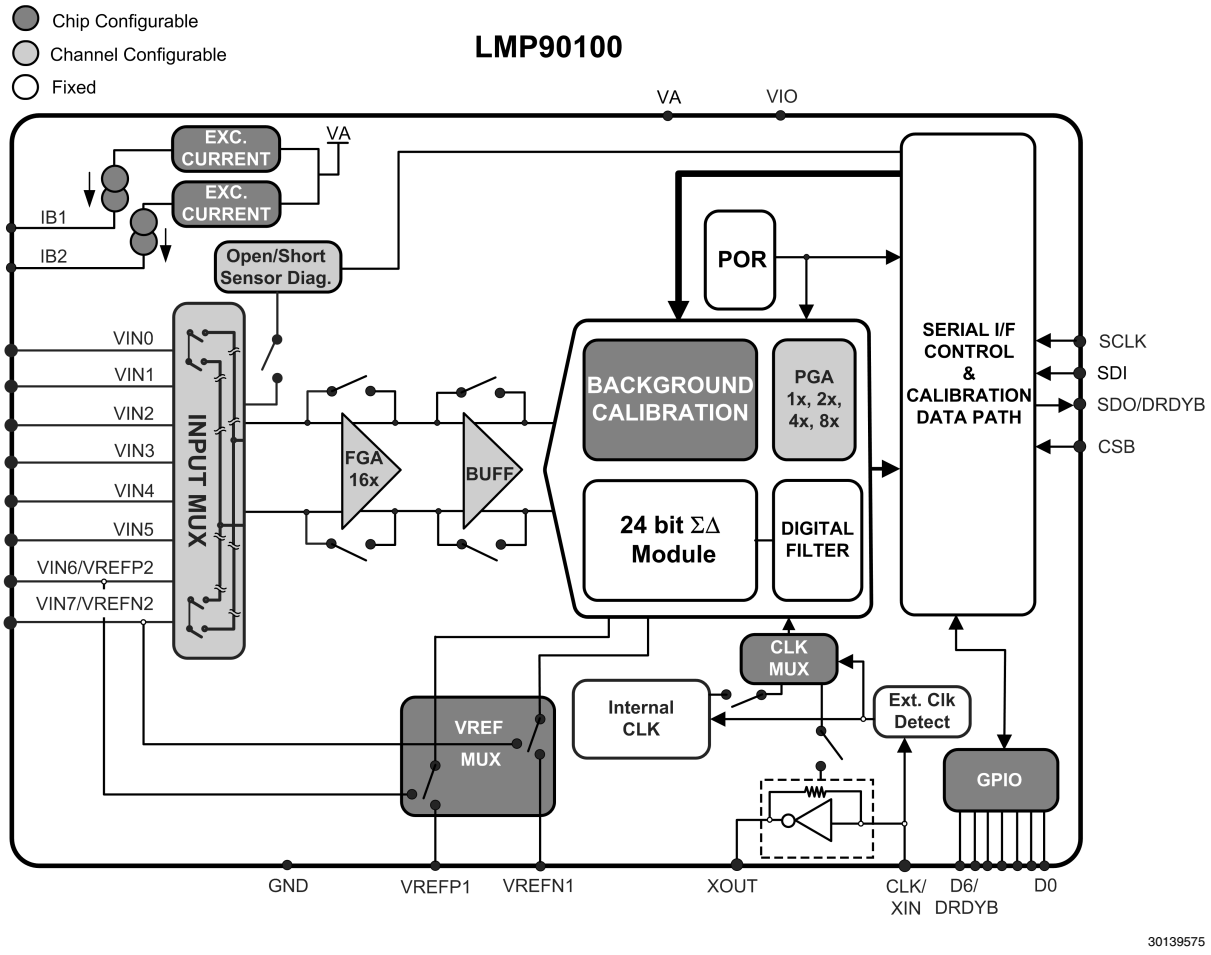


FIGURE 1. Block Diagram

• True Continuous Background Calibration

The LMP90100 features a 24 bit ΣΔ core with continuous background calibration to compensate for gain and offset errors in the ADC, virtually eliminating any drift with time and temperature. The calibration is performed in the background without user or ADC input interruption, making it unique in the industry and eliminating down time associated with field calibration required with other solutions. Having this continuous calibration improves performance over the entire life span of the end product.

• Continuous Background Sensor Diagnostics

Sensor diagnostics are also performed in the background, without interfering with signal path performance, allowing the detection of sensor shorts, opens, and out-of-range signals, which vastly improves system reliability. In addition, the fully flexible input multiplexer described below allows any input pin to be connected to any ADC input channel providing additional sensor path diagnostic capability.

• Flexible Input MUX Channels

The flexible input MUX allows interfacing to a wide range of sensors such as thermocouples, RTDs, thermistors, and bridge sensors. In its most common configuration, the LMP90100's multiplexer supports 4 differential channels. Each effective input voltage that is digitized is VIN = VINx – VINy, where $0 \leq x \leq 7$, $0 \leq y \leq 7$. In addition, the input multiplexer also supports 7 single-ended channels, where the common ground is any one of the VIN0 to VIN7 inputs.

• Programmable Gain Amplifiers (FGA & PGA)

The LMP90100 contains an internal 16x fixed gain amplifier (FGA) and a 1x, 2x, 4x, or 8x programmable gain amplifier (PGA). This allows accurate gain settings of 1x, 2x, 4x, 8x, 16x, 32x, 64x, or 128x through configuration of internal registers. Having an internal amplifier eliminates the need for external amplifiers that are costly, space consuming, and difficult to calibrate.

• Excitation Current Sources (IB1 & IB2)

Two matched internal excitation currents, IB1 and IB2, can be used for sourcing currents to a variety of sensors. The current range is from 100 µA to 1000 µA in steps of 100 µA.

Table of Contents

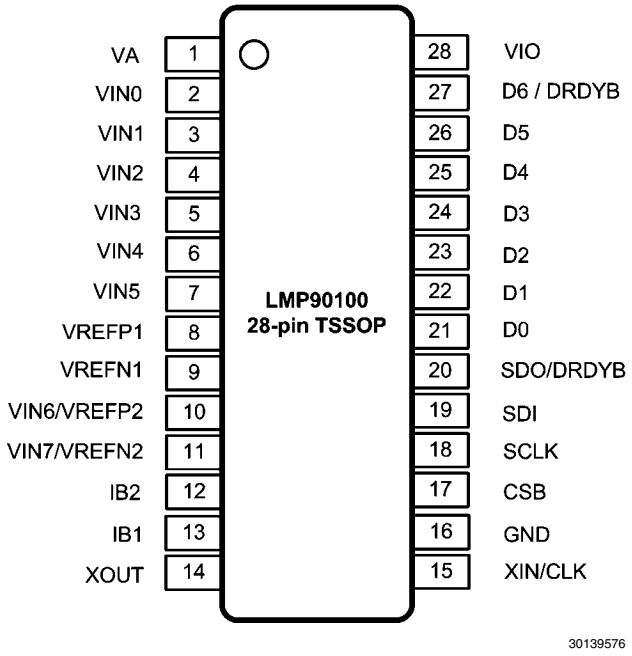
List of Figures

List of Tables

7.0 Ordering Information

Order Code	Temperature Range	Description
LMP90100MH/NOPB	−40°C to +105°C	28-Lead TSSOP Package, Rail of 48
LMP90100MHE/NOPB	−40°C to +105°C	28-Lead TSSOP Package, Reel of 250
LMP90100MHX/NOPB	−40°C to +105°C	28-Lead TSSOP Package, Reel of 2500

8.0 Connection Diagram



9.0 Pin Descriptions

Pin #	Pin Name	Type	Function
1	VA	Analog Supply	Analog power supply pin
2 - 7	VIN0 - VIN5	Analog Input	Analog input pins
8	VREFP1	Analog Input	Positive reference input
9	VREFN1	Analog Input	Negative reference input
10	VIN6 / VREFP2	Analog Input	Analog input pin or VREFP2 input
11	VIN7 / VREFN2	Analog Input	Analog input pin or VREFN2 input
12 - 13	IB2 & IB1	Analog output	Excitation current sources for external RTDs
14	XOUT	Analog output	External crystal oscillator connection
15	XIN / CLK	Analog input	External crystal oscillator connection or external clock input
16	GND	Ground	Power supply ground
17	CSB	Digital Input	Chip select bar
18	SCLK	Digital Input	Serial clock
19	SDI	Digital Input	Serial data input
20	SDO / DRDYB	Digital Output	Serial data output and data ready bar
21 - 26	D0 - D5	Digital IO	General purpose input/output (GPIO) pins
27	D6 / DRDYB	Digital IO	General purpose input/output pin or data ready bar
28	VIO	Digital Supply	Digtal input/output supply pin

10.0 Absolute Maximum Ratings (Note 1, Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Analog Supply Voltage, VA	-0.3V to 6.0V
Digital I/O Supply Voltage, VIO	-0.3V to 6.0V
Reference Voltage, VREF	-0.3V to VA+0.3V
Voltage on Any Analog Input Pin to GND (Note 3)	-0.3V to VA+0.3V
Voltage on Any Digital Input PIN to GND (Note 3)	-0.3V to VIO+0.3V
Voltage on SDO (Note 3)	-0.3V to VIO + 0.3V
Input Current at Any Pin (Note 3)	5mA
Output Current Source or Sink by SDO	3mA
Total Package Input and Output Current	20mA
ESD Susceptibility	
Human Body Model (HBM)	2500V
Machine Models (MM)	200V
Charged Device Model (CDM)	1250V
Junction Temperature (T_{JMAX})	+150°C
Storage Temperature Range	–65°C to +150°C
For soldering specifications:	
see product folder at www.national.com and www.national.com/ms/MS/MS-SOLDERING.pdf	

11.0 Operating Ratings

Analog Supply Voltage, VA	+2.85V to 5.5V
Digital I/O Supply Voltage, VIO	+2.7V to 5.5V
Full Scale Input Range, VIN	±VREF / PGA
Reference Voltage, VREF	+0.5V to VA
Temperature Range for Electrical Characteristics	T_{MIN} = –40°C T_{MAX} = +105°C
Operating Temperature Range	–40°C ≤ T_A ≤ +105°C
Junction to Ambient Thermal Resistance (θ_{JA}) (Note 4)	41°C/W

12.0 Electrical Characteristics

Unless otherwise noted, the key for the condition is (VA = VIO = VREF) / ODR (SPS) / buffer / calibration / gain . Boldface limits apply for T_{MIN} ≤ T_A ≤ T_{MAX}; the typical values apply for T_A = +25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
n	Resolution			24		Bits
ENOB / NFR	Effective Number of Bits and Noise Free Resolution	3V / all / ON / OFF / all. Shorted input.		Table 1		Bits
		5V / all / ON / OFF / all. Shorted input.		Table 3		Bits
ODR	Output Data Rates		1.6675	Table 1	214.6	SPS
	Gain	FGA × PGA	1	Table 1	128	
INL	Integral Non-Linearity	3V / 214.65 / ON / ON / 1	-15	± 7	+15	ppm of FSR
		3V & 5V / 214.65 / ON / ON / 16		± 15		ppm of FSR
	Total Noise	3V / all / ON / ON / all. Shorted input.		Table 2		µV
		5V / all / ON / OFF / all. Shorted input.		Table 4		µV
OE	Offset Error	3V & 5V / all / ON or OFF / ON / all		Below Noise Floor (rms)		µV
		3V / 214.65 / ON / ON / 1		1.22	9.52	µV
		3V / 214.65 / ON / ON / 128		0.00838	0.70	µV
		5V / 214.65 / ON / ON / 1		1.79	8.25	µV
		5V / 214.65 / ON / ON / 128		0.0112	0.63	µV
	Offset Drift Over Temp (Note 5)	3V & 5V / 214.65 / ON or OFF / OFF / 1-8		100		nV/°C
		3V & 5V / 214.65 / ON / ON / 1-8		3		nV/°C
		3V & 5V / 214.65 / ON / OFF / 16		25		nV/°C
		3V & 5V / 214.65 / ON / ON / 16		0.4		nV/°C
		3V & 5V / 214.65 / ON / OFF / 128		6		nV/°C
		3V & 5V / 214.65 / ON / ON / 128		0.125		nV/°C
	Offset Drift over Time (Note 5)	5V / 214.65 / ON / OFF / 1, T_A = 150°C		2360		nV / 1000 hours
		5V / 214.65 / ON / ON / 1, T_A = 150°C		100		nV / 1000 hours

Symbol	Parameter	Conditions	Min	Typ	Max	Units
GE	Gain Error	3V & 5V / 214.65 / ON / ON / 1	**-80**	7	**80**	ppm
		3V & 5V / 13.42 / ON / ON / 16		50		ppm
		3V & 5V / 13.42 / ON / ON / 64		50		ppm
		3V & 5V / 13.42 / ON / ON / 128		100		ppm
	Gain Drift over Temp (*Note 5*)	3V & 5V / 214.65 / ON / ON / all		0.5		ppm/°C
	Gain Drift over Time (*Note 5*)	5V / 214.65 / ON / OFF / 1, T_A = 150°C		5.9		ppm / 1000 hours
		5V / 214.65 / ON / ON / 1, T_A = 150°C		1.6		ppm / 1000 hours
CONVERTER'S CHARACTERISTIC						
CMRR	Input Common Mode Rejection Ratio	DC, 3V / 214.65 / ON / ON / 1	**70**	117		dB
		DC, 5V / 214.65 / OFF / OFF / 1	**90**	120		dB
		50/60 Hz, 5V / 214.65 / OFF / OFF / 1		117		dB
	Reference Common Mode Rejection	VREF = 2.5V		101		dB
PSRR	Power Supply Rejection Ratio	DC, 3V / 214.65 / ON / ON / 1	75	115		dB
		DC, 5V / 214.65 / ON / ON / 1		112		dB
NMRR	Normal Mode Rejection Ratio (*Note 5*)	50 Hz, 5V / 214.65 / OFF / OFF / 1	**89**	93	**100**	dB
		60 Hz, 5V / 214.65 / OFF / OFF / 1	**95**	100	**110**	dB
		47 Hz to 63 Hz, 5V / 13.42 / OFF / OFF / 1	**78**			dB
	Cross-talk	3V / 214.65 / OFF / OFF / 1	**95**	136		dB
		5V / 214.65 / OFF / OFF / 1	**95**	143		dB
POWER SUPPLY CHARACTERISTICS						
VA	Analog Supply Voltage		2.85	3.0	5.5	V
VIO	Digital Supply Voltage		2.7	3.3	5.5	V
IVA	Analog Supply Current	3V / 13.42 / OFF / OFF / 1, ext. CLK		400	**500**	µA
		5V / 13.42 / OFF / OFF / 1, ext. CLK		464	**555**	µA
		3V / 13.42 / ON / OFF / 64, ext. CLK		600	**700**	µA
		5V / 13.42 / ON / OFF / 64, ext. CLK		690	**800**	µA
		3V / 214.65 / ON / OFF / 64, int. CLK		1547	**1700**	µA
		5V / 214.65 / ON / OFF / 64, int. CLK		1760	**2000**	µA
		3V / 214.65 / OFF / OFF / 1, int. CLK		826	**1000**	µA
		5V / 214.65 / OFF / OFF / 1, int. CLK		941	**1100**	µA
		Standby, 3V , int. CLK		3	10	µA
		Standby, 3V , ext. CLK		257		µA
		Standby, 5V, int. CLK		5	15	µA
		Standby, 3V, ext. CLK		300		µA
		Power-down, 3V, int/ext CLK		2.6	**5**	µA
		Power-down, 5V, int/ext CLK		4.6	**9**	µA

Symbol	Parameter	Conditions	Min	Typ	Max	Units
REFERENCE INPUT						
VREFP	Positive Reference		VREFN + 0.5		VA	V
VREFN	Negative Reference		GND		VREFP - 0.5	V
VREF	Differential Reference	VREF = VREFP - VREFN	0.5		VA	V
ZREF	Reference Impedance	3V / 13.42 / OFF / OFF / 1		10		MOhm
IREF	Reference Input	3V / 13.42 / ON or OFF / ON or OFF / all		±2		µA
CREFP	Capacitance of the Positive Reference	(*Note 5*), gain = 1		6		pF
CREFN	Capacitance of the Negative Reference	(*Note 5*), gain = 1		6		pF
ILREF	Reference Leakage Current	Power-down		1		nA
ANALOG INPUT						
VINP	Positive Input (VIN0 - VIN7)	Gain = 1-8, buffer ON	GND + 0.1		VA - 0.1	V
		Gain = 16 - 128, buffer ON	GND + 0.4		VA - 1.5	V
		Gain = 1-8, buffer OFF	GND		VA	V
VINN	Negative Input (VIN0 - VIN7)	Gain = 1-8, buffer ON	GND + 0.1		VA - 0.1	V
		Gain = 16 - 128, buffer ON	GND + 0.4		VA - 1.5	V
		Gain = 1-8, buffer OFF	GND		VA	V
VIN	Differential Input	VIN = VINP - VINN		±VREF / PGA		
ZIN	Differential Input Impedance	ODR = 13.42 SPS		15.4		MOhm
CINP	Capacitance of the Positive Input	5V / 214.65 / OFF / OFF / 1		4		pF
CINN	Capacitance of the Negative Input	5V / 214.65 / OFF / OFF / 1		4		pF
IIN	Input Leakage Current	3V & 5V / 13.42 / ON / OFF / 1-8		500		pA
		3V & 5V / 13.42 / ON / OFF / 16 - 128		100		pA
DIGITAL INPUT CHARACTERISTICS at VA = VIO = VREF = 3.0V						
VIH	Logical "1" Input Voltage		0.7 x VIO			V
VIL	Logical "0" Input Voltage				0.3 x VIO	V
IIL	Digital Input Leakage Current		-10		+10	µA
VHYST	Digital Input Hysteresis			0.1 x VIO		V
DIGITAL OUTPUT CHARACTERISTICS at VA = VIO = VREF = 3.0V						
VOH	Logical "1" Output Voltage	Source 300 µA	2.6			V
VOL	Logical "0" Output Voltage	Sink 300 µA			0.4	V
IOZH, IOZL	TRI-STATE®Leakage Current		-10		10	µA
COUT	TRI-STATE Capacitance	(*Note 5*)		5		pF

Symbol	Parameter	Conditions	Min	Typ	Max	Units
EXCITATION CURRENT SOURCES CHARACTERISTICS						
IB1, IB2	Excitation Current Source Output			0, 100, 200, 300, 400, 500, 600, 700, 800, 900, 1000		µA
	IB1/IB2 Tolerance	VA = VREF = 3V	**-7**	2.5	**7**	%
		VA = VREF = 5V	**-3.5**	0.2	**3.5**	%
	IB1/IB2 Output Compliance Range	VA = 3.0V & 5.0V, IB1/IB2 = 100 µA to 1000 µA		VA - 0.8		V
	IB1/IB2 Regulation	VA = 5.0V, IB1/IB2 = 100 µA to 1000 µA		0.07		% / V
IBTC	IB1/IB2 Drift	VA = 3.0V		95		ppm/°C
		VA = 5.0V		60		ppm/°C
IBMT	IB1/IB2 Matching	3V & 5V / 214.65 / OFF / OFF / 1, IB1/IB2 = 100 µA		0.34	**1.53**	%
		3V & 5V / 214.65 / OFF / OFF / 1, IB1/IB2 = 200 µA		0.22	**1**	%
		3V & 5V / 214.65 / OFF / OFF / 1, IB1/IB2 = 300 µA		0.2	**0.85**	%
		3V & 5V / 214.65 / OFF / OFF / 1, IB1/IB2 = 400 µA		0.15	**0.8**	%
		3V & 5V / 214.65 / OFF / OFF / 1, IB1/IB2 = 500 µA		0.14	**0.7**	%
		3V & 5V / 214.65 / OFF / OFF / 1, IB1/IB2 = 600 µA		0.13	**0.7**	%
		3V & 5V / 214.65 / OFF / OFF / 1, IB1/IB2 = 700 µA		0.075	**0.65**	%
		3V & 5V / 214.65 / OFF / OFF / 1, IB1/IB2 = 800 µA		0.085	**0.6**	%
		3V & 5V / 214.65 / OFF / OFF / 1, IB1/IB2 = 900 µA		0.11	**0.55**	%
		3V & 5V / 214.65 / OFF / OFF / 1, IB1/IB2 = 1000 µA		0.11	**0.45**	%
IBMTC	IB1/IB2 Matching Drfit	VA = 3.0V & 5.0V, IB1/IB2 = 100 µA to 1000 µA		2		ppm/°C
INTERNAL/EXTERNAL CLK						
CLKIN	Internal Clock Frequency			893		kHz
CLKEXT	External Clock Frequency	(*Note 5*)	1.8	3.5717	7.2	MHz
	External Crystal Frequency	Input Low Voltage		0		V
		Input High Voltage		1		V
		Frequency	1.8	3.5717	7.2	MHz
		Start-up time		7		ms
SCLK	Serial Clock				10	MHz

TABLE 1. ENOB (Noise Free Resolution) vs. Sampling Rate and Gain at VA = VIO = VREF = 3V

ODR (SPS)	Gain							
	1	2	4	8	16	32	64	128
1.6775	20.5 (18)	20.5 (18)	19.5 (17)	19 (16.5)	20.5 (18)	19.5 (17)	19 (16.5)	18 (15.5)
3.355	20 (17.5)	20 (17.5)	19 (16.5)	18.5 (16)	20 (17.5)	19 (16.5)	18.5 (16)	17 (14.5)
6.71	19.5 (17)	19.5 (17)	18.5 (16)	18 (15.5)	19.5 (17)	18.5 (16)	17.5 (15)	17 (14.5)
13.42	19 (16.5)	18.5 (16)	18 (15.5)	17.5 (15)	19 (16.5)	18 (15.5)	17.5 (15)	16.5 (14)
26.83125	20.5 (18)	20 (17.5)	19.5 (17)	19 (16.5)	20 (17.5)	19 (16.5)	18 (15.5)	17.5 (15)
53.6625	20 (17.5)	19.5 (17)	19 (16.5)	18.5 (16)	19.5 (17)	18.5 (16)	17.5 (15)	17 (14.5)
107.325	19.5 (17)	19 (16.5)	18.5 (16)	18 (15.5)	19 (16.5)	18 (15.5)	17 (14.5)	16.5 (14)
214.65	19 (16.5)	18.5 (16)	18 (15.5)	17.5 (15)	18.5 (16)	17.5 (15)	17 (14.5)	16 (13.5)

TABLE 2. RMS Noise (μV) vs. Sampling Rate and Gain at VA = VIO = VREF = 3V

ODR (SPS)	Gain of the ADC							
	1	2	4	8	16	32	64	128
1.6775	3.08	1.90	1.53	1.27	0.23	0.21	0.15	0.14
3.355	4.56	2.70	2.21	1.67	0.34	0.27	0.24	0.26
6.71	6.15	4.10	3.16	2.39	0.51	0.40	0.37	0.35
13.42	8.60	5.85	4.29	3.64	0.67	0.54	0.51	0.49
26.83125	3.35	2.24	1.65	1.33	0.33	0.27	0.26	0.25
53.6625	4.81	3.11	2.37	1.90	0.44	0.39	0.37	0.36
107.325	6.74	4.51	3.38	2.66	0.63	0.54	0.52	0.49
214.65	9.52	6.37	4.72	3.79	0.90	0.79	0.72	0.70

TABLE 3. ENOB (Noise Free Resolution) vs. Sampling Rate and Gain at VA = VIO = VREF = 5V

SPS	Gain of the ADC							
	1	2	4	8	16	32	64	128
1.6775	21.5 (19)	21.5 (19)	20.5 (18)	20 (17.5)	21 (18.5)	20.5 (18)	19.5 (17)	18.5 (16)
3.355	21 (18.5)	21 (18.5)	20 (17.5)	19.5 (17)	20.5 (18)	20 (17.5)	19 (16.5)	18 (15.5)
6.71	20.5 (18)	20 (17.5)	19.5 (17)	19 (16.5)	20 (17.5)	19.5 (17)	19 (16.5)	17.5 (15)
13.42	20 (17.5)	19.5 (17)	19 (16.5)	18.5 (16)	20 (17.5)	19 (16.5)	18 (15.5)	17.5 (15)
26.83125	21.5 (19)	21 (18.5)	20.5 (18)	20 (17.5)	21 (18.5)	20 (17.5)	19.5 (17)	18 (15.5)
53.6625	21 (18.5)	20.5 (18)	20 (17.5)	19.5 (17)	20.5 (18)	19.5 (17)	18.5 (16)	17.5 (15)
107.325	20.5 (18)	20 (17.5)	19.5 (17)	19 (16.5)	20 (17.5)	19 (16.5)	18 (15.5)	17 (14.5)
214.65	20 (17.5)	19.5 (17)	19 (16.5)	18.5 (16)	19.5 (17)	18.5 (16)	17.5 (15)	16.5 (14)

TABLE 4. RMS Noise (μV) vs. Sampling Rate and Gain at VA = VIO = VREF = 5V

SPS	Gain of the ADC							
	1	2	4	8	16	32	64	128
1.6775	2.68	1.65	1.24	1.00	0.22	0.19	0.17	0.16
3.355	3.86	2.36	1.78	1.47	0.34	0.27	0.22	0.22
6.71	5.23	3.49	2.47	2.09	0.44	0.34	0.30	0.32
13.42	7.94	5.01	3.74	2.94	0.61	0.50	0.45	0.43
26.83125	2.90	1.86	1.34	1.08	0.29	0.24	0.23	0.23
53.6625	4.11	2.60	1.90	1.50	0.39	0.35	0.32	0.31
107.325	5.74	3.72	2.72	2.11	0.56	0.48	0.46	0.44
214.65	8.25	5.31	3.82	2.97	0.79	0.68	0.64	0.63

13.0 Timing Diagrams

Unless otherwise noted, specified limits apply for VA = VIO = 3.0V. Boldface limits apply for $T_{MIN} \leq T_A \leq T_{MAX}$; the typical values apply for T_A = +25°C.

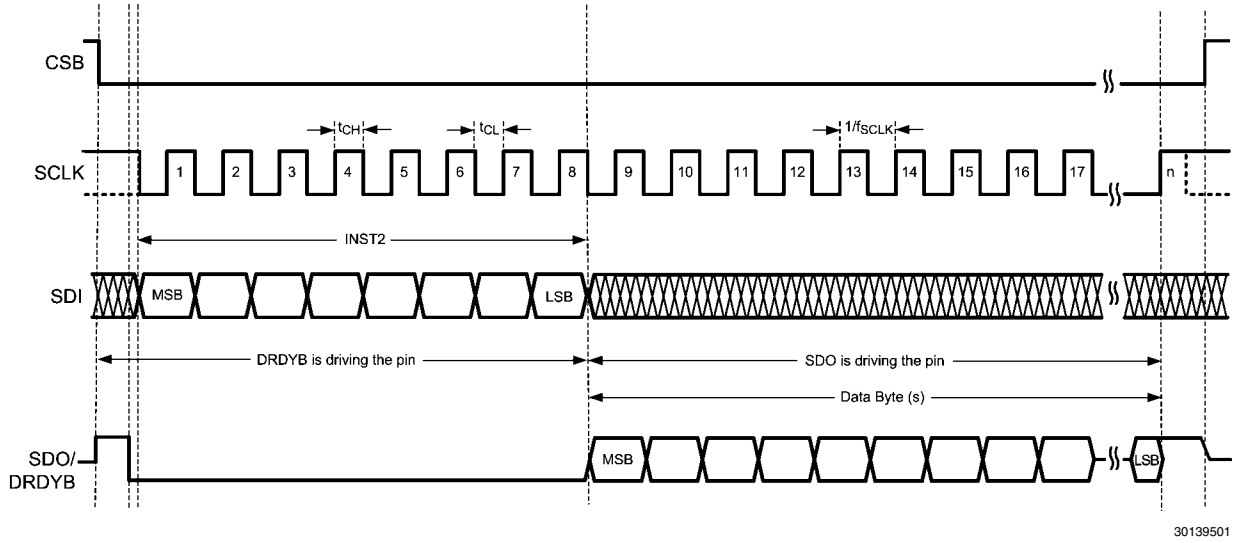
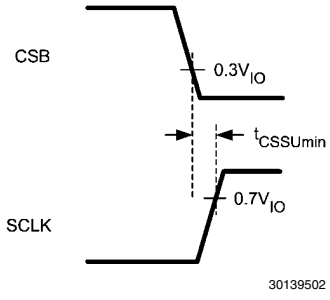
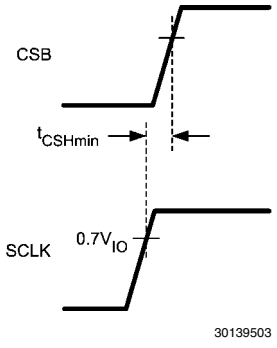


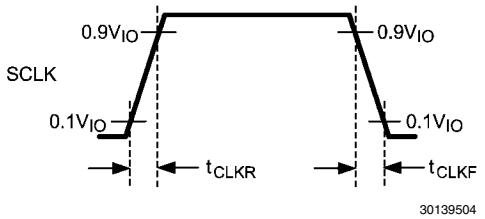
FIGURE 2. Timing Diagram

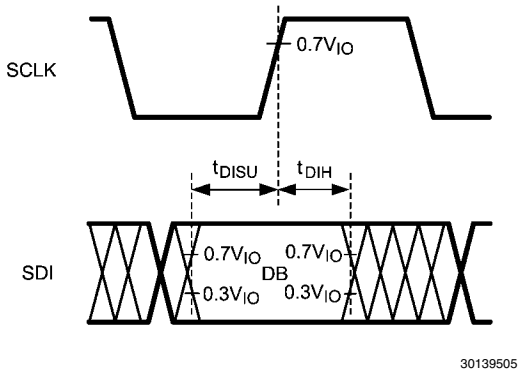
Symbol	Parameter	Conditions	Min	Typical	Max	Units
f_{SCLK}					10	MHz
t_{CH}	SCLK High time		0.4 / f_{SCLK}			ns
t_{CL}	SCLK Low time		0.4 / f_{SCLK}			ns



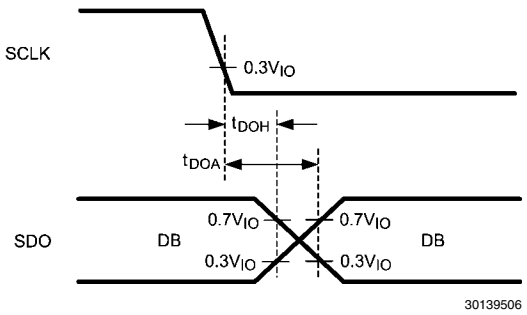


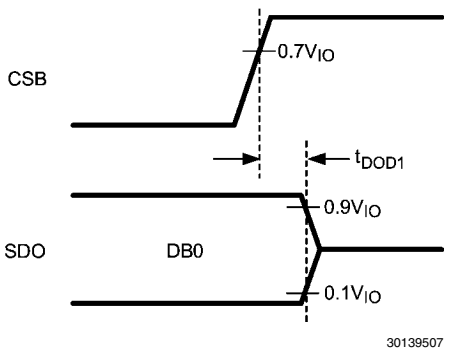
Symbol	Parameter	Conditions	Min	Typical	Max	Units
t_{CSSU}	CSB Setup time prior to an SCLK rising edge		5			ns
t_{CSH}	CSB Hold time after the last rising edge of SCLK		6			ns



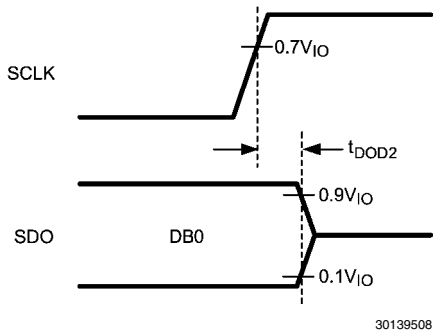


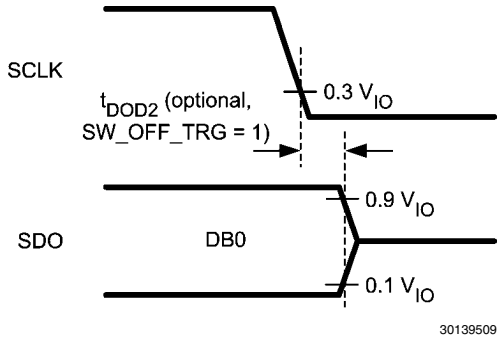
Symbol	Parameter	Conditions	Min	Typical	Max	Units
t_{CLKR}	SCLK Rise time			1.15		ns
t_{CLKF}	SCLK Fall time			1.15		ns
t_{DISU}	SDI Setup time prior to an SCLK rising edge		5			ns
t_{DIH}	SDI Hold time after an SCLK rising edge		6			ns



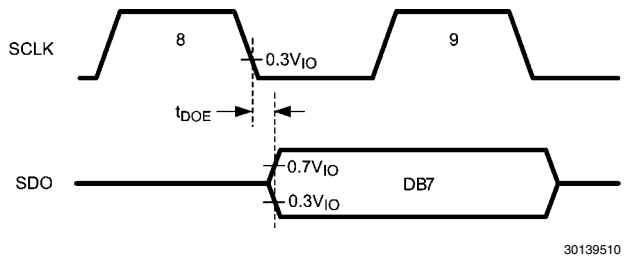


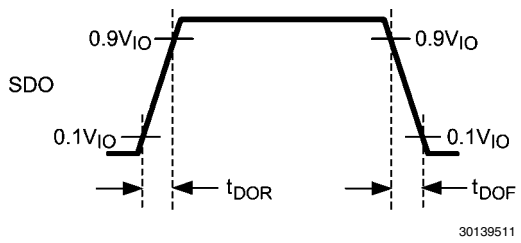
Symbol	Parameter	Conditions	Min	Typical	Max	Units
t_{DOA}	SDO Access time after an SCLK falling edge				35	ns
t_{DOH}	SDO Hold time after an SCLK falling edge		5			ns
t_{DOD1}	SDO Disable time after the rising edge of CSB				5	ns





Symbol	Parameter	Conditions	Min	Typical	Max	Units
t_{DOD2}	SDO Disable time after either edge of SCLK				27	ns





Symbol	Parameter	Conditions	Min	Typical	Max	Units
t_{DOE}	SDO Enable time from the falling edge of the 8th SCLK				35	ns
t_{DOR}	SDO Rise time	(*Note 5*)		7		ns
t_{DOF}	SDO Fall time	(*Note 5*)		7		ns
t_{DRDYB}	Data Ready Bar pulse at every 1/ODR second, see *Figure 19*	ODR ≤ 13.42 SPS		64		µs
		13.42 < ODR ≤ 214.65 SPS		4		µs

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to GND, unless otherwise specified

Note 3: When the input voltage (VIN) exceeds the power supply (VIN < GND or VIN > VA), the current at that pin must be limited to 5mA and VIN has to be within the Absolute Maximum Rating for that pin. The 20 mA package input current rating limits the number of pins that can safely exceed the power supplies with current flow to four pins.

Note 4: The maximum power dissipation is a function of $T_{J(MAX)}$ AND θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / \theta_{JA}$.

Note 5: This parameter is guaranteed by design and/or characterization and is not tested in production.

14.0 Specific Definitions

COMMON MODE REJECTION RATIO is a measure of how well in-phase signals common to both input pins are rejected. To calculate CMRR, the change in output offset is measured while the common mode input voltage is changed.

CMRR = 20 LOG(ΔCommon Input / ΔOutput Offset)

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) – says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits. LMP90100's ENOB is a DC ENOB spec, not the dynamic ENOB that is measured using FFT and SINAD. Its equation is as follows:

$$\text{ENOB} = \log_2\left(\frac{2 \times \text{VREF/Gain}}{\text{RMS Noise}}\right)$$

GAIN ERROR is the deviation from the ideal slope of the transfer function.

INTEGRAL NON-LINEARITY (INL) is a measure of the deviation of each individual code from a straight line through the input to output transfer function. The deviation of any given code from this straight line is measured from the center of that code value. The end point fit method is used. INL for this product is specified over a limited range, per the Electrical Tables.

NEGATIVE FULL-SCALE ERROR is the difference between the differential input voltage at which the output code transitions to negative full scale and (-VREF + 1LSB).

NEGATIVE GAIN ERROR is the difference between the negative full-scale error and the offset error divided by (VREF / Gain).

NOISE FREE RESOLUTION is a method of specifying the number of bits for a converter with noise.

$$\text{NFR} = \log_2\left(\frac{2 \times \text{VREF/Gain}}{\text{Peak-to-Peak Noise}}\right)$$

ODR Output Data Rate.

OFFSET ERROR is the difference between the differential input voltage at which the output code transitions from code 0000h to 0001h and 1 LSB.

POSITIVE FULL-SCALE ERROR is the difference between the differential input voltage at which the output code transitions to positive full scale and (VREF – 1LSB).

POSITIVE GAIN ERROR is the difference between the positive full-scale error and the offset error divided by (VREF / Gain).

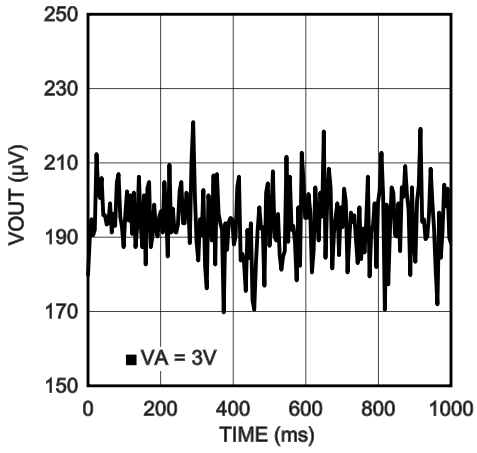
POWER SUPPLY REJECTION RATIO (PSRR) is a measure of how well a change in the analog supply voltage is rejected. PSRR is calculated from the ratio of the change in offset error for a given change in supply voltage, expressed in dB.

PSRR = 20 LOG (ΔVA / ΔOutput Offset)

15.0 Typical Performance Characteristics

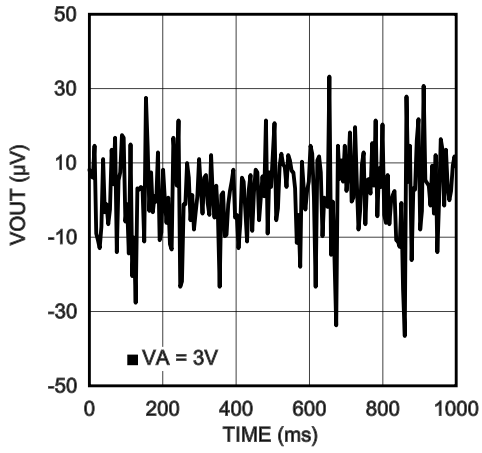
Unless otherwise noted, specified limits apply for VA = VIO = VREF = 3.0V. The maximum and minimum values apply for $T_A = T_{MIN}$ to T_{MAX}; the typical values apply for T_A = +25°C.

Noise Measurement without Calibration at Gain = 1



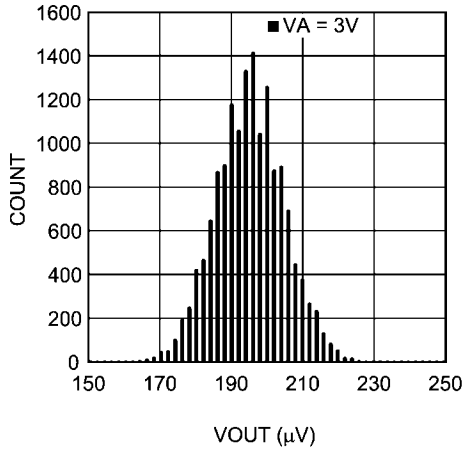
30139515

Noise Measurement with Calibration at Gain = 1



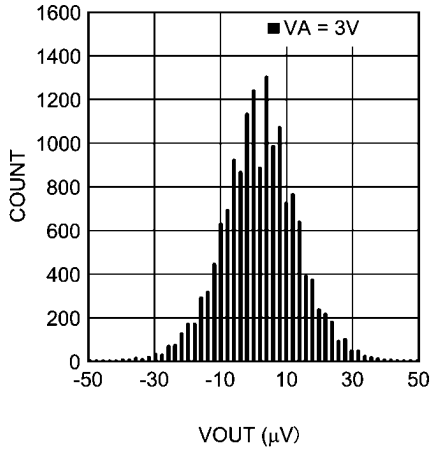
30139516

Histogram without Calibration at Gain = 1



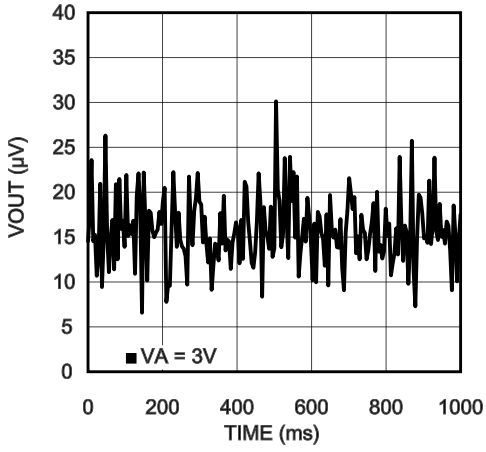
30139521

Histogram with Calibration at Gain = 1



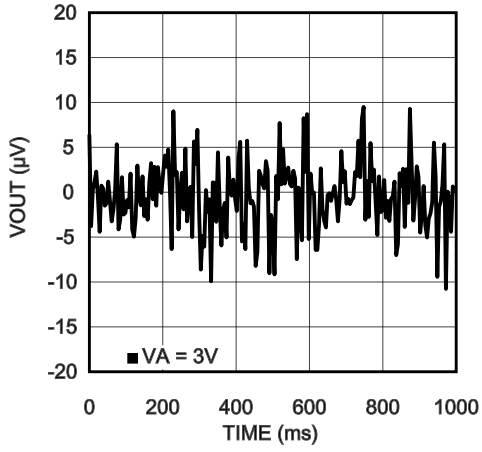
30139522

Noise Measurement without Calibration at Gain = 8



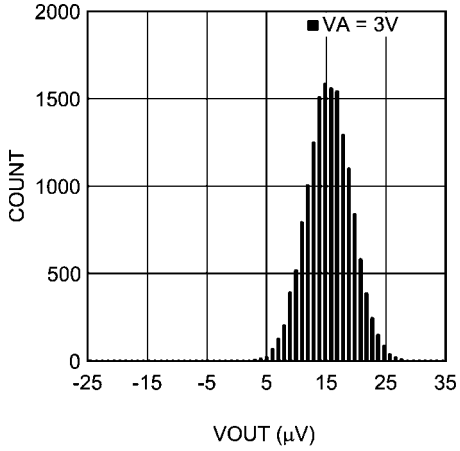
30139517

Noise Measurement with Calibration at Gain = 8



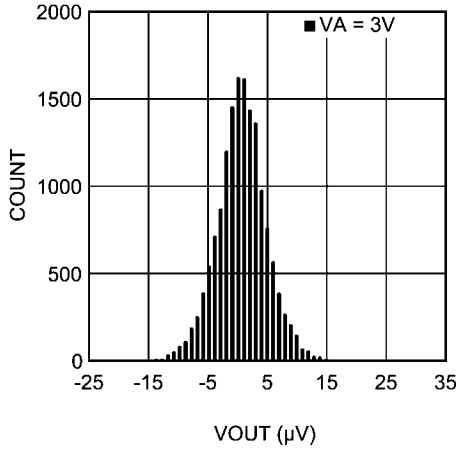
30139518

Histogram without Calibration at Gain = 8



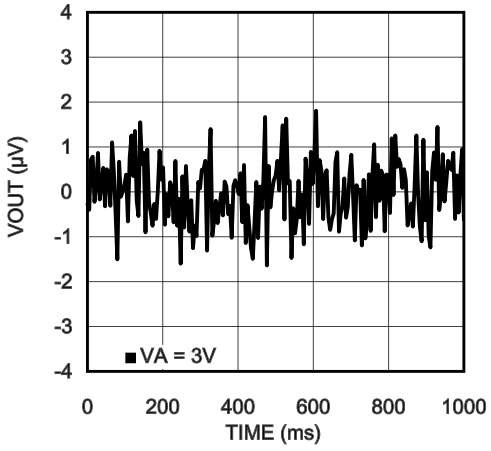
30139523

Histogram with Calibration at Gain = 8



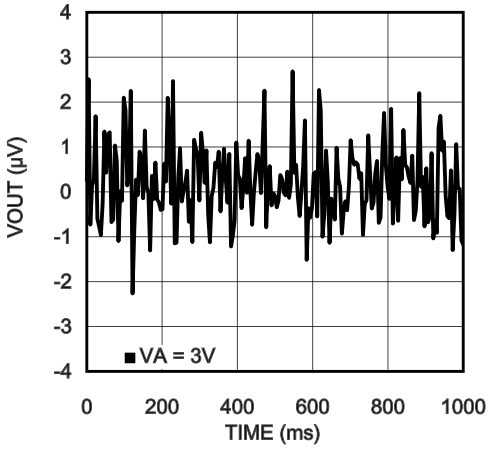
30139524

Noise Measurement without Calibration at Gain = 128



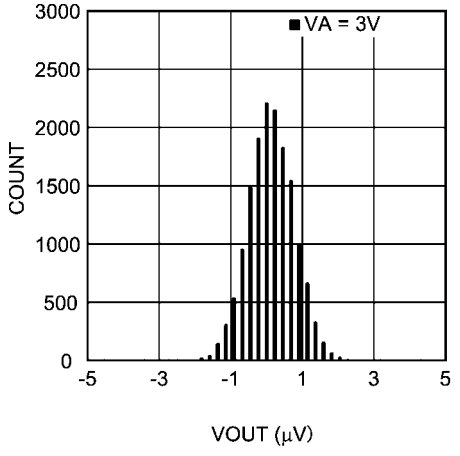
30139519

Noise Measurement without Calibration at Gain = 128



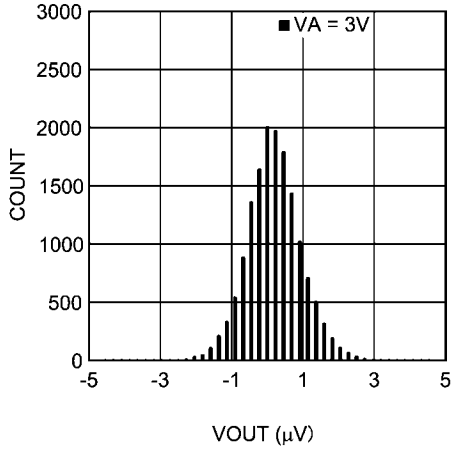
30139520

Histogram without Calibration at Gain = 128



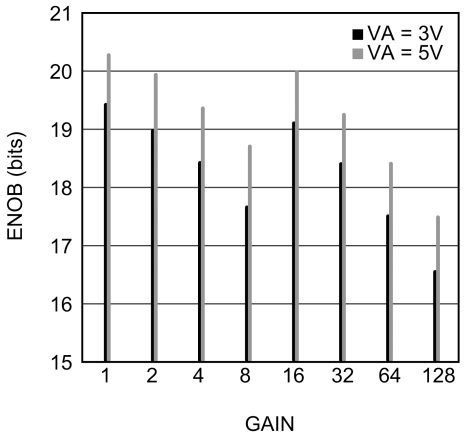
30139525

Histogram with Calibration at Gain = 128



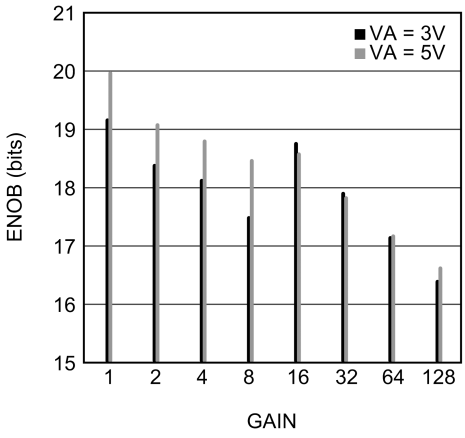
30139526

ENOB vs. Gain without Calibration at ODR = 13.42 SPS



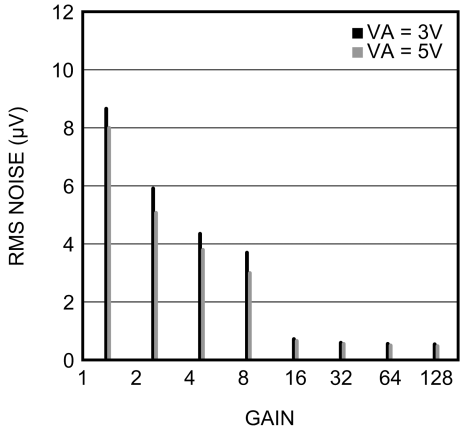
30139528

ENOB vs. Gain with Calibration at ODR = 13.42 SPS



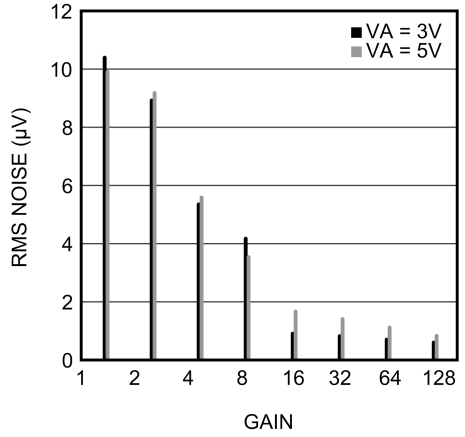
30139534

Noise vs. Gain without Calibration at ODR = 13.42 SPS



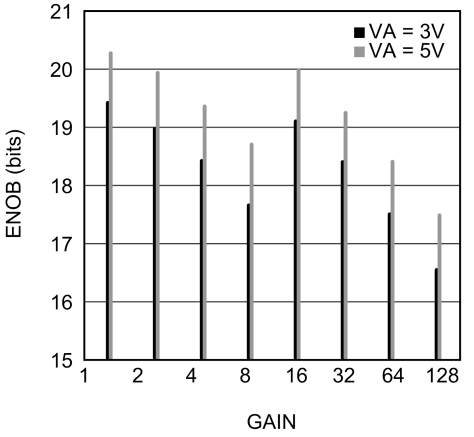
30139541

Noise vs. Gain with Calibration at ODR = 13.42 SPS



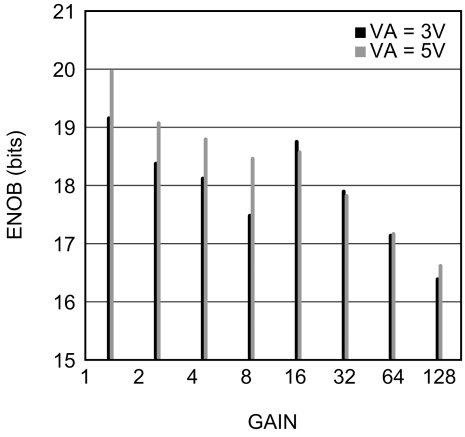
30139548

ENOB vs. Gain without Calibration at ODR = 214.65 SPS



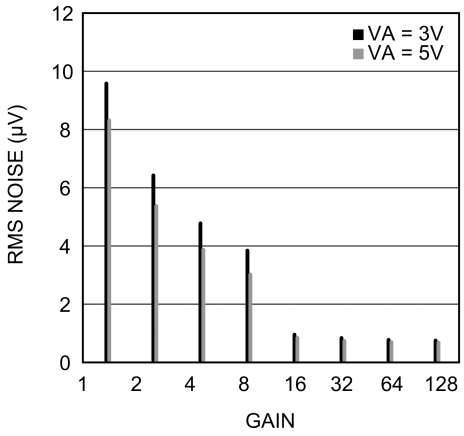
30139535

ENOB vs. Gain with Calibration at ODR = 214.65 SPS



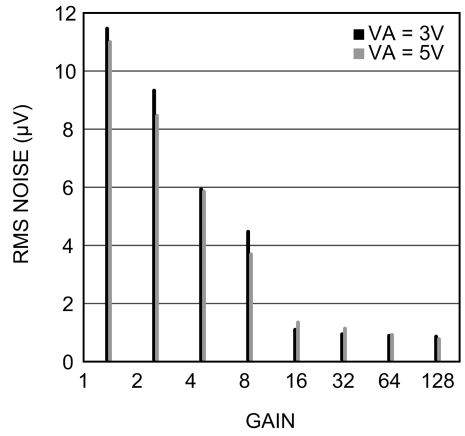
30139540

Noise vs. Gain without Calibration at ODR = 214.65 SPS



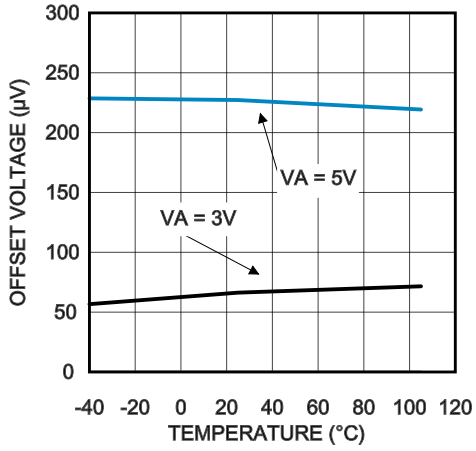
30139549

Noise vs. Gain with Calibration at ODR = 214.65 SPS



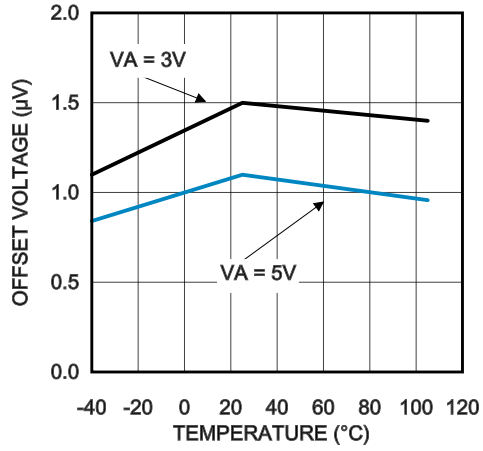
30139550

Offset Error vs. Temperature without Calibration at Gain = 1



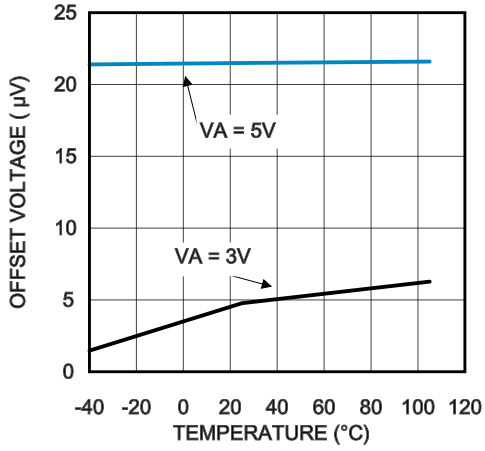
30139561

Offset Error vs. Temperature with Calibration at Gain = 1



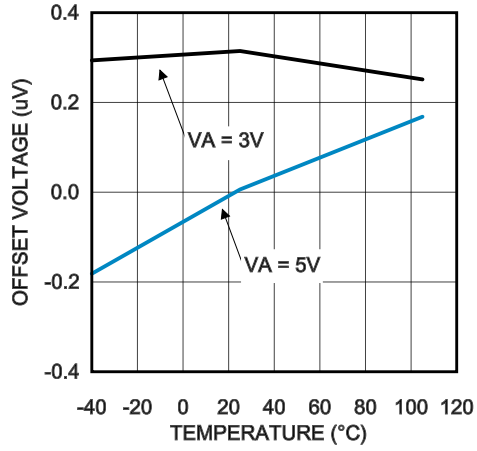
30139564

Offset Error vs. Temperature without Calibration at Gain = 8



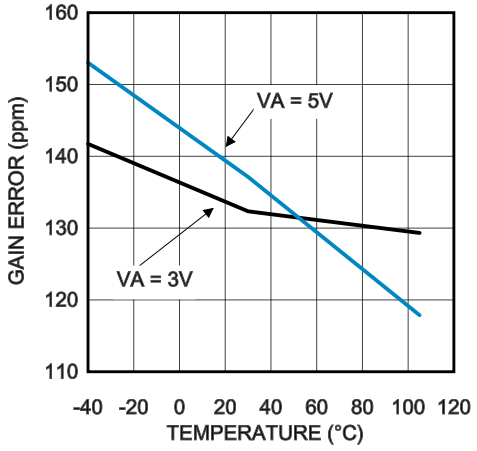
30139562

Offset Error vs. Temperature with Calibration at Gain = 8



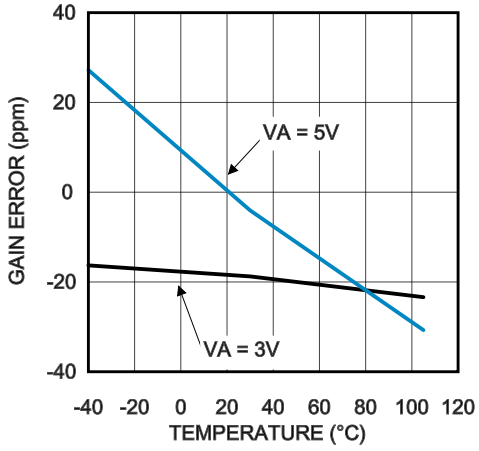
30139565

Gain Error vs. Temperature without Calibration at Gain = 1



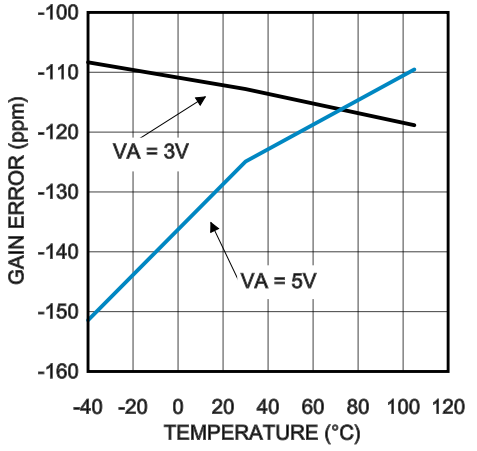
30139567

Gain Error vs. Temperature with Calibration at Gain = 1



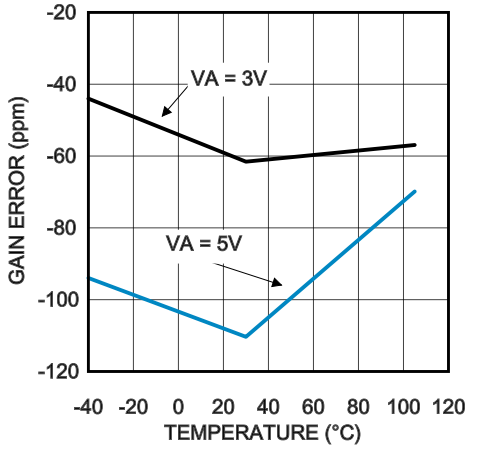
30139570

Gain Error vs. Temperature without Calibration at Gain = 8



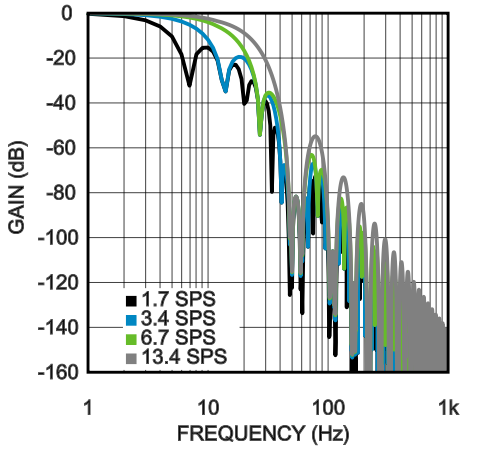
30139568

Gain Error vs. Temperature with Calibration at Gain = 8



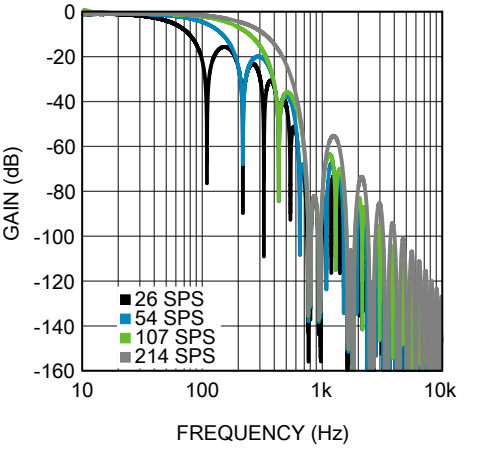
30139571

Digital Filter Frequency Response

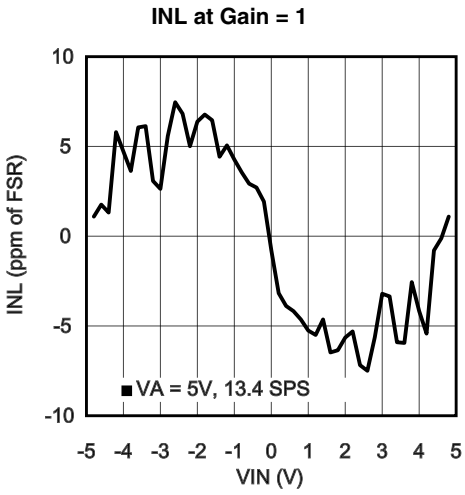


30139551

Digital Filter Frequency Response



30139554


INL at Gain = 1
10
5
0
-5
-10
INL (ppm of FSR)
VA = 5V, 13.4 SPS
-5 -4 -3 -2 -1 0 1 2 3 4 5
VIN (V)

30139527

16.0 Functional Description

The LMP90100 is a low-power 24-Bit ΣΔ ADC with 4 fully differential or 7 single-ended analog channels. Its serial data output is two's complement format. The output data rate (ODR) ranges from 1.6775 SPS to 214.65 SPS.

The serial communication for LMP90100 is SPI, a synchronous serial interface that operates using 4 pins: chip select bar (CSB), serial clock (SCLK), serial data in (SDI), and serial data out / data ready bar (SDO/DRYDYB).

True continuous built-in offset and gain background calibration is also available to improve measurement accuracy. Unlike other ADCs, the LMP90100's background calibration can run without interrupting the input signal. This unique technique allows for positive as well as negative gain calibration and is available at all gain settings.

The registers can be found in *Section 18.0 Registers*, and a detailed description of the LMP90100 are provided in the following sections.

16.1 SIGNAL PATH

16.1.1 Reference Input (VREF)

The differential reference voltage VREF (VREFP – VREFN) sets the range for VIN.

The muxed VREF allows the user to choose between VREF1 or VREF2 for each channel. This selection can be made by programming the VREF_SEL bit in the CHx_INPUTCN registers (CHx_INPUTCN: VREF_SEL). The default mode is VREF1. If VREF2 is used, then VIN6 and VIN7 cannot be used as inputs because they share the same pin.

Refer to *Section 17.2.2 VREF* for VREF applications information.

16.1.2 Flexible Input MUX (VIN)

LMP90100 provides a flexible input MUX as shown in *Figure 3*. The input that is digitized is VIN = VINP – VINN; where VINP can be any of the VIN0 to VIN7 input, and VINN can be any of the VIN0 to VIN7 input.

The digitized input is also known as a channel, where CH = VIN = VINP – VINN. Thus, there are a maximum of 4 differential channels: CH0, CH1, CH2, and CH3.

LMP90100 can also be configured single-endedly, where the common ground is any one of the VIN0 to VIN7 inputs. There are a maximum of 7 single-ended channels: CH0, CH1, CH2, CH3, CH4, CH5, and CH6.

The input MUX can be programmed in the CHx_INPUTCN registers. For example, to program CH0 = VIN = VIN4 – VIN1, go to the CH0_INPUTCN register and set:

1. VINP = 0x4
2. VINN = 0x1

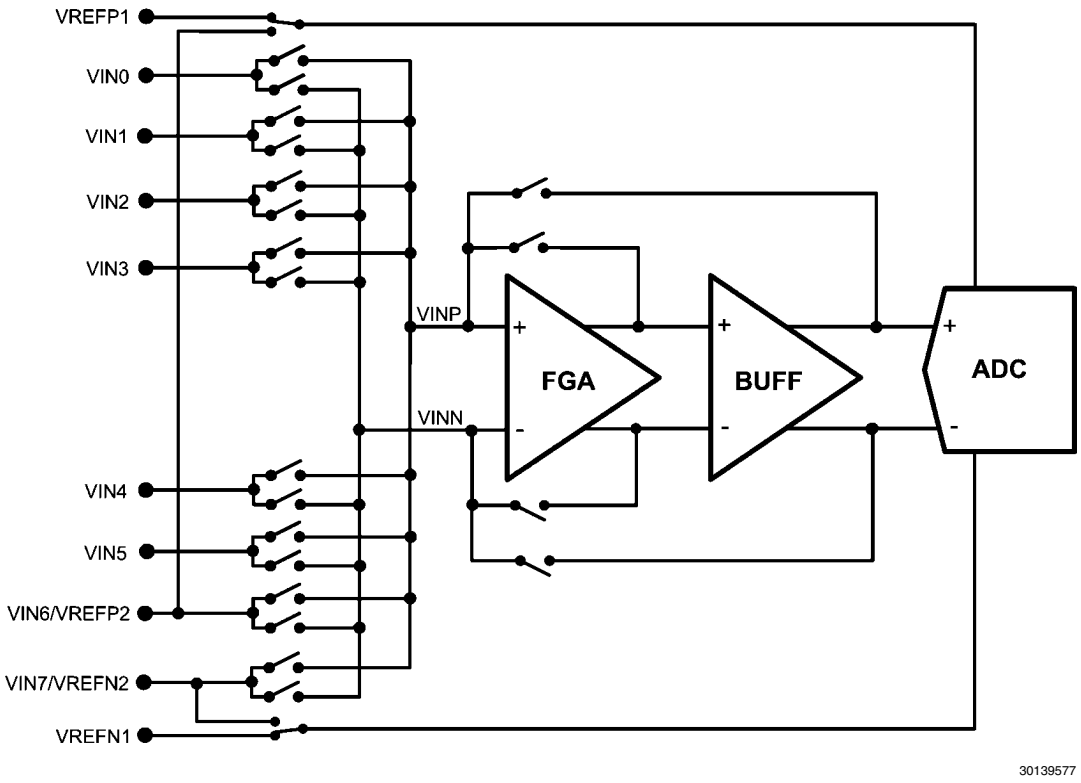


FIGURE 3. Simplified VIN Circuitry

16.1.3 Selectable Gains (FGA & PGA)

LMP90100 provides two types of gain amplifiers: a fixed gain amplifier (FGA) and a programmable gain amplifier (PGA). FGA has a fixed gain of 16x or it can be bypassed, while the PGA has programmable gain settings of 1x, 2x, 4x, or 8x.

Total gain is defined as FGA x PGA. Thus, LMP90100 provides gain settings of 1x, 2x, 4x, 8x, 16x, 32x, 64x, or 128x with true continuous background calibration.

The gain is channel specific, which means that one channel can have one gain, while another channel can have the same or a different gain.

The gain can be selected by programming the CHx_CONFIG: GAIN_SEL bits.

16.1.4 Buffer (BUFF)

There is an internal unity gain buffer that can be included or excluded from the signal path. Including the buffer provides a high input impedance but increases the power consumption.

When gain ≥ 16, the buffer is automatically included in the signal path. When gain < 16, including or excluding the buffer from the signal path can be done by programming the CHX_CONFIG: BUF_EN bit.

16.1.5 Internal/External CLK Selection

LMP90100 allows two clock options: internal CLK or external CLK (crystal (XTAL) or clock source).

There is an "External Clock Detection" mode, which detects the external XTAL if it is connected to XOUT and XIN. When operating in this mode, the LMP90100 shuts off the internal clock to reduce power consumption. Below is a flow chart to help set the appropriate clock registers.

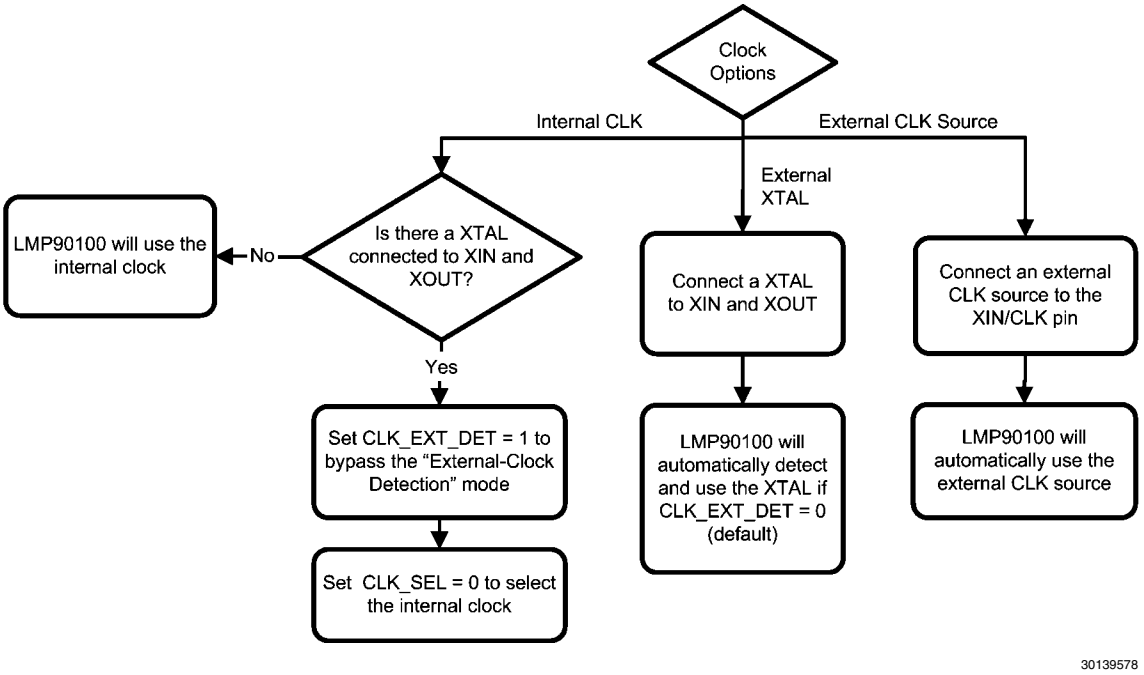


FIGURE 4. CLK Register Settings

The recommended value for the external CLK is discussed in the next sections.

16.1.6 Programmable ODRs

If using the internal CLK or external CLK of 3.5717 MHz, then the output date rates (ODR) can be selected (using the ODR_SEL bit) as:

1. 13.42/8 = 1.6775 SPS
2. 13.42/4 = 3.355 SPS
3. 13.42/2 = 6.71SPS
4. 13.42 SPS
5. 214.65/8 = 26.83125 SPS
6. 214.65/4 = 53.6625 SPS
7. 214.65/2 = 107.325 SPS
8. 214.65 SPS (default)

If the internal CLK is not being used and the external CLK is not 3.5717 MHz, then the ODR will be different. If this is the case, use the equation below to calculate the new ODR values.

$$ODR\_Base1 = (CLK_{EXT}) / (266{,}240)$$

$$ODR\_Base2 = (CLK_{EXT}) / (16{,}640)$$

$$ODR1 = (ODR\_Base1) / n, \text{ where } n = 1,2,4,8$$

$$ODR2 = (ODR\_Base2) / n, \text{ where } n = 1,2,4,8$$

For example, a 3.6864 MHz XTAL or external clock has the following ODR values:

ODR_Base1 = (3.6864 MHz) / (266,240) = 13.85 SPS

ODR_Base2 = (3.6864 MHz) / (16,640) = 221.54 SPS

ODR1 = (13.85 SPS) / n = 13.85, 6.92, 3.46, 1.73 SPS

ODR2 = (221.54 SPS) / n = 221.54, 110.77, 55.38, 27.69 SPS

The ODR is channel specific, which means that one channel can have one ODR, while another channel can have the same or a different ODR.

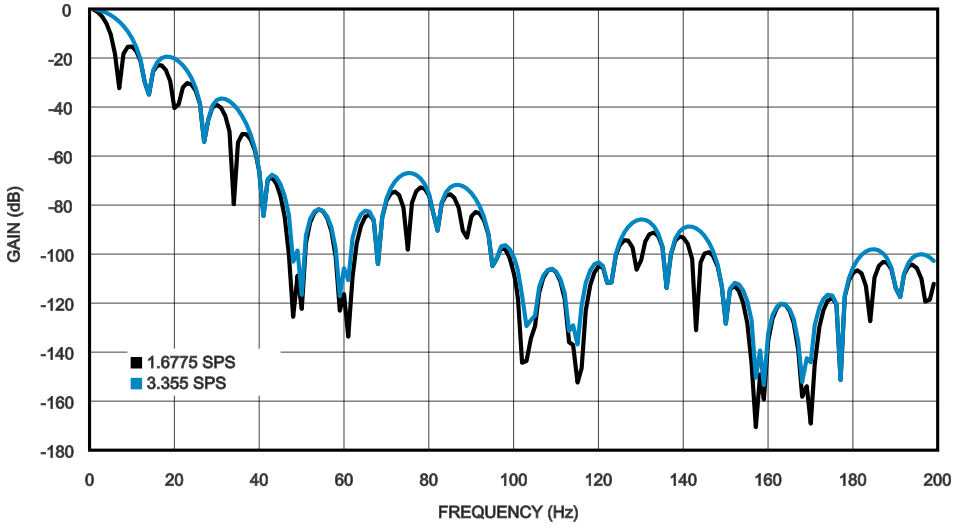
Note that these ODRs are meant for a single channel conversion; the ODR needs to be divided by n for n channels scanning. For example, if the ADC were running at 214.65 SPS and four channels are being scanned, then the ODR per channel would be 214.65/4 = 53.6625 SPS.

16.1.7 Digital Filter

The LMP90100 has a fourth order rotated sinc filter that is used to configure various ODRs and to reject power supply frequencies of 50Hz and 60Hz. The 50/60 Hz rejection is only effective when the device is operating at ODR ≤ 13.42 SPS. If the internal CLK or the external CLK of 3.5717 MHz is used, then the LMP90100 will have the frequency response shown in *Table 5* and *Figure 5* through *Figure 8*.

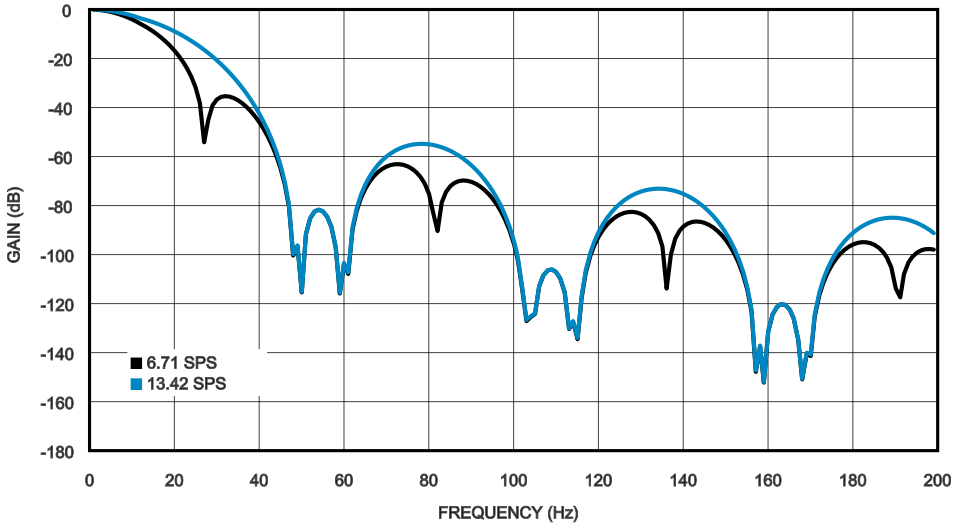
TABLE 5. Digital Filter Attenuation

DATA RATE	ATTENUATION (dB)			
	f = 50 Hz ± 0.3 Hz	f = 60 Hz ± 0.3 Hz	f = 50 Hz ± 1 Hz	f = 60 Hz ± 1 Hz
1.6775 SPS	−109	−114	−96	−114
3.355 SPS	−102	−105	−92	−105
6.71 SPS	−100	−103	−92	−103
13.42 SPS	−100	−103	−91	−103
26.83125 SPS				
53.6625 SPS				
107.325 SPS				
214.65 SPS				



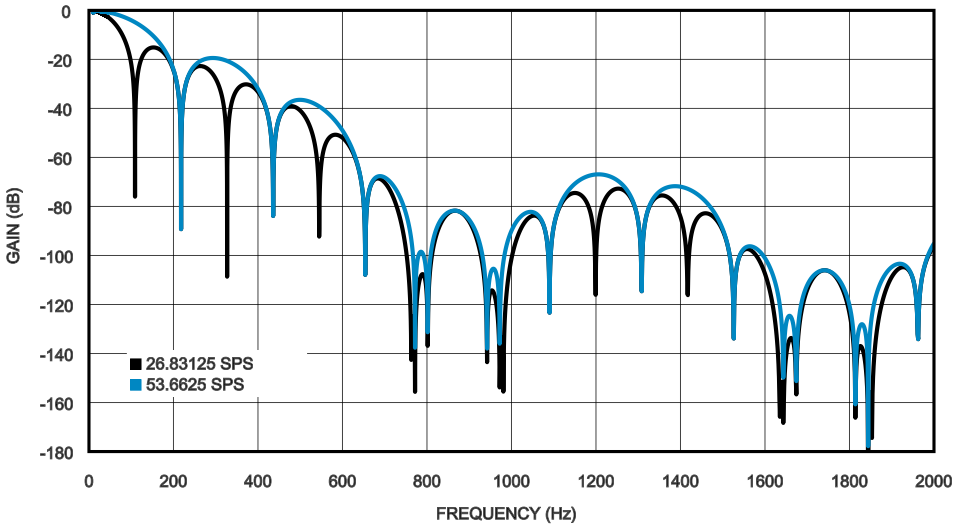
30139560

FIGURE 5. Digital Filter Response, 1.6775 SPS and 3.355 SPS



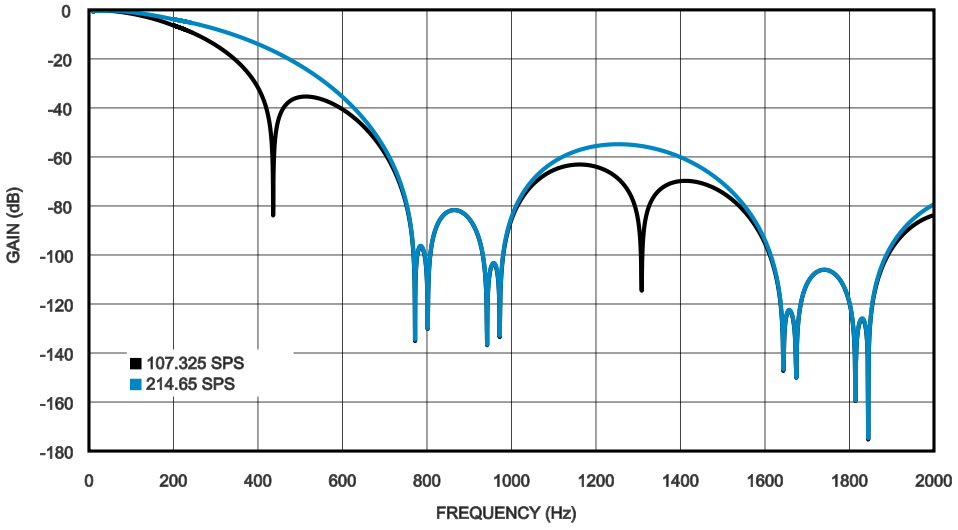
30139573

FIGURE 6. Digital Filter Response, 6.71 SPS and 13.42 SPS



30139586

FIGURE 7. Digital Filter Response, 26.83125 SPS and 53.6625 SPS



30139587

FIGURE 8. Digital Filter Response 107.325 SPS and 214.65 SPS

If the internal CLK is not being used and the external CLK is not 3.5717 MHz, then the filter response would be the same as the response shown above, but the frequency will change according to the equation:

$$f_{NEW} = [(CLK_{EXT}) / 256] \times (f_{OLD} / 13.952k)$$

Using the equation above, an example of the filter response for a 3.5717 MHz XTAL versus a 3.6864 MHz XTAL can be seen in *Figure 9*.

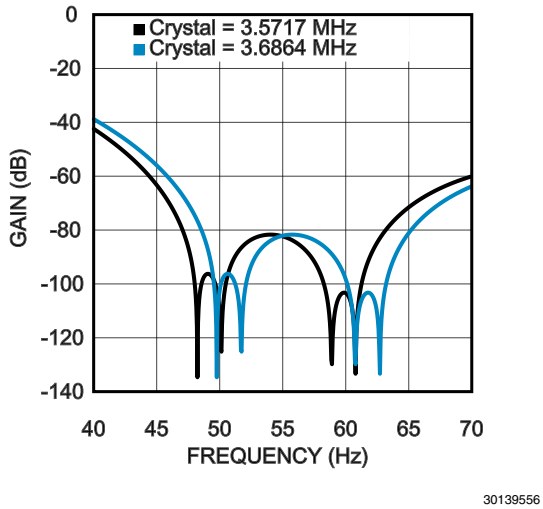


FIGURE 9. Digital Filter Response for a 3.5717MHz versus 3.6864 MHz XTAL

16.1.8 GPIO (D0–D6)

Pins D0-D6 are general purpose input/output (GPIO) pins that can be used to control external LEDs or switches. Only a high or low value can be sourced to or read from each pin.

Figure 10 shows a flowchart how these GPIOs can be programmed.

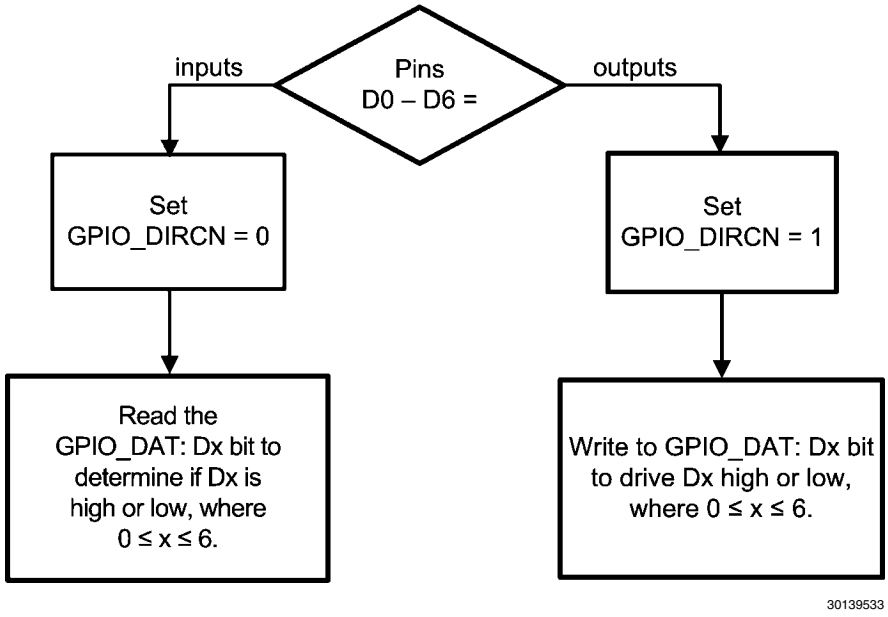


FIGURE 10. GPIO Register Settings

16.2 CALIBRATION

As seen in *Figure 11*, there are two types of calibration: background calibration and system calibration. These calibrations are further described in the next sections.

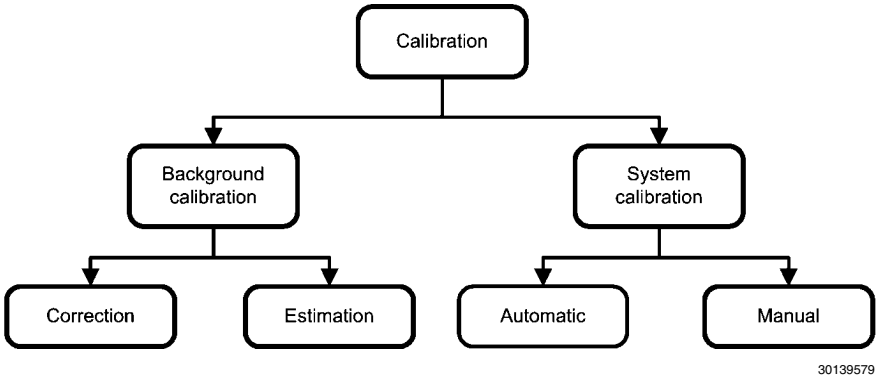


FIGURE 11. Types of Calibration

16.2.1 Background Calibration

Background calibration is the process of continuously determining and applying the offset and gain calibration coefficients to the output codes to minimize the LMP90100's offset and gain errors. Background calibration is a feature built into the LMP90100 and is automatically done by the hardware without interrupting the input signal.

Four differential channels, CH0-CH3, each with its own gain and ODRs, can be calibrated to improve the accuracy.

Types of Background Calibration:

Figure 11 also shows that there are two types of background calibration:

1. Type 1: Correction - the process of continuously determining and applying the offset and gain calibration coefficients to the output codes to minimize the LMP90100's offset and gain errors.
   This method keeps track of changes in the LMP90100's gain and offset errors due to changes in the operating condition such as voltage, temperature, or time.
2. Type 2: Estimation - the process of determining and continuously applying the last known offset and gain calibration coefficients to the output codes to minimize the LMP90100's offset and gain errors.
   The last known offset or gain calibration coefficients can come from two sources. The first source is the default coefficient which is pre-determined and burnt in the device's non-volatile memory. The second source is from a previous calibration run of Type 1: Correction.

The benefits of using type 2 calibration is a higher throughput, lower power consumption, and slightly better noise. The exact savings would depend on the number of channels being scanned, and the ODR and gain of each channel.

Using Background Calibration:

There are four modes of background calibration, which can be programmed using the BGCALCN bits. They are as follows:

1. BgcalMode0: Background Calibration OFF
2. BgcalMode1: Offset Correction / Gain Estimation
3. BgcalMode2: Offset Correction / Gain Correction
   Follow *Figure 12* to set other appropriate registers when using this mode.
4. BgcalMode3: Offset Estimation / Gain Estimation

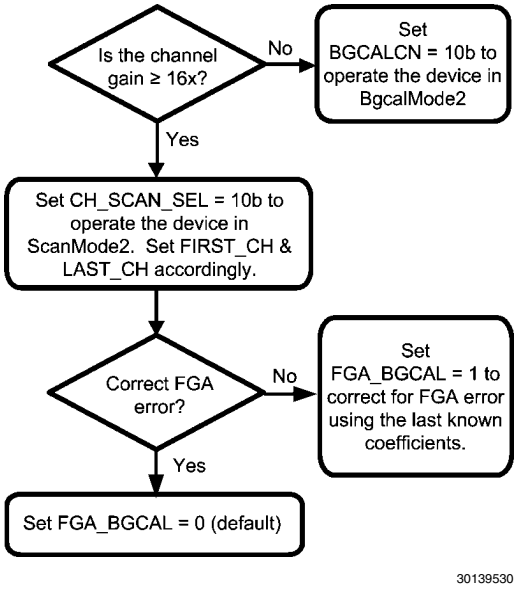


FIGURE 12. BgcalMode2 Register Settings

If operating in BgcalMode2, four channels (with the same ODR) are being converted, and FGA_BGCAL = 0 (default), then the ODR is reduced by:

1. 0.19% of 1.6775 SPS
2. 0.39% of 3.355 SPS
3. 0.78% of 6.71 SPS
4. 1.54% of 13.42 SPS
5. 3.03% of 26.83125 SPS
6. 5.88% of 53.6625 SPS
7. 11.11% of 107.325 SPS
8. 20% of 214.65 SPS

16.2.2 System Calibration

The LMP90100 provides System Calibration Offset and Gain coefficients that can be used to remove system offset and system gain errors respectively. The system offset calibration coefficient is subtracted from the result prior to the division by the system gain coefficient. These coefficients are typically filled up by performing system zero-scale and system full-scale calibrations. System zero-scale and full-scale calibrations can be performed by setting up the respective calibrating

conditions in the system and by appropriate programming of the System Calibration Control Register (SCALCN bits).

The system zero-scale calibration must be performed prior to the full-scale calibration and both need to be repeated when the gain (or the signal path) is changed.

The System Gain coefficient can be filled in even if system full-scale calibration setup cannot done but instead, a setup can be done where a known fraction of the full scale (like 0.75 times full scale or 1.25 times full scale) is applied. Here, the fractional information is entered in the System Gain coefficient register (in 1.23 fixed-point format) before the calibration is initiated. The device will then automatically compute the System Gain coefficient and overwrite the register with the computed value. This way, one can make use of other known reference inputs, even if they are not full scale inputs.

The computed calibration coefficients are accurate only to the effective resolution of the device and will probably contain some noise. The noise factor can be minimized by computing over many times, averaging (externally) and putting the resultant values back into the registers.

There are four distinct sets of System Calibration Offset and Gain Coefficient Registers for use with Channels 0-3. Channels 4–6 will reuse the System Calibration Offset and Gain Coefficient values of channels 0–2 respectively.

There are three system calibration coefficients: offset, gain, and scale. A data-flow diagram of these coefficients and their register names can be seen in *Figure 13*.

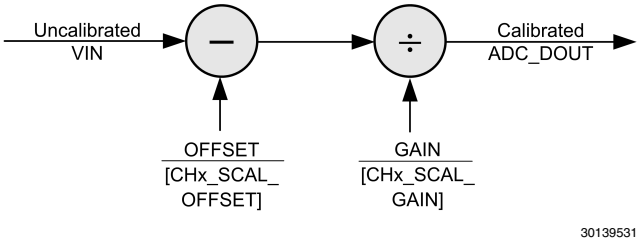


FIGURE 13. System Calibration Data-Flow Diagram

Types of System Calibration

As seen in *Figure 11*, there are two types of system calibration: automatic and manual. The automatic calibration occurs when the LMP90100 computes the offset or gain coefficient once, stores it in the appropriate registers, and continuously calibrates the system using this coefficient.

The manual calibration occurs when the user has to manually compute the offset coefficient or expected output code once, and store it in the appropriate registers. After this process, LMP90100 will use this coefficient to continuously calibrate for the system errors.

Automatic Offset Calibration

Follow the steps below to automatically compute the system offset coefficient:

1. Apply a zero scale condition for CH0, CH1, CH2, or CH3 (CHx_INPUTCN).
2. If the device is to be used in one of the four high ODRs (214.65, 107.325, 53.6625, or 26.83125 SPS) run the device at 26.83125 SPS. If the device is to be used in one of the four low ODRs (13.42, 6.71, 3.355, 1.6775) run the device at 1.6775 SPS to reduce noise (CHx_CONFIG: ODR_SEL bit)
3. Enter the “System Calibration Offset Coefficient Determination” mode (SCALCN bits)
4. LMP90100 starts a fresh conversion.
5. LMP90100 computes the system offset calibration coefficient once, stores this coefficient in the CHx_SCAL_OFFSET registers, and continuously calibrates the system using this coefficient.
6. LMP90100 exits the “System Calibration Offset Coefficient Determination” mode.

Automatic Gain Calibration

Follow the steps below to automatically compute the system gain coefficient:

1. Repeat the "Automatic Offset Calibration" mode to calibrate for the offset error first
2. Apply a full scale condition in which VIN = VINP - VINN = VREF for CH0, CH1, CH2, or CH3 (CHx_INPUTCN)
3. Enter the “System Calibration Gain Coefficient Determination” mode (SCALCN bits)
4. LMP90100 starts a fresh conversion.
5. LMP90100 computes the system gain calibration coefficient once, stores this coefficient in the CHx_SCAL_GAIN registers, and continuously calibrates the system using this coefficient.
6. LMP90100 exits the “System Calibration Gain Coefficient Determination” mode.

Manual Offset Calibration

The “Automatic Offset Calibration” data is accurate only to the effective resolution of the device and will probably contain some variation or noise. This probable variation can be reduced by performing the “Manual Offset Calibration”.

In this mode, the coefficient has to be known and entered into the appropriate registers. One way in which the user can manually compute the coefficient is shown in the following steps:

1. Repeat the "Automatic Offset Calibration" mode and externally store this coefficient
2. Repeat step 1 until a finite amount of coefficients are obtained
3. Compute the average offset coefficient and enter this value in the CHx_SCAL_OFFSET registers
4. LMP90100 will use this coefficient to continuously calibrate for the offset error.

The computed offset coefficient has to be a 24-bit two‘s-complement number. For example, if the offset is 200µV for VREF = 4.1V, then the offset coefficient = $[(200\mu V)(2^{24})] / [(2)(4.1V)]$ = 409d = 0x199.

If the offset is -200µV for VREF = 4.1V, then the offset coefficient is $[(-200\mu V)(2^{24})] / [(2)(4.1V)]$ = -409d = 0XFF_FE67.

Manual Gain Calibration

Another way to use the system gain calibration is programming the expected output code and letting LMP90100 calibrate itself. For example, suppose VIN =¾(VREF), and thus the expected output code is 0x60_0000.

1. Apply VIN = VINP - VINN = ¾ (VREF) for CH0, CH1, CH2, or CH3 (CHx_INPUTCN)
2. Program the expected output code 0x60_0000 in the CHx_SCAL_GAIN registers
3. Enter the “System Calibration Gain Coefficient Determination” mode (SCALCN bits)

4. LMP90100 starts a fresh conversion.
5. LMP90100 computes the system gain calibration coefficient once, stores this coefficient in the CHx_SCAL_GAIN registers, and continuously calibrates the system using this coefficient.
6. LMP90100 exits the "System Calibration Gain Coefficient Determination" mode.

16.3 CHANNELS SCAN MODE

There are four scan modes. These scan modes are selected using the CH_SCAN: CH_SCAN_SEL bit. The first scanned channel is FIRST_CH, and the last scanned channel is LAST_CH; they are both located in the CH_SCAN register.

The CH_SCAN register is double buffered. That is, user inputs are stored in a slave buffer until the start of the next conversion during which time they are transfered to the master buffer. Once the slave buffer is written, subsequent updates are disregarded until a transfer to the master buffer happens. Hence, it may be appropriate to check the CH_SCAN_NRDY bit before programming the CH_SCAN register.

ScanMode0: Single-Channel Continuous Conversion

LMP90100 continuously converts the selected FIRST_CH.

Do not operate in this scan mode if gain ≥ 16 and the LMP90100 is running in background calibration modes BgcalMode1 or BgcalMode2. If this is the case, then it is more suitable to operate the device in ScanMode2 instead.

ScanMode1: Multiple-Channels Single Scan

LMP90100 converts one or more channels starting from FIRST_CH to LAST_CH, and then enters the stand-by state.

ScanMode2: Multiple-Channels Continuous Scan

LMP90100 continuously converts one or more channels starting from FIRST_CH to LAST_CH, and then it repeats this process.

ScanMode3: Multiple-Channels Continuous Scan with Burnout Currents

This mode is the same as ScanMode2 except that the burnout current is provided in a serially scanned fashion (injected in a channel after it has undergone a conversion). Thus it avoids burnout current injection from interfering with the conversion result for the channel.

The sensor diagnostic burnout currents are available for all four scan modes. The burnout current is further gated by the BURNOUT_EN bit for each channel. ScanMode3 is the only mode that scans multiple channels while injecting burnout currents without interfering with the signal. This is described in details in *Section 16.4.2 Burnout Currents*.

16.4 SENSOR INTERFACE

LMP90100 contains two types of current sources: excitation currents (IB1 & IB2) and burnout currents. They are described in the next sections.

16.4.1 IB1 & IB2 - Excitation Currents

IB1 and IB2 can be used for providing currents to external sensors, such as RTDs or bridge sensors. 100µA to 1000µA, in steps of 100µA, can be sourced by programming the ADC_AUXCN: RTD_CUR_SEL bits.

Refer to *Section 17.6.1 3–Wire RTD* to see how IB1 and IB2 can be used to source a 3-wire RTD.

16.4.2 Burnout Currents

As shown in *Figure 14*, the LMP90100 contains two internal 10 µA burnout current sources, one sourcing current from VA to VINP, and the other sinking current from VINN to ground. These currents are used for sensor diagnostics and can be enabled for each channel using the CHx_INPUTCN: BURNOUT_EN bit.

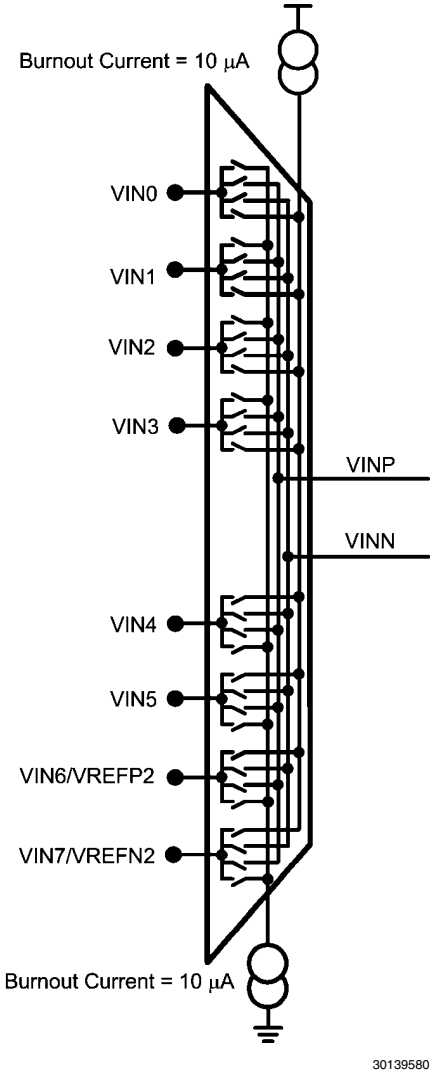


FIGURE 14. Burnout Currents

Burnout Current Injection:

Burnout currents are injected differently depending on the channel scan mode selected.

When BURNOUT_EN = 1 and the device is operating in ScanMode0, 1, or 2, the burnout currents are injected into all the channels for which the BURNOUT_EN bit is selected. This will cause problems and hence in this mode, more than one channel should not have its BURNOUT_EN bit selected. Also, the burnout current will interfere with the signal and introduce a fixed error depending on the particular external sensor.

When BURNOUT_EN = 1 and the device is operating in ScanMode3, burnout currents are injected into the last sampled channel on a cyclical basis (*Figure 15*). In this mode, burnout currents injection is truly done in the background without affecting the accuracy of the on-going conversion. Operating in this mode is recommended.

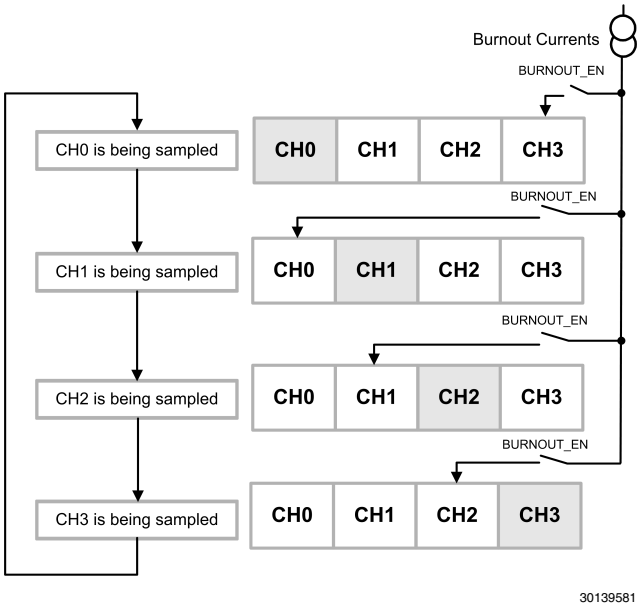


FIGURE 15. Burnout Currents Injection for ScanMode3

16.4.3 Sensor Diagnostic Flags

Burnout currents can be used to verify that an external sensor is still operational before attempting to make measurements on that channel. A non-operational sensor means that there is a possibility the connection between the sensor and the LMP90100 is open circuited, short circuited, shorted to VA or GND, overloaded, or the reference may be absent. The sensor diagnostic flags diagram can be seen in *Figure 16*.

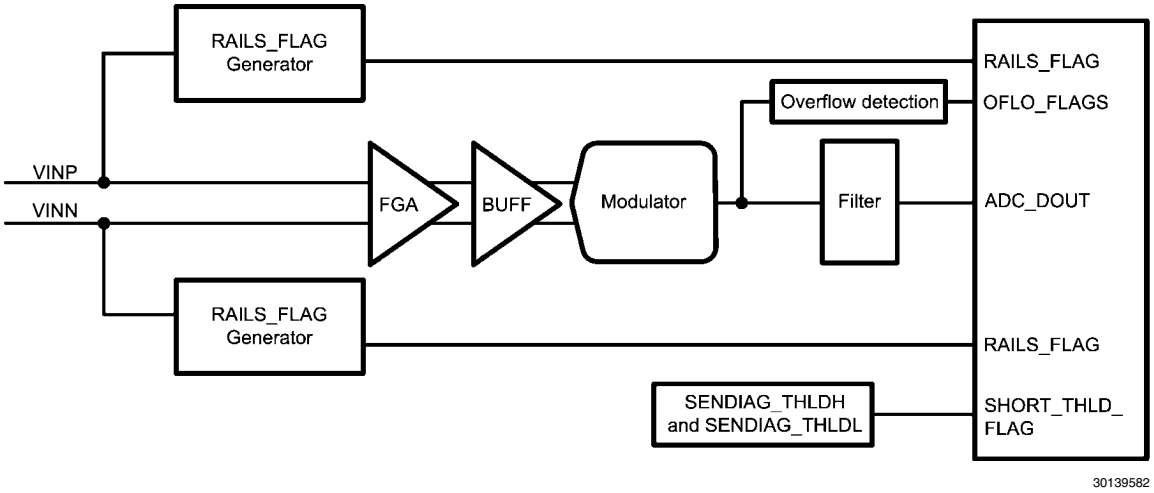


FIGURE 16. Sensor Diagnostic Flags Diagram

The sensor diagnostic flags are located in the SENDIAG_FLAGS register and are described in further details below.

SHORT_THLD_FLAG:

The short circuit threshold flag is used to report a short-circuit condition. It is set when the output voltage (VOUT) is within the absolute Vthreshold. Vthreshold can be programmed using the 8-bit SENDIAG_THLDH register concatenated with the 8-bit SENDIAG_THLDL register.

For example, assume VREF = 5V, gain = 1, SENDIAG_THLDH = 0xFA, and SENDIAG_THLDL = 0x45. In this case, Dthreshold = 0xFA45 = 64069d, and Vthreshold can be calculated as:

$$Vthreshold = [(Dthreshold)(2)(VREF)] / [(Gain)(2^{24})]$$

$$Vthreshold = [(64069)(2)(5V)] / [(1)(2^{24})]$$

$$Vthreshold = 38.2\ mV$$

When (-38.2mV) ≤ VOUT ≤ (38.2mV), then SHORT_THLD_FLAG = 1; otherwise, SHORT_THLD_FLAG = 0.

RAILS_FLAG:

The rails flag is used to detect if one of the sampled channels is within 50mV of the rails potential (VA or VSS). This can be further investigated to detect an open-circuit or short-circuit condition. If the sampled channel is near a rail, then RAILS_FLAG = 1; otherwise, RAILS_FLAG = 0.

POR_AFT_LST_RD:

If POR_AFT_LST_READ = 1, then there was a power-on reset since the last time the SENDIAG_FLAGS register was read. This flag's status is cleared when this bit is read, unless this bit is set again on account of another power-on-reset event in the intervening period.

OFLO_FLAGS:

OFLO_FLAGS is used to indicate whether the modulator is over-ranged or under-ranged. The following conditions are possible:

1. OFLO_FLAGS = 0x0: Normal Operation
2. OFLO_FLAGS = 0x1: The modulator was not overranged, but ADC_DOUT got clamped to 0x7f_ffff (positive fullscale) or 0x80_0000 (negative full scale). For example, if VREF = 5V, VIN = 2V, and gain = 128, then OFLO_FLAGS would be 01b.
3. OFLO_FLAGS = 0x2: The modulator was over-ranged towards +VREF.
4. OFLO_FLAGS = 0x3: The modulator was over-ranged towards −VREF.

The condition of OFLO_FLAGS = 10b or 11b can be used in conjunction with the RAILS_FLAG to determine the fault condition.

SAMPLED_CH:

These three bits show the channel number for which the ADC_DOUT and SENDIAG_FLAGS are available. This does not necessarily indicate the current channel under conversion because the conversion frame and computation of results from the channels are pipelined. That is, while the conversion is going on for a particular channel, the results for the previous conversion (of the same or a different channel) are available.

16.5 SERIAL DIGITAL INTERFACE

A synchronous 4-wire serial peripheral interface (SPI) provides access to the internal registers of LMP90100 via CSB, SCLK, SDI, SDO/DRDYB.

16.5.1 Register Address (ADDR)

All registers are memory-mapped. A register address (ADDR) is composed of an upper register address (URA) and lower register address (LRA) as shown in *ADDR Map*. For example, ADDR 0x3A has URA=0x3 and LRA=0xA.

ADDR Map

Bit	**[6:4]**	**[3:0]**
Name	URA	LRA

16.5.2 Register Read/Write Protocol

Figure 17 shows the protocol how to write to or read from a register.

Transaction 1 sets up the upper register address (URA) where the user wants to start the register-write or register-read.

Transaction 2 sets the lower register address (LRA) and includes the Data Byte(s), which contains the incoming data from the master or outgoing data from the LMP90100.

Examples of register-reads or register-writes can be found in *Section 17.4 REGISTER READ/WRITE EXAMPLES*.

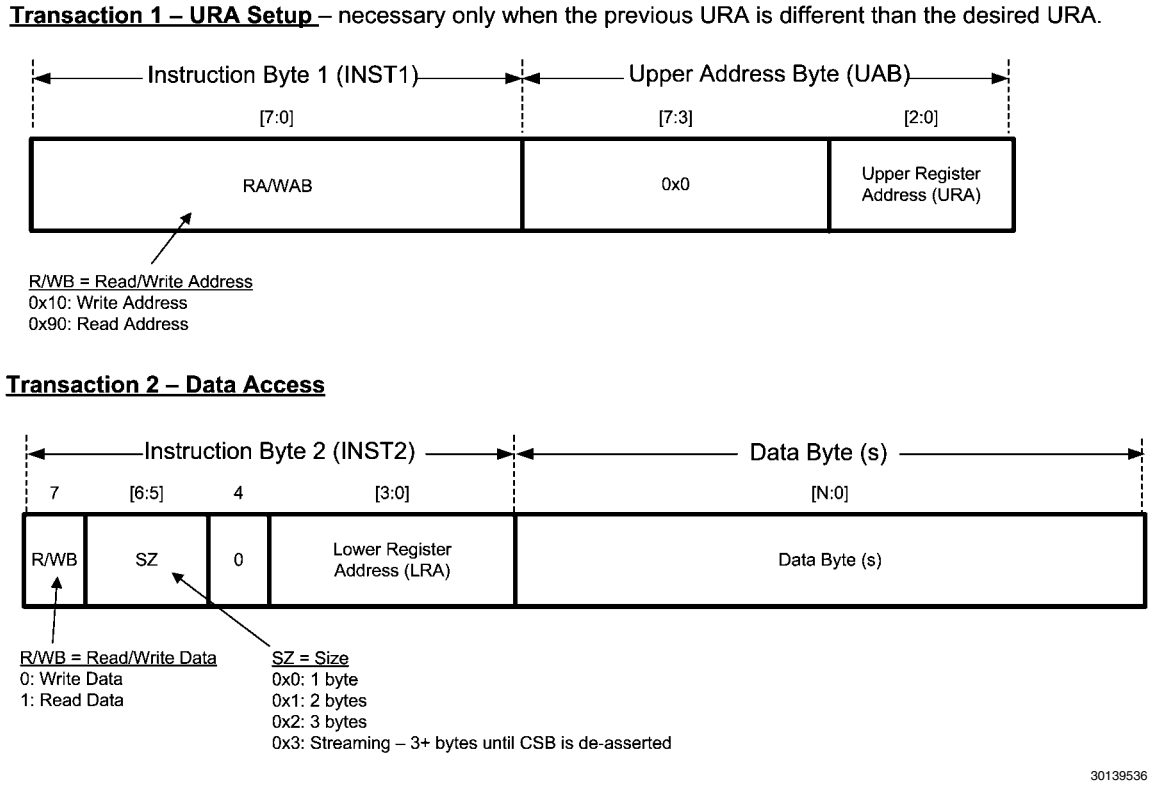


FIGURE 17. Register Read/Write Protocol

16.5.3 Streaming

When writing/reading 3+ bytes, the user must operate the device in Normal Streaming mode or Controlled Streaming mode. In the Normal Streaming mode, which is the default mode, data runs continuously starting from ADDR until CSB deasserts. This mode is especially useful when programming all the configuration registers in a single transaction. See *Section 17.5.1 Normal Streaming Example* for an example of the Normal Streaming mode.

In the Controlled Streaming mode, data runs continuously starting from ADDR until the data has run through all (STREAM_RANGE + 1) registers. For example, if the starting ADDR is 0x1C, STREAM_RANGE = 5, then data will be written to or read from the following ADDRs: 0x1C, 0x1D, 0x1E, 0x1F, 0x20, 0x21. Once the data reaches ADDR 0x21, LMP90100 will wrap back to ADDR 0x1C and repeat this process until CSB deasserts. See *Section 17.5.2 Controlled Streaming Example* for an example of the Controlled Streaming mode.

If streaming reaches ADDR 0x7F, then it will wrap back to ADDR 0x00. Furthermore, reading back the Upper Register Address after streaming will report the Upper Register Address at the start of streaming, not the Upper Register Address at the end of streaming.

To stream, write 0x3 to INST2's SZ bits as seen in *Figure 17*. To select the stream type, program the SPI_STREAMCN: STRM_TYPE bit. The STRM_RANGE can also be programmed in the same register.

16.5.4 SPI Protocol

An SPI transaction begins when the master asserts CSB and ends when the master deasserts CSB. Each transaction must be separated by a CSB deassertion. Once CSB is asserted, it must not pulse (deassert and assert again) during a (desired) transaction.

A transaction contains variable number of bytes. Bits in each byte are arranged MSB first.

16.5.5 DRDYB - Data Ready Bar

DRDYB is a signal generated by the LMP90100 that fresh conversion data is available in the ADC_DOUT registers.

DRDYB is automatically asserted every (1/ODR) second. For a complete reading, DRDYB deasserts whenever the LSB of ADC_DOUTL is read out (*Figure 18*).

FIGURE 18. DRDYB Behavior for a Complete ADC_DOUT Reading

If ADC_DOUT is not completely read out (*Figure 19*) or is not read out at all, but a new ADC_DOUT is available, then DRDYB will automatically pulse for t_{DRDYB} second. The value for t_{DRDYB} can be found in *Section 13.0 Timing Diagrams*.

FIGURE 19. DRDYB Behavior for an Incomplete ADC_DOUT Reading

DRDYB can also be access via registers using the DT_AVAIL_B bit. This bit indicates when fresh conversion data is available in the ADC_DOUT registers. If new conversion data is available, then DT_AVAIL_B = 0; otherwise, DT_AVAIL_B = 1.

Opposed to the drdyb signal, a complete reading for DT_AVAIL_B occurs when the MSB of ADC_DOUTH is read out. This bit cannot be reset even if REG_AND_CNV_RST = 0xC3.

DrdybCase1: Combining SDO/DRDYB

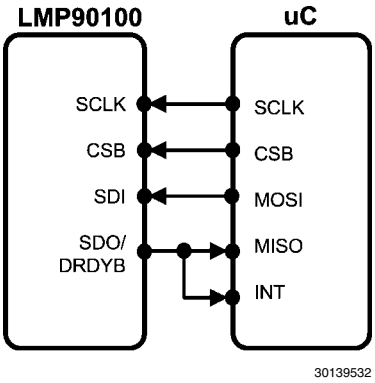


FIGURE 20. DrdybCase1 Connection Diagram

As shown in *Figure 20*, the drdyb signal and SDO can be multiplexed on the same pin as their functions are mostly complementary. In fact, this is the default mode for the SDO/DRDYB pin.

Figure 21 shows a timing protocol for DrdybCase1. In this case, start by asserting CSB first to monitor a drdyb assertion. When the drdyb signal asserts, begin writing the Instruction Bytes (INST1, UAB, INST2) to read from or write to registers.

Note that INST1 and UAB are omitted from the figure below because this transaction is only required if a new UAB needs to be implemented.

While the CSB is asserted, DRDYB is driving the SDO/DRDYB pin unless the device is reading data, in which case, SDO will be driving the pin. If CSB is deasserted, then the SDO/DRDYB pin is High-Z. This behavior can be changed by programming SDO_DRDYB_DRIVER.

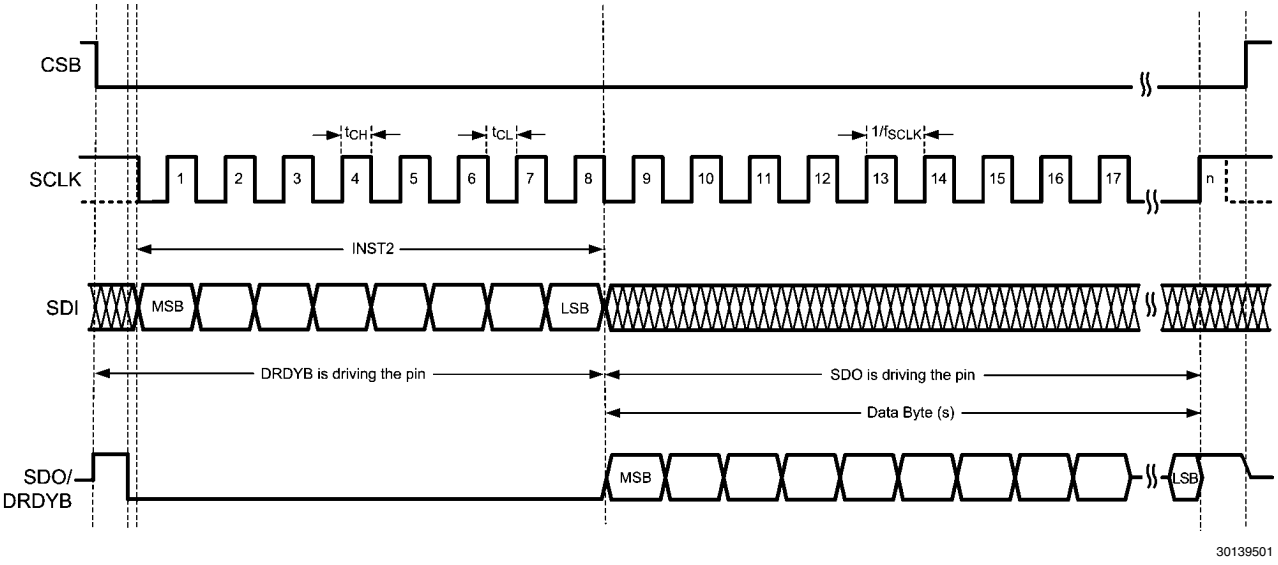


FIGURE 21. Timing Protocol for DrdybCase1

DrdybCase2: Routing DRDYB to D6

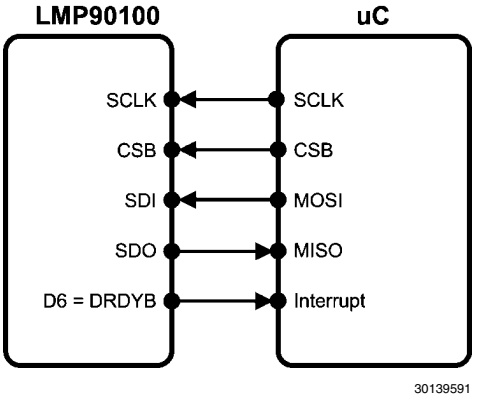


FIGURE 22. DrdybCase2 Connection Diagram

The drdyb signal can be routed to pin D6 by setting SPI_DRDYB_D6 high and SDO_DRDYB_DRIVER to 0x4. This is the behavior for DrdybCase2 as shown in *Figure 22*.

The timing protocol for this case can be seen in *Figure 23*. Since DRDYB is separated from SDO, CSB doesn't need to be asserted in advanced in order to detect a drdyb assertion.

The drdyb signal can be monitored using the interrupt or polling method. If polled, the drdyb signal needs to be polled faster than t_{DRDYB} to detect a drdyb assertion. When drdyb asserts, assert CSB to start the SPI transaction and begin writing the Instruction Bytes (INST1, UAB, INST2) to read from or write to registers.

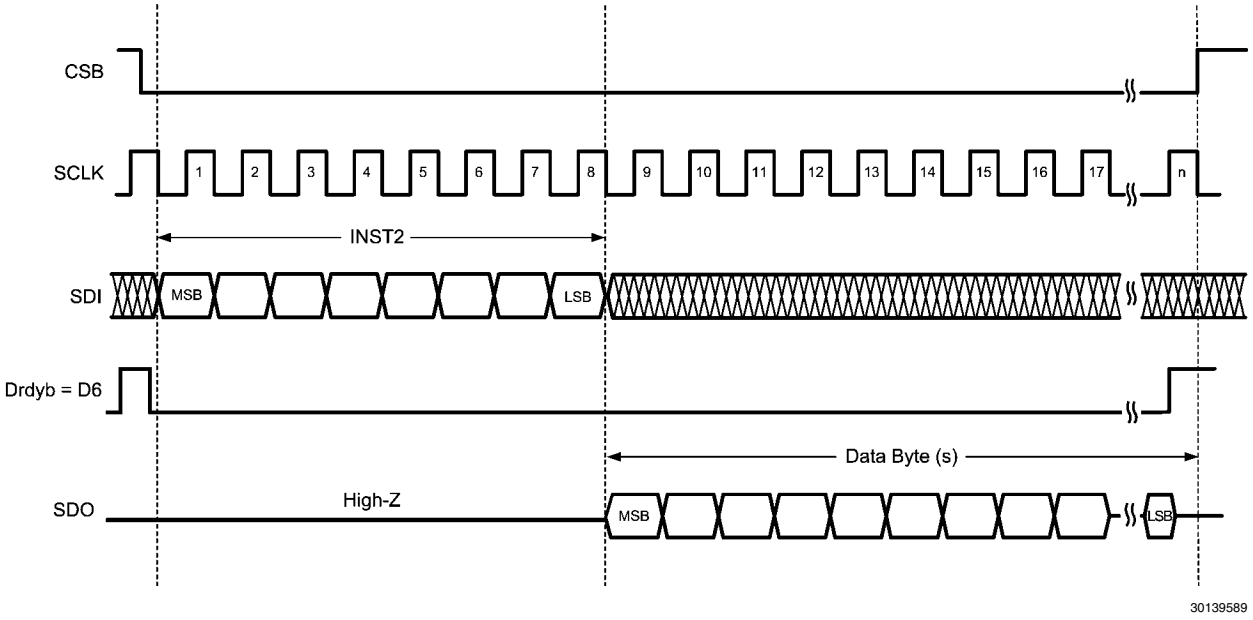


FIGURE 23. Timing Protocol for DrdybCase2

16.5.6 Data Only Read Transaction

In a data only read transaction, one can directly access the data byte(s) as soon as the CSB is asserted without having to send any instruction byte. This is useful as it brings down the latency as well as the overhead associated with the instruction byte (as well as the Upper Address Byte, if any).

In order to use the data only transaction, the device must be placed in the data first mode. The following table lists transaction formats for placing the device in and out of the data first mode and reading the mode status.

TABLE 6. Data First Mode Transactions

	Bit[7]	Bits[6:5]	Bit[4]	Bits[3:0]	Data Bytes
Enable Data First Mode Instruction	1	11	1	1010	None
Disable Data First Mode Instruction	1	11	1	1011	None
Read Mode Status Instruction	1	00	1	1111	One

Note that while being in the data first mode, once the data bytes in the data only read transaction are sent out, the device is ready to start on any normal (non-data-only) transaction including the disable data first mode instruction. The current status of the data first mode (enabled/disabled status) can be read back using the read mode status transaction. This transaction consists of the read mode status instruction followed by a single data byte (driven by the device). The data first mode status is available on bit [1] of this data byte.

The data only read transaction allows reading up to eight consecutive registers, starting from any start address. Usually, the start address will be the address of the most significant byte of conversion data, but it could just as well be any other address. The start address and number of bytes to be read during the data only read transaction can be programmed using the DATA_ONLY_1 AND DATA_ONLY_2 registers respectively.

The upper register address is unaffected by a data only read transaction. That is, it retains its setting even after encountering a data only transaction. The data only transaction uses its own address (including the upper address) from the DATA_ONLY_1 register. When in the data first mode, the SCLK must stop high before entering the data only read transaction.

16.5.7 Cyclic Redundancy Check (CRC)

CRC can be used to ensure integrity of data transfer. To enable CRC, set EN_CRC high. Once CRC is enabled, the CRC value is calculated and stored in SPI_CRC_DAT so that the master device can periodically read for data comparison. Conveniently, the SPI_CRC_DAT register address is located next to the ADC_DOUT register address so that the CRC value can be easily read as part of the data set. The CRC is automatically reset when CSB or DRDYB is deasserted.

The CRC format for LMP90100 is $x^8 + x^5 + x^4 + 1$. The reset value of the SPI_CRC_DAT register is zero, and the final value is ones-complemented before it is sent out. Note that CRC computation only includes the bits sent out on SDO and does not include the bits of the SPI_CRC_DAT itself; thus it is okay to read SPI_CRC_DAT repeatedly.

The drdyb signal normally deasserts (active high) every 1/ODR second or when the LSB of ADC_DOUTL is read. However, this behavior can be changed so that drdyb deassertion can occur after SPI_CRC_DAT is read. This is done by setting bit DRDYB_AFT_CRC high.

The timing protocol for CRC can be found in the following figure.

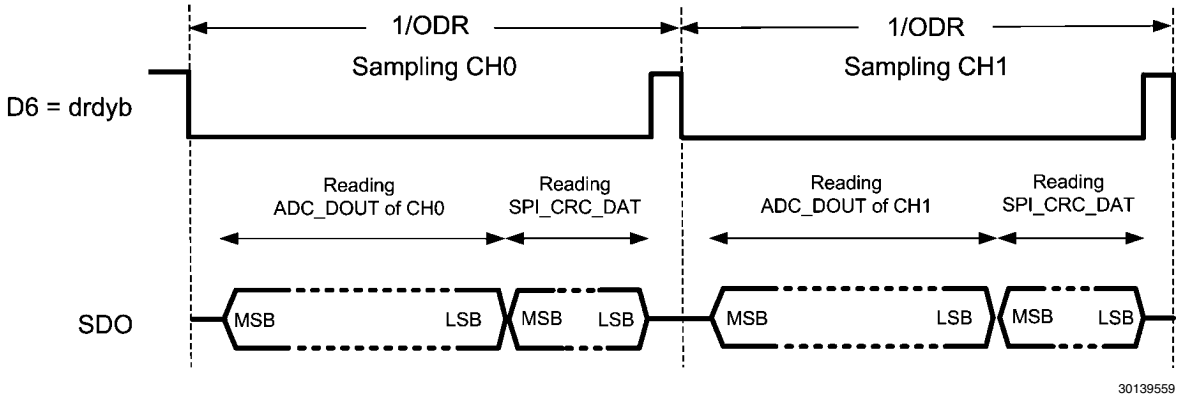


FIGURE 24. Timing Protocol for Reading SPI_CRC_DAT

16.6 POWER MANAGEMENT

The device can be placed in Active, Power-Down, or Stand-By state.

In Power-Down, the ADC is not converting data, contents of the registers are unaffected, and there is a drastic power reduction. In Stand-By, the ADC is not converting data, but the power is only slightly reduced so that the device can quickly transition into the active state if desired.

These states can be selected using the PWRCN register. When written, PWRCN brings the device into the Active, Power-Down, or Stand-By state. When read, PWRCN indicates the state of the device.

The read value would confirm the write value after a small latency (approximately 15 µs with the internal CLK). It may be appropriate to wait for this latency to confirm the state change. Requests not adhering to this latency requirement may be rejected.

It is not possible to make a direct transition from the power-down state to the stand-by state. This state diagram is shown below.

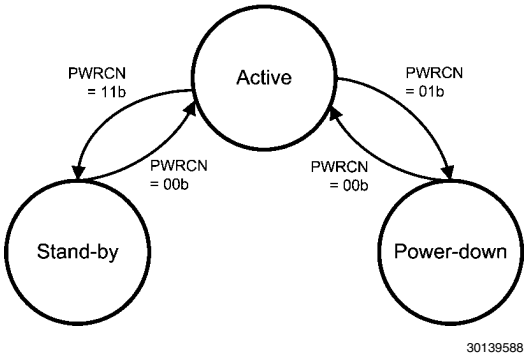


FIGURE 25. Active, Power-Down, Stand-by State Diagram

16.7 RESET and RESTART

Writing 0xC3 to the REG_AND_CNV_RST field will reset the conversion and most of the programmable registers to their default values. The only registers that will not be reset are the System Calibration Registers (CHx_SCAL_OFFSET, CHx_SCAL_GAIN) and the DT_AVAIL_B bit.

If it is desirable to reset the System Calibration Coefficient Registers, then set RESET_SYSCAL = 1 before writing 0xC3 to REG_AND_CNV_RST. If the device is operating in the "System Calibration Offset/Gain Coefficient Determination" mode (SCALCN register), then write REG_AND_CNV_RST = 0xC3 twice to get out of this mode.

After a register reset, any on-going conversions will be aborted and restarted. If the device is in the power-down state, then a register reset will bring it out of the power-down state.

To restart a conversion, write 1 to the RESTART bit. This bit can be used to synchronize the conversion to an external event.

17.0 Applications Information

17.1 QUICK START

This section shows step-by-step instructions to configure the LMP90100 to perform a simple DC reading from CH0.

1. Apply VA = VIO = VREFP1 = 5V, and ground VREFN1
2. Apply VINP = ¾VREF and VINN = ¼VREF for CH0. Thus, set CH0 = VIN = VINP - VINN = ½VREF (CH0_INPUTCN register)
3. Set gain = 1 (CH0_CONFIG: GAIN_SEL = 0x0)
4. Exclude the buffer from the signal path (CH0_CONFIG: BUF_EN = 1)
5. Set the background to BgcalMode2 (BGCALCN = 0x2)
6. Select VREF1 (CH0_INPUTCN: VREF_SEL = 0)
7. To use the internal CLK, set CLK_EXT_DET = 1 and CLK_SEL = 0.
8. Follow the register read/write protocol (*Figure 17*) to capture ADC_DOUT from CH

17.2 CONNECTING THE SUPPLIES

17.2.1 VA and VIO

Any ADC architecture is sensitive to spikes on the analog voltage, VA, digital input/output voltage, VIO, and ground pins. These spikes may originate from switching power supplies, digital logic, high power devices, and other sources. To diminish these spikes, the LMP90100's VA and VIO pins should be clean and well bypassed. A 0.1 µF ceramic bypass capacitor and a 1 µF tantalum capacitor should be used to bypass the LMP90100 supplies, with the 0.1 µF capacitor placed as close to the LMP90100 as possible.

Since the LMP90100 has both external VA and VIO pins, the user has two options on how to connect these pins. The first option is to tie VA and VIO together and power them with the same power supply. This is the most cost effective way of powering the LMP90100 but is also the least ideal because noise from VIO can couple into VA and negatively affect performance. The second option involves powering VA and VIO with separate power supplies. These supply voltages can have the same amplitude or they can be different.

17.2.2 VREF

Operation with VREF below VA is also possible with slightly diminished performance. As VREF is reduced, the range of acceptable analog input voltages is also reduced. Reducing the value of VREF also reduces the size of the LSB. When the LSB size goes below the noise floor of the LMP90100, the noise will span an increasing number of codes and performance will degrade. For optimal performance, VREF should be the same as VA and sourced with a clean source that is bypassed with a ceramic capacitor value of 0.1 µF and a tantalum capacitor of 10 µF.

LMP90100 also allows ratiometric connection for noise immunity reasons. A ratiometric connection is when the ADC's VREFP and VREFN are used to excite the input device's (i.e. a bridge sensor) voltage references. This type of connection severely attenuates any VREF ripple seen the ADC output, and is thus strongly recommended.

17.3 ADC_DOUT CALCULATION

The output code of the LMP90100 can be calculated as:

$$ADC\_DOUT = \pm \left(\frac{(VINP - VINN) \times GAIN}{VREFP - VREFN} \right) \times \left(2^{23}\right)$$

Equation 1 — Output Code

ADC_DOUT is in 24–bit two's complement binary format. The largest positive value is 0x7F_FFFF while the largest negative value is 0x80_0000. In case of an over range the value is automatically clamped to one of these two values.

Figure 26 shows the theoretical output code, ADC_DOUT, vs. analog input voltage, VIN, using the equation above.

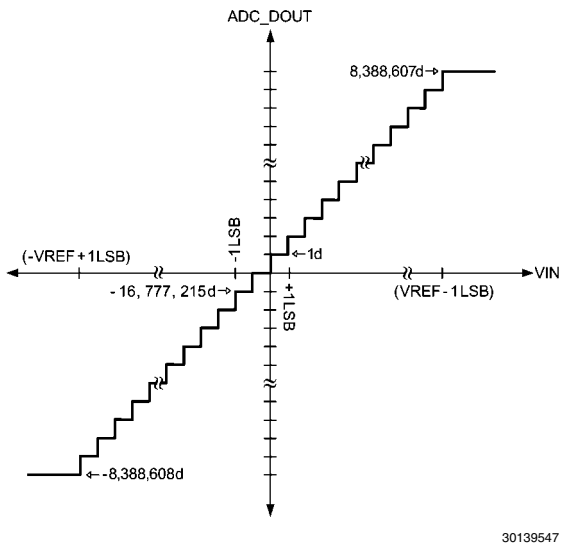


FIGURE 26. ADC_DOUT vs. VIN of a 24-Bit Resolution (VREF = 5.5V, Gain = 1).

17.4 REGISTER READ/WRITE EXAMPLES

17.4.1 Writing to Register Examples

Using the register read/write protocol shown in *Figure 17*, the following example shows how to write three data bytes starting at register address (ADDR) 0x1F. CSB should pulse between each transaction, and after the last byte has been written to ADDR 0x21, deassert CSB to end the register-write.

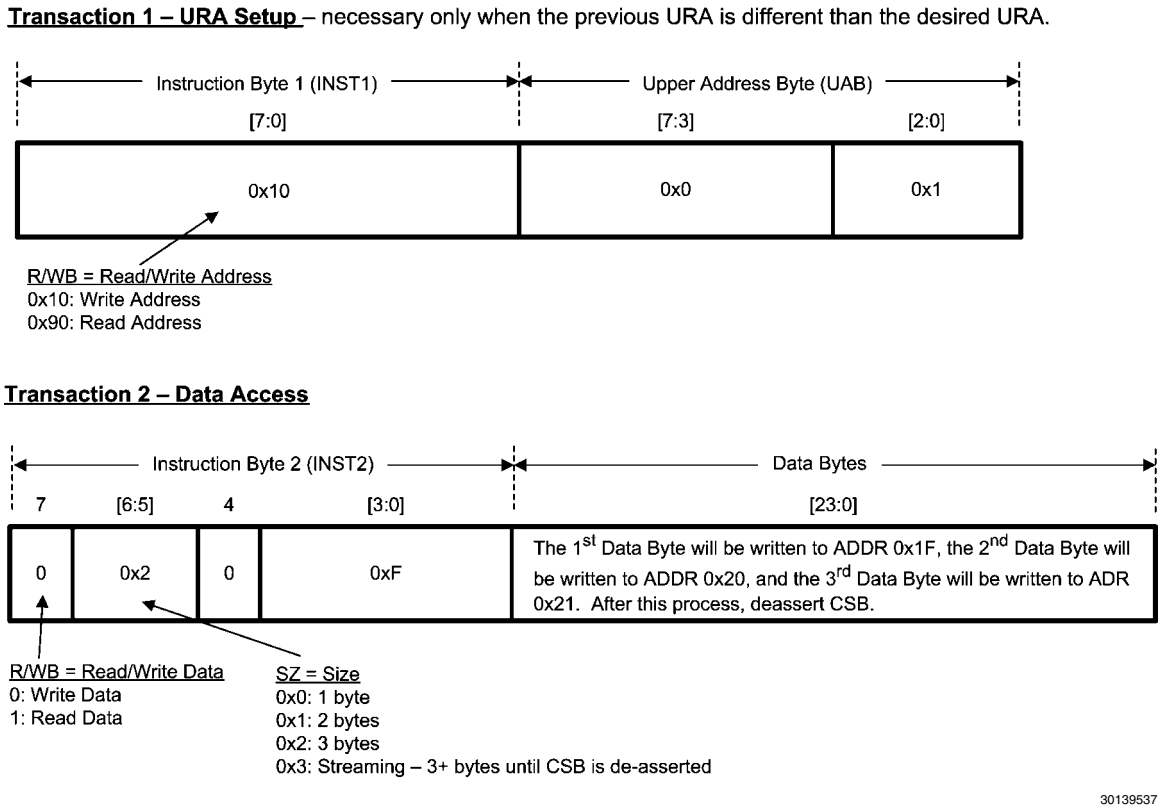


FIGURE 27. Register-Write Example 1

The next example shows how to write one data byte to ADDR 0x12. Since the URA for this example is the same as the last example, transaction 1 can be omitted.

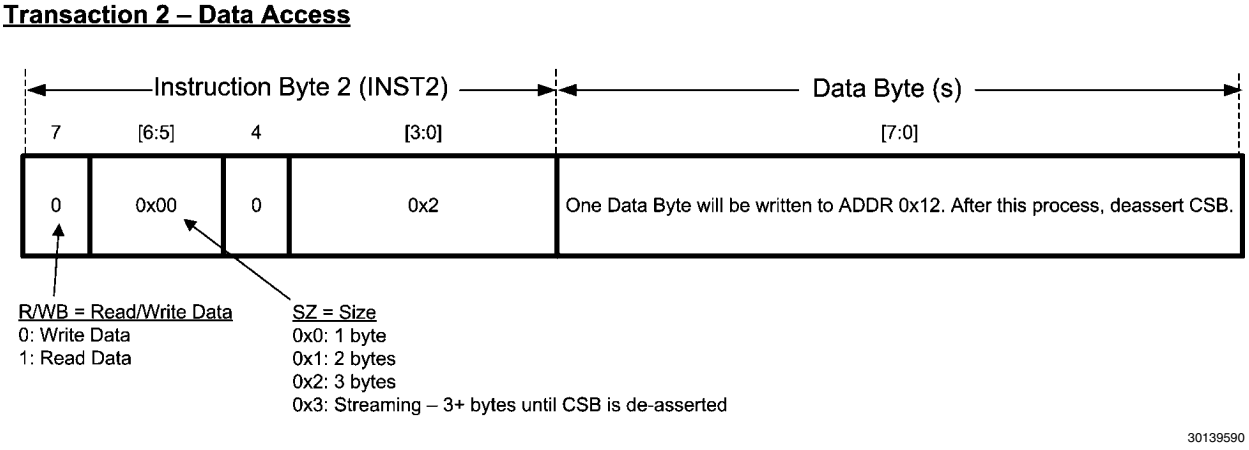


FIGURE 28. Register-Write Example 2

17.4.2 Reading from Register Example

The following example shows how to read two bytes. The first byte will be read from starting ADDR 0x24, and the second byte will be read from ADDR 0x25.

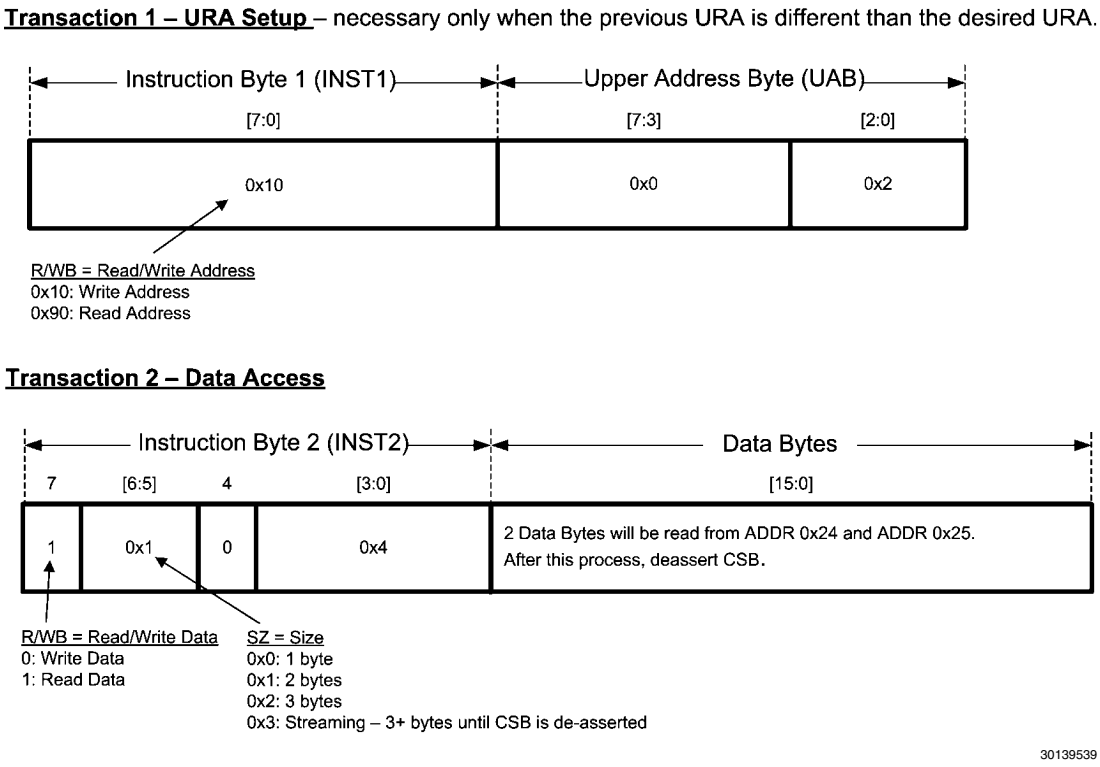


FIGURE 29. Register-Read Example

17.5 STREAMING EXAMPLES

17.5.1 Normal Streaming Example

This example shows how to write six data bytes starting at ADDR 0x28 using the Normal Streaming mode. Because the default STRM_TYPE is the Normal Streaming mode, setting up the SPI_STREAMCN register can be omitted.

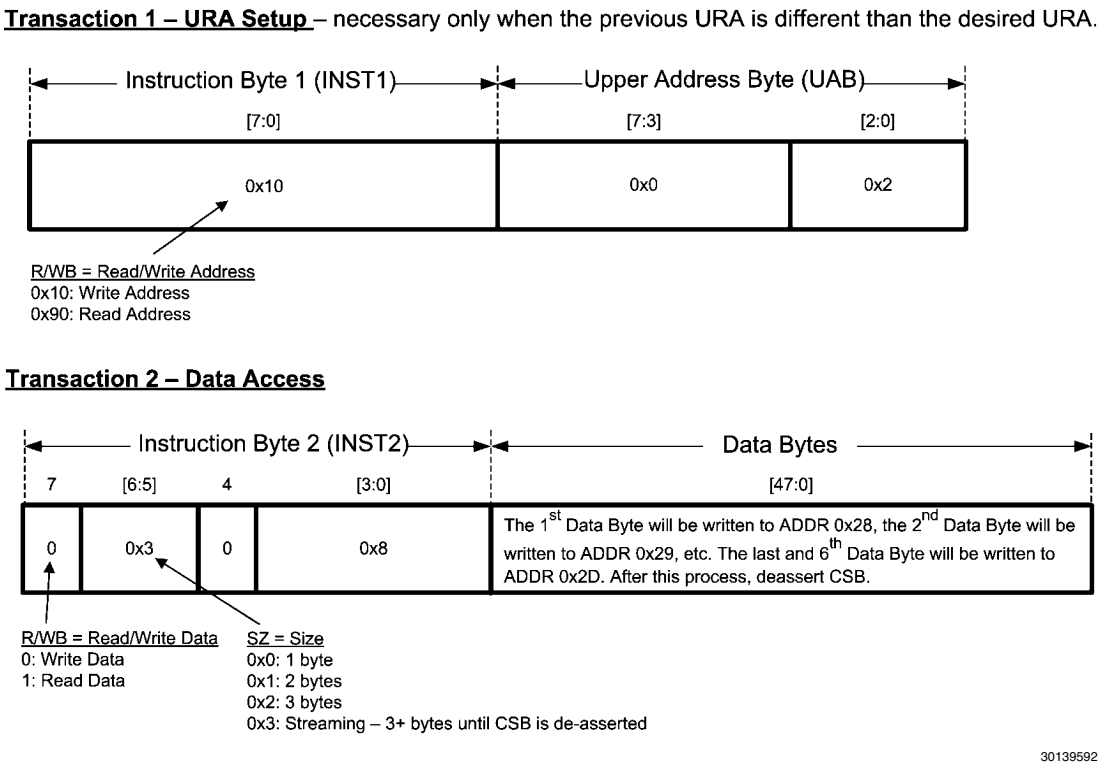


FIGURE 30. Normal Streaming Example

17.5.2 Controlled Streaming Example

This example shows how to read the 24-bit conversion data (ADC_DOUT) four times using the Controlled Streaming mode. The ADC_DOUT registers consist of ADC_DOUTH at ADDR 0x1A, ADC_DOUTM at ADDR 0x1B, and ADC_DOUTL at ADDR 0x1C.

The first step (*Figure 31*) sets up the SPI_STREAMCN register. This step enters the Controlled Streaming mode by setting STRM_TYPE high in ADDR 0x03. Since three registers (ADDR 0x1A - 0x1C) need to be read, the STRM_RANGE is 2.

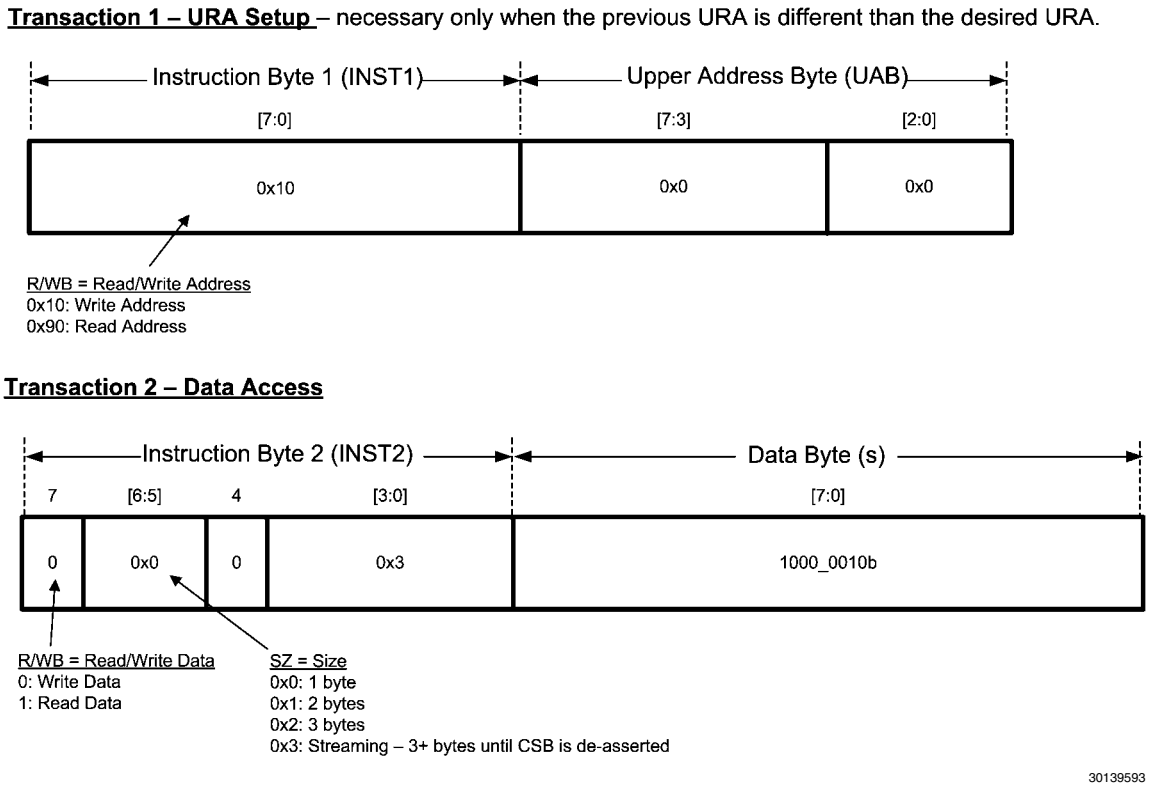
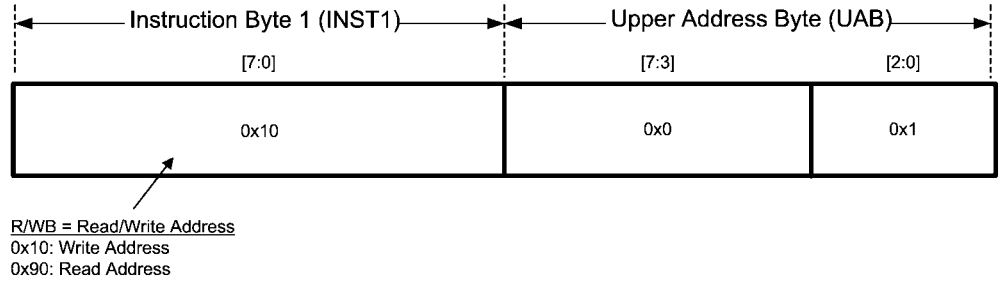


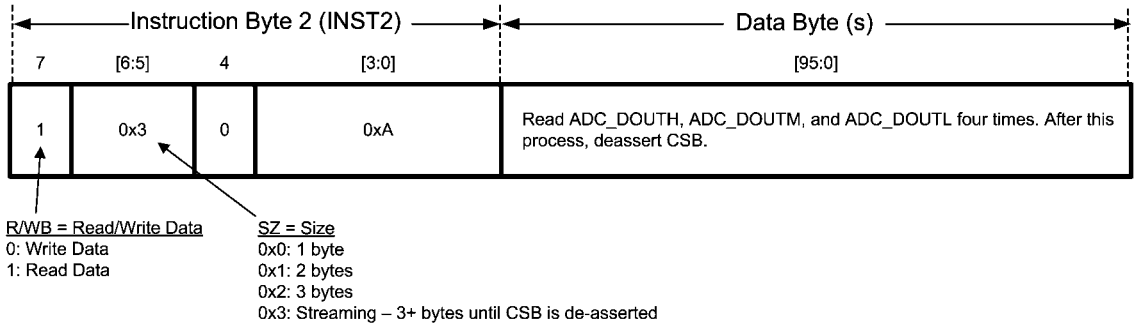
FIGURE 31. Setting up SPI_STREAMCN

The next step shows how to perform the Controlled Streaming mode so that the master device will read ADC_DOUT from ADDR 0x1A, 0x1B, 0x1C, then wrap back to ADDR 0x1A, and repeat this process for four times. After this process, deassert CSB to end the Controlled Streaming mode.

Transaction 1 – URA Setup – necessary only when the previous URA is different than the desired URA.



Transaction 2 – Data Access



30139594

FIGURE 32. Controlled Streaming Example

17.6 EXAMPLE APPLICATIONS

17.6.1 3–Wire RTD

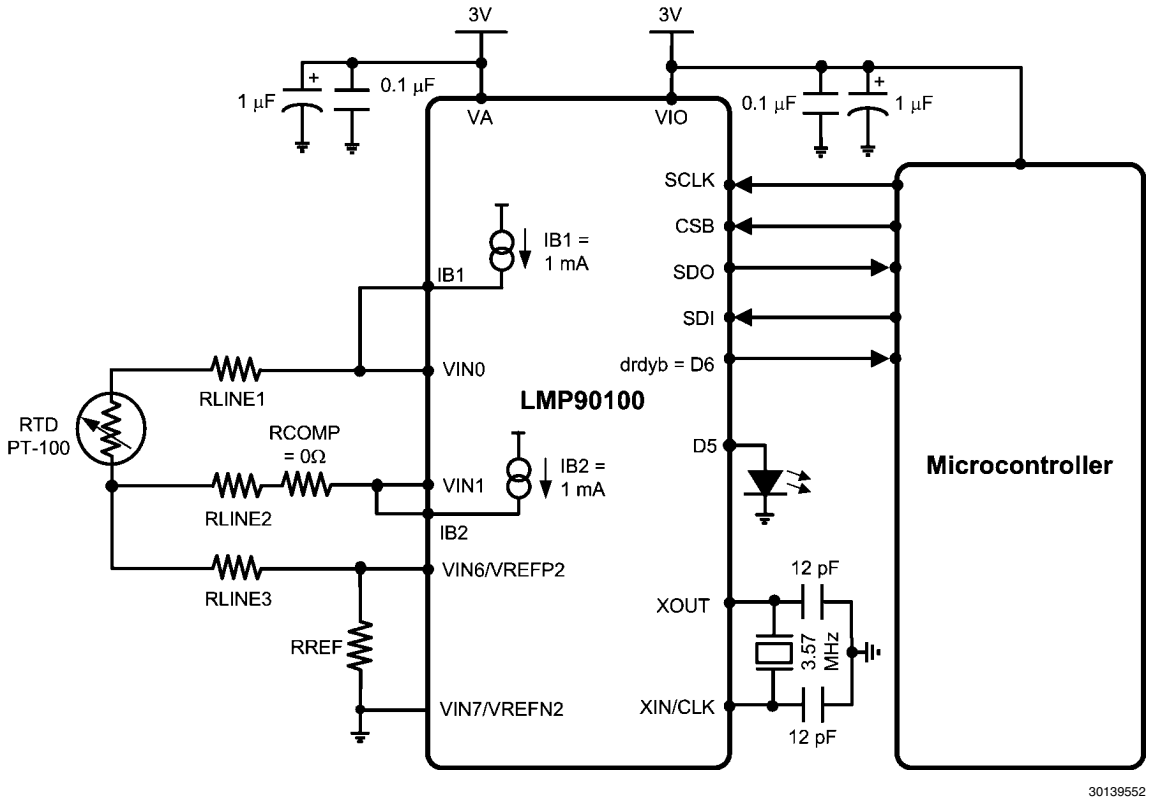


FIGURE 33. Topology #1: 3-wire RTD Using 2 Current Sources

Figure 33 shows the first topology for a 3-wire resistive temperature detector (RTD) application. Topology #1 uses two excitation current sources, IB1 and IB2, to create a differential voltage across VIN0 and VIN1. As a result of using both IB1 and IB2, only one channel (VIN0-VIN1) needs to be measured. As shown in Equation 2, the equation for this channel is IB1 x (RTD – RCOMP) assuming that RLINE1 = RLINE2.

VIN0 = IB1 (RLINE1 + RTD) + (IB1 + IB2) (RLINE3 + RREF)
VIN1 = IB2 (RLINE2 + RCOMP) + (IB1 + IB2) (RLINE3 + RREF)
If RLINE1 = RLINE2, then:
VIN = (VIN0 - VIN1) = IB1 (RTD - RCOMP)

Equation 2 — VIN Equation for Topology #1

The PT-100 changes linearly from 100 Ohm at 0°C to 146.07 Ohm at 120°C. If desired, choose a suitable compensating resistor (RCOMP) so that VIN can be virtually 0V at any desirable temperature. For example, if RCOMP = 100 Ohm, then at 0°C, VIN = 0V and thus a higher gain can be used.

The advantage of this circuit is its ratiometric configuration, where VREF = (IB1 + IB2) x (RREF). Equation 3 shows that a ratiometric configuration eliminates IB1 and IB2 from the output equation, thus increasing the overall performance.

$$ADC\_DOUT = \frac{VIN(Gain)}{2VREF}(2^n)$$

$$ADC\_DOUT = \frac{[IB1(RTD - RCOMP)Gain]}{2(IB1+IB2)RREF}(2^n)$$

$$ADC\_DOUT = \frac{[(RTD - RCOMP)Gain]}{2(2)RREF}(2^n)$$

Equation 3 — ADC_DOUT Showing IB1 & IB2 Elimination

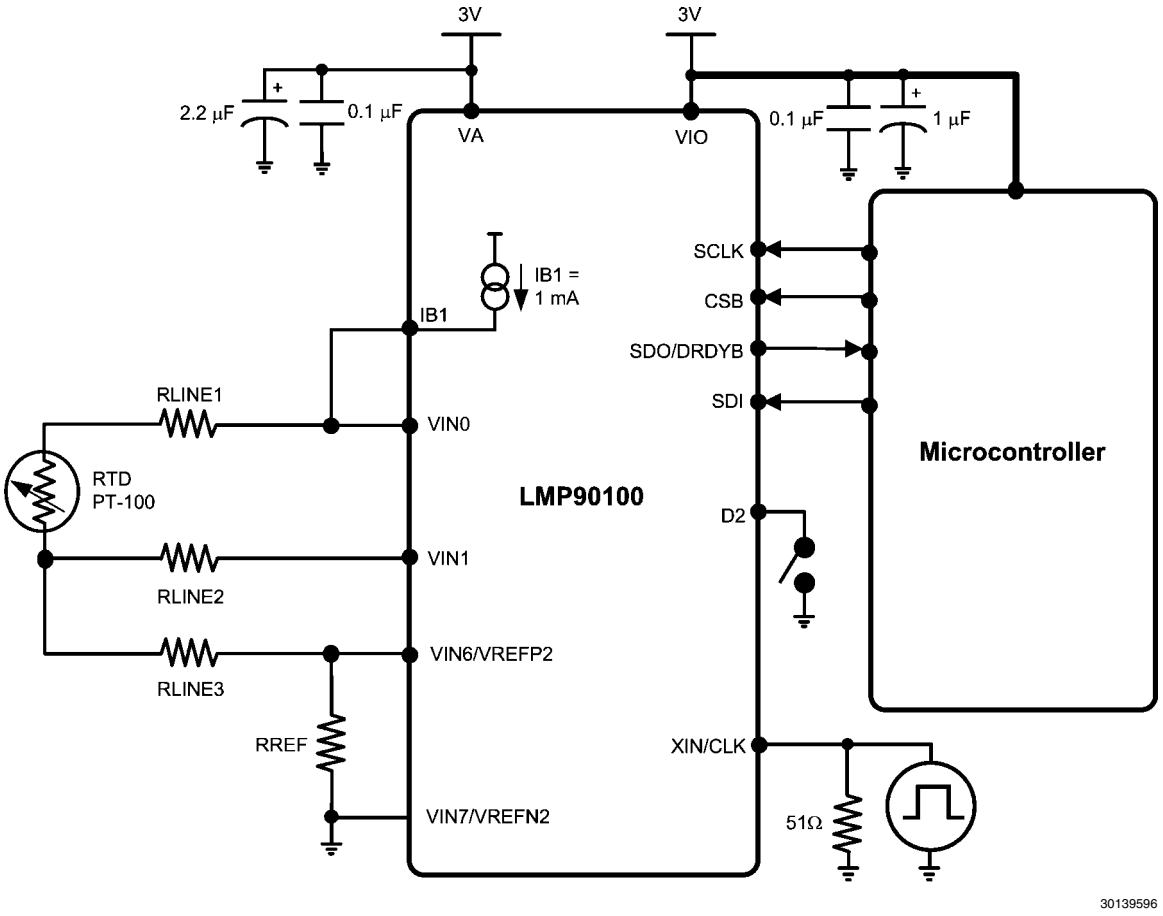


FIGURE 34. Topology #2: 3-wire RTD Using 1 Current Source

Figure 34 shows the second topology for a 3-wire RTD application. Topology #2 shows the same connection as topology #1, but without IB2. Although this topology eliminates a current source, it requires two channel measurements as shown in Equation 4.

VIN0 = IB1 (RLINE1 + RTD + RLINE3 + RREF)
VIN1 = IB1 (RLINE3 + RREF)
VIN6 = IB1 (RREF)

CH0 = VIN0 - VIN1 = IB1 (RLINE1 + RTD)
CH1 = VIN1 - VIN6 = IB1 (RLINE3)

Assume RLINE1 = RLINE3, thus:
CH0 - CH1 = IB1 (RTD)

Equation 4 — VIN Equation for Topology #2

17.6.2 Thermocouple and IC Analog Temperature

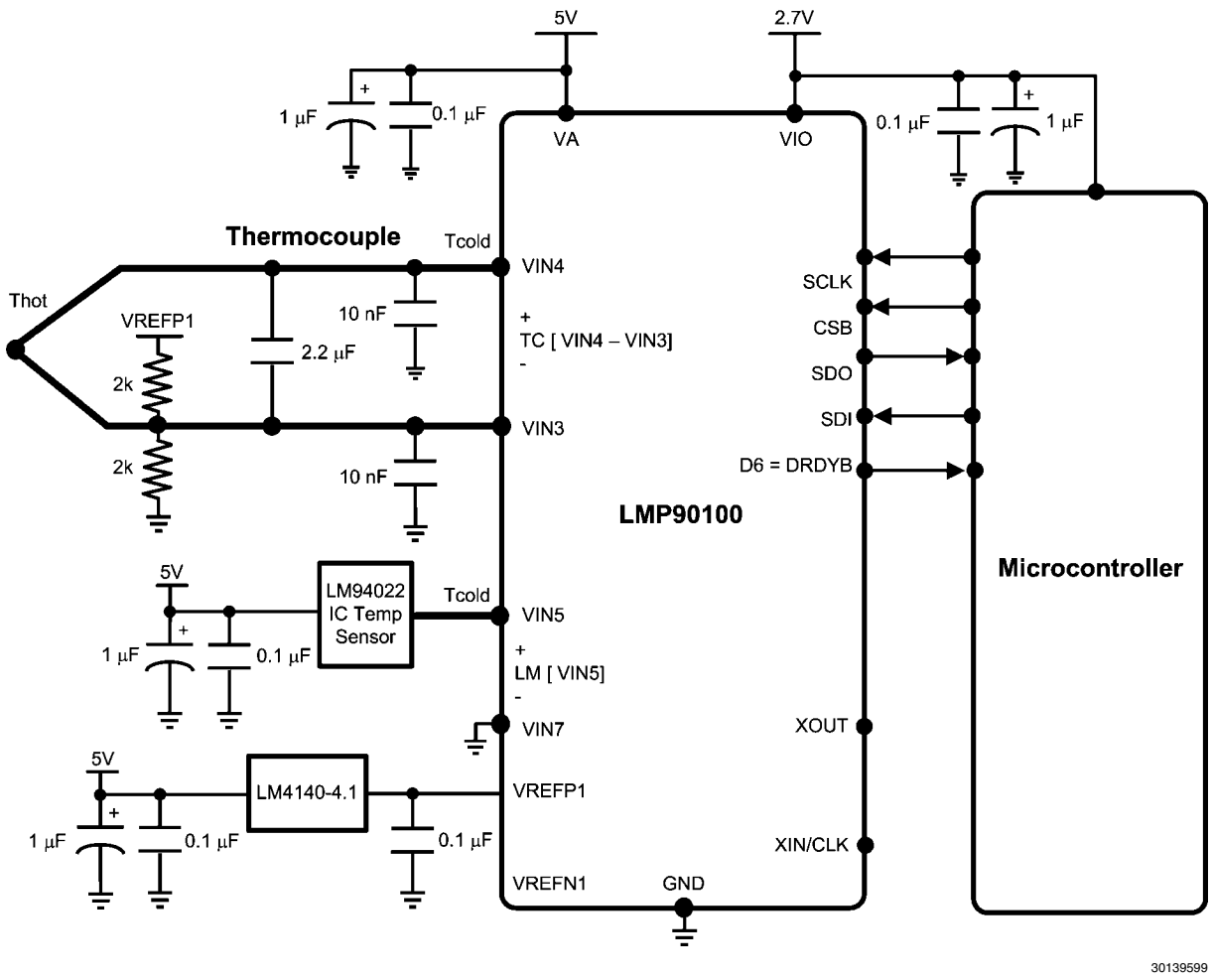


FIGURE 35. Thermocouple with CJC

The LMP90100 is also ideal for thermocouple temperature applications. Thermocouples have several advantages that make them popular in many industrial and medical applications. Compare to RTDs, thermistors, and IC sensors, thermocouples are the most rugged, least expensive, and can operate over the largest temperature range.

A thermocouple is a sensor whose junction generates a differential voltage, VIN, that is relative to the temperature difference (Thot – Tcold). Thot is also known as the measuring junction or "hot" junction, which is placed at the measured environment. Tcold is also known as the reference or "cold" junction, which is placed at the measuring system environment.

Because a thermocouple can only measure a temperature difference, it does not have the ability to measure absolute temperature. To determine the absolute temperature of the measured environment (Thot), a technique known as cold junction compensation (CJC) must be used.

In a CJC technique, the "cold" junction temperature, Tcold, is sensed by using an IC temperature sensor, such as the LM94022. The temperature sensor should be placed within close proximity of the reference junction and should have an isothermal connection to the board to minimize any potential temperature gradients.

Once Tcold is obtained, use a standard thermocouple look-up-table to find its equivalent voltage. Next, measure the differential thermocouple voltage and add the equivalent cold junction voltage. Lastly, convert the resulting voltage to temperature using a standard thermocouple look-up-table.

For example, assume Tcold = 20°C. The equivalent voltage from a type K thermocouple look-up-table is 0.798 mV. Next, add the measured differential thermocouple voltage to the Tcold equivalent voltage. For example, if the thermocouple voltage is 4.096 mV, the total would be 0.798 mV + 4.096 mV = 4.894 mV. Referring to the type K thermocouple table gives a temperature of 119.37°C for 4.894 mV.

18.0 Registers

1. If written to, RESERVED bits must be written to only 0 unless otherwise indicated.
2. Read back value of RESERVED bits and registers is unspecified and should be discarded.
3. Recommended values must be programmed and forbidden values must not be programmed where they are indicated in order to avoid unexpected results.
4. If written to, registers indicated as Reserved must have the indicated default value as shown below. Any other value can cause unexpected results.

18.1 REGISTER MAP

Register Name		ADDR (URA & LRA)	Type	Default
RESETCN	Reset Control	0x00	WO	-
SPI_HANDSHAKECN	SPI Handshake Control	0x01	R/W	0x00
Reserved	-	0x02	-	0x00
SPI_STREAMCN	SPI Stream Control	0x03	R/W	0x00
Reserved	-	0x04 - 0x07	-	0x00
PWRCN	Power Mode Control and Status	0x08	RO & WO	0x00
DATA_ONLY_1	Data Only Read Control 1	0x09	R/W	0x1A
DATA_ONLY_2	Data Only Read Control 2	0x0A	R/W	0x02
ADC_RESTART	ADC Restart Conversion	0x0B	WO	-
Reserved	-	0x0C - 0x0D	-	0x00
GPIO_DIRCN	GPIO Direction Control	0x0E	R/W	0x00
GPIO_DAT	GPIO Data	0x0F	RO & WO	-
BGCALCN	Background Calibration Control	0x10	R/W	0x00
SPI_DRDYBCN	SPI Data Ready Bar Control	0x11	R/W	0x03
ADC_AUXCN	ADC Auxiliary Control	0x12	R/W	0x00
SPI_CRC_CN	CRC Control	0x13	R/W	0x02
SENDIAG_THLD	Sensor Diagnostic Threshold 1,0	0x14 - 0x15	R/W	0x0000
Reserved	-	0x16	-	0x00
SCALCN	System Calibration Control	0x17	R/W	0x00
ADC_DONE	ADC Data Available	0x18	RO	-
SENDIAG_FLAGS	Sensor Diagnostic Flags	0x19	RO	-
ADC_DOUT	Conversion Data 2,1,0	0x1A - 0x1C	RO	-
SPI_CRC_DAT	CRC Data	0x1D	RO & WO	-
CHANNEL CONFIGURATION REGISTERS				
CH_STS	Channel Status	0x1E	RO	0x00
CH_SCAN	Channel Scan Mode	0x1F	R/W	0x30
CH0_INPUTCN	CH0 Input Control	0x20	R/W	0x01
CH0_CONFIG	CH0 Configuration	0x21	R/W	0x70
CH1_INPUTCN	CH1 Input Control	0X22	R/W	0x13
CH1_CONFIG	CH1 Configuration	0x23	R/W	0x70
CH2_INPUTCN	CH2 Input Control	0x24	R/W	0x25
CH2_CONFIG	CH2 Configuration	0x25	R/W	0x70
CH3_INPUTCN	CH3 Input Control	0x26	R/W	0x37
CH3_CONFIG	CH3 Configuration	0x27	R/W	0x70
CH4_INPUTCN	CH4 Input Control	0x28	R/W	0x01
CH4_CONFIG	CH4 Configuration	0x29	R/W	0x70
CH5_INPUTCN	CH5 Input Control	0x2A	R/W	0x13
CH5_CONFIG	CH5 Configuration	0x2B	R/W	0x70
CH6_INPUTCN	CH6 Input Control	0x2C	R/W	0x25

Register Name		ADDR (URA & LRA)	Type	Default
CH6_CONFIG	CH6 Configuration	0x2D	R/W	0x70
Reserved	-	0x2E - 0x2F	-	0x00
SYSTEM CALIBRATION REGISTERS				
CH0_SCAL_OFFSET	CH0 System Calibration Offset Coefficients	0x30 - 0x32	R/W	0x00_0000
CH0_SCAL_GAIN	CH0 System Calibration Gain Coefficients	0x33 - 0x35	R/W	0x80_0000
Reserved	-	0x36	-	0x01
Reserved	-	0x37	-	0x00
CH1_SCAL_OFFSET	CH1 System Calibration Offset Coefficients	0x38 - 0x3A	R/W	0x00_0000
CH1_SCAL_GAIN	CH1 System Calibration Gain Coefficient	0x3B - 0x3D	R/W	0x80_0000
Reserved	-	0x3E	-	0x01
Reserved	-	0x3F	-	0x00
CH2_SCAL_OFFSET	CH2 System Calibration Offset Coefficients	0x40 - 0x42	R/W	0x00_0000
CH2_SCAL_GAIN	CH2 System Calibration Gain Coefficient	0x43 - 0x45	R/W	0x80_0000
Reserved	-	0x46	-	0x01
Reserved	-	0x47	-	0x00
CH3_SCAL_OFFSET	CH3 System Calibration Offset Coefficients	0x48 - 0x4A	R/W	0x00_0000
CH3_SCAL_GAIN	CH3 System Calibration Gain Coefficient	0x4B - 0x4D	R/W	0x80_0000
Reserved	-	0x4E	-	0x01
Reserved	-	0x4F - 0x7F	-	0x00

18.2 POWER AND RESET REGISTERS

RESETCN: Reset Control (Address 0x00)

Bit	Bit Symbol	Bit Description
[7:0]	REG_AND_CNV_ RST	Register and Conversion Reset **0xC3:** Register and conversion reset **Others:** Neglected

PWRCN: Power Mode Control and Status (Address 0x08)

Bit	Bit Symbol	Bit Description
[7:2]	Reserved	-
[1:0]	PWRCN	Power Control Write Only – power down mode control **0x0:** Active Mode **0x1:** Power-down Mode **0x3:** Stand-by Mode Read Only – the present mode is: **0x0 (default):** Active Mode **0x1:** Power-down Mode **0x3:** Stand-by Mode

18.3 ADC REGISTERS

ADC_RESTART: ADC Restart Conversion (Address 0x0B)

Bit	Bit Symbol	Bit Description
[7:1]	Reserved	-
0	RESTART	Restart conversion **1**: Restart conversion.

14.2.1. ADC_AUXCN: ADC Auxiliary Control (Address 0x12)

Bit	Bit Symbol	Bit Description
7	Reserved	-
6	RESET_SYSCAL	The System Calibration registers (CHx_SCAL_OFFSET and CHx_SCAL_GAIN) are: **0 (default):** preserved even when "REG_AND_CNV_ RST" = 0xC3. **1:** reset by setting "REG_AND_CNV_ RST" = 0xC3.
5	CLK_EXT_DET	External clock detection **0 (default):** "External Clock Detection" is operational **1:** "External-Clock Detection" is bypassed
4	CLK_SEL	Clock select – only valid if CLK_EXT_DET = 1 **0 (default):** Selects internal clock **1:** Selects external clock
[3:0]	RTD_CUR_SEL	Selects RTD Current as follows: **0x0 (default):** 0 µA **0x1:** 100 µA **0x2:** 200 µA **0x3:** 300 µA **0x4:** 400 µA **0x5:** 500 µA **0x6:** 600 µA **0x7**: 700 µA **0x8:** 800 µA **0x9:** 900 µA **0xA:** 1000 µA

ADC_DONE: ADC Data Available (Address 0x18)

Bit	Bit Symbol	Bit Description
[7:0]	DT_AVAIL_B	Data Available – indicates if new conversion data is available **0x00 – 0xFE:** Available **0xFF:** Not available

ADC_DOUT: 24-bit Conversion Data (two's complement) (Address 0x1A - 0x1C)

Address	Name	Register Description
0x1A	ADC_DOUTH	ADC Conversion Data [23:16]
0x1B	ADC_DOUTM	ADC Conversion Data [15:8]
0x1C	ADC_DOUTL	ADC Conversion Data [7:0]

Note: Repeat reads of these registers are allowed as long as such reads are spaced apart by at least 72 µs.

18.4 CHANNEL CONFIGURATION REGISTERS

CH_STS: Channel Status (Address 0x1E)

Bit	Bit Symbol	Bit Description
[7:2]	Reserved	-
1	CH_SCAN_NRDY	Channel Scan Not Ready – indicates if it is okay to program CH_SCAN 0: Update not pending, CH_SCAN register is okay to program 1: Update pending, CH_SCAN register is not ready to be programmed
0	INV_OR_RPT_RD_STS	Invalid or Repeated Read Status 0: ADC_DOUT just read was valid and hitherto unread 1: ADC_DOUT just read was either invalid (not ready) or there was a repeated read.

CH_SCAN: Channel Scan Mode (Address 0x1F)

Bit	Bit Symbol	Bit Description
[7:6]	CH_SCAN_SEL	Channel Scan Select **0x0 (default):** ScanMode0: Single-Channel Continuous Conversion **0x1:** ScanMode1: One or more channels Single Scan **0x2:** ScanMode2: One or more channels Continuous Scan **0x3**: ScanMode3: One or more channels Continuous Scan with Burnout Currents
[5:3]	LAST_CH	Last channel for conversion **0x0:** CH0 **0x1:** CH1 **0x2:** CH2 **0x3:** CH3 **0x4:** CH4 **0x5:** CH5 **0x6 (default):** CH6 Note: LAST_CH cannot be smaller than FIRST_CH. For example, if LAST_CH = CH5, then FIRST_CH cannot be CH6. If 0x7 is written it is ignored.
[2:0]	FIRST_CH	Starting channel for conversion **0x0 (default):** CH0 **0x1:** CH1 **0x2:** CH2 **0x3:** CH3 **0x4:** CH4 **0x5:** CH5 **0x6:** CH6 Note: FIRST_CH cannot be greater than LAST_CH. For example, if FIRST_CH = CH1, then LAST_CH cannot be CH0. If 0x7 is written it is ignored.

Note: While writing to the CH_SCAN register, if 0x7 is written to FIRST_CH or LAST_CH the write to the entire CH_SCAN register is ignored.

CHx_INPUTCN: Channel Input Control

Register Address (hex):

a. CH0: 0x20

b. CH1: 0X22

c. CH2: 0x24

d. CH3: 0x26

e. CH4: 0x28

f. CH5: 0x2A

g. CH6: 0x2C

Bit	Bit Symbol	Bit Description
7	BURNOUT_EN	Enable sensor diagnostic **0 (default):** Disable Sensor Diagnostics current injection for this Channel **1:** Enable Sensor Diagnostics current injection for this Channel
6	VREF_SEL	Select the reference 0 (Default): Select VREFP1 and VREFN1 1: Select VREFP2 and VREFN2
[5:3]	VINP	Positive input select **0x0:** VIN0 **0x1:** VIN1 **0x2:** VIN2 **0x3:** VIN3 **0x4:** VIN4 **0x5:** VIN5 **0x6:** VIN6 **0x7:** VIN7 Note: to see the default values for each channel, refer to the table below.
[2:0]	VINN	Negative input select **0x0:** VIN0 **0x1:** VIN1 **0x2:** VIN2 **0x3:** VIN3 **0x4:** VIN4 **0x5:** VIN5 **0x6:** VIN6 **0x7:** VIN7 Note: to see the default values for each channel, refer to the table below.

Default VINx for CH0-CH6

	VINP	**VINN**
CH0	VIN0	VIN1
CH1	VIN2	VIN3
CH2	VIN4	VIN5
CH3	VIN6	VIN7
CH4	VIN0	VIN1
CH5	VIN2	VIN3
CH6	VIN4	VIN5

CHx_CONFIG: Channel Configuration

Register Address (hex):

a. CH0: 0x21

b. CH1: 0x23

c. CH2: 0x25

d. CH3: 0x27

e. CH4: 0x29

f. CH5: 0x2B

g. CH6: 0x2D

Bit	Bit Symbol	Bit Description
7	Reserved	-
[6:4]	ODR_SEL	ODR Select **0x0:** 13.42 / 8 = 1.6775 SPS **0x1:** 13.42 / 4 = 3.355 SPS **0x2:** 13.42 / 2 = 6.71 SPS **0x3:** 13.42 SPS **0x4:** 214.65 / 8 = 26.83125 SPS **0x5:** 214.65 / 4 = 53.6625 SPS **0x6:** 214.65 / 2 = 107.325 SPS **0x7 (default):** 214.65 SPS
[3:1]	GAIN_SEL	Gain Select **0x0 (default):** 1 (FGA OFF) **0x1:** 2 (FGA OFF) **0x2:** 4 (FGA OFF) **0x3:** 8 (FGA OFF) **0x4:** 16 (FGA ON) **0x5:** 32 (FGA ON) **0x6:** 64 (FGA ON) **0x7:** 128 (FGA ON)
0	BUF_EN	Enable/Disable the buffer **0 (default):** Include the buffer in the signal path **1:** Exclude the buffer from the signal path Note: When gain ≥ 16, the buffer is automatically included in the signal path irrespective of this bit.

18.5 CALIBRATION REGISTERS

BGCALCN: Background Calibration Control (Address 0x10)

Bit	Bit Symbol	Bit Description
[7:2]	Reserved	-
[1:0]	BGCALN	Background calibration control – selects scheme for continuous background calibration. **0x0 (default):** BgcalMode0: Background Calibration OFF **0x1:** BgcalMode1: Offset Correction / Gain Estimation **0x2:** BgcalMode2: Offset Correction / Gain Correction **0x3:** BgcalMode3: Offset Estimation / Gain Estimation

SCALCN: System Calibration Control (Address 0x17)

Bit	Bit Symbol	Bit Description
[7:2]	Reserved	-
[1:0]	SCALCN	System Calibration Control When written, set SCALCN to: **0x0 (default):** Normal Mode **0x1:** “System Calibration Offset Coefficient Determination” mode **0x2:** “System Calibration Gain Coefficient Determination” mode **0x3:** Reserved When read, this bit indicates the system calibration mode is in: **0x0:** Normal Mode **0x1:** "System Calibration Offset Coefficient Determination" mode **0x2:** "System Calibration Gain Coefficient Determination" mode **0x3:** Reserved Note: when read, this bit will indicate the current System Calibration status. Since this coefficient determination mode will only take 1 conversion cycle, reading this register will only return 0x00, unless this register is read within 1 conversion window.

CHx_SCAL_OFFSET: CH0-CH3 System Calibration Offset Registers (Two's-Complement)

ADDR				Name	Description
CH0	CH1	CH2	CH3		
0x30	0x38	0x40	0x48	CHx_SCAL_OFFSETH	System Calibration Offset Coefficient Data [23:16]
0x31	0x39	0x41	0x49	CHx_SCAL_OFFSETM	System Calibration Offset Coefficient Data [15:8]
0x32	0x3A	0x42	0x4A	CHx_SCAL_OFFSETL	System Calibration Offset Coefficient Data[7:0]

CHx_SCAL_GAIN: CH0-CH3 System Calibration Gain Registers (Two's-Complement)

ADDR				Name	Description
CH0	CH1	CH2	CH3		
0x33	0x3B	0x43	0x4B	CHx_SCAL_GAINH	System Calibration Gain Coefficient Data [23:16]
0x34	0x3C	0x44	0x4C	CHx_SCAL_GAINM	System Calibration Gain Coefficient Data [15:8]
0x35	0x3D	0x45	0x4D	CHx_SCAL_GAINL	System Calibration Gain Coefficient Data[7:0]

18.6 SENSOR DIAGNOSTIC REGISTERS

SENDIAG_THLD: Sensor Diagnostic Threshold (Address 0x14 - 0x15)

Address	Name	Register Description
0x14	SENDIAG_THLDH	Sensor Diagnostic threshold [15:8]
0x15	SENDIAG_THLDL	Sensor Diagnostic threshold [7:0]

SENDIAG_FLAGS: Sensor Diagnostic Flags (Address 0x19)

Bit	Bit Symbol	Bit Description
7	SHORT_THLD_ FLAG	Short Circuit Threshold Flag = 1 when the absolute value of VOUT is within the absolute threshold voltage set by SENDIAG_THLDH and SENDIAG_THLDL.
6	RAILS_FLAG	Rails Flag = 1 when at least one of the inputs is near rail (VA or VSS).
5	POR_AFT_LST_RD	Power-on-reset after last read = 1 when there was a power-on-reset event since the last time the SENDIAG_FLAGS register was read.
[4:3]	OFLO_FLAGS	Overflow flags **0x0:** Normal operation **0x1:** The modulator was not overranged, but ADC_DOUT got clamped to 0x7f_ffff (positive fullscale) or 0x80_0000 (negative full scale) **0x2:** The modulator was over-ranged towards VA **0x3:** The modulator was over-ranged towards VSS
[2:0]	SAMPLED_CH	Channel Number – the sampled channel for ADC_DOUT and SENDIAG_FLAGS.

18.7 SPI REGISTERS

SPI_HANDSHAKECN: SPI Handshake Control (Address 0x01)

Bit	Bit Symbol	Bit Description			
[7:4]	Reserved	-			
[3:1]	SDO_DRDYB_ DRIVER	SDO/DRDYB Driver – sets who is driving the SDO/DRYB pin			
			Whenever CSB is Asserted and the Device is Reading ADC_DOUT	**Whenever CSB is Asserted and the Device is Not Reading ADC_DOUT**	**CSB is Deasserted**
		0x0 (default)	SDO is driving	DRDYB is driving	High-Z
		0x3	SDO is driving	DRDYB is driving	DRDYB is driving
		0x4	SDO is driving	High-Z	High-Z
		Others	Forbidden		
0	SW_OFF_TRG	Switch-off trigger - refers to the switching of the output drive from the slave to the master. **0 (default):** SDO will be high-Z after the last (16th, 24th, 32nd, etc) rising edge of SCLK. This option allows time for the slave to transfer control back to the master at the end of the frame. **1:** SDO's high-Z is postponed to the subsequent falling edge following the last (16th, 24th, 32nd, etc) rising edge of SCLK. This option provides additional hold time for the last bit, DB0, in non-streaming read transfers.			

SPI_STREAMCN: SPI Streaming Control (Address 0x03)

Bit	Bit Symbol	Bit Description
7	STRM_TYPE	Stream type **0 (default):** Normal Streaming mode **1:** Controlled Streaming mode
[6:0]	STRM_ RANGE	Stream range – selects Range for Controlled Streaming mode **Default:** 0x00

DATA_ONLY_1: Data Only Read Control 1 (Address 0x09)

Bit	Bit Symbol	Bit Description
7	Reserved	-
[6:0]	DATA_ONLY_ADR	Start address for the Data Only Read Transaction **Default:** 0x1A Please refer to the description of DT_ONLY_SZ in DATA_ONLY_2 register.

DATA_ONLY_2: Data Only Read Control 2 (Address 0x0A)

Bit	Bit Symbol	Bit Description
[7:3]	Reserved	-
[2:0]	DATA_ONLY_SZ	Number of bytes to be read out in Data Only mode. A value of 0x0 means read one byte and 0x7 means read 8 bytes. **Default:** 0x2

SPI_DRDYBCN: SPI Data Ready Bar Control (Address 0x11)

Bit	Bit Symbol	Bit Description
7	SPI_DRDYB_D6	Enable DRDYB on D6 **0 (default):** D6 is a GPIO **1:** D6 = drdyb signal
[6:4]	Reserved	-
5	DIS_DRDYB_QLFN	Enable DRDYB on D6 **0 (default):** Enter Data-Only mode when both DRDYB and CSB are asserted **1:** Enter Data-Only mode when CSB is asserted
3	FGA_BGCAL	Gain background calibration **0 (default):** Correct FGA gain error. This is useful only if the device is operating in BgcalMode2 and ScanMode2 or ScanMode3. **1:** Correct FGA gain error using the last known coefficients.
[2:0]	Reserved	Default - 0x3 (do not change this value)

SPI_CRC_CN: CRC Control (Address 0x13)

Bit	Bit Symbol	Bit Description
[7:5]	Reserved	-
4	EN_CRC	Enable CRC **0 (default):** Disable CRC **1:** Enable CRC
3	DIS_CRC_RST	**0:** CRC is not reinitialized at the end of the data only transaction. This way, CRC checking can be extended to include any ADC_DOUT that follows the data only read transaction. It could also include ADC_DOUT of subsequent data only read transactions. **1 (default):** CRC is reinitialized at the end of the data only read transaction.
2	DRDYB_AFT_CRC	DRDYB After CRC **0 (default):** DRDYB is deasserted (active high) after ADC_DOUTL is read. **1:** DRDYB is deasserted after SPI_CRC_DAT (which follows ADC_DOUTL), is read.
[1:0]	Reserved	-

SPI_CRC_DAT: CRC Data (Address 0x1D)

Bit	Bit Symbol	Bit Description
[7:0]	CRC_DAT	CRC Data When written, this register reset CRC: **Any Value:** Reset CRC When read, this register indicates the CRC data.

18.8 GPIO REGISTERS

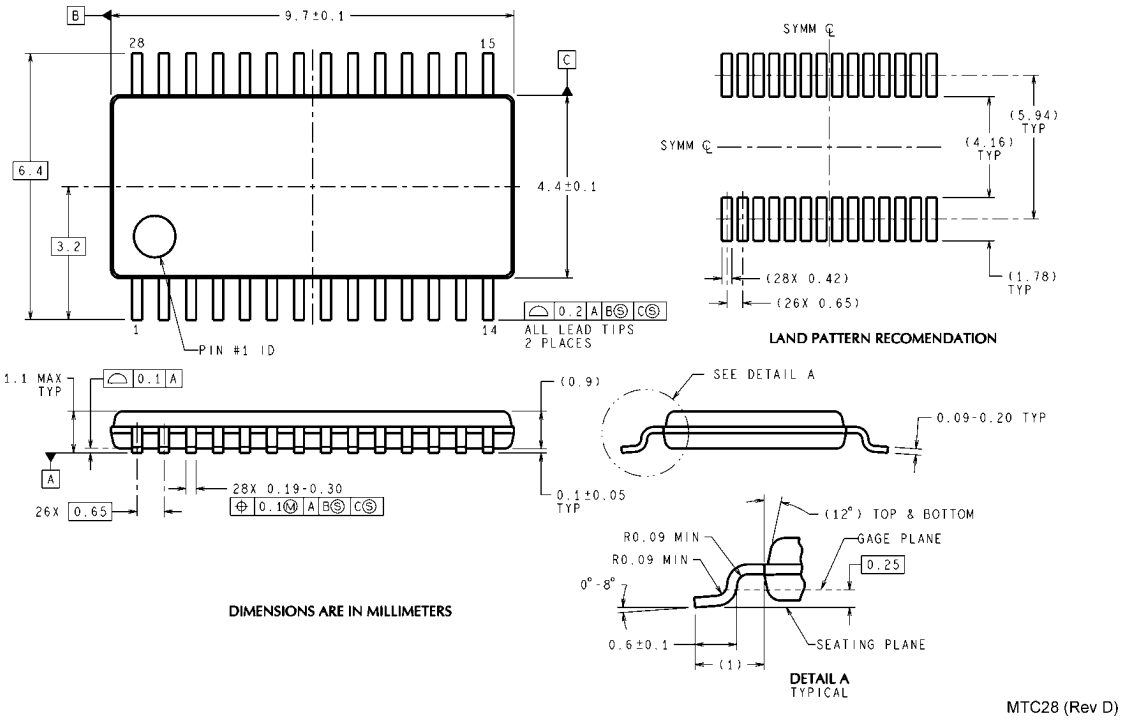
GPIO_DIRCN: GPIO Direction (Address 0x0E)

Bit	Bit Symbol	Bit Description
7	Reserved	-
x	GPIO_DIRCNx	GPIO direction control – these bits are used to control the direction of each General Purpose Input/Outputs (GPIO) pins D0 - D6. **0 (default):** Dx is an Input **1:** Dx is an Output where 0 ≤ x ≤ 6. For example, writing a 1 to bit 6 means D6 is an Output. Note: If D6 is used for DRDYB, then it cannot be used for GPIO.

GPIO_DAT: GPIO Data (Address 0x0F)

Bit	Bit Symbol	Bit Description
7	Reserved	-
x	Dx	Write Only - when GPIO_DIRCN = 0 0: Dx is LO 1: Dx is HI Read Only - when GPIO_DIRCN = 1 0: Dx driven LO 1: Dx driven HI where 0 ≤ x ≤ 6. For example, writing a 0 to bit 4 means D4 is LO.

19.0 Physical Dimensions inches (millimeters) unless otherwise noted



MTC28 (Rev D)

28-Lead Molded Plastic TSSOP
Order NumberLMP90100MH/NOPB, LMP90100MHE/NOPB, LMP90100MHX/NOPB
NS Package Number MO-153

Notes

Notes

For more National Semiconductor product information and proven design tools, visit the following Web sites at:
www.national.com

Products		Design Support	
Amplifiers	www.national.com/amplifiers	WEBENCH® Tools	www.national.com/webench
Audio	www.national.com/audio	App Notes	www.national.com/appnotes
Clock and Timing	www.national.com/timing	Reference Designs	www.national.com/refdesigns
Data Converters	www.national.com/adc	Samples	www.national.com/samples
Interface	www.national.com/interface	Eval Boards	www.national.com/evalboards
LVDS	www.national.com/lvds	Packaging	www.national.com/packaging
Power Management	www.national.com/power	Green Compliance	www.national.com/quality/green
Switching Regulators	www.national.com/switchers	Distributors	www.national.com/contacts
LDOs	www.national.com/ldo	Quality and Reliability	www.national.com/quality
LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback
Voltage References	www.national.com/vref	Design Made Easy	www.national.com/easy
PowerWise® Solutions	www.national.com/powerwise	Applications & Markets	www.national.com/solutions
Serial Digital Interface (SDI)	www.national.com/sdi	Mil/Aero	www.national.com/milaero
Temperature Sensors	www.national.com/tempsensors	SolarMagic™	www.national.com/solarmagic
PLL/VCO	www.national.com/wireless	PowerWise® Design University	www.national.com/training

For the most current product information visit us at www.national.com

National Semiconductor Americas Technical Support Center
Email: support@nsc.com
Tel: 1-800-272-9959

National Semiconductor Europe Technical Support Center
Email: europe.support@nsc.com

National Semiconductor Asia Pacific Technical Support Center
Email: ap.support@nsc.com

National Semiconductor Japan Technical Support Center
Email: jpn.feedback@nsc.com