

# BGA758L7

5-6 GHz LNA for WLAN

## Data Sheet

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Preliminary

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**BGA758L7 5-6 GHz LNA for WLAN**
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Page	Subjects (major changes since last revision)
all	Preliminary data sheet
all	New document layout
7, 8, 10	Electrical Characteristics adjusted

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Last Trademarks Update 2009-10-19

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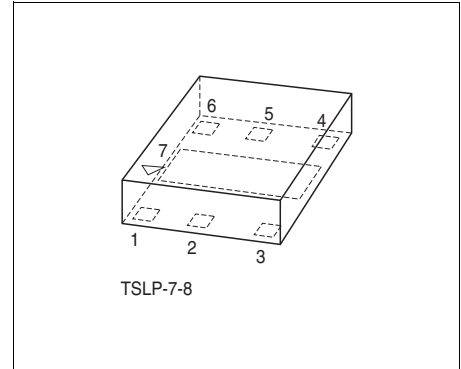
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**Features**

- Gain,  $|S_{21}|^2 = 12.5$  dB at 5.5 GHz
- High Linearity, Input  $P_{-1dB} = -3.5$  dBm at 5.5 GHz
- Low noise figure,  $NF = 1.3$  dB at 5.5 GHz
- Internal output matching on chip
- AC coupled RF output port
- Temperature compensated internal biasing circuit
- Digital On/Off switch on chip
- Low external part count
- 1 kV HBM ESD protection for IN-pin
- 2 kV HBM ESD protection for all other pins
- B7HFM silicon germanium technology
- Tiny TSLP-7-8 leadless package
- Pb-free (RoHS compliant) package



**Application**

- Low noise amplifier for WLAN application

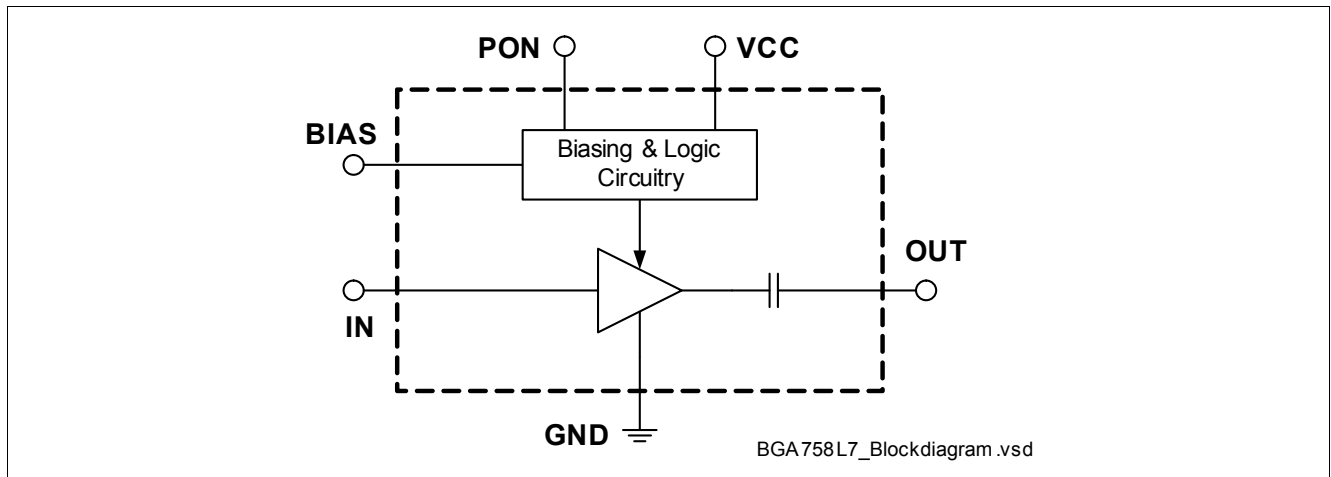


Figure 1 Block Diagram

Product Name	Marking	Package
BGA758L7	BA	TSLP-7-8

**Description**

The BGA758L7 is a 5 - 6 GHz Silicon Germanium low noise amplifier MMIC in tiny TSLP-7-8 package. The LNA delivers a gain of 12.5 dB while giving an excellent noise figure of 1.3 dB in the application configuration described in [Chapter 3](#). The supply current of 7.0 mA is chosen to maintain a high input compression point of -3.5 dBm.

The temperature compensated internal biasing circuit provides stable current conditions over temperature range. Output matching is done by on chip matching circuits in combination with the bonding wire inductances. The application circuit requires only three external elements.

With only one additional external element an ultra low noise figure of 1.1 dB can be achieved. For detailed information please refer to Infineon BGA758L7 Application Note.

**Pin Definition and Function**
**Table 1 Pin Definition and Function**

Pin No.	Name	Function
1	PON	Power on control
2	IN	RF input
3	BIAS	DC bias
4	n.c.	not connected
5	VCC	DC Supply
6	OUT	RF output
7	GND	RF ground and DC ground for bias and logic circuitry



# 1 Maximum Ratings

**Table 2 Maximum Ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Voltage at pin VCC	$V_{CC}$	-0.3	–	4	V	1)
Voltage at pin IN	$V_{IN}$	-0.3	–	0.9	V	–
Voltage at pin BIAS	$V_{BIAS}$	-0.3	–	0.9	V	–
Voltage at pin OUT	$V_{OUT}$	-0.3	–	$V_{CC} + 0.3$	V	–
Voltage at pin PON	$V_{PON}$	-0.3	–	$V_{CC} + 0.3$	V	–
Voltage at pin GND	$V_{GND}$	-0.3	–	0.3	V	–
Current into pin VCC	$I_{CC}$	–	–	12	mA	–
RF input power	$P_{IN}$	–	–	0	dBm	–
Total power dissipation, $T_S < 120^\circ\text{C}^2)$	$T_J$	–	–	48	mW	–
Junction temperature	$P_{tot}$	–	–	150	°C	–
Ambient temperature range	$T_A$	-30	–	85	°C	–
Storage temperature range	$T_{STG}$	-65	–	150	°C	–
ESD capability all pins	$V_{ESD-HBM}$	–	–	1000	V	according to JESD22A-114
ESD capability all pins, excluding pin IN	$V_{ESD-HBM}$	–	–	2000	V	according to JESD22A-114, w/o pin IN
ESD capability all pins	$V_{ESD-MM}$	–	–	100	V	according to JESD22A-115

1) All voltages refer to GND-Node unless otherwise noted

2)  $T_S$  is measured on the ground lead at the soldering point

**Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.**

## Thermal Resistance

**Table 3 Thermal Resistance**

Parameter	Symbol	Value	Unit
Junction - soldering point <sup>1)</sup>	$R_{thJS}$	615	K/W

1) For calculation of  $R_{thJA}$  please refer to Application Note Thermal Resistance

## 2 Electrical Characteristics

### 2.1 Electrical Parameter

**Table 4** Electrical Characteristics<sup>1)</sup>:  $T_A = 25\text{ °C}$ ,  $V_{CC} = 3.3\text{ V}$ ,  $V_{PON,ON} = 3.3\text{ V}$ ,  $V_{PON,OFF} = 0\text{ V}$ ,  $f = 5.5\text{ GHz}$ 

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Pass band frequency range	$F_{BW}$	5.0	–	6.0	GHz	
Gain	$ S_{21} ^2$	–	12.5	–	dB	
Gain flatness	$\Delta G$	–	0.3	–	dB	In any 50 MHz instantaneous bandwidth
Reverse isolation	$ S_{12} $	–	21	–	dB	
Noise figure <sup>2)</sup>	$NF$	–	1.3	–	dB	
Input return loss	$RL_{in}$	–	18	–	dB	50 $\Omega$
Output return loss	$RL_{out}$	–	20	–	dB	50 $\Omega$
Input power at 1dB compression point	$P_{-1dB}$	–	-3.5	–	dBm	
Maximum gain out of band	$ S_{21} $	–	-3	–	dB	DC - 1.7 GHz
		–	1	–	dB	1.7 - 2.0 GHz
		–	6	–	dB	2.3 - 2.7 GHz
		–	12	–	dB	3.3 - 3.9 GHz
		–	4	–	dB	9.0 - 10 GHz
		–	3	–	dB	10 - 18 GHz
Minimum input 1dB compression out of band	$P_{-1dB}$	–	-4	–	dBm	0.8 - 1.0 GHz
		–	-12	–	dBm	1.7 - 2.0 GHz
		–	-9	–	dBm	2.3 - 4.0 GHz
		–	-8	–	dBm	4.4 - 4.5 GHz
		–	0	–	dBm	9.0 - 10 GHz
Turn-on time	$t_{on}$	–	0.2	–	$\mu\text{s}$	Measured from ON signal turns on (90%) to the point where LNA output power stabilizes to within 0.5 dB of final value
Supply current at $V_{CC}$	$I_{CC}$	5.0	7.0	9.0	mA	
Shutdown current	$I_{off}$	–		6	$\mu\text{A}$	$V_{PON} = 0\text{ V}$
Stability factor	$k$	–	>1	–		Unconditional stable for all frequencies

1) Measured on application board according to application schematic on page 12, including PCB losses (unless noted otherwise)

2) PCB losses subtracted

## 2.2 Digital Signals

**Table 5 Digital Control Parameter**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Power on control voltage range	$V_{PON}$	-0.3	–	$V_{CC}$	V	–
Control voltage for power on	$V_{PON,on}$	2	–	$V_{CC}$	V	–
Control voltage for power off	$V_{PON,off}$	-0.3	–	1.1	V	–
Capacitance at power on pin	$C_{in}$	–	1	–	pF	–
Input current at power on pin	$I_{PON}$	–	10	–	$\mu$ A	$V_{PON} = 3.3$ V

### 3 Application Information

#### Application Board Configuration

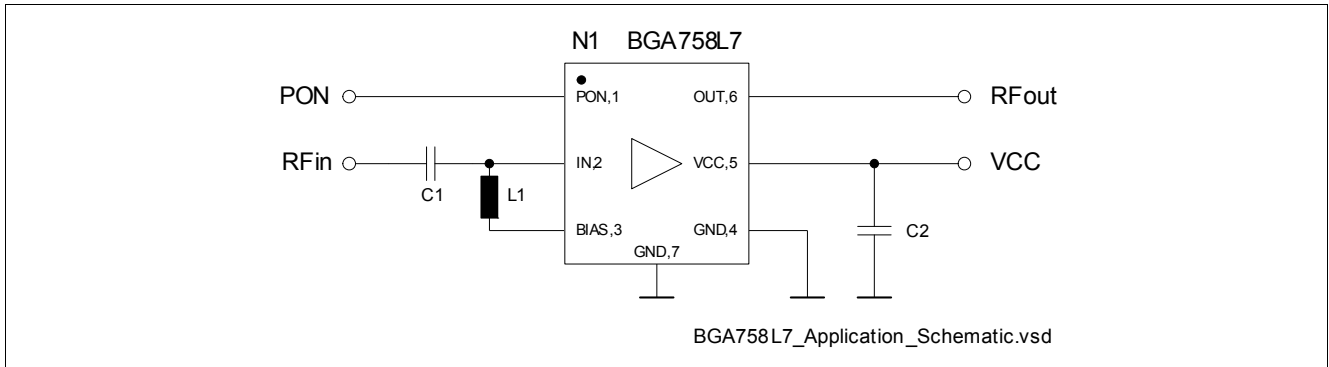


Figure 2 Application Schematic

Table 6 Bill of Materials

Name	Value	Package	Manufacturer	Function
C1	2.7 pF	0402	Various	DC blocking
C2	1 nF	0402	Various	Supply voltage filtering
L1	3.9 nH	0402	Murata LQW type	Bias feed and input matching
N1		TSLP-7-8	Infineon	5-6 GHz LNA

A list of all application notes is available at <http://goto.infineon.com/smallsignaldiscretes-appnotes>.

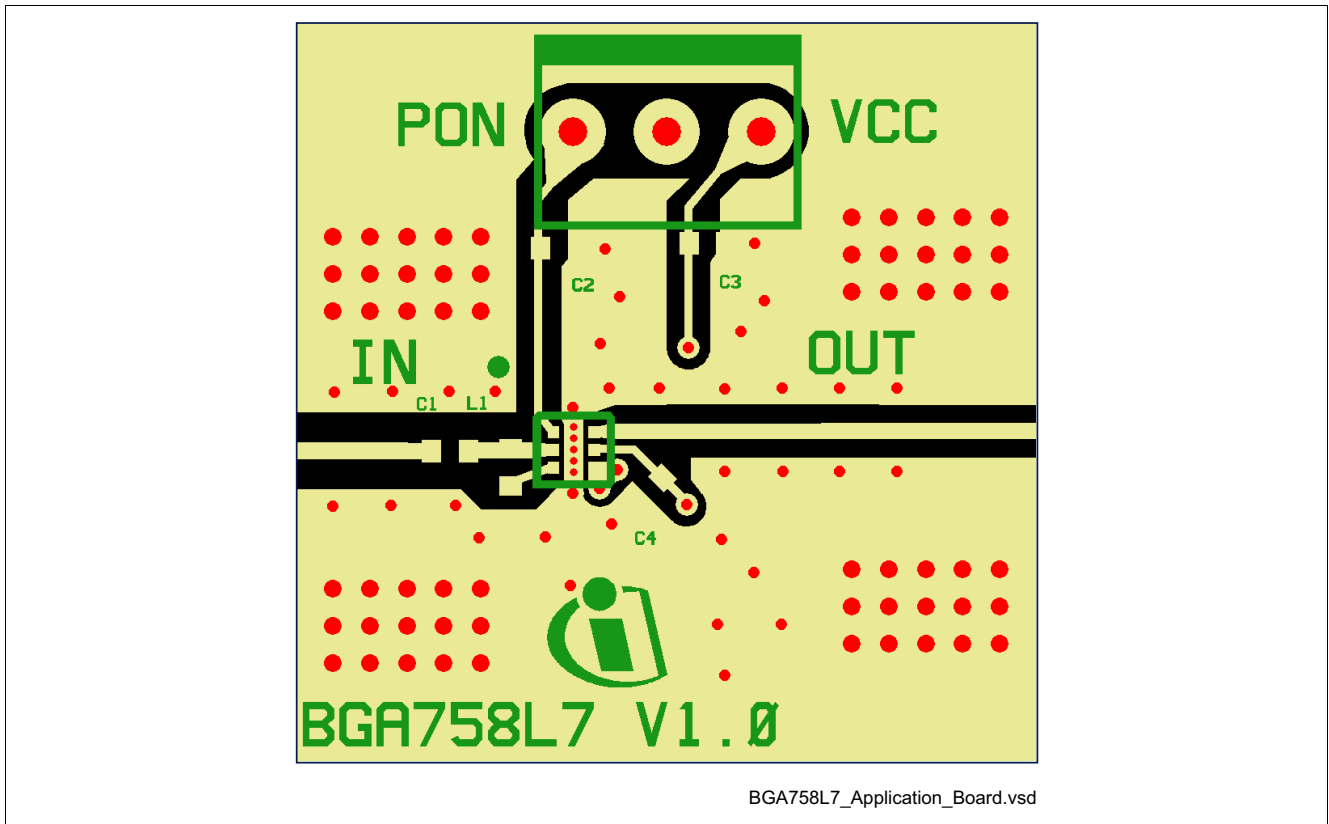


Figure 3 Drawing of Application Board

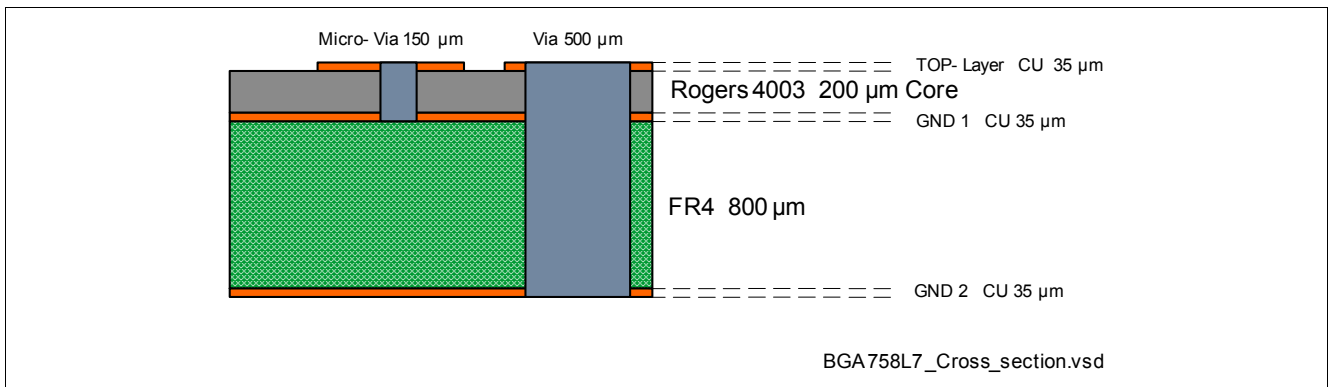
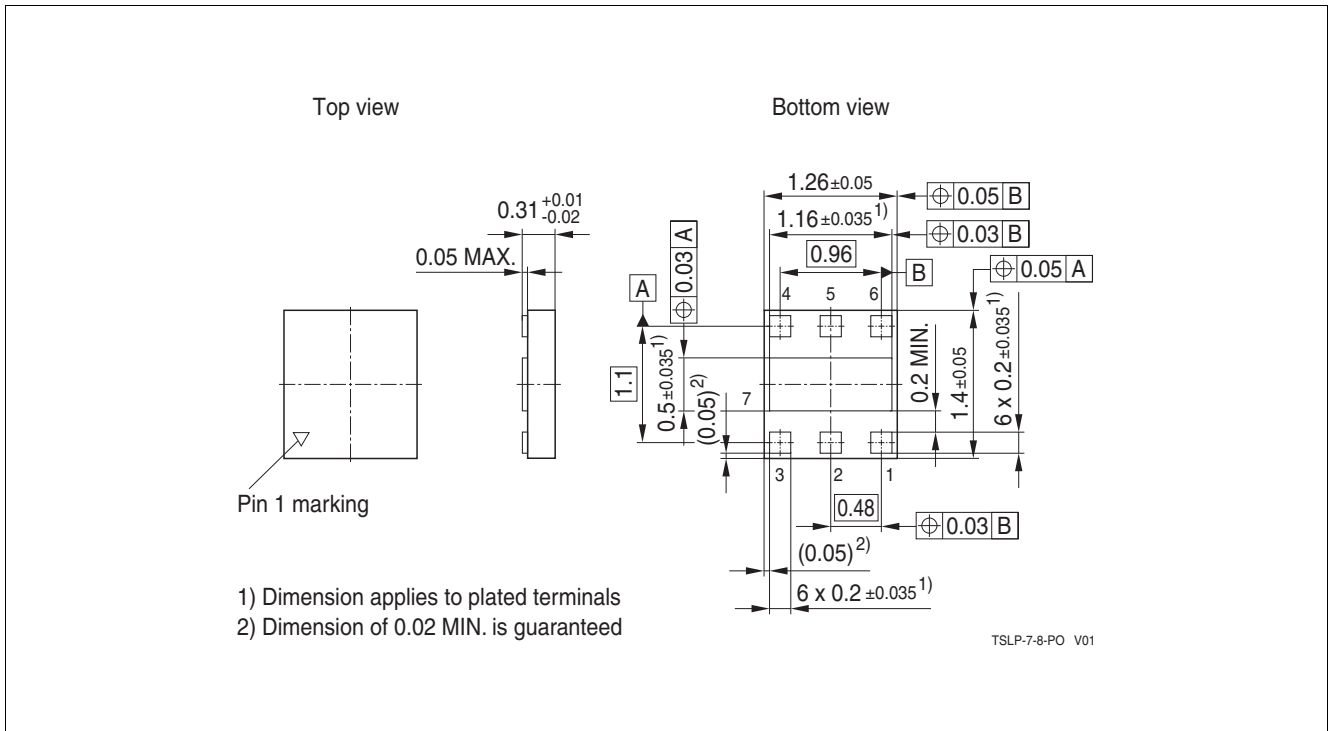
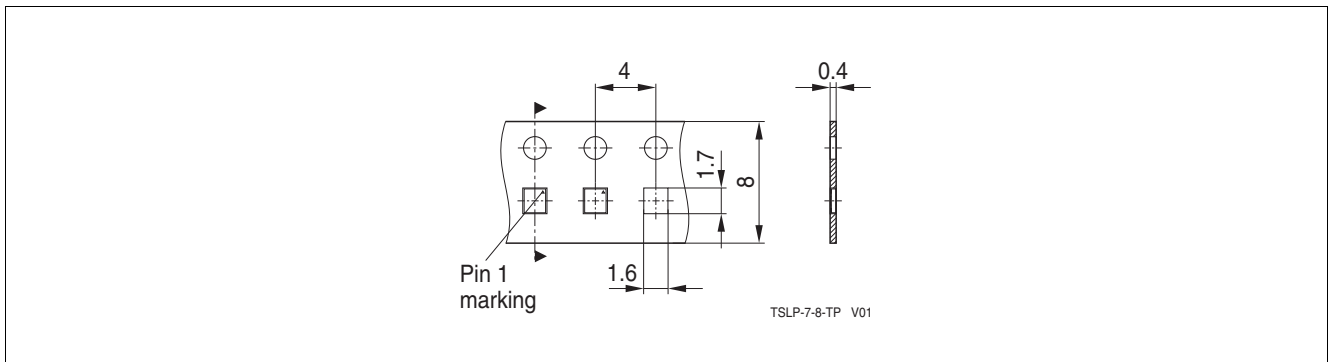


Figure 4 Cross-section of Application Board

## 4 Package Information



**Figure 5** Package Outline TSLP-7-8 (side and bottom view)



**Figure 6** Marking Layout (top view)

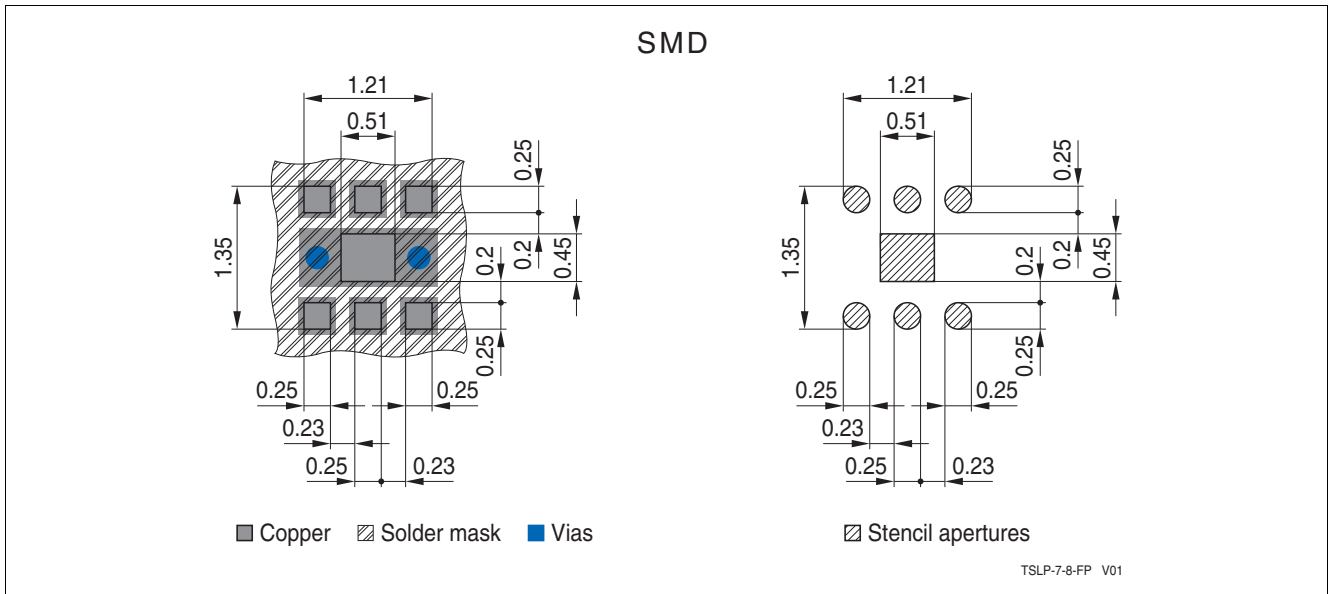


Figure 7 Footprint TSLP-7-8

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