National Semiconductor

January 14, 2011

DS92LX2121 / DS92LX2122

10 - 50 MHz DC-Balanced Channel Link III Bi-Directional Control Serializer and Deserializer

General Description

The DS92LX2121/DS92LX2122 chipset offers a Channel Link III interface with a high-speed forward channel and a full-duplex control channel for data transmission over a single differential pair. The DS92LX2121/DS92LX2122 incorporates differential signaling on both the high-speed and bi-directional back channel control data paths. The Serializer/Deserializer pair is targeted for direct connections between graphics host controller and displays modules. This chipset is ideally suited for driving video data to displays requiring 18-bit color depth (RGB666 + HS, VS, and DE) along with a bi-directional back channel control bus. The primary transport converts 21 bit data over a single high-speed serial stream, along with a separate low latency bi-directional back channel transport that accepts control information from an I2C port. Using National's embedded clock technology allows transparent full-duplex communication over a single differential pair, carrying asymmetrical bi-directional back channel control information in both directions. This single serial stream simplifies transferring a wide data bus over PCB traces and cable by eliminating the skew problems between parallel data and clock paths. This significantly saves system cost by narrowing data paths that in turn cable width, connector size and pins.

In addition, the Deserializer provides input equalization to compensate for loss from the media over longer distances. Internal DC balanced encoding/decoding is used to support AC-Coupled interconnects.

A sleep function provides a power-savings mode when the high speed forward channel and embedded bi-directional control channel are not needed.

The Serializer is offered in a 40-pin lead in LLP and Deserializer is offered in a 48-pin LLP packages.

Features

- Up to 1050 Mbits/sec data throughput
- 10 MHz to 50 MHz input clock support
- Supports 18-bit color depth (RGB666 + HS, VS, DE)
- Embedded clock with DC Balanced coding to support AC-coupled interconnects
- Capable to drive up to 10 meters shielded twisted-pair
- Bi-directional control interface channel with I²C support
- I²C interface for device configuration. Single-pin ID addressing
- Up to 4 GPI on DES and GPO on SER
- AT-SPEED BIST diagnosis feature to validate link integrity
- Individual power-down controls for both SER and DES
- User-selectable clock edge for parallel data on both SER and DES
- Integrated termination resistors
- 1.8V- or 3.3V-compatible parallel bus interface
- Single power supply at 1.8V
- IEC 61000–4–2 ESD compliant
- Temperature range –40°C to +85°C

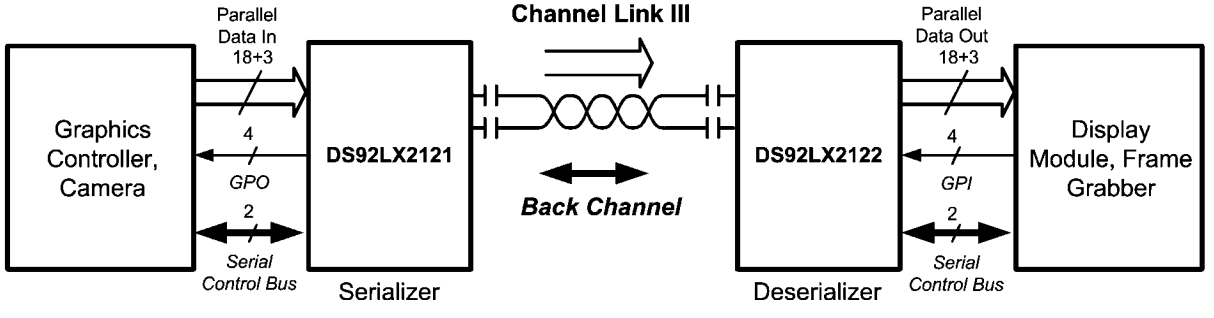
DESERIALIZER — DS92LX2122

- No reference clock required on Deserializer
- Programmable Receive Equalization
- LOCK output reporting pin to ensure
- EMI/EMC Mitigation
  Programmable Spread Spectrum (SSCG) outputs
  Receiver Output Drive Strength control (RDS)
  Receiver staggered outputs

Applications

- Industrial Displays, Touch Screens
- Medical Imaging

Typical Application Diagram



30125127

TRI-STATE® is a registered trademark of National Semiconductor Corporation.

Block Diagrams

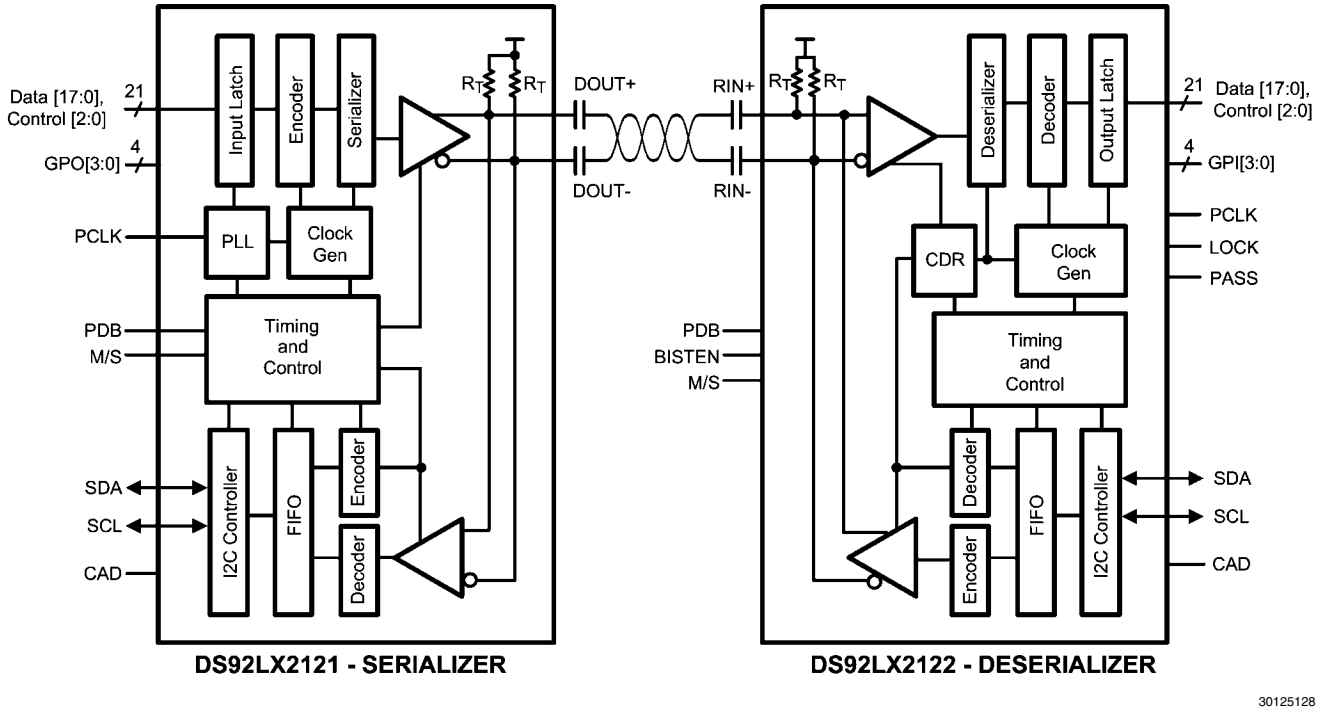


FIGURE 1. Block Diagram

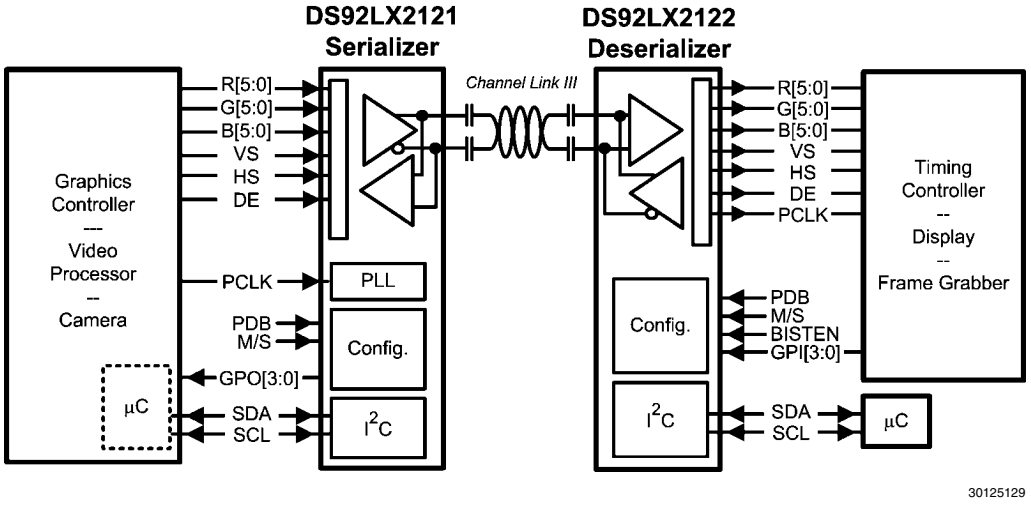
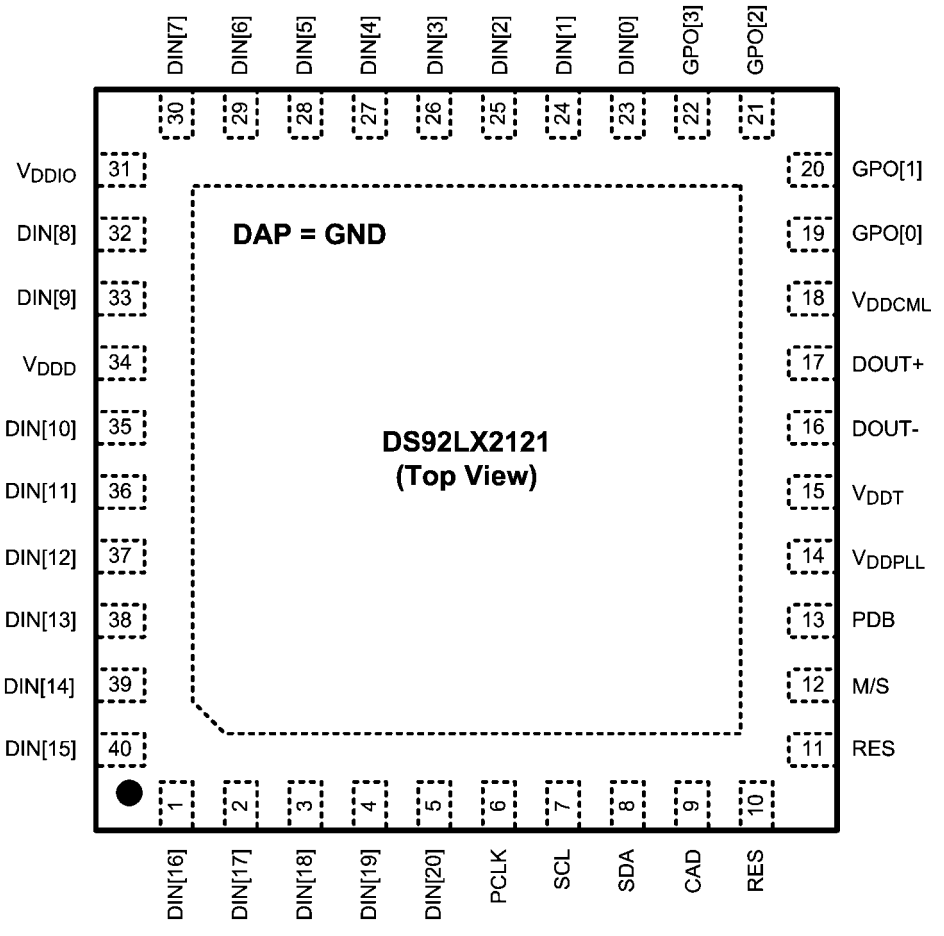


FIGURE 2. Application Block Diagram

Ordering Information

NSID	Package Description	Quantity	SPEC	Package ID
DS92LX2121SQE	40-pin LLP, 6.0 X 6.0 X 0.8 mm, 0.5 mm pitch	250	NOPB	SQA40A
DS92LX2121SQ	40-pin LLP, 6.0 X 6.0 X 0.8 mm, 0.5 mm pitch	1000	NOPB	SQA40A
DS92LX2121SQX	40-pin LLP, 6.0 X 6.0 X 0.8 mm, 0.5 mm pitch	4500	NOPB	SQA40A
DS92LX2122SQE	48-pin LLP, 7.0 X 7.0 X 0.8 mm, 0.5 mm pitch	250	NOPB	SQA48A
DS92LX2122SQ	48-pin LLP, 7.0 X 7.0 X 0.8 mm, 0.5 mm pitch	1000	NOPB	SQA48A
DS92LX2122SQX	48-pin LLP, 7.0 X 7.0 X 0.8 mm, 0.5 mm pitch	4500	NOPB	SQA48A

DS92LX2121 Pin Diagram

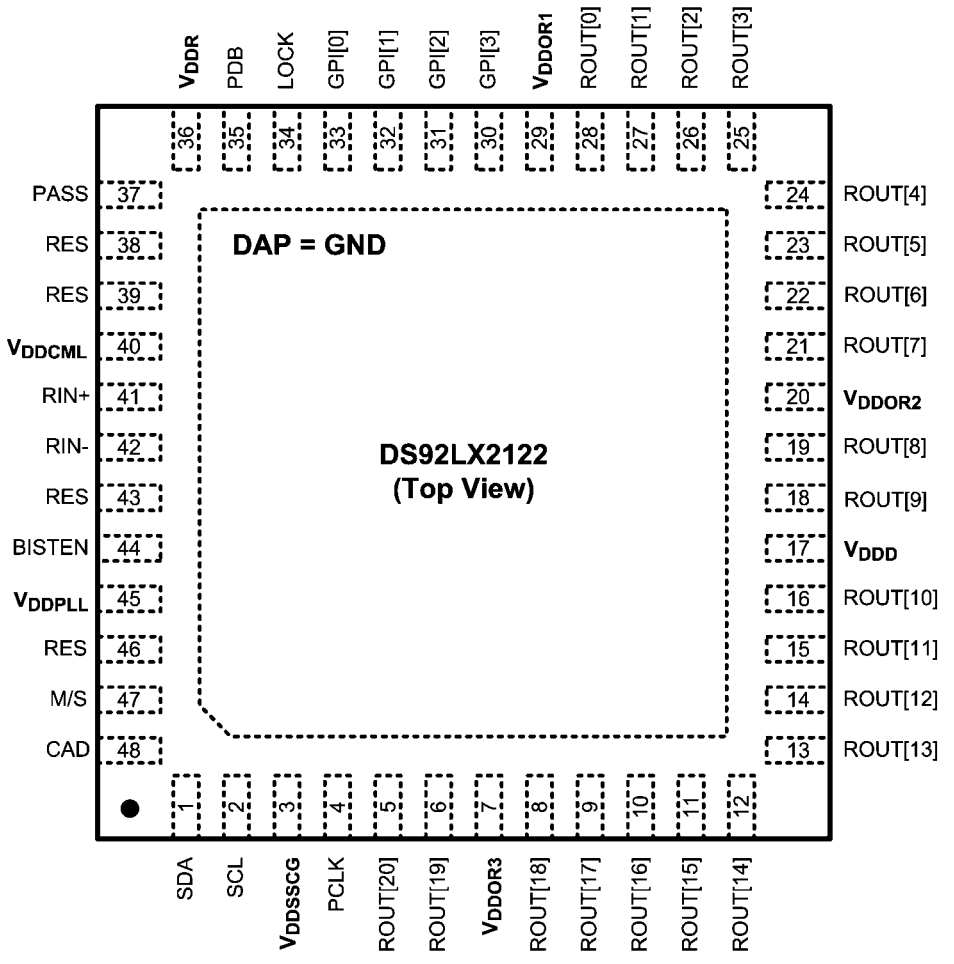


Serializer - DS92LX2121 — Top View

DS92LX2121 Serializer Pin Descriptions

Pin Name	Pin No.	I/O, Type	Description
LVCMOS PARALLEL INTERFACE			
DIN[20:0]	5, 4, 3, 2, 1, 40, 39, 38, 37, 36, 35, 33, 32, 30, 29, 28, 27, 26, 25, 24, 23	Inputs, LVCMOS w/ pull down	Parallel data inputs.
PCLK	6	Input, LVCMOS w/ pull down	Pixel Clock Input Pin. Strobe edge set by TRFB configuration.
GENERAL PURPOSE OUTPUT (GPO)			
GPO[3:0]	22, 21, 20, 19	Output, LVCMOS	General-purpose pins individually configured as outputs; which are used to control and respond to various commands.
SERIAL CONTROL BUS - I²C COMPATIBLE			
SCL	7	Input/Output, Open Drain	Clock line for the serial control bus communication SCL requires an external pull-up resistor to V_{DDIO}.
SDA	8	Input/Output, Open Drain	Data line for the serial control bus communication SDA requires an external pull-up resistor to V_{DDIO}.
M/S	12	Input, LVCMOS w/ pull down	I²C Mode Select M/S = L, Master mode (default); device generates and drives the SCL clock line. Device is connected to a slave peripheral on the bus. (Serializer initially starts up in Standby mode and is enabled through remote wakeup by the Deserializer) M/S = H, Slave; device accepts SCL clock input
CAD	9	Input, analog	Continuous Address Decoder Input pin to select the Slave Device Address. Input is connect to external resistor divider to programmable Device ID address (see Serial Control Bus Connection).
CONTROL AND CONFIGURATION			
PDB	13	Input, LVCMOS w/ pull down	Power down Mode Input Pin. PDB = H, Transmitter is enabled and is ON. PDB = L, Transmitter is in Sleep (Power Down). When the transmitter is in the SLEEP state, the PLL is shutdown, and IDD is minimized.
RES	10, 11	Input, LVCMOS w/ pull down	Reserved. This pin MUST be tied LOW.
Channel Link III INTERFACE			
DOUT+	17	Input/Output, CML	Non-inverting differential output, back-channel input.
DOUT-	16	Input/Output, CML	Inverting differential output, back-channel input.
Power and Ground			
VDDPLL	14	Power, Analog	PLL Power, 1.8V ±5%
VDDT	15	Power, Analog	Tx Analog Power, 1.8V ±5%
VDDCML	18	Power, Analog	LVDS & BC Dr Power, 1.8V ±5%
VDDD	34	Power, Digital	Digital Power, 1.8V ±5%
VDDIO	31	Power, Digital	Power for input stage, The single-ended inputs are powered from V_{DDIO}.
VSS	DAP	Ground, DAP	DAP must be grounded. Connect to the ground plane (GND) with at least 16 vias.

DS92LX2122 Pin Diagram



30125120

Deserializer - DS92LX2122 — Top View

DS92LX2122 Deserializer Pin Descriptions

Pin Name	Pin No.	I/O, Type	Description
LVCMOS PARALLEL INTERFACE			
ROUT[20:0]	5, 6, 8, 9, 10, 11, 12, 13, 14, 15, 16, 18, 19, 21, 22, 23, 24, 25, 26, 27, 28	Outputs, LVCMOS	Parallel data outputs.
PCLK	4	Output, LVCMOS	Pixel Clock Output Pin. Strobe edge set by RFB configuration. In SLEEP, outputs are controlled by the OSS_SEL.
General Purpose Input (GPI)			
GPI[3:0]	30, 31, 32, 33	Input/Output, Digital	General-purpose pins individually configured as inputs; which are used to control and respond to various commands.
SERIAL CONTROL BUS - I²C COMPATIBLE			
SCL	2	Input/Output, Open Drain	Clock line for the serial control bus communication SCL requires an external pull-up resistor to V_{DDIO}.
SDA	1	Input/Output, Open Drain	Data line for serial control bus communication SDA requires an external pull-up resistor to V_{DDIO}.
M/S	47	Input, LVCMOS w/ pull up	I²C Mode Select M/S = L, Master; device generates and drives the SCL clock line. Device is connected to slave peripheral on teh bus. M/S = H, Slave (default); device accepts SCL clock input and is attached to an I²C controller master on the bus. Slave mode does not generate the SCL clock, but uses the clock generated by teh Master for teh data transfer.
CAD	48	Input, analog	Continuous Address Decoder Input pin to select the Slave Device Address. Input is connect to external resistor divider to programmable Device ID address (see Serial Control Bus Connection)
CONTROL AND CONFIGURATION			
PDB	35	Input, LVCMOS w/ pull down	Power down Mode Input Pin. PDB = H, Receiver is enabled and is ON. PDB = L, Receiver is in Sleep (Power down mode). When the Receiver is in the SLEEP state, the LVCMOS Outputs are in TRI-STATE, the PLL is shutdown and IDD is minimized.
LOCK	34	Output, LVCMOS	LOCK Status Output Pin. LOCK = H, PLL is Locked, outputs are active LOCK = L, PLL is unlocked, ROUT and PCLK output states are controlled by OSS_SEL. May be used as Link Status.
RES	38, 39, 43, 46	-	Reserved. Pin 43: Leave pin open. Pin 46: This pin MUST be tied LOW. Pins 38, 39: Route to test point as differential pair or leave open if unused.
BIST MODE			
BISTEN	44	Input, LVCMOS w/ pull down	BIST Enable Pin. BISTEN = H, BIST Mode is enabled. BISTEN = L, BIST Mode is disabled.
PASS	37	Output, LVCOMS	PASS Output Pin for BIST mode. PASS = H, ERROR FREE Transmission PASS = L, one or more errors were detected in the received payload. Leave Open if unused. Route to test point (pad) recommended.
Channel Link III INTERFACE			

Pin Name	Pin No.	I/O, Type	Description
RIN+	41	Input/Output, CML	Non-inverting differential input, back channel output. The interconnect must be AC coupled with a 0.1µF capacitor.
RIN-	42	Input/Output, CML	Inverting differential input, back channel output. The interconnect must be AC coupled with a 0.1 µF capacitor.
POWER AND GROUND			
VDDSSCG	3	Digital Power	SSCG Power, 1.8V ±5% Power supply must be connect regardless if SSCG function is in operation
VDDOR1/2/3	29, 20, 7	Digital Power	TTL Output Buffer Power, The single-ended outputs and control input are powered from V_{DDIO}. V_{DDIO} can be connected to a 1.8V ±5% or 3.3V ±10%
VDDD	17	Digital Power	Digital Core Power, 1.8V ±5%
VDDR	36	Analog Power	Rx Analog Power, 1.8V ±5%
VDDCML	40	Analog Power	Bi-directional Channel Driver Power, 1.8V ±5%
VDDPLL	45	Analog Power	PLL Power, 1.8V ±5%
VSS	DAP	Ground, DAP	DAP must be grounded. Connect to the ground plane (GND) with at least 16 vias.

Absolute Maximum Ratings (*Note 1*)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{DD1V8})	−0.3V to +2.5V
Supply Voltage (V_{DD3V3})	−0.3V to +4.0V
LVCMOS Input Voltage (V_{DD1V8})	−0.3V to +(V_{DD1V8} + 0.3V)
LVCMOS Input Voltage (V_{DD3V3})	−0.3V to +(V_{DD3V3} + 0.3V)
LVCMOS Output Voltage (V_{DD})	−0.3V to +(V_{DD} + 0.3V)
CML Receiver Input Voltage (V_{DD1V8})	−0.3V to (V_{DD1V8} + 0.3V)
CML Driver Output Voltage (V_{DD1V8})	−0.3V to (V_{DD1V8} + 0.3V)
Junction Temperature	+150°C
Storage Temperature	−65°C to +150°C
Maximum Package Power Dissipation Capacity	1/θ_{JA} °C/W above +25°
Package Derating: DS92LX2121 40L LLP	
θ_{JA} *(based on 16 thermal vias)*	30.7 °C/W
θ_{JC} *(based on 16 thermal vias)*	6.8 °C/W
DS92LX2122 48L LLP	
θ_{JA} *(based on 16 thermal vias)*	26.9 °C/W
θ_{JC} *(based on 16 thermal vias)*	4.4 °C/W
ESD Rating (IEC61000–4–2)	R_D = 330Ω, C_S = 150 pF
Air Discharge (DOUT+, DOUT-, RIN+, RIN-)	≥±25 kV
Contact Discharge (DOUT+, DOUT-, RIN+, RIN-)	≥±10 kV
ESD Rating (HBM)	≥±8 kV

For soldering specifications:
see product folder at www.national.com and www.national.com/ms/MS/MS-SOLDERING.pdf

Recommended Operating Conditions

	Min	Nom	Max	Units
V_{DD} (1.8V)	1.71	1.8	1.89	V
V_{DDIO} (1.8V Mode)	1.71	1.8	1.89	V
V_{DDIO} (3.3V Mode)	3	3.3	3.6	V
Supply Noise				
V_{DDn} (1.8 V)			25	mV_{P-P}
V_{DDIO} (1.8 V)			25	mV_{P-P}
V_{DDIO} (3.3 V)			50	mV_{P-P}
Operating Free Air Temperature (T_A)	-40	25	85	°C
Input Clock Rate	10		50	MHz

Serializer Electrical Characteristics (*Note 2*, *Note 3*, *Note 4*)

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
LVCMOS DC SPECIFICATIONS 3.3V I/O (TX INPUTS, RX OUTPUTS, GPIO, CONTROL INPUTS AND OUTPUTS)							
V_{IH}	High Level Input Voltage	VIN = 3.0V to 3.6V		2.0		V_{IN}	V
V_{IL}	Low Level Input Voltage	VIN = 3.0V to 3.6V		GND		0.8	V
I_{IN}	Input Current	VIN = 0V or 3.6V VIN = 3.0V to 3.6V		-20	±1	+20	µA
V_{OH}	High Level Output Voltage	V_{DDIO} = 3.0V to 3.6V		2.4		V_{DDIO}	V
V_{OL}	Low Level Output Voltage	V_{DDIO} = 3.0V to 3.6V I_{OH} = +4mA		GND		0.4	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V	Serializer GPO Outputs		-24		mA
			Deserializer LVCMOS Outputs		-39		
I_{OZ}	TRI-STATE® Output Current	RPWDNB = 0V, V_{OUT} = 0V or V_{DD}	Register Address (OSS_SEL = 0)	-20		+20	µA
LVCMOS DC SPECIFICATIONS 1.8V I/O (TX INPUTS, RX OUTPUTS, GPIO, CONTROL INPUTS AND OUTPUTS)							
V_{IH}	High Level Input Voltage	V_{IN} = 1.71V to 1.89V		0.65 V_{IN}		V_{IN} + 0.3	V
V_{IL}	Low Level Input Voltage	V_{IN} = 1.71V to 1.89V		GND		0.35 V_{IN}	
I_{IN}	Input Current	V_{IN} = 0V or 1.89V V_{IN} = 1.71V to 1.89V		-20	±1	+20	µA
V_{OH}	High Level Output Voltage	V_{DDIO} = 1.71V to 1.89V I_{OH} = −4mA		V_{DDIO} - 0.45		V_{DDIO}	V
V_{OL}	Low Level Output Voltage	V_{DDIO} = 1.71V to 1.89V I_{OL} = +4 mA		GND		0.45	V

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V (*Note 11*)	Serializer GPO Outputs		-11		mA
			Deserializer LVCMOS Outputs		-20		
I_{OZ}	TRI-STATE® Output Current	RPWDNB = 0V, V_{OUT} = 0V or V_{DD}	Register Address (OSS_SEL = 0)	-20	±1	+20	µA
CML DRIVER DC SPECIFICATIONS (DOUT+, DOUT-)							
$\|V_{OD}\|$	Output Differential Voltage	R_T = 100Ω (*Figure 6*)		268	340	412	mV
ΔV_{OD}	Output Differential Voltage Unbalance	R_L = 100Ω			1	50	mV
V_{OS}	Output Differential Offset Voltage	R_L = 100Ω (*Figure 6*)		$V_{DD\ (MIN)}$ - $V_{OD\ (MAX)}$	V_{DD} - V_{OD}	$V_{DD\ (MAX)}$ - $V_{OD\ (MIN)}$	V
ΔV_{OS}	Offset Voltage Unbalance	RL = 100Ω			1	50	mV
I_{OS}	Output Short Circuit Current	DOUT+/- = 0V, PDB = L or H (*Note 11*)			-27		mA
R_T	Differential Internal Termination Resistance	Differential across DOUT+ and DOUT-		80	100	120	Ω
CML RECEIVER DC SPECIFICATIONS (RIN+, RIN-)							
V_{TH}	Differential Threshold High Voltage	V_{CM} = 1.2V				+90	mV
V_{TL}	Differential Threshold Low Voltage			-90			
V_{IN}	Differential Input Voltage Range	RIN+ - RIN-		180			mV
I_{IN}	Input Current	V_{IN} = V_{DD} or 0 V, V_{DD} = 1.89 V		-20	±1	+20	µA
R_T	Differential Internal Termination Resistance	Differential across RIN+ and RIN-		80	100	120	Ω
SER/DES SUPPLY CURRENT *DIGITAL, PLL, AND ANALOG VDDS							
I_{DDT}	Serializer (Tx) Total Supply Current Mode (includes load current)	RT = 100Ω WORST CASE pattern (*Figure 4*)	V_{DDn} = 1.89 V f = 50 MHz Default Registers		62	90	mA
		RT = 100Ω RANDOM pattern			55		
I_{DDIOT}	Serializer (Tx) VDDIO Supply Current (includes load current)	RT = 100Ω WORST CASE pattern (*Figure 4*)	V_{DDIO} = 1.89 V PCLK = 50 MHz Default Registers		2	5	mA
			V_{DDIO} = 3.6 V PCLK = 50 MHz Default Registers		7	15	
I_{DDTZ}	Serializer (Tx) Supply Current Power-down	PDB = 0V; All other LVCMOS Inputs = 0V	V_{DD} = 1.89 V		370	775	µA
I_{DDIOTZ}			V_{DDIO} = 1.89 V		55	125	
			V_{DDIO} = 3.6 V		65	135	

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{DDR}	Deserializer (Rx) VDDn Supply Current (includes load current)	V_{DDn} = 1.89V CL = 8pF WORST CASE Pattern (*Figure 4*)	PCLK = 50 MHz SSCG[3:0] = ON Default Registers		60	96	mA
		V_{DDn} = 1.89V CL = 8pF RANDOM Pattern	PCLK = 50 MHz Default Registers		53		
I_{DDIOR}	Deserializer (Rx) VDDIO Supply Current (includes load current)	V_{DDIO} = 1.89 V CL = 8pF WORST CASE Pattern (*Figure 4*)	PCLK = 50 MHz Default Registers		21	32	mA
		V_{DDIO} = 3.6 V CL = 8pF WORST CASE Pattern (*Figure 4*)	PCLK = 50 MHz Default Registers		49	83	
I_{DDRZ}	Deserializer (Rx) Supply Current Power-down	PDB = 0V; All other LVCMOS Inputs = 0V	V_{DDn} = 1.89 V		42	400	µA
			V_{DDIO} = 1.89 V		8	40	
I_{DDIORZ}			V_{DDIO} = 3.6 V		350	800	

Recommended Serializer Timing for PCLK

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{TCP}	Transmit Clock Period	10 MHz – 50 MHz (*Note 11*)	20	T	100	ns
t_{TCIH}	Transmit Clock Input High Time		0.4T	0.5T	0.6T	ns
t_{TCIL}	Transmit Clock Input Low Time		0.4T	0.5T	0.6T	ns
t_{CLKT}	PCLK Input Transition Time		0.5		3	ns
t_{OSC}	Internal oscillator clock source			25		MHz

Serializer Switching Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{LHT}	CML Low-to-High Transition Time	R_L = 100Ω (*Figure 5*)		150	330	ps
t_{HLT}	CML High-to-Low Transition Time	R_L = 100Ω (*Figure 5*)		150	330	ps
t_{DIS}	Data Input Setup to PCLK	Serializer Data Inputs (*Figure 9*)	2.0			ns
t_{DIH}	Data Input Hold from PCLK		2.0			ns
t_{PLD}	Serializer PLL Lock Time	R_L = 100Ω		1	2	ms
t_{SD}	Serializer Delay	RT = 100Ω f = 10-50 MHz Reg Address 0x03h b[0] (TRFB = 1) (*Figure 11*)	6.386T + 5	6.386T + 12	6.386T + 19.7	ns
t_{JIND}	Serializer Output Deterministic Jitter	Serializer output intrinsic deterministic jitter . Measured (cycle-cycle) with PRBS-7 test pattern PCLK = 50 MHz		0.13		UI
t_{JINR}	Serializer Output Random Jitter	Serializer output intrinsic random jitter (cycle-cycle). Alternating-1,0 pattern. PCLK = 50 MHz		0.04		UI

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{JINT}	Peak-to-peak Serializer Output Jitter	Serializer output peak-to-peak jitter includes deterministic jitter, random jitter, and jitter transfer from serializer input. Measured (cycle-cycle) with PRBS-7 test pattern. PCLK = 50MHz		0.396		UI
λ_{STXBW}	Serializer Jitter Transfer Function -3 dB Bandwidth	PCLK = 50 MHz Default Registers		1.90		MHz
δ_{STX}	Serializer Jitter Transfer Function (Peaking	PCLK = 50 MHz Default Registers		0.944		dB
δ_{STXf}	Serializer Jitter Transfer Function (Peaking Frequency)	PCLK = 50 MHz Default Registers		500		kHz

Deserializer Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
t_{RCP}	Receiver Output Clock Period	$t_{RCP} = t_{TCP}$	PCLK	20	T	100	ns
t_{PDC}	PCLK Duty Cycle		PCLK	45	50	55	%
t_{CLH}	LVCMOS Low-to-High Transition Time	V_{DDIO}: 1.71 V to 1.89 V or 3.0 V to 3.6 V, CL = 8pF (lumped load) Default Registers ( ) (*Note 10*)	Deserializer PCLK Output	1.3	2.0	2.8	ns
t_{CHL}	LVCMOS High-to-Low Transition Time			1.3	2.0	2.8	
t_{CLH}	LVCMOS Low-to-High Transition Time	V_{DDIO}: 1.71 V to 1.89 V or 3.0 V to 3.6 V, CL = 8pF (lumped load) Default Registers (*Figure 13*) (*Note 10*)	Deserializer Data Outputs	1.6	2.4	3.3	ns
t_{CHL}	LVCMOS High-to-Low Transition Time			1.6	2.4	3.3	
t_{ROS}	ROUT Setup Data to PCLK	V_{DDIO}: 1.71 V to 1.89 V or 3.0 V to 3.6 V, CL = 8pF (lumped load) Default Registers	Deserializer Data Outputs	0.38	0.5		T
t_{ROH}	ROUT Hold Data to PCLK			0.38T	0.5T		
t_{DD}	Deserializer Delay	Default Registers Register 0x03h b[0] (RRFB = 1) *Figure 14*	10 MHz - 50 MHz	4.571T + 8	4.571T + 12	4.571T + 16	ns
t_{DDLT}	Deserializer Data Lock Time	(*Note 5*)	10 MHz - 50 MHz			10	ms
t_{RJIT}	Receiver Input Jitter Tolerance	(*Note 13*, *Note 14*)	50 MHz		0.53		UI
t_{DCJ}	Deserializer Clock Jitter	PCLK SSCG[3:0] = OFF (*Note 6*, *Note 11*)	10 MHz		300	550	ps
			50 MHz		120	250	
t_{DPJ}	Deserializer Period Jitter	PCLK SSCG[3:0] = OFF (*Note 7*, *Note 11*)	10 MHz		425	600	ps
			50 MHz		320	480	
t_{DCCJ}	Deserializer Cycle-to-Cycle Clock Jitter	PCLK SSCG[3:0] = OFF (*Note 8*, *Note 11*)	10 MHz		320	500	ps
			50 MHz		300	500	
f_{DEV}	Spread Spectrum Clocking Deviation Frequency	LVCMOS Output Bus SSC[3:0] = ON *Figure 16*	20 MHz - 50 MHz		±0.5% to ±2.0%		%
f_{MOD}	Spread Spectrum Clocking Modulation Frequency		20 MHz - 50 MHz		9 kHz to 66 kHz		kHz

Bi-Directional Control Bus AC Timing Specifications (SCL, SDA) - I²C Compliant (*Figure 3*)

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RECOMMENDED INPUT TIMING REQUIREMENTS ()						
f_{SCL}	SCL Clock Frequency	f_{SCL} = 100 kHz	>0		100	kHz
f_{LOW}	SCL Low Period		4.7			µs
f_{HIGH}	SCL High Period		4.0			µs
$t_{HD:STA}$	Hold time for a start or a repeated start condition		4.0			µs
$t_{SU:STA}$	Set Up time for a start or a repeated start condition		4.7			µs
$t_{HD:DAT}$	Data Hold Time		0		3.45	µs
$t_{SU:DAT}$	Data Set Up Time		250			ns
$t_{SU:STO}$	Set Up Time for STOP Condition,		4.0			µs
t_r	SCL & SDA Rise Time				1000	ns
t_f	SCL & SDA Fall Time				300	ns
C_b	Capacitive load for bus				400	pF
SWITCHING CHARACTERISTICS ()						
f_{SCL}	SCL Clock Frequency	Serializer MODE = 0 – R/W Register 0x05 = 0x40'h		100		kHz
		Deserializer MODE = 0 – READ Register 0x06 b[6:4] = 0x00'h		100		
t_{LOW}	SCL Low Period	Serializer MODE = 0 – R/W Register 0x05 = 0x40'h	4.7			µs
		Deserializer MODE = 0 – READ Register 0x06 b[6:4] = 0x00'h				
t_{HIGH}	SCL High Period	Serializer MODE = 0 – R/W Register 0x05 = 0x40'h	4.0			µs
		Deserializer MODE = 0 – READ Register 0x06 b[6:4] = 0x00'h				
$t_{HD:STA}$	Hold time for a start or a repeated start condition	Serializer MODE = 0 Register 0x05 = 0x40'h	4.0			µs
tSU:STA	Set Up time for a start or a repeated start condition	Serializer MODE = 0 Register 0x05 = 0x40'h	4.7			µs
$t_{HD:DAT}$	Data Hold Time		0		3.45	µs
$t_{SU:DAT}$	Data Set Up Time		250			µs
$t_{SU:STO}$	Set Up Time for STOP Condition	Serializer M/S = 0	4.0			µs
t_f	SCL & SDA Fall Time				300	µs
t_{BUF}	Bus free time between a stop and start condition	Serializer M/S = 0	4.7			µs
$t_{TIMEOUT}$	NACK Time out	Serializer		1		ms
		Deserializer		25		

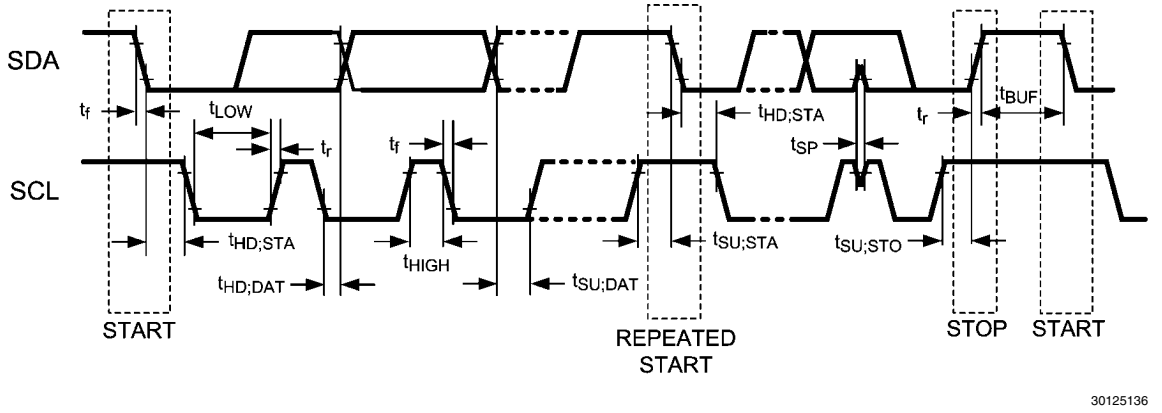


FIGURE 3. Serial Control Bus Timing

Bi-Directional Control Bus DC Characteristics (SCL, SDA) - I²C Compliant

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Input High Level	SDA and SCL	0.7 x V_{DDIO}		V_{DDIO}	V
V_{IL}	Input Low Level Voltage	SDA and SCL	GND		0.3 x V_{DDIO}	V
V_{HY}	Input Hysteresis			>50		mV
I_{OZ}	TRI-STATE® Output Current	PDB = 0V VOUT = 0V or VDD	-20	±1	+20	µA
I_{IN}	Input Current	SDA or SCL, Vin = V_{DDIO} or GND	-20	±1	+20	µA
C_{IN}	Input Pin Capacitance			<5		pF
V_{OL}	Low Level Output Voltage	SCL and SDA VDDIO = 3.0V IOL = 1.5 mA			0.36	V
		SCL and SDA VDDIO = 1.71V IOL = 1 mA			0.36	V

Note 1: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional; the device should not be operated beyond such conditions.

Note 2: The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.

Note 3: Current into device pins is defined as positive. Current out of a device pin is defined as negative. Voltages are referenced to ground except VOD, ΔVOD, VTH and VTL which are differential voltages.

Note 4: Typical values represent most likely parametric norms at 1.8V or 3.3V, T_A = +25°C, and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

Note 5: t_{PLD} and t_{DDLT} is the time required by the serializer and deserializer to obtain lock when exiting power-down state with an active PCLK.

Note 6: t_{DCJ} is the maximum amount of jitter measured over 30,000 samples based on Time Interval Error (TIE).

Note 7: t_{DPJ} is the maximum amount the period is allowed to deviate measured over 30,000 samples.

Note 8: t_{DCCJ} is the maximum amount of jitter between adjacent clock cycles measured over 30,000 samples.

Note 9: Supply noise testing was done with minimum capacitors (as shown on Figures 35, 36) on the PCB. A sinusoidal signal is AC coupled to the V_{DDn} (1.8V) supply with amplitude = 25 mVp-p measured at the device V_{DDn} pins. Bit error rate testing of input to the Ser and output of the Des with 10 meter cable shows no error when the noise frequency on the Ser is less than 1 MHz. The Des on the other hand shows no error when the noise frequency is less than 750 kHz.

Note 10: Specification is guaranteed by design and is not tested in production.

Note 11: Specification is guaranteed by characterization and is not tested in production.

Note 12: Recommended Input Timing Requirements are input specifications and not tested in production.

Note 13: UI – Unit Interval is equivalent to one ideal serialized data bit width. The UI scales with PCLK frequency.

Note 14: t_{RJIT} max (0.61UI) is limited by instrumentation and actual t_{RJIT} of in-band jitter at low frequency (<2 MHz) is greater 1 UI.

AC Timing Diagrams and Test Circuits

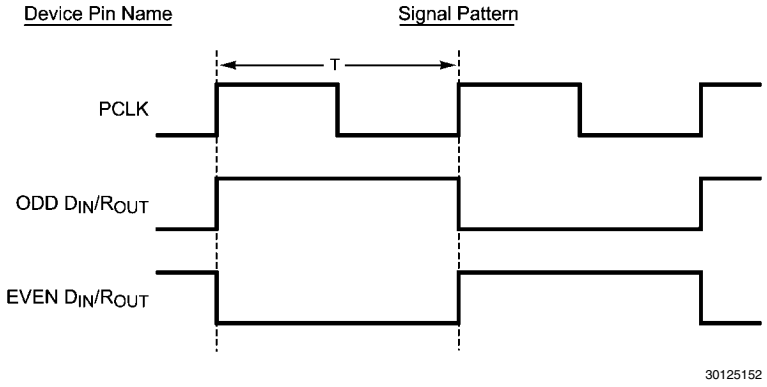
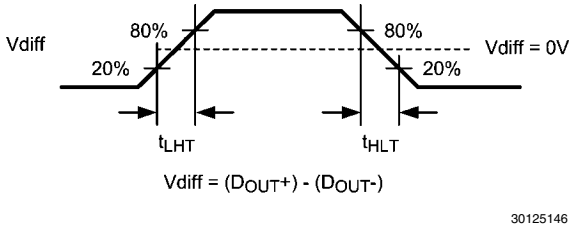


FIGURE 4. "Worst Case" Test Pattern



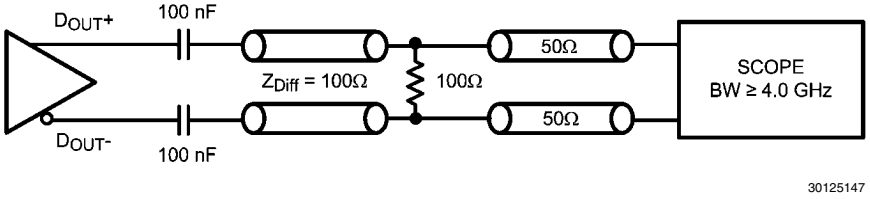
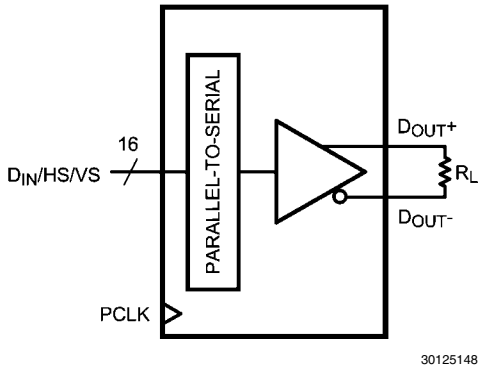


FIGURE 5. Serializer CML Output Load and Transition Times



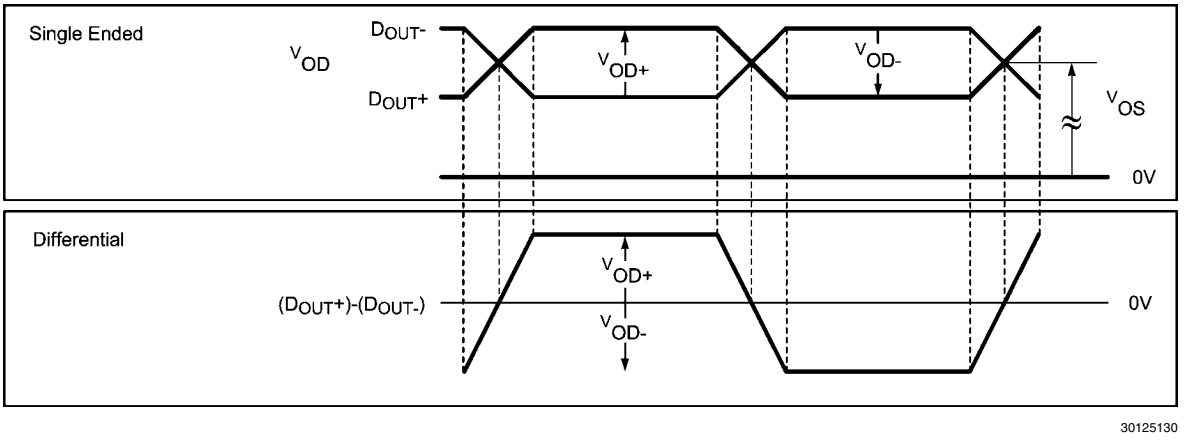


FIGURE 6. Serializer VOD DC Diagram

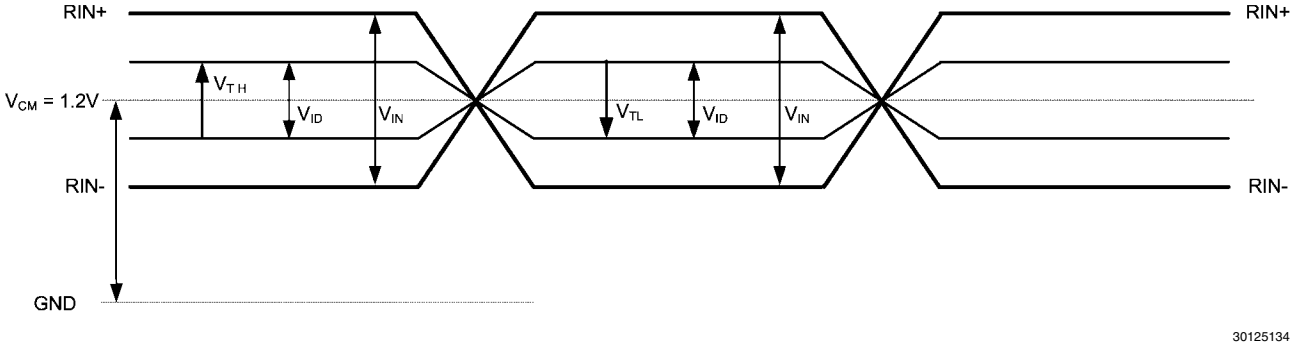


FIGURE 7. Low-Voltage Differential VTH/VTL Definition Diagram

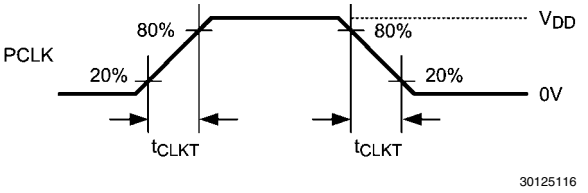


FIGURE 8. Serializer Input Clock Transition Times

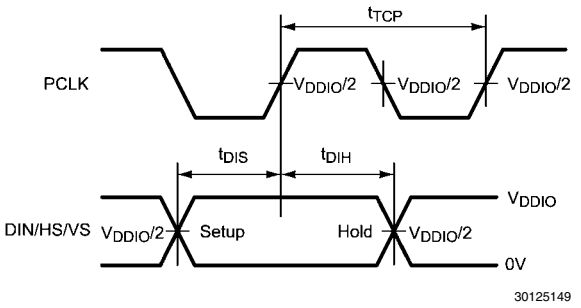


FIGURE 9. Serializer Setup/Hold Times

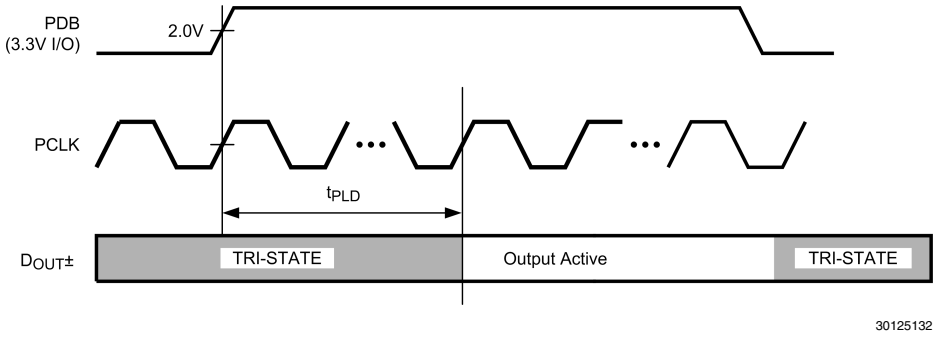


FIGURE 10. Serializer Data Lock Time

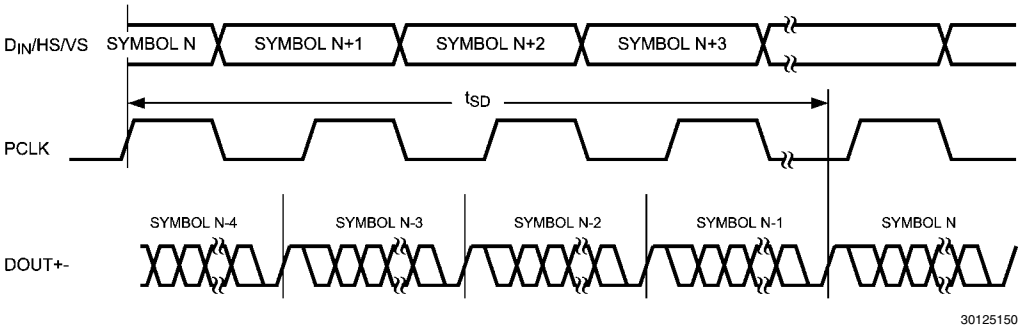


FIGURE 11. Serializer Delay

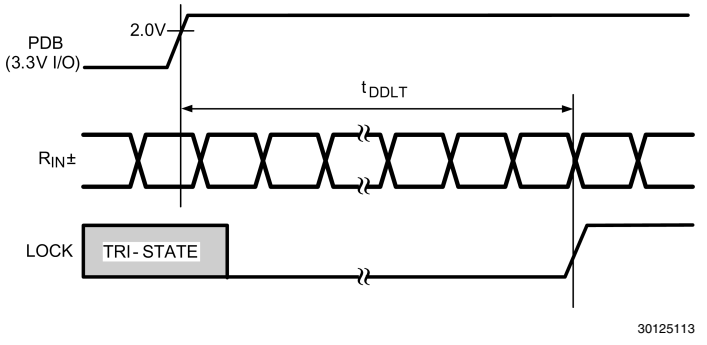


FIGURE 12. Deserializer Data Lock Time

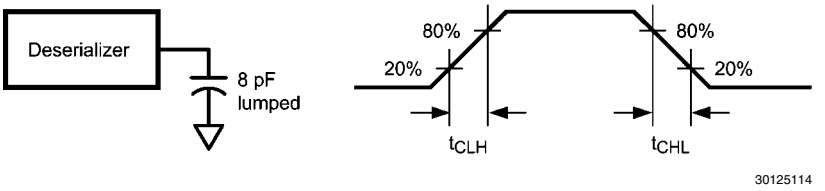


FIGURE 13. Deserializer LVCMOS Output Load and Transition Times

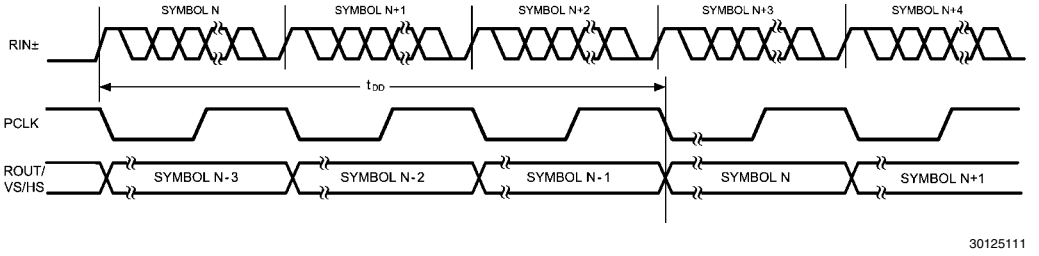


FIGURE 14. Deserializer Delay

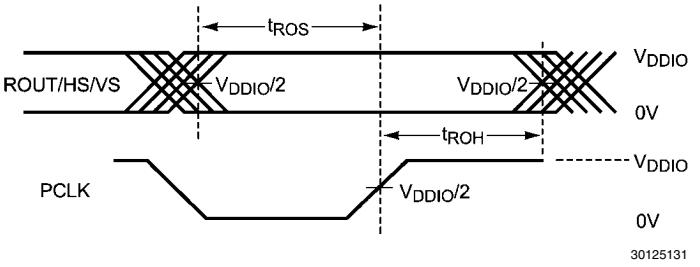


FIGURE 15. Deserializer Output Setup/Hold Times

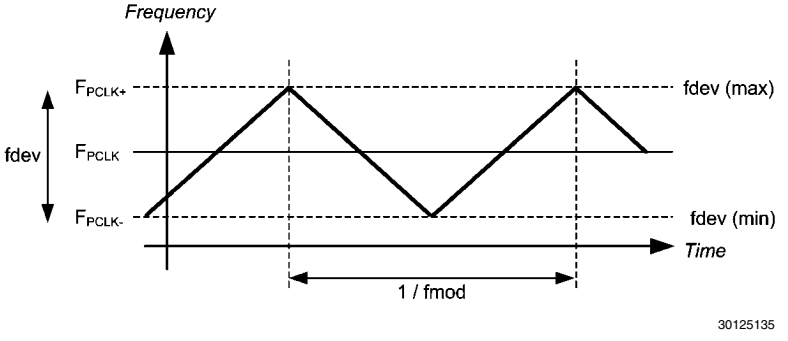


FIGURE 16. Spread Spectrum Clock Output Profile

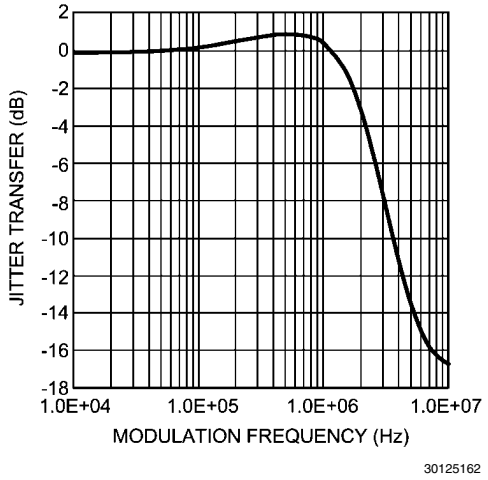


FIGURE 17. Typical Serializer Jitter Transfer Function Curve at 43 MHz

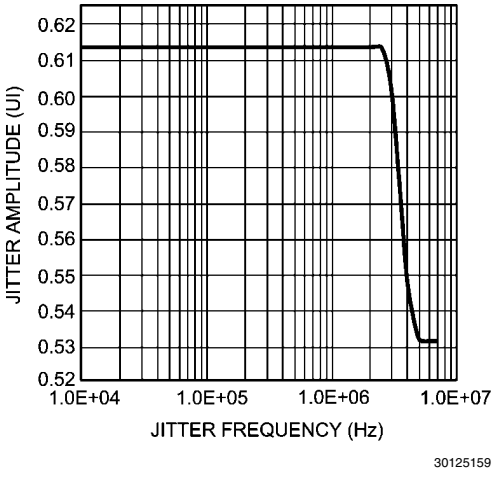


FIGURE 18. Typical Deserializer Input Jitter Tolerance Curve at 43 MHz

TABLE 1. DS92LX2121 Control Registers

Addr (Hex)	Name	Bits	Field	R/W	Default	Description
0	I²C Device ID	7:1	DEVICE ID	RW	0x58	7-bit address of Serializer; 0x58h (1011_000X) default
		0	SER ID	RW	0	0: Device ID is from CAD 1: Register I²C Device ID overrides CAD
1	Reset	7:3	RESERVED		0	Reserved.
		2	$\overline{\text{STANDBY}}$	RW	0	Standby mode control. Retains control register data. Supported only when M/S = 0 0: Enabled. Low-current Standby mode with wake-up capability. Suspends all clocks and functions. 1: Disabled. Standby and wake-up disabled
		1	DIGITAL RESET0	RW	0 self clear	1: Digital Reset, retained register value
		0	DIGITAL RESET1	RW	0 self clear	1: Digital Reset, retains all register values
2	Reserved	7:0	RESERVED		0x20'h	Reserved.
3	Reserved	7:6	RESERVED		11'b	Reserved.
	VDDIO Control	5	VDDIO CONTOL	RW	1	Auto V_{DDIO} detect Allows manual setting of V_{DDIO} by register. 0: Disable 1: Enable (auto detect mode)
	VDDIO Mode	4	VDDIO MODE	RW	1	V_{DDIO} voltage set Only used when VDDIOCONTROL = 0 0: 1.8V 1: 3.3V
	I²C Pass-Through	3	I²C PASS-THROUGH	RW	1	I²C Pass-Through Mode 0: Disabled 1: Enabled
	Reserved	2	RESERVED		0	Reserved.
	PCLK_AUTO	1	PCLK_AUTO	RW	1	Switch over to internal 25 MHz oscillator clock in the absence of PCLK 0: disable 1: enable
	TRFB	0	TRFB	RW	1	Pixel Clock Edge Select: 0: Parallel Interface Data is strobed on the Falling Clock Edge. 1: Parallel Interface Data is strobed on the Rising Clock Edge.
4	Reserved	7:0	RESERVED		0x80'h	Reserved.
5	I²C Bus Rate	7:0	I²C BUS RATE	RW	0x40'h	I²C SCL frequency is determined by the following: f_{SCL} = 6.25 MHz / Register value (in decimal) 0x40'h = ~100 kHz SCL (default) Note: Register values <0x32'h are NOT supported.
6	DES ID	7:1	DES DEV ID	RW	0x60'h	Deserializer Device ID = 0x60 (1100_000X) default
		0	RESERVED		0	Reserved.
7	Slave ID	7:1	SLAVE DEV ID	RW	0	Slave Device ID. Sets remote slave I2C address.
		0	RESERVED		0	Reserved.
8	Reserved	7:0	RESERVED		0	Reserved.
9	Reserved	7:0	RESERVED		0x01'h	Reserved.
A	Reserved	7:0	RESERVED		0	Reserved.

Addr (Hex)	Name	Bits	Field	R/W	Default	Description
B	Reserved	7:0	RESERVED		0	Reserved.
C	Reserved	7:3	RESERVED		0	Reserved.
	PCLK Detect	2	PCLK DETECT	R	0	1: Valid PCLK detected 0: Valid PCLK not detected
	Reserved	1	RESERVED			Reserved.
	Cable Link Detect Status	0	LINK DETECT	R	0	0: Cable link not detected 1: Cable link detected
D	Reserved	7:0	RESERVED			Reserved.
E	Reserved	7:0	RESERVED			Reserved.
F	Reserved	7:0	RESERVED			Reserved.
10	Reserved	7:0	RESERVED			Reserved.
11	Reserved	7:0	RESERVED			Reserved.
12	Reserved	7:0	RESERVED			Reserved.
13	General Purpose Control Reg	7:0	GPCR[7] GPCR[6] GPCR[5] GPCR[4] GPCR[3] GPCR[2] GPCR[1] GPCR[0]	RW	0	0: LOW 1: HIGH

TABLE 2. DS92LX2122 Control Registers

Addr (Hex)	Name	Bits	Field	R/W	Default	Description
0	I_2C Device ID	7:1	DEVICE ID	RW	0x60h	7-bit address of Deserializer; 0x60h (1100_000X) default
		0	DES ID	RW	0	0: Device ID is from CAD 1: Register I_2C Device ID overrides CAD
1	Reset	7:3	RESERVED			Reserved
		2	REM_WAKEUP	RW	0	Remote Wake-up Select 1: Enable. Generate remote wakeup signal automatically wake-up the Serializer in Standby mode 0: Disable. Puts the Serializer in Standby mode
		1	DIGITALRESET0	RW	0 self clear	1: Resets the device to default register values. Does not affect device I^2C Bus or Device ID
		0	DIGITALRESET1	RW	0 self clear	1: Digital Reset, retained register value
2	Reserved	7:6	RESERVED		0	Reserved.
	Auto Clock	5	AUTO_CLOCK	RW	0	1: Output PCLK or internal 25 MHz Oscillator clock 0: Only PCLK when valid PCLK present
	OSS Select	4	OSS_SEL	RW	0	Output Sleep State Select 0: Outputs = LOW , when LOCK = L 1: Outputs = TRI-STATE®, when LOCK = L
	SSCG	3:0	SSCG		0	SSCG Select 0000: Normal Operation, SSCG OFF 0001: fmod (KHz) PCLK/2168, fdev ±0.50% 0010: fmod (KHz) PCLK/2168, fdev ±1.00% 0011: fmod (KHz) PCLK/2168, fdev ±1.50% 0100: fmod (KHz) PCLK/2168, fdev ±2.00% 0101: fmod (KHz) PCLK/1300, fdev ±0.50% 0110: fmod (KHz) PCLK/1300, fdev ±1.00% 0111: fmod (KHz) PCLK/1300, fdev ±1.50% 1000: fmod (KHz) PCLK/1300, fdev ±2.00% 1001: fmod (KHz) PCLK/868, fdev ±0.50% 1010: fmod (KHz) PCLK/868, fdev ±1.00% 1011: fmod (KHz) PCLK/868, fdev ±1.50% 1100: fmod (KHz) PCLK/868, fdev ±2.00% 1101: fmod (KHz) PCLK/650, fdev ±0.50% 1110: fmod (KHz) PCLK/650, fdev ±1.00% 1111: fmod (KHz) PCLK/650, fdev +/-1.50%

Addr (Hex)	Name	Bits	Field	R/W	Default	Description
3	Reserved	7:6	RESERVED		11'b	Reserved.
	VDDIO Control	5	VDDIO CONTROL	RW	1	Auto voltage control 0: Disable 1: Enable (auto detect mode)
	VDDIO Mode	4	VDDIO MODE	RW	0	VDDIO voltage set Only used when VDDIOCONTROL = 0 0: 1.8V 1: 3.3V
	I²C Pass-Through	3	I²C PASS-THROUGH	RW	1	I²C Pass-Through Mode 0: Pass-Through Enabled 1: Pass-Through Disabled
	Auto ACK	2	AUTO ACK	RW	0	0: Disable 1: Enable
	Reserved	1	RESERVED		0	Reserved.
	RRFB	0	RRFB	RW	1	Pixel Clock Edge Select 0: Parallel Interface Data is strobed on the Falling Clock Edge 1: Parallel Interface Data is strobed on the Rising Clock Edge.
4	EQ Control	7:0	EQ	RW	0	EQ Gain 00'h = ~0.0 dB 01'h = ~4.5 dB 03'h = ~6.5 dB 07'h = ~7.5 dB 0F'h = ~8.0 dB 1F'h = ~11.0 dB 3F'h = ~12.5 dB FF'h = ~14.0 dB
5	Reserved	7:0	RESERVED		0	Reserved.
6	Reserved	7	RESERVED			Reserved.
	SCL Prescale	6:4	SCL_PRESCALE	RW	0	Prescales the SCL clock line when reading data byte from a slave device (MODE = 0) 000 : ~100 kHz SCL (default) 001 : ~125 kHz SCL 101 : ~11 kHz SCL 110 : ~33 kHz SCL 111 : ~50 kHz SCL Other values are NOT supported.
	Remote NACK	3	REM_NACK_TIMER	RW	1	Remote NACK Timer Enable In slave mode (MODE = 1) if bit is set the I2C core will automatically timeout when no acknowledge condition was detected. 1: Enable 0: Disable
	Remote NACK	2:0	REM_NACK_TIMER	RW	111'b	Remote NACK Timeout 000: 2.0 ms 001: 5.2 ms 010: 8.6 ms 011: 11.8 ms 100: 14.4 ms 101: 18.4 ms 110: 21.6 ms 111: 25.0 ms

Addr (Hex)	Name	Bits	Field	R/W	Default	Description
7	SER ID	7:1	SER DEV ID	RW	0x58h	Serializer Device ID = 0x58 (1011_000X) default
		0	RESERVED		0	Reserved
8	ID[0] Index	7:1	ID[0] INDEX	RW	0	Target slave Device ID slv_id1 [7:1]
		0	RESERVED		0	Reserved.
9	ID[1] Index	7:1	ID[1] INDEX	RW	0	Target slave Device ID slv_id1 [7:1]
		0	RESERVED		0	Reserved.
A	ID[2] Index	7:1	ID[2] INDEX	RW	0	Target slave Device ID slv_id2 [7:1]
		0	RESERVED		0	Reserved.
B	ID[3] Index	7:1	ID[3] INDEX	RW	0	Target slave Device ID slv_id3 [7:1]
		0	RESERVED		0	Reserved.
C	ID[4] Index	7:1	ID[4] INDEX	RW	0	Target slave Device ID slv_id4 [7:1]
		0	RESERVED		0	Reserved.
D	ID[5] Index	7:1	ID[5] INDEX	RW	0	Target slave Device ID slv_id5 [7:1]
		0	RESERVED		0	Reserved.
E	ID[6] Index	7:1	ID[6] INDEX	RW	0	Target slave Device ID slv_id6 [7:1]
		0	RESERVED		0	Reserved.
F	ID[7] Index	7:1	ID[7] INDEX	RW	0	Target slave Device ID slv_id7 [7:1]
		0	RESERVED		0	Reserved.
10	ID[0] Match	7:1	ID[0] MATCH	RW	0	Alias to match Device ID slv_id0 [7:1]
		0	RESERVED		0	Reserved.
11	ID[1] Match	7:1	ID[1] MATCH	RW	0	Alias to match Device ID slv_id1 [7:1]
		0	RESERVED		0	Reserved.
12	ID[2] Match	7:1	ID[2] MATCH	RW	0	Alias to match Device ID slv_id2 [7:1]
		0	RESERVED		0	Reserved.
13	ID[3] Match	7:1	ID[3] MATCH	RW	0	Alias to match Device ID slv_id3 [7:1]
		0	RESERVED		0	Reserved.
14	ID[4] Match	7:1	ID[4] MATCH	RW	0	Alias to match Device ID slv_id4 [7:1]
		0	RESERVED		0	Reserved.
15	ID[5] Match	7:1	ID[5] MATCH	RW	0	Alias to match Device ID slv_id5 [7:1]
		0	RESERVED		0	Reserved
16	ID[6] Match	7:1	ID[6] MATCH	RW	0	Alias to match Device ID slv_id6 [7:1]
		0	RESERVED		0	Reserved.
17	ID[7] Match	7:1	ID[7] MATCH	RW	0	Alias to match Device ID slv_id [7:1]
		0	RESERVED		0	Reserved.
18	Reserved	7:0	RESERVED		0	Reserved.
19	Reserved	7:0	RESERVED		0x01'h	Reserved.
1A	Reserved	7:0	RESERVED		0	Reserved.
1B	Reserved	7:0	RESERVED		0	Reserved.
1C	Reserved	7:2	RESERVED		0	
	Signal Detect Status	1		R	0	0: Active signal not detected 1: Active signal detected
	LOCK Pin Status	0		R	0	0: CDR/PLL Unlocked 1: CDR/PLL Locked
1D	Reserved	7:0	RESERVED		0x17'h	Reserved.
1E	Reserved	7:0	RESERVED		0x07'h	Reserved.
1F	Reserved	7:0	RESERVED		0x01'h	Reserved.
20	Reserved	7:0	RESERVED		0x01'h	Reserved.
21	Reserved	7:0	RESERVED		0x01'h	Reserved.

Addr (Hex)	Name	Bits	Field	R/W	Default	Description
22	Reserved	7:0	RESERVED		0x01'h	Reserved.
23	General Purpose Control Reg	7:00	GPCR[7] GPCR[6] GPCR[5] GPCR[4] GPCR[3] GPCR[2] GPCR[1] GPCR[0]	RW	0	0: LOW 1: HIGH
24	Reserved	7:1	RESERVED		0	Reserved.
	BIST	0	BIST_EN	RW	0	BIST Enable 0: Normal operation 1: Bist Enable
25	BIST_ERR	7:0	BIST_ERR	R	0	Bist Error Counter
26	Remote Wake Enable	7:6	REM_WAKEUP_EN	RW	0	11: Enable remote wake up mode 00: Normal operation mode Other values are NOT supported.
		5:0	RESERVED	RW	0	Reserved

Functional Description

The DS92LX2121 / DS92LX2122 Channel Link III chipset is intended for camera applications. The Serializer/ Deserializer chipset operates from a 10 MHz to 50 MHz pixel clock frequency. The DS92LX2121 transforms a 21-bit wide parallel LVCMOS data bus along with a bi-directional back channel control bus into a single high-speed differential pair. The high speed serial bit stream contains an embedded clock and DC-balance information which enhances signal quality to support AC coupling. The DS92LX2122 receives the single serial data stream and converts it back into a 21-bit wide parallel data bus together with the back channel data bus.

The control channel function of the DS92LX2121 / DS92LX2122 provides bi-directional communication between the image sensor and Electronic Control Unit (ECU). The integrated back channel transfers data bi-directionally over the same differential pair used for video data interface. This interface offers advantages over other chipsets by eliminating the need for additional wires for programming and control. The back channel bus is controlled via an I²C port. The bi-directional back channel offers asymmetrical communication and is not dependent on video blanking intervals.

DISPLAY APPLICATION

The DS92LX2121 / DS92LX2122 chipset is intended for interface between a host (graphics processor, FPGA, etc.) and a Display. It supports a 21 bit parallel video bus for 18-bit color depth (RGB666) display format. In a RGB666 configuration, 18 color bits (R [5:0], G[5:0], B[5:0]), Pixel Clock (PCLK) and three control bits (VS, HS and DE) are supported across the serial link. The DS92LX2121 Serializer accepts a 21-bit parallel data bus along with a bi-directional control bus. The parallel data and bi-directional control channel information is converted into a single differential link. The integrated bi-directional control channel bus supports I²C compatible operation for controlling auxiliary data transport to and from host processor and display module. The DS92LX2122 Deserializer extracts the clock/control information from the incoming data stream and reconstructs the 21-bit data with control channel data.

SERIAL FRAME FORMAT

The DS92LX2121 / DS92LX2122 chipset will transmit and receive a pixel of data in the following format:

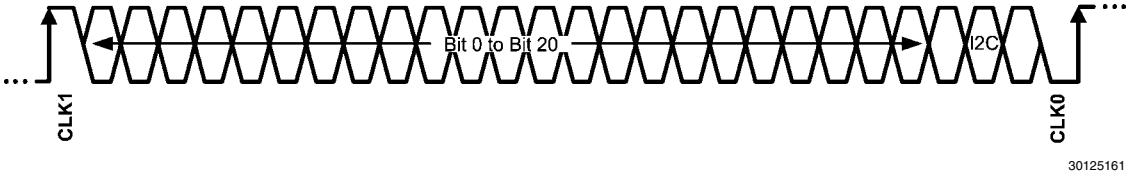


FIGURE 19. Serial Bitstream for 28-bit Symbol

The High Speed Forward Channel is a 28-bit symbol composed of 21 bits of data containing video data & control information transmitted from Serializer to Deserializer. CLK1 and CLK0 represent the embedded clock in the serial stream. CLK1 is always HIGH and CLK0 is always LOW. This data payload is optimized for signal transmission over an AC coupled link. Data is randomized, balanced and scrambled.

The bi-directional control channel data is transferred along with the high-speed forward data over the same serial link. This architecture provides a full duplex low speed forward channel across the serial link together with a high speed forward channel without the dependence of the video blanking phase.

DESCRIPTION OF BI-DIRECTIONAL CONTROL BUS AND I²C MODES

The I²C compatible interface allows programming of the DS92LX2121, DS92LX2122, or an external remote device (such as a display) through the bi-directional control channel. Register programming transactions to/from the DS92LX2121 / DS92LX2122 chipset are employed through the clock (SCL) and data (SDA) lines. These two signals have open drain I/Os and both lines must be pulled-up to V_{DDIO} by external resistor. *Figure 3* shows the timing relationships of the clock (SCL) and data (SDA) signals. Pull-up resistors or current sources are required on the SCL and SDA busses to pull them high when they are not being driven low. A logic zero is transmitted by driving the output low. A logic high is transmitted by releasing the output and allowing it to be pulled-up externally. The appropriate pull-up resistor values will depend upon the total bus capacitance and operating speed. The DS92LX2121 / DS92LX2122 I²C bus data rate supports up to 100 kbps according to I2C specification.

To start any data transfer, the DS92LX2121 / DS92LX2122 must be configured in the proper I2C mode. Each device can function as an I²C slave proxy or master proxy depending on the mode determined by M/S pin. The Ser/Des interface acts as a virtual bridge between the host device and the remote device. When the M/S pin is set to HIGH, the device is treated as a slave proxy; and acts as a slave on behalf of the remote slave. When addressing a remote peripheral or Serializer/ Deserializer (not wired directly to the host device), the slave proxy will forward any byte transactions sent by the host controller to the target device. When M/S pin is set to LOW, the device will function as a master proxy device, and acts as a master on behalf of the I²C master controller. Note that the devices must have complementary settings for the M/S configuration. For example, if the Serializer M/S pin is set to HIGH then the Deserializer M/S pin must be set to LOW and vice-versa.

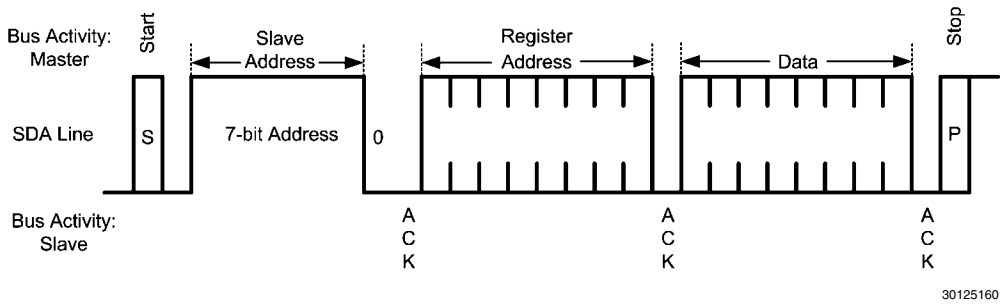


FIGURE 20. Write Byte

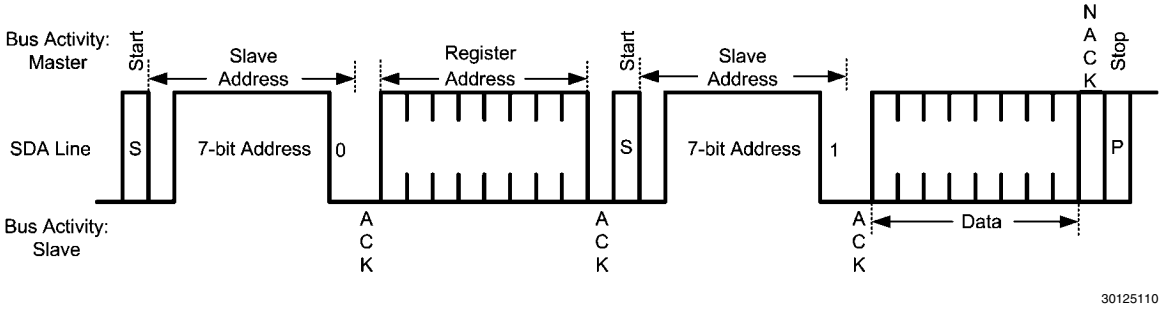


FIGURE 21. Read Byte

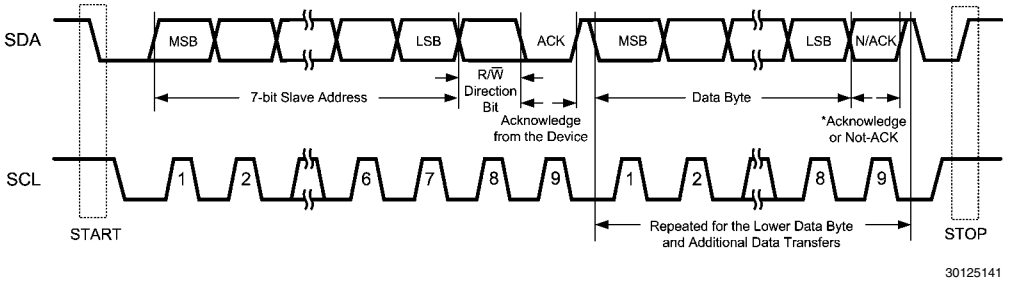


FIGURE 22. Basic Operation

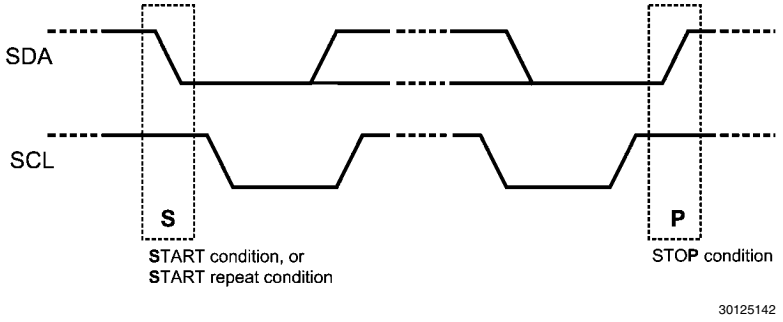


FIGURE 23. START and STOP Conditions

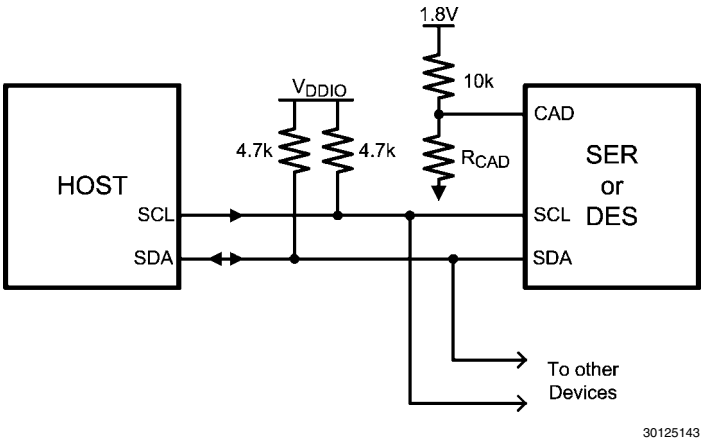


FIGURE 24. Serial Control Bus Connection

SLAVE CLOCK STRETCHING

In order to communicate and synchronize with remote devices on the I²C bus through the bi-directional control channel, slave clock stretching must be supported by the I²C master controller/host device. The chipset utilizes bus clock stretching (holding the SCL line low) during data transmission; where the I2C slave pulls the SCL line low on the 9th clock of every I²C data transfer (before the ACK signal). The slave device will not control the clock and only stretches it until the remote peripheral has responded; which is typically in the order of 12 µs (typical).

CAD PIN ADDRESS DECODER

The CAD pin is used to decode and set the physical slave address of the Serializer/Deserializer (I²C only) to allow up to six devices on the bus using only a single pin. The pin sets one of six possible addresses for each Serializer/Deserializer device. The pin must be pulled to VDD (1.8V, NOT VDDIO)) with a 10 kΩ resistor and a pull down resistor (RID) of the recommended value to set the physical device address. The recommended maximum resistor tolerance is 0.1% worst case (0.2% total tolerance).

TABLE 3. DS92LX2121 RID Resistor Values

CAD Values - DS92LX2121 Ser		
Resistor RID kΩ	**Address 7'b**	**Address 8'b 0 appended (WRITE)**
0 GND	7b' 101 1000 (h'58)	8b' 1011 0000 (h'B0)
2.0k	7b' 101 1001 (h'59)	8b' 1011 0010 (h'B2)
4.7k	7b' 101 1010 (h'5A)	8b' 1011 0100 (h'B4)
8.2k	7b' 101 1011 (h'5B)	8b' 1011 0110 (h'B6)
12.1k	7b' 101 1100 (h'5C)	8b' 1011 1000 (h'B8)
39.0k	7b' 101 1110 (h'5E)	8b' 1011 1100 (h'BC)

TABLE 4. DS92LX2122 RID Resistor Values

CAD Values - DS92LX2122 Des		
Resistor RID kΩ	**Address 7'b**	**Address 8'b 0 appended (WRITE)**
0 GND	7b' 110 0000 (h'60)	8b' 1100 0000 (h'C0)
2.0k	7b' 110 0001 (h'61)	8b' 1100 0010 (h'C2)
4.7k	7b' 110 0010 (h'62)	8b' 1100 0100 (h'C4)
8.2k	7b' 110 0011 (h'62)	8b' 1101 0110 (h'C6)
12.1k	7b' 110 0100 (h'62)	8b' 1101 1000 (h'C8)
39.0k	7b' 110 0110 (h'66)	8b' 1100 1100 (h'CC)

CAMERA MODE OPERATION

In Camera mode, I²C transactions originate from the Deserializer from the host controller. The I²C slave core in the Deserializer will detect if a transaction is intended for the Serializer or a slave at the Serializer. Commands are sent over the bi-directional control channel to initiate the transactions. The Serializer will receive the command and generate an I²C transaction on its local I²C bus. At the same time, the Serializer will capture the response on the I²C bus and return the response as a command on the forward channel link. The Deserializer parses the response and passes the appropriate response to the Deserializer I²C bus.

To configure the devices for camera mode operation, set the Serializer M/S pin to LOW and the Deserializer M/S pin to HIGH. Before initiating any I²C commands, the Deserializer needs to be programmed with the target slave device addresses and Serializer device address. SER_DEV_ID Register 0x07h sets the Serializer device address and SLAVE_x_MATCH/SLAVE_x_INDEX registers 0x08h~0x17h set the remote target slave addresses. The slave address match registers must also be set. In slave mode the address register is compared with the address byte sent by the I2C master. If the addresses are equal to any of registers values, the I²C slave will acknowledge the transaction to the I²C master allowing reads or writes to target device.

DISPLAY MODE OPERATION

In Display mode, I²C transactions originate from the controller attached to the Serializer. The I²C slave core in the Serializer will detect if a transaction targets (local) registers within the Serializer or the (remote) registers within the Deserializer or a remote slave connected to the I²C master interface of the Deserializer. Commands are sent over the forward channel link to initiate the transactions. The Deserializer will receive the command and generate an I²C transaction on its local I²C bus. At the same time, the Deserializer will capture the response on the I²C bus and return the response as a command on the bi-directional control channel. The Serializer parses the response and passes the appropriate response to the Serializer I²C bus.

The physical device ID of the I²C slave in the Serializer is determined by the analog voltage on the CAD pin input. It can be reprogrammed by using the SER_DEV_ID register and setting the bit . The device ID of the logical I²C slave in the Deserializer is determined by programming the DES ID in the Serializer. The state of the CAD pin input on the Deserializer is used to set the device ID. The I²C transactions between Ser/ Des will be bridged between the host to the remote slave.

To configure the devices for display mode operation, set the Serializer M/S pin to HIGH and the Deserializer M/S pin to LOW. Before initiating any I²C commands, the Serializer needs to be programmed with the target slave device address and Serializer device address. DES_DEV_ID Register 0x06h sets the Deserializer device address and SLAVE_DEV_ID register 0x7h sets the remote target slave address. If the I²C slave address matches any of registers values, the I²C slave will acknowledge the transaction allowing read or write to target device. Note: In Display mode operation, registers 0x08h~0x17h on Deserializer must be reset to 0x00.

PROGRAMMABLE CONTROLLER

An integrated I²C slave controller is embedded in each of the DS92LX2121 Serializer and DS92LX2122 Deserializer. It must be used to access and program the extra features embedded within the configuration registers. Refer to *Table 1* and *Table 2* for details of control registers.

I²C PASS THROUGH

I²C pass-through provides an alternative means to independently address slave devices. The mode enables or disables I²C bidirectional control channel communication to the remote I²C bus. This option is used to determine whether or not an I²C instruction is to be transferred over to the remote I²C device. When enabled, the I²C bus traffic will continue to pass through and will be received by I²C devices downstream. If disabled, I²C commands will be excluded to the remote I²C device. The pass through function also provides access and communication to only specific devices on the remote bus. The feature is effective for both Camera mode and Display mode.

SYNCHRONIZING MULTIPLE LINKS

For applications requiring synchronization across multiple links, it is recommended to utilize the General Purpose Input/ Output (GPI/GPO) pins to transmit control signals to synchronize slave peripherals together. To synchronize the peripherals properly, the system controller needs to provide a sync signal output. Note this form of synchronization timing relationship has a non-deterministic latency. After the control data is reconstructed from the bi-directional control channel, there will be a time variation of the GPI/GPO signals arriving at the different target devices (between the parallel links). The maximum latency delta (t1) of the GPI/GPO data transmitted across multiple links is 25 µs.

Note: The user must verify that the timing variations between the different links are within their system and timing specifications.

The maximum time (t1) between the rising edge of GPI/GPO (i.e. sync signal) arriving at Camera A and Camera B is 25 µs.

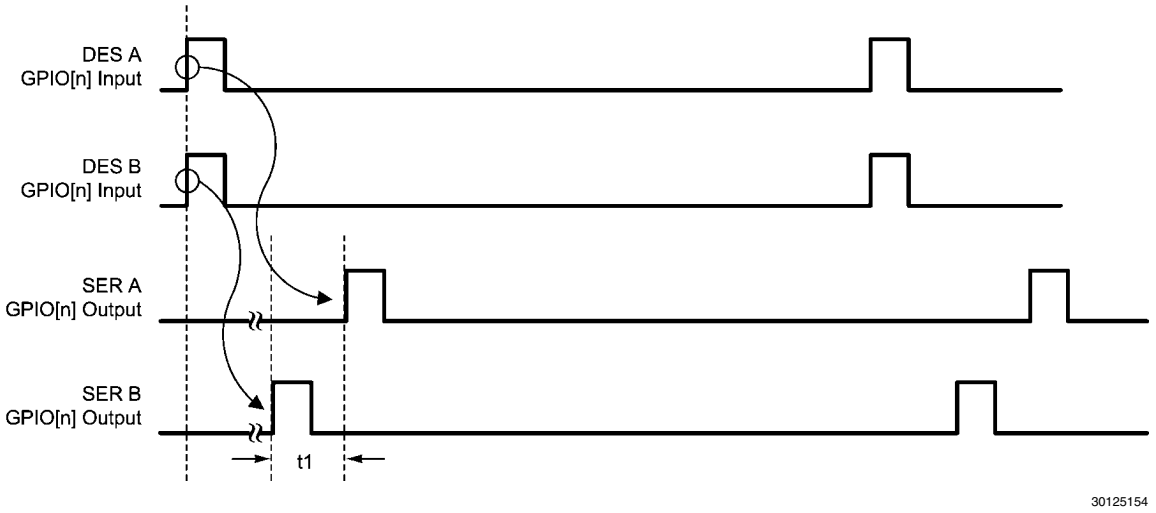


FIGURE 25. GPIO Delta Latency

GENERAL PURPOSE I/O (GPIO)

The DS92LX2121 / DS92LX2122 has up to 4 GPO and 4 GPI on the Serializer and Deserializer respectively. The GPI/GPO maximum switching rate is up to 66 kHz for communication between Deserializer GPI to Serializer GPO.

AT-SPEED BIST (BISTEN, PASS)

An optional AT SPEED Built in Self Test (BIST) feature supports at speed testing of the high-speed serial and the back-channel link. Control pins allow the system to initiate the test and set the duration. A HIGH on PASS pin indicates that all payloads received during the test were error free during the BIST duration test. A LOW on this pin at the conclusion of this test indicates that one or more payloads were detected with errors.

The BIST duration is defined by the width of BISTEN. BIST starts when BISTEN goes HIGH. BIST ends when BISTEN goes LOW. PASS flag will go HIGH when no errors detected after BIST Duration completes. Any errors detected after the BIST Duration are not included in PASS logic.

The following diagram shows how to perform system AT SPEED BIST:

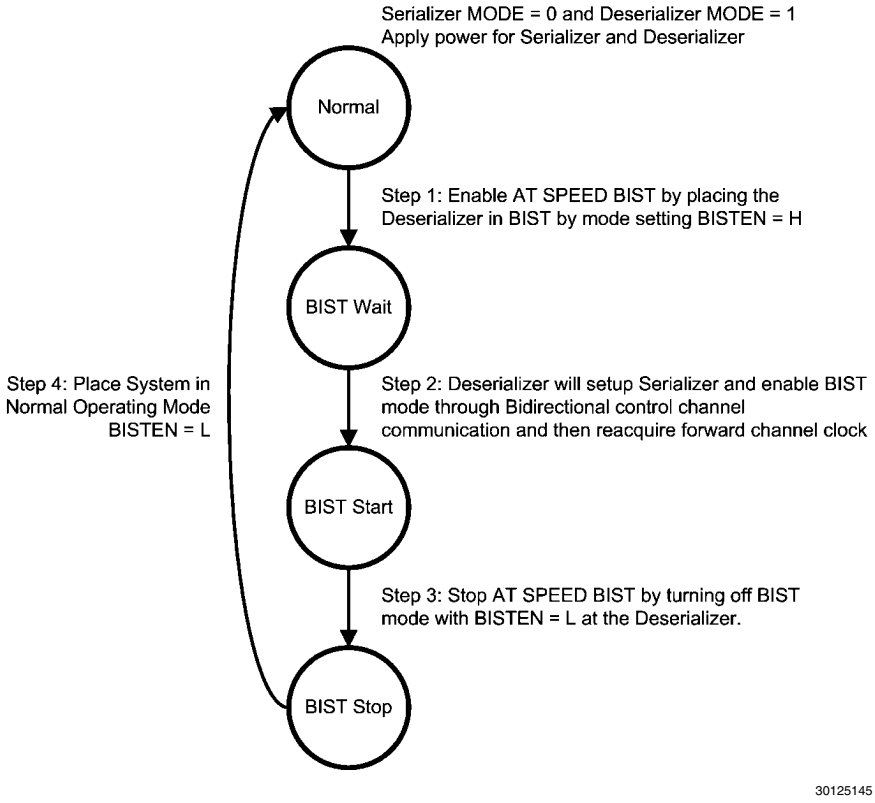


FIGURE 26. AT-SPEED BIST System Flow Diagram

Step 1: Place the Deserializer in BIST Mode.

Serializer and Deserializer power supply must be supplied. Set the Serializer M/S pin to LOW and the Deserializer M/S pin to HIGH. Enable the AT SPEED BIST mode on the Deserializer by setting the BISTEN pin High. The DS92LX2122 GPIO[1:0] pins are used to select the PCLK frequency of the on-chip oscillator for the BIST test on high speed data path.

Oscillator Frequency Select

Freq Control	Oscillator Range	min (MHz)	typ (MHz)	max (MHz)
00	External PCLK	10		50
01	Internal		50	
10	Internal		25	
11	Internal		12.5	

The Deserializer GPIO[1:0] set to 00 will bypass the on-chip oscillator and an external oscillator to Serializer PCLK input is required. This allows the user to operate BIST under different frequencies other than the predefined ranges.

Step 2: Enable AT SPEED BIST by placing the Serializer into BIST mode.

Deserializer will communicate through the back-channel to configure Serializer into BIST mode. Once the BIST mode is set, the Serializer will initiate BIST transmission to the Deserializer.

Wait 10 ms for Deserializer to acquire lock and then monitor the LOCK pin transition from LOW to HIGH. At this point, AT SPEED BIST is operational and the BIST process has begun.

The Serializer will start transfer of an internally generated PRBS data pattern through the high speed serial link. This pattern traverses across the interconnecting link to the Deserializer. Check the status of the PASS pin; a HIGH indicates a pass, a LOW indicates a fail. A fail will stay LOW for ½ a clock cycle. If two or more bits fail in a row the PASS pin will toggle ½ clock cycle HIGH and ½ clock cycle low. The user can use the PASS pin to count the number of fails on the high speed link. In addition, there is a defined SER and DES register that will keep track of the accumulated error count. The Serializer DS92LX2121 GPIO[0] pin will be assigned as a PASS flag error indicator for the back-channel link.

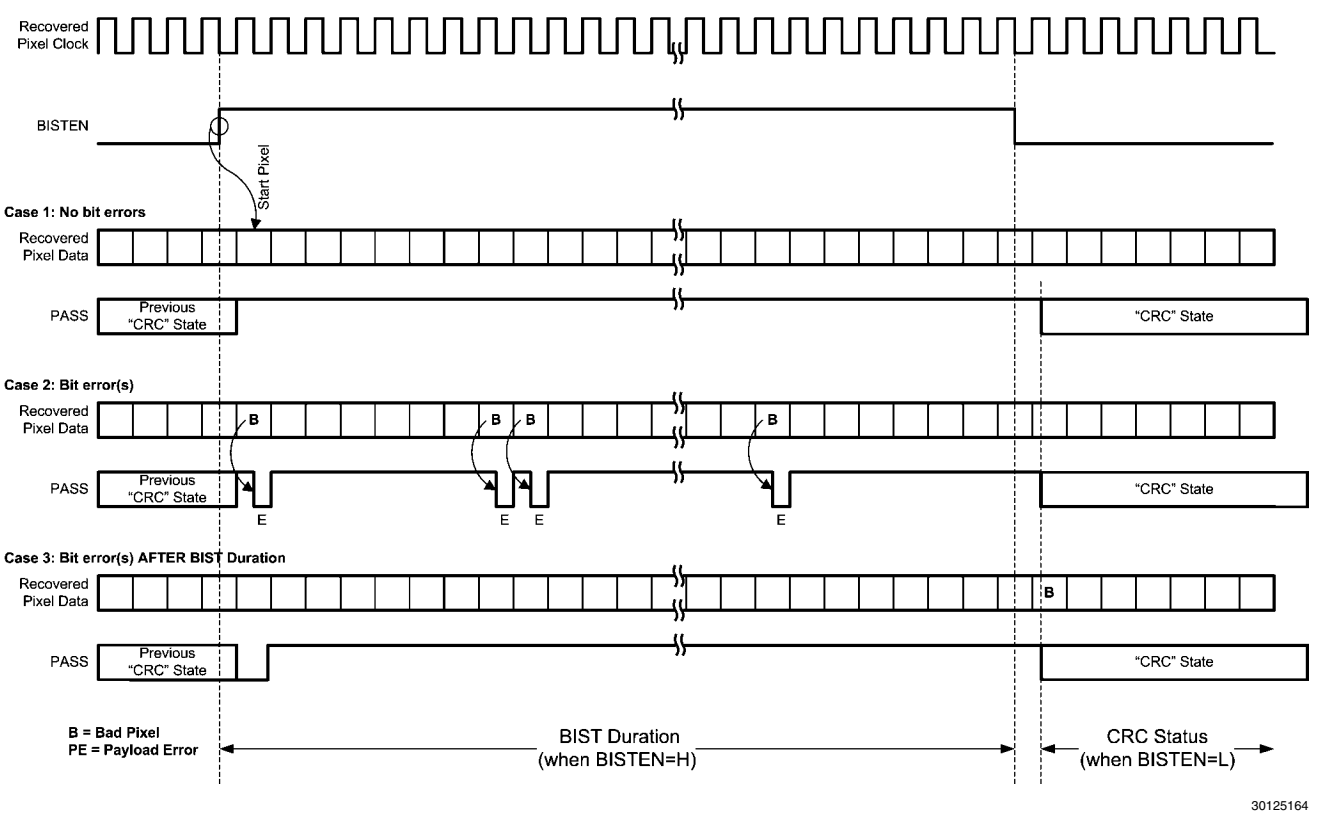


FIGURE 27. BIST Timing Diagram

Step 3: Stop at SPEED BIST by turning off BIST mode in the Deserializer to determine Pass/Fail.

To end BIST, the system must pull BISTEN pin of the Deserializer LOW. The BIST duration is fully defined by the BISTEN width and thus the Bit Error Rate is determined by how long the system holds BISTEN HIGH.

$$\frac{\text{BIST Duration (s)}}{\text{1 Pixel period (ns) x Total Bits}} = \text{BIST Duration (s)} \times \frac{f_{pixel}\ (\text{MHz})}{\text{Pixel}} \times \text{Total Pixels Transmitted} = \text{Total Bits Transmitted}$$

$$\therefore \quad \text{Bit (Pixel) Error Rate (for passing BIST)} = [\text{Total Bits Transmitted}]^{-1}$$

$$= [\text{Total Bits Transmitted x Bits/Pixel}]^{-1}$$

30125105

FIGURE 28. BIST BER Calculation

For instance, if BISTEN is held HIGH for 1 second and the PCLK is running at 43 MHz with 16 bpp, then the Bit Error Rate is no better than 1.46E-9.

Step 4: Place system in Normal Operating Mode by disabling BIST at the Serializer.

Once Step 3 is complete, AT SPEED BIST is over and the Deserializer is out of BIST mode. To fully return to Normal mode, apply Normal input data into the Serializer.

Any PASS result will remain unless it is changed by a new BIST session or cleared by asserting and releasing PDB. The default state of PASS after a PDB toggle is HIGH.

It is important to note that AT SPEED BIST will only determine if there is an issue on the link that is not related to the clock and data recovery of the link (whose status is flagged with LOCK pin).

LVCMOS VDDIO OPTION

1.8V or 3.3V SER Inputs and DES Outputs are user configurable to provide compatibility with 1.8V and 3.3V system interfaces.

REMOTE WAKE UP (Camera Mode)

After initial power up, the SER is in a low-power Standby mode. The DES (controlled by the host) 'Remote Wakeup' register allows the DES side to generate a signal across the link to remotely wakeup the SER. Once the SER detects the wakeup signal, the SER switches from Standby mode to active mode. In active mode, the SER locks onto PCLK input (if present), otherwise the on-chip oscillator is used as the input clock source. Note the host controller should monitor the DES

LOCK pin and confirm LOCK = H before performing any I²C communication across the link.

For Remote Wakeup to function properly:

- The chipset needs to be configured in Camera mode: Serializer M/S = 0 and Deserializer M/S = 1
- The SER expects remote wake up by default at power on.
- Configure the control channel driver of the DES to be in remote wake up mode by setting DES register 0x26 to 0xC0.
- Perform remote wake up on SER by setting DES register 0x01 b[2] to 1.
- Return the control channel driver of the DES to the normal operation mode by setting DES register 0x26 to 0.

The SER can also be put into standby mode by programming the DES remote wake up control register 0x01 b[2] REM_WAKEUP to 0.

POWERDOWN

The SER has a PDB input pin to ENABLE or Powerdown the device. The modes can be controlled by the host and is used to disable the Link to save power when the remote device is not operational. An auto mode is also available. In this mode, the PDB pin is tied High and the SER switches over to an internal oscillator when the PCLK stops or not present. When a PCLK starts again, the SER will then lock to the valid input PCLK and transmits the data to the DES. In powerdown mode, the high-speed driver outputs are static (HIGH).

The DES has a PDB input pin to ENABLE or Powerdown the device. This pin can be controlled by the system and is used to disable the DES to save power. An auto mode is also available. In this mode, the PDB pin is tied High and the DES will enter powerdown when the serial stream stops. When the serial stream starts up again, the DES will lock to the input stream and assert the LOCK pin and output valid data. In powerdown mode, the Data and PCLK outputs are set by the OSS_SEL control register.

POWER UP REQUIREMENTS AND PDB PIN

The VDD (VDDn and VDDIO) supply ramp should be faster than 1.5 ms with a monotonic rise. If slower then 1.5 ms then a capacitor on the PDB pin is needed to ensure PDB arrives after all the VDD have settled to the recommended operating voltage. When PDB pin is pulled to VDDIO, it is recommended to use a 10 kΩ pull-up and a 22 uF cap to GND to delay the PDB input signal.

SIGNAL QUALITY ENHANCERS

Des - Receiver Input Equalization (EQ)

The receiver inputs provided input equalization filter in order to compensate for loss from the media. The level of equalization is controlled via register setting.

EMI REDUCTION

Des - Receiver Staggered Output

The Receiver staggered outputs allows for outputs to switch in a random distribution of transitions within a defined window. Outputs transitions are distributed randomly. This minimizes the number of outputs switching simultaneously and helps to reduce supply noise. In addition it spreads the noise spectrum out reducing overall EMI.

Des Spread Spectrum Clocking Compatibilty

The DS92LX2122 parallel data and clock outputs have programmable SSCG ranges from 70 kHz and +-2% (4% total) from 20 MHz to 50 MHz. The modulation rate and modulation frequency variation of output spread is controlled through the SSC control registers.

PIXEL CLOCK EDGE SELECT (TRFB/RRFB)

The TRFB/RRFB selects which edge of the Pixel Clock is used. For the SER, this register determines the edge that the data is latched on. If TRFB register is 1, data is latched on the Rising edge of the PCLK. If TRFB register is 0, data is latched on the Falling edge of the PCLK. For the DES, this register determines the edge that the data is strobed on. If RRFB register is 1, data is strobed on the Rising edge of the PCLK. If RRFB register is 0, data is strobed on the Falling edge of the PCLK.

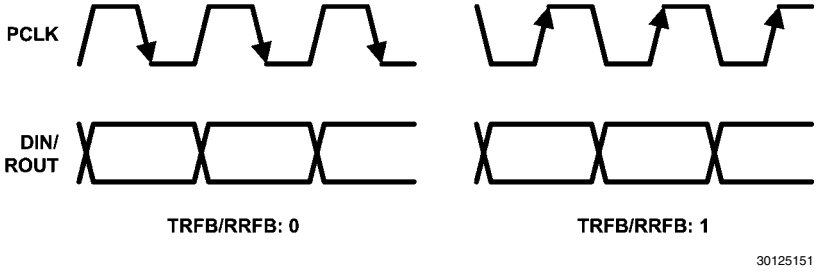


FIGURE 29. Programmable PCLK Strobe Select

Applications Information

AC COUPLING

The SER/DES supports only AC-coupled interconnects through an integrated DC balanced decoding scheme. External AC coupling capacitors must be placed in series in the Channel Link III signal path as illustrated in Figure 34.

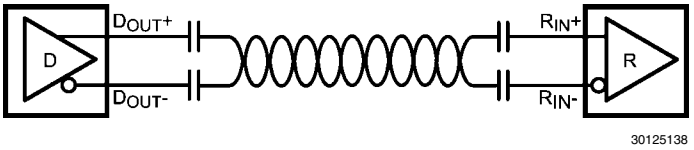


FIGURE 30. AC-Coupled Application

For high-speed Channel Link III transmissions, the smallest available package should be used for the AC coupling capacitor. This will help minimize degradation of signal quality due to package parasitics. The I/O's require a 0.1 µF AC coupling capacitors to the line.

TYPICAL APPLICATION CONNECTION

Figure 31 shows a typical connection of the DS92LX2121 Serializer.

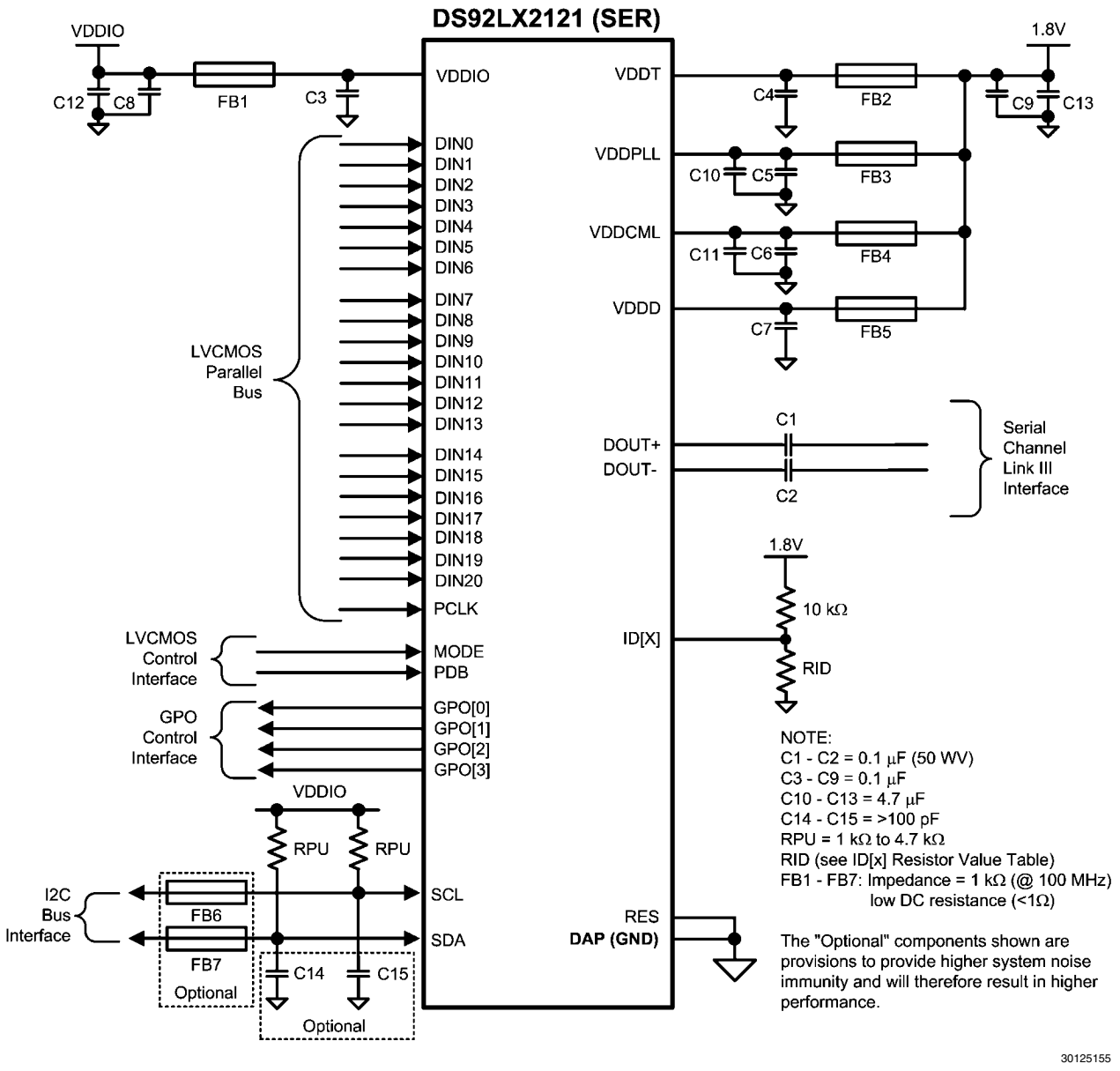


FIGURE 31. DS92LX2121 Typical Connection Diagram

Figure 32 shows a typical connection of the DS92LX2122 Deserializer.

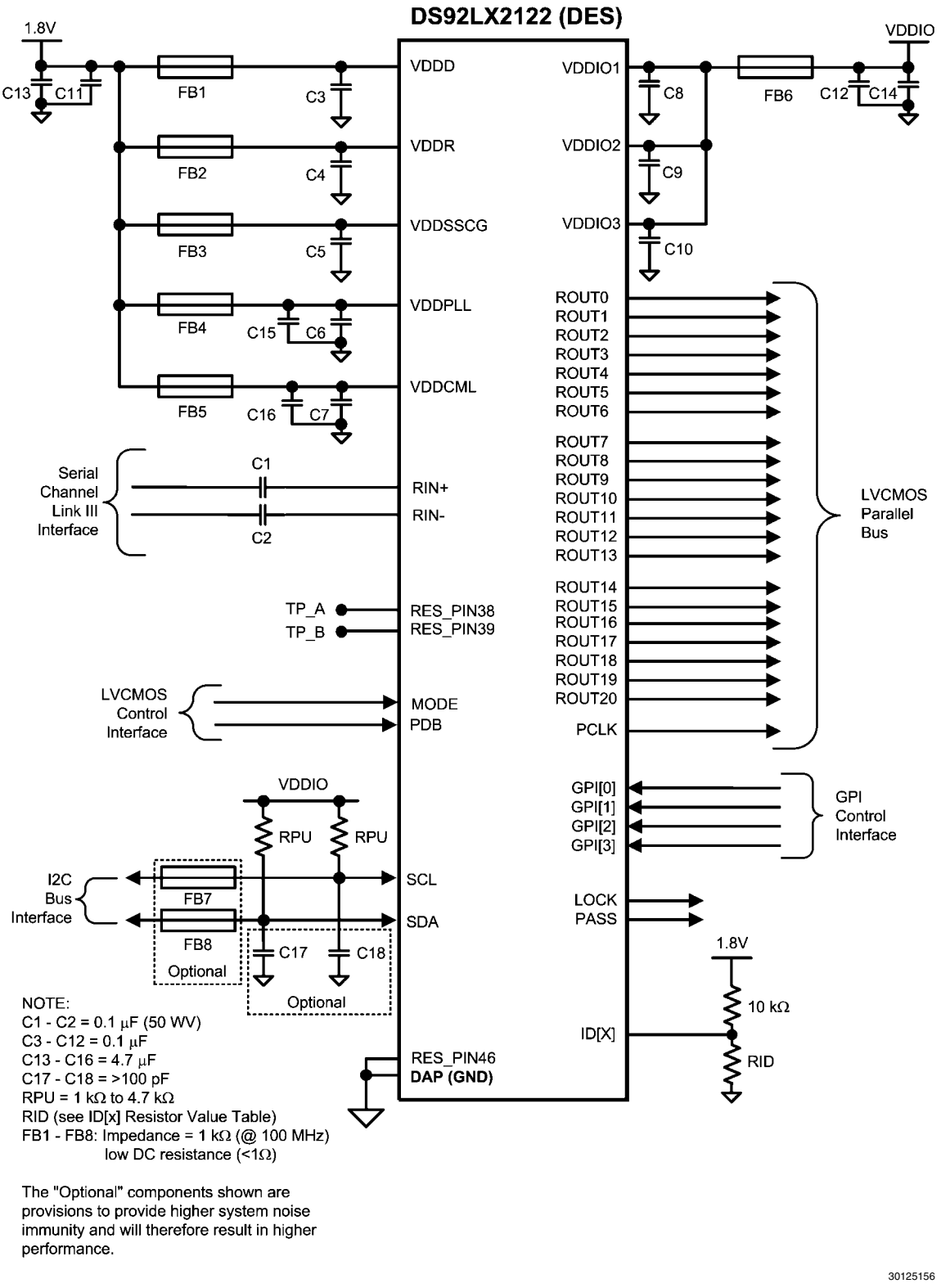


FIGURE 32. DS92LX2122 Typical Connection Diagram

TRANSMISSION MEDIA

The Ser/Des chipset is intended to be used over a wide variety of balanced cables depending on distance and signal quality requirements. The Ser/Des employ internal termination providing a clean signaling environment. The interconnect for Channel Link III interface should present a differential impedance of 100 Ohms. Use of cables and connectors that have matched differential impedance will minimize impedance discontinuities. Shielded or un-shielded cables may be used depending upon the noise environment and application requirements. The chipset's optimum cable drive performance is achieved at 43 MHz at 10 meters length. The maximum signaling rate increases as the cable length decreases. Therefore, the chipset supports 50 MHz at shorter distances. Other cable parameters that may limit the cable's performance boundaries are: cable attenuation, near-end crosstalk and pair-to-pair skew.

For obtaining optimal performance the system should use:

- Shielded Twisted Pair (STP) cable
- 100Ω differential impedance and 24 AWG (or lower AWG) cable
- Low skew, impedance matched
- Terminate unused conductors

PCB LAYOUT AND POWER SYSTEM CONSIDERATIONS

Circuit board layout and stack-up for the Ser/Des devices should be designed to provide low-noise power feed to the device. Good layout practice will also separate high frequency or high-level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mils) for power / ground sandwiches. This arrangement provides plane capacitance for the PCB power system with low-inductance parasitics, which has proven especially effective at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range of 0.01 uF to 0.1 uF. Tantalum capacitors may be in the 2.2 uF to 10 uF range. Voltage rating of the tantalum capacitors should be at least 5X the power supply voltage being used.

Surface mount capacitors are recommended due to their smaller parasitics. When using multiple capacitors per supply pin, locate the smaller value closer to the pin. A large bulk capacitor is recommend at the point of power entry. This is typically in the 50uF to 100uF range and will smooth low frequency switching noise. It is recommended to connect power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with via on both ends of the capacitor. Connecting power or ground pins to an external bypass capacitor will increase the inductance of the path.

A small body size X7R chip capacitor, such as 0603, is recommended for external bypass. Its small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20-30 MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency.

Some devices provide separate power for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin Description tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter many be used to provide clean power to sensitive circuits such as PLLs.

Use at least a four layer board with a power and ground plane. Locate LVCMOS signals away from the differential lines to prevent coupling from the LVCMOS lines to the differential lines. Closely-coupled differential lines of 100 Ohms are typically recommended for differential interconnect. The closely coupled lines help to ensure that coupled noise will appear as common-mode and thus is rejected by the receivers. The tightly coupled lines will also radiate less.

Information on the LLP style package is provided in National Application Note: AN-1187.

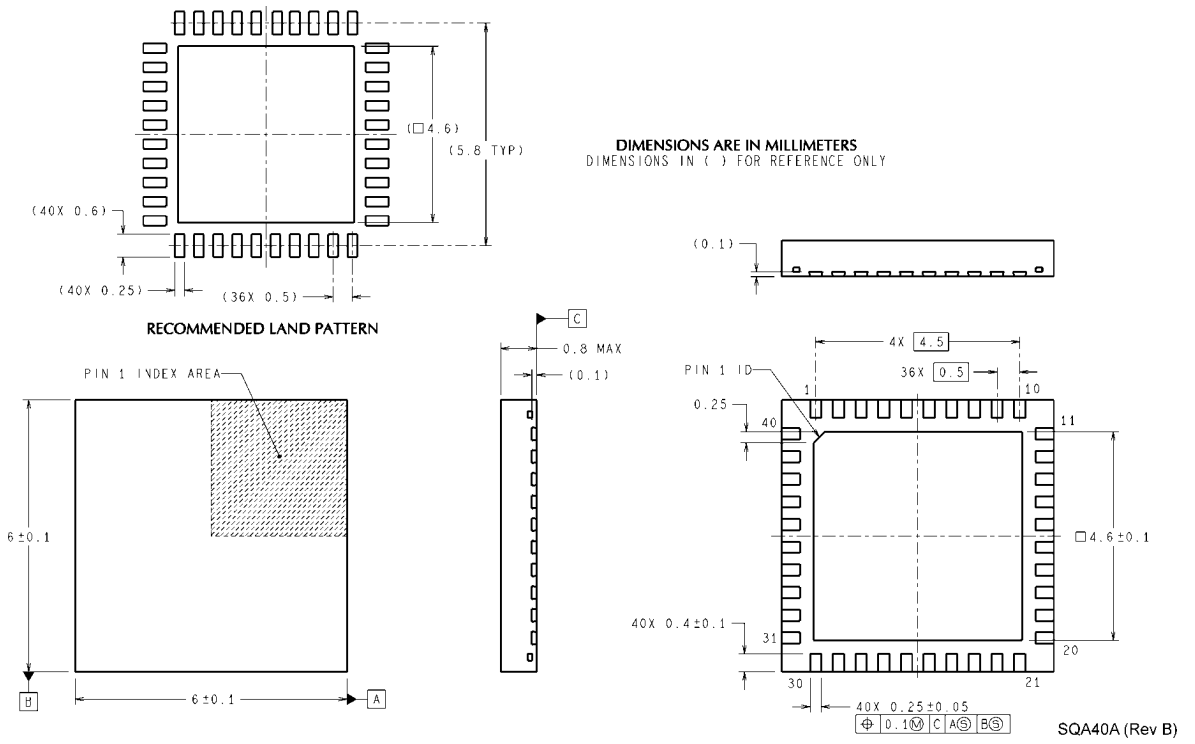
INTERCONNECT GUIDELINES

See AN-1108 and AN-905 for full details.

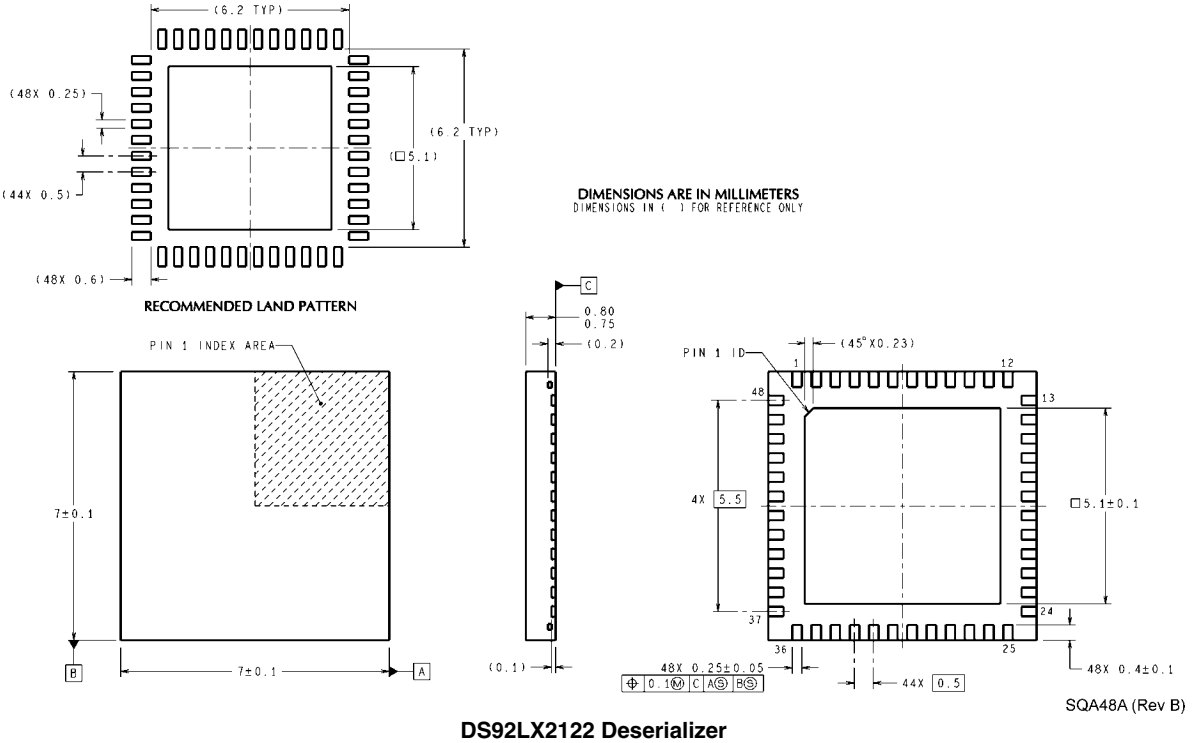
- Use 100Ω coupled differential pairs
- Use the S/2S/3S rule in spacings
  - S = space between the pair
  - 2S = space between pairs
  - 3S = space to LVCMOS signal
- Minimize the number of Vias
- Use differential connectors when operating above 500Mbps line speed
- Maintain balance of the traces
- Minimize skew within the pair

Additional general guidance can be found in the LVDS Owner's Manual - available in PDF format from the National web site at: www.national.com/lvds

Physical Dimensions inches (millimeters) unless otherwise noted



DS92LX2121 Serializer
NS Package Number SQA40A



DS92LX2122 Deserializer
NS Package Number SQA48A

Notes

For more National Semiconductor product information and proven design tools, visit the following Web sites at: www.national.com

Products		Design Support	
Amplifiers	www.national.com/amplifiers	WEBENCH® Tools	www.national.com/webench
Audio	www.national.com/audio	App Notes	www.national.com/appnotes
Clock and Timing	www.national.com/timing	Reference Designs	www.national.com/refdesigns
Data Converters	www.national.com/adc	Samples	www.national.com/samples
Interface	www.national.com/interface	Eval Boards	www.national.com/evalboards
LVDS	www.national.com/lvds	Packaging	www.national.com/packaging
Power Management	www.national.com/power	Green Compliance	www.national.com/quality/green
Switching Regulators	www.national.com/switchers	Distributors	www.national.com/contacts
LDOs	www.national.com/ldo	Quality and Reliability	www.national.com/quality
LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback
Voltage References	www.national.com/vref	Design Made Easy	www.national.com/easy
PowerWise® Solutions	www.national.com/powerwise	Applications & Markets	www.national.com/solutions
Serial Digital Interface (SDI)	www.national.com/sdi	Mil/Aero	www.national.com/milaero
Temperature Sensors	www.national.com/tempsensors	SolarMagic™	www.national.com/solarmagic
PLL/VCO	www.national.com/wireless	PowerWise® Design University	www.national.com/training

National Semiconductor Americas Technical Support Center
Email: support@nsc.com
Tel: 1-800-272-9959

National Semiconductor Europe Technical Support Center
Email: europe.support@nsc.com

National Semiconductor Asia Pacific Technical Support Center
Email: ap.support@nsc.com

National Semiconductor Japan Technical Support Center
Email: jpn.feedback@nsc.com