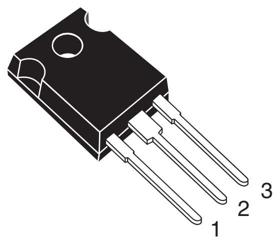
STW88N65M5

N-channel 650 V, 0.024 Ω, 84 A, MDmesh™ V Power MOSFET in TO-247

Features

Order code	V_{DSS} @$T_{jmax.}$	$R_{DS(on)}$ max.	I_D
STW88N65M5	710 V	< 0.029 Ω	84 A

- Worldwide best $R_{DS(on)}$ in TO-247
- Higher V_{DSS} rating
- Higher dv/dt capability
- Excellent switching performance
- Easy to drive
- 100% avalanche tested



TO-247

Applications

- High efficiency switching applications: servers, PV inverters, telecom infrastructure, multi kW battery chargers.

Description

This device is a N-channel MDmesh™ V Power MOSFET based on an innovative proprietary vertical process technology, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

Figure 1. Internal schematic diagram

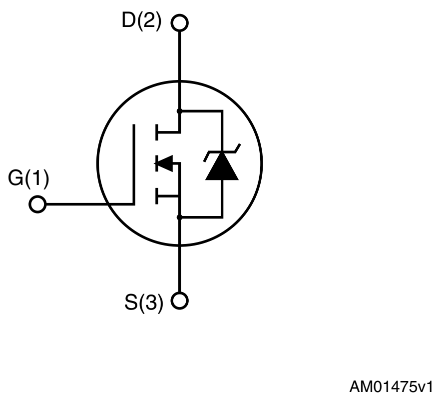


Table 1. Device summary

Order code	Marking	Package	Packaging
STW88N65M5	88N65M5	TO-247	Tube

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate- source voltage	25	V
I_D	Drain current (continuous) at T_C = 25 °C	84	A
I_D	Drain current (continuous) at T_C = 100 °C	50.5	A
I_{DM} (1)	Drain current (pulsed)	336	A
P_{TOT}	Total dissipation at T_C = 25 °C	450	W
I_{AR}	Max current during repetitive or single pulse avalanche (pulse width limited by T_{JMAX})	15	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	2000	mJ
dv/dt (2)	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature	- 55 to 150	°C
T_j	Max. operating junction temperature	150	°C

1. Pulse width limited by safe operating area
2. $I_{SD} \leq$ 84 A, di/dt = 400 A/µs, peak $V_{DS} < V_{(BR)DSS}$, V_{DD} = 400 V

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.28	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient max	50	°C/W
T_l	Maximum lead temperature for soldering purpose	300	°C

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	650			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 650 V V_{DS} = 650 V, T_C=125 °C			1 100	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 25 V			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 42 A		0.024	0.029	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0	-	8825 223 11	-	pF pF pF
$C_{o(tr)}$(1)	Equivalent capacitance time related	V_{GS} = 0, V_{DS} = 0 to 520 V	-	778	-	pF
$C_{o(er)}$(2)	Equivalent capacitance energy related	V_{GS} = 0, V_{DS} = 0 to 520 V	-	202	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	1.79	-	Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 520 V, I_D = 42 A, V_{GS} = 10 V (see *Figure 16*)	-	204 51 84	-	nC nC nC

1. $C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
2. $C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(V)}$ $t_{r(V)}$ $t_{f(i)}$ $t_{c(off)}$	Voltage delay time Voltage rise time Current fall time Crossing time	V_{DD} = 400 V, I_D = 56 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 17*) (see *Figure 20*)	-	141 16 29 56	-	ns ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)		-		84 336	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 84 A, V_{GS} = 0	-		1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 84 A, di/dt = 100 A/µs V_{DD} = 100 V (see *Figure 17*)	-	544 14 50		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 84 A, di/dt = 100 A/µs V_{DD} = 100 V, T_j = 150 °C (see *Figure 17*)	-	660 20 60		ns µC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

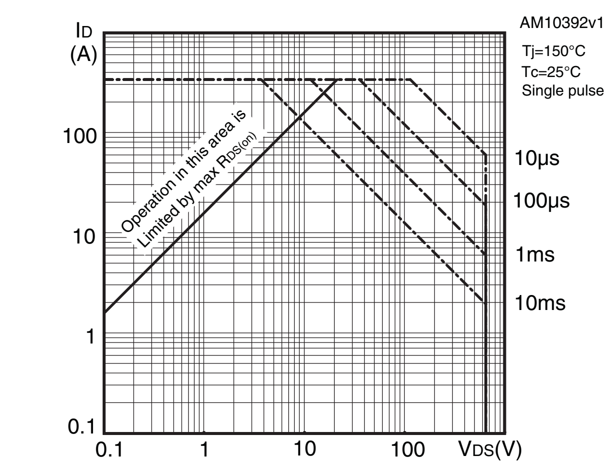


Figure 3. Thermal impedance

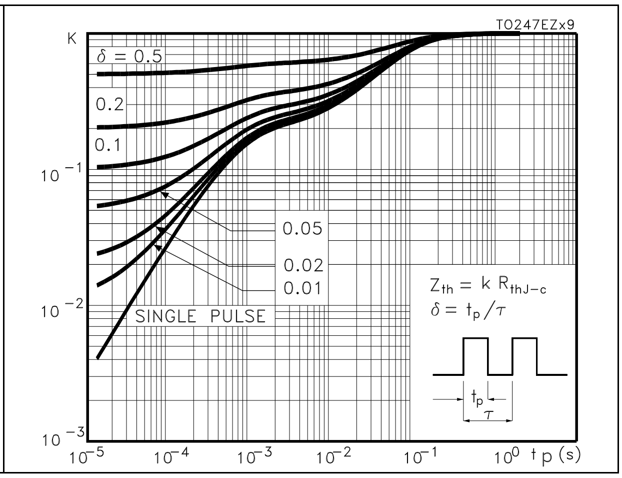


Figure 4. Output characteristics

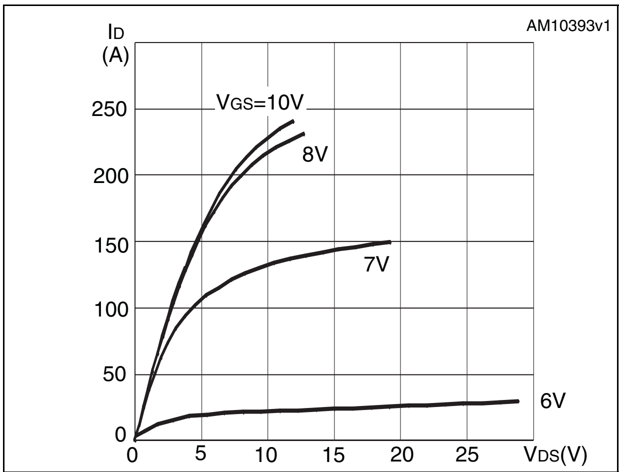


Figure 5. Transfer characteristics

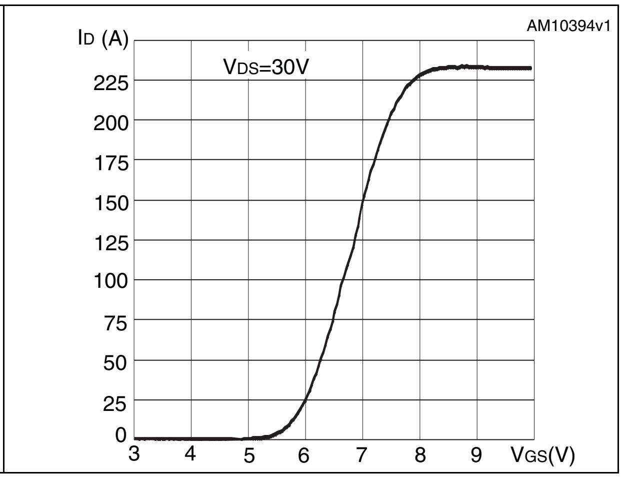


Figure 6. Gate charge vs gate-source voltage

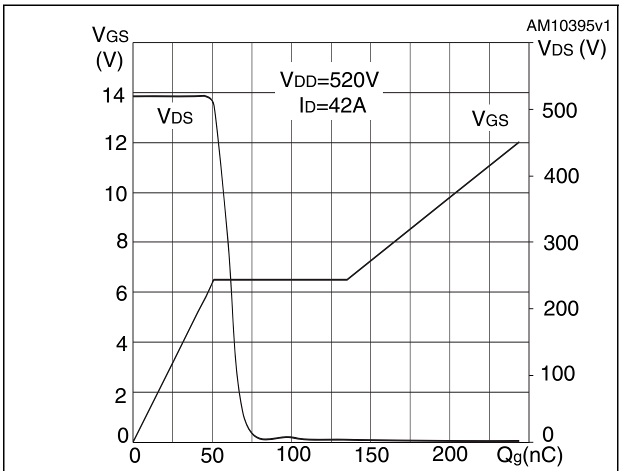


Figure 7. Static drain-source on resistance

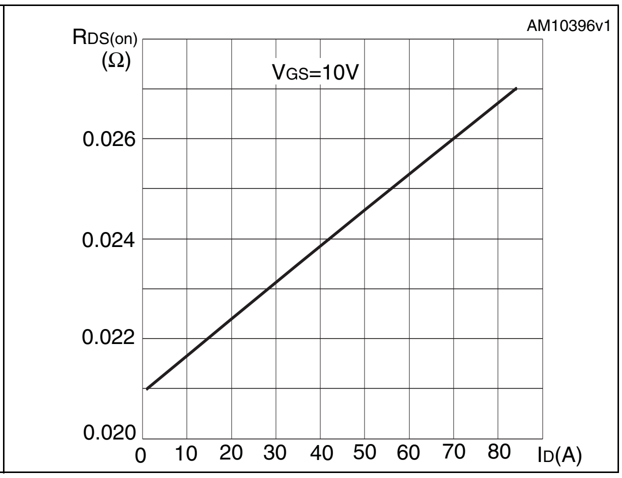


Figure 8. Capacitance variations

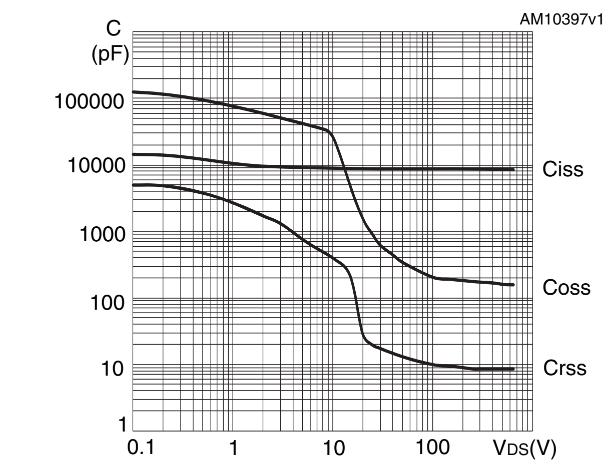


Figure 9. Output capacitance stored energy

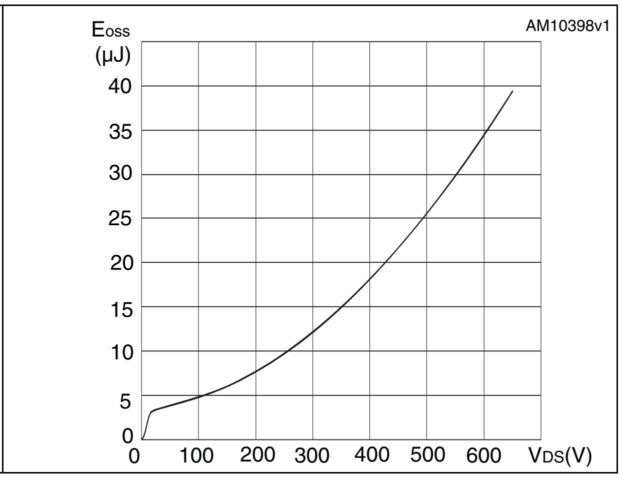


Figure 10. Normalized gate threshold voltage vs temperature

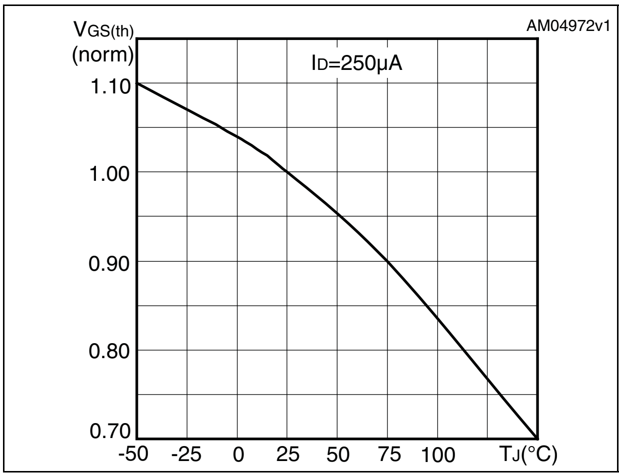


Figure 11. Normalized on resistance vs temperature

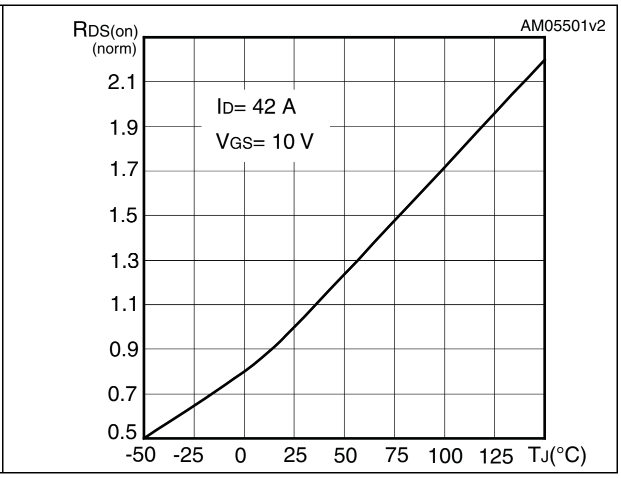


Figure 12. Source-drain diode forward characteristics

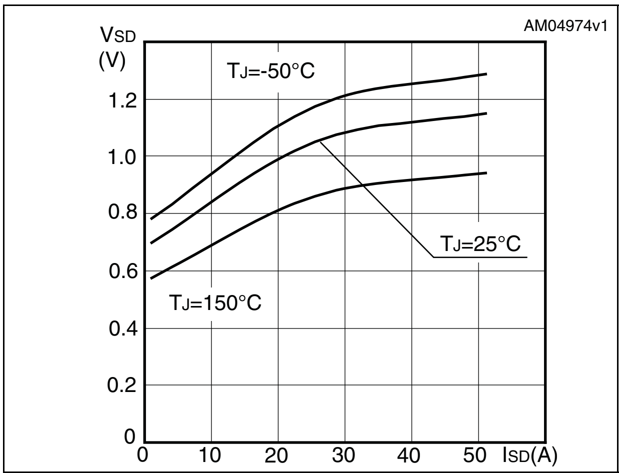


Figure 13. Normalized V_{DS} vs temperature

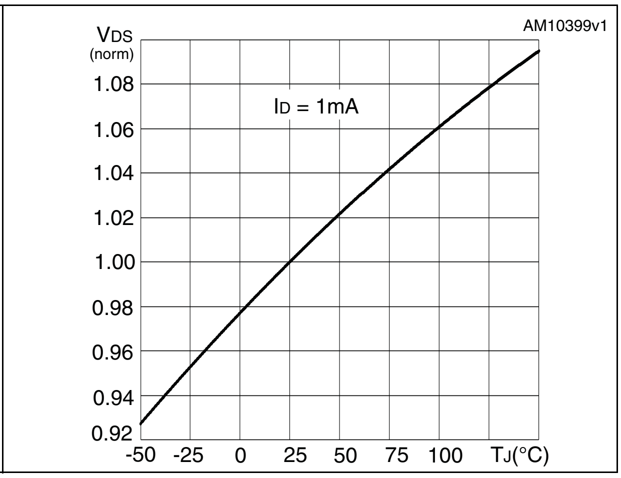
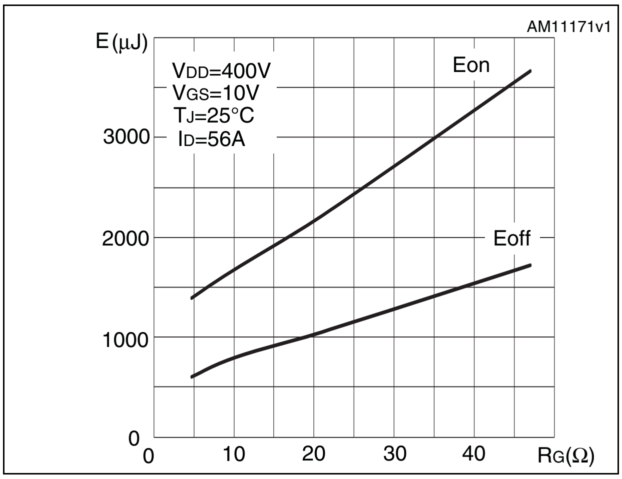


Figure 14. Switching losses vs gate resistance (1)



1. Eon including reverse recovery of a SiC diode

3 Test circuits

Figure 15. Switching times test circuit for resistive load

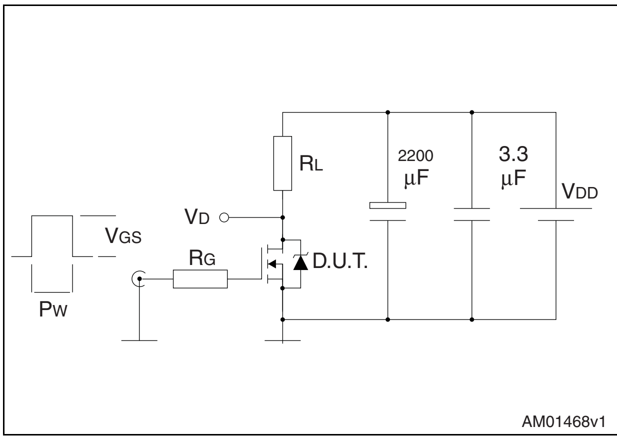


Figure 16. Gate charge test circuit

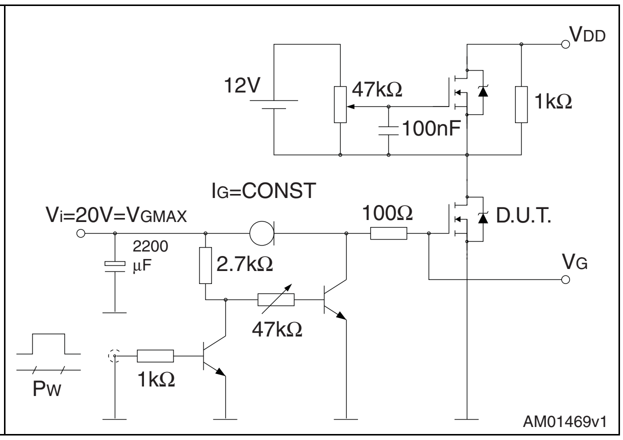


Figure 17. Test circuit for inductive load switching and diode recovery times

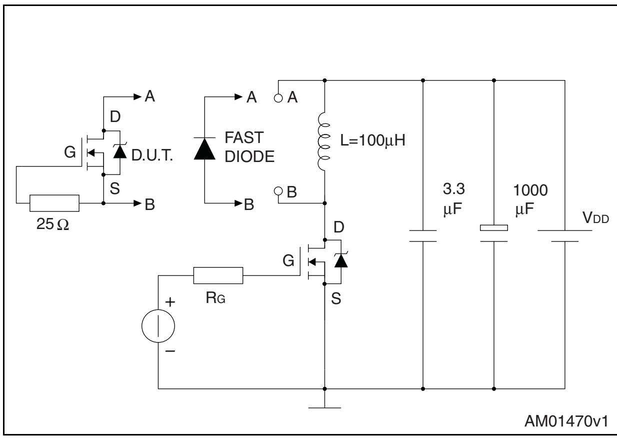


Figure 18. Unclamped inductive load test circuit

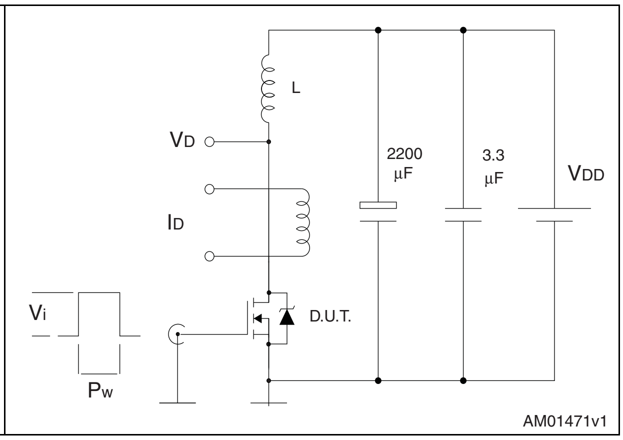


Figure 19. Unclamped inductive waveform

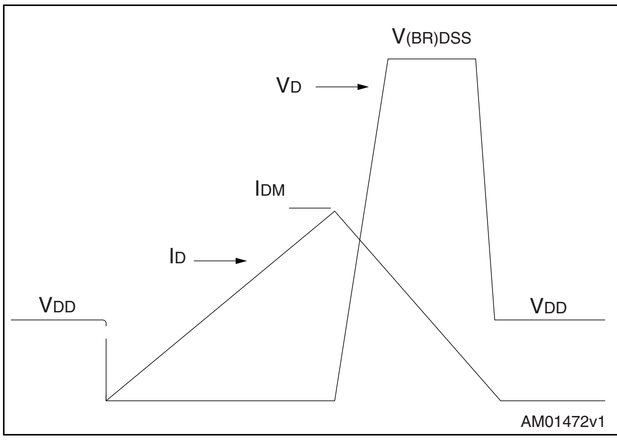
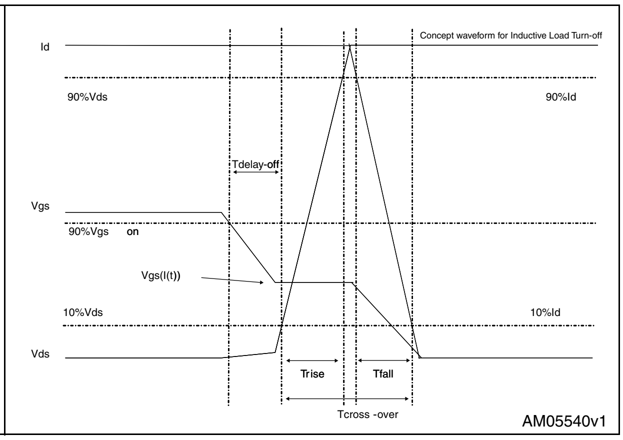


Figure 20. Switching time waveform



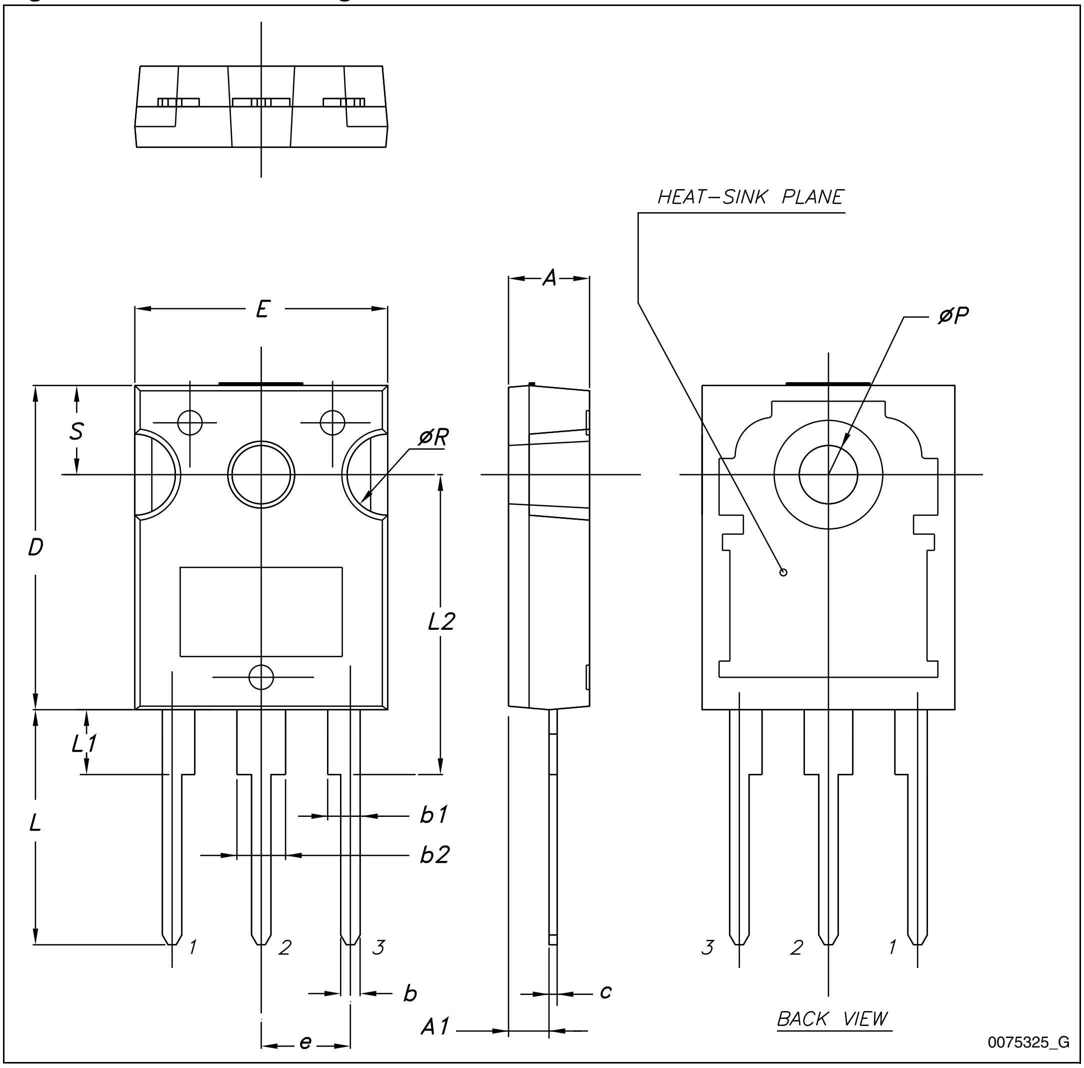
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. TO-247 mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
∅P	3.55		3.65
∅R	4.50		5.50
S	5.30	5.50	5.70

Figure 21. TO-247 drawing



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
23-Nov-2011	1	First release.
09-Dec-2011	2	Document status promoted from preliminary data to datasheet.