Concerto Microcontrollers

1 F28M35x (Concerto™) MCUs

1.1 Features

- **Master Subsystem — ARM® Cortex™-M3**
  - **100 MHz**
  - **Embedded Memory**
    - **Up to 512KB Flash (ECC)**
    - **Up to 32KB RAM (ECC/Parity)**
    - **Up to 64KB Shared RAM**
    - **2KB IPC Message RAM**
  - **5 Universal Asynchronous Receiver/Transmitters (UARTs)**
  - **4 Synchronous Serial Interfaces (SSIs)/ Serial Peripheral Interface (SPI)**
  - **2 Inter-integrated Circuits (I2Cs)**
  - **Universal Serial Bus On-the-Go (USB-OTG) + PHY**
  - **10/100 ENET 1588 MII**
  - **2 Controller Area Networks (CANs)**
  - **32-Channel Direct Memory Access (µDMA)**
  - **Dual Security Zones (128-Bit Password per Zone)**
  - **External Peripheral Interface (EPI)**
  - **Micro Cyclic Redundancy Check (µCRC) Module**
  - **4 General-Purpose Timers**
  - **2 Watchdog Timer Modules**
  - **Endianness: Little Endian**
- **Clocking**
  - **On-chip Crystal Oscillator/External Clock Input**
  - **Dynamic PLL Ratio Changes Supported**
- **1.2-V Digital, 1.8-V Analog, 3.3-V I/O Design**
- **Interprocessor Communications (IPC)**
  - **32 Handshaking Channels**
  - **4 Channels Generate IPC Interrupts**
  - **Can be Used to Coordinate Transfer of Data Through IPC Message RAMs**
- **Up to 74 Individually Programmable, Multiplexed GPIO Pins**
- **Control Subsystem — TMS320C28x™ 32-Bit CPU**
  - **150 MHz**
  - **Embedded Memory**
    - **Up to 512KB Flash (ECC)**
    - **Up to 36KB RAM (ECC/Parity)**
    - **Up to 64KB Shared RAM**
    - **2KB IPC Message RAM**
  - **IEEE-754 Single-Precision Floating-Point Unit (FPU)**
  - **Viterbi, Complex Math, CRC Unit (VCU)**
  - **Serial Communications Interface (SCI)**
  - **Serial Peripheral Interface (SPI)**
  - **Inter-integrated Circuit (I2C)**
  - **6-Channel Direct Memory Access (DMA)**
  - **9 Enhanced Pulse Width Modulator (ePWM) Modules**
    - **18 Outputs (16 High-Resolution)**
  - **6 32-Bit Enhanced Capture (eCAP) Modules**
  - **3 32-Bit Enhanced Quadrature Encoder (eQEP) Modules**
  - **Multi-Channel Buffered Serial Port (McBSP)**
  - **One Security Zone (128-Bit Password)**
  - **3 32-Bit Timers**
  - **Endianness: Little Endian**
- **Analog Subsystem**
  - **Dual 12-Bit Analog-to-Digital Converters (ADCs)**
  - **Up to 2.88 MSPS**
  - **Up to 20 Channels**
  - **4 Sample-and-Hold (S/H) Circuits**
  - **Up to 6 Comparators With 10-Bit Digital-to-Analog Converter (DAC)**
  - **On-chip Temperature Sensor**
- **Package**
  - **144-Pin RFP PowerPAD™ Thermally Enhanced Thin Quad Flatpack (HTQFP)**

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1.2 Description

The Concerto™ family is a multi-core system-on-chip microcontroller (MCU) with independent communication and real-time control subsystems. The F28M35x is the first series in the Concerto family.

The communications subsystem is based on the industry-standard 32-bit ARM® Cortex™-M3 CPU and features a wide variety of communication peripherals, including Ethernet 1588, USB OTG with PHY, CAN, UART, SSI, I2C, and an external interface.

The real-time control subsystem is based on TI's industry-leading proprietary 32-bit C28x™ Floating-Point CPU and features the most flexible and high-precision control peripherals, including ePWMs with fault protection, and encoders and captures—all as implemented by TI's C2000™ Piccolo™ and Delfino™ families. In addition, the C28-CPU has been enhanced with the addition of the Viterbi, Complex Math, CRC Unit (VCU) instruction accelerator that implements efficient Viterbi, Complex Arithmetic, 16-bit FFTs and CRC algorithms.

A high-speed analog subsystem and supplementary RAM memory is shared, along with on-chip voltage regulation and redundant clocking circuitry. Safety considerations also include Error Correction Code (ECC), Parity, and Code Secure Memory, as well as documentation to assist with system-level industrial safety certification.

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1.3 Functional Block Diagram

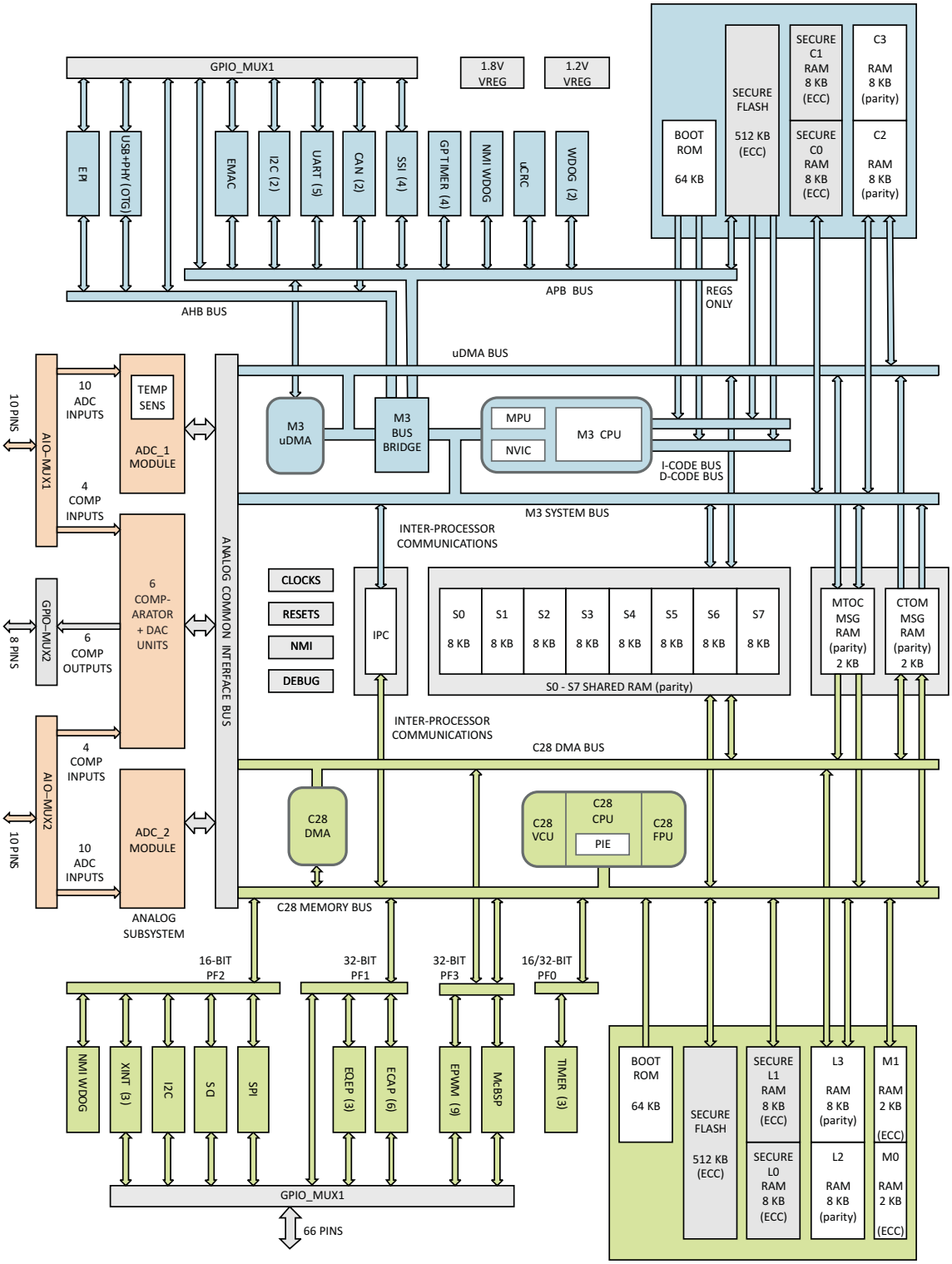

Figure 1-1. Functional Block Diagram

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

This data sheet revision history highlights the technical changes made to the ***SPRS742A*** device-specific data sheet to make it an ***SPRS742B*** revision.

Scope: Added Section 4.1, Absolute Maximum Ratings.
Added Section 4.2, Recommended Operating Conditions.
Added Section 4.3, Electrical Characteristics.
Restructured Section 2, Device Overview.
Added Section 6, Device and Documentation Support.
See table below.

LOCATION	ADDITIONS, DELETIONS, AND MODIFICATIONS
Section 1.1	Features: • Master Subsystem — ARM® Cortex™-M3: – Changed "Universal Serial Bus On-the-Go (USB-**OTB**) + PHY" to "Universal Serial Bus On-the-Go (USB-**OTG**) + PHY" – Added "Endianness: Little Endian" • Control Subsystem — TMS320C28x™ 32-Bit CPU: – Embedded Memory: • Added "Up to 64KB Shared RAM" – Added "Endianness: Little Endian"
Figure 1-1	Updated "Functional Block Diagram"
Section 2	Device Overview: • Added NOTE about color-coding
Table 2-1	Hardware Features: • "Product status" row: Changed "TMX" to "**x**F28M35..." • Updated footnote about product status
Table 2-8	Control Subsystem Flash, ECC, OTP, Boot ROM: • Sector N: Added "(not available for 256KB Flash configuration)" • Sector M: Added "(not available for 256KB Flash configuration)" • Sector L: Added "(not available for 256KB Flash configuration)" • Sector K: Added "(not available for 256KB Flash configuration)" • Sector J: Added "(not available for 256KB Flash configuration)" • Sector I: Added "(not available for 256KB Flash configuration)" • Sector H: Added "(not available for 256KB Flash configuration)"
Table 2-9	Master Subsystem Flash, ECC, OTP, Boot ROM: • Sector I: Added "(not available for 256KB Flash configuration)" • Sector H: Added "(not available for 256KB Flash configuration)" • Sector G: Added "(not available for 256KB Flash configuration)" • Sector F: Added "(not available for 256KB Flash configuration)"
Table 2-11	Master Subsystem Peripherals: • 4000 1000 – 4000 1FFF: Added "Watchdog Timer 1 Registers" • 400F B900 – 400F B93F: Added "0000 0880 – 0000 0890 (Read Only)" in "C Address (x16 Aligned)" column
Section 2.3.1	Updated "Cortex™-M3 CPU" section
Figure 2-1	Updated "Master Subsystem" figure
Section 2.3.3	Added "Cortex™-M3 Interrupts" section
Section 2.3.4	Added "Cortex™-M3 Vector Table" section
Section 2.3.5	Updated "Cortex™-M3 Local Peripherals" section
Section 2.3.7	Updated "Cortex™-M3 Accessing Shared Resources and Analog Peripherals" section
Figure 2-2	Updated "Control Subsystem" figure
Table 2-16	Added "PIE Peripheral Interrupts" table

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LOCATION	ADDITIONS, DELETIONS, AND MODIFICATIONS
Section 2.4.4	Updated "C28x Local Peripherals" section
Section 2.4.6	Updated "C28x Accessing Shared Resources and Analog Peripherals" section
Section 2.5	Updated "Analog Subsystem" section
Section 2.5.1	Updated "ADC1" section
Section 2.5.2	Updated "ADC2" section
Figure 2-3	Updated "Analog Subsystem" figure
Section 2.5.3	Updated "Analog Comparator + DAC" section
Section 2.5.4	Updated "Analog Common Interface Bus (ACIB)" section
Section 2.6	Updated "Master Subsystem NMIs" section
Section 2.7	Updated "Control Subsystem NMIs" section
Figure 2-4	Updated "Cortex™-M3 NMI and C28x NMI" figure
Section 2.8	Updated "Resets" section
Section 2.8.1	Updated "Cortex™-M3 Resets" section
Figure 2-5	Updated "Resets" figure
Section 2.8.4	Added "Device Boot Sequence" section
Section 2.9	Updated "Master Subsystem Clocking" section
Table 2-19	Added "Master Subsystem Low-Power Modes" table
Figure 2-6	Updated "Cortex™-M3 Clocks and Low-Power Modes" figure
Section 2.9.1	Updated "Cortex™-M3 Run Mode" section
Section 2.9.2	Updated "Cortex™-M3 Sleep Mode" section
Section 2.9.3	Updated "Cortex™-M3 Deep Sleep Mode" section
Section 2.10	Updated "Control Subsystem Clocking" section
Table 2-20	Added "Control Subsystem Low-Power Modes" table
Figure 2-7	Updated "C28x Clocks and Low-Power Modes" figure
Section 2.10.1	Updated "C28x Normal Mode" section
Section 2.10.3	Updated "C28x Standby Mode" section
Section 2.11	Updated "Analog Subsystem Clocking" section
Section 2.12	Added "Shared Resources Clocking" section
Section 2.13	Changed section title from "GPIOs" to "GPIOs and Other Pins"
Section 2.13	Updated "GPIOs and Other Pins" section
Section 2.13.1	Updated "GPIO_MUX1" section
Figure 2-8	Updated "GPIOs and Other Pins" figure
Figure 2-9	Added "GPIO_MUX1 Block" figure
Figure 2-10	Added "GPIO_MUX1 Pin Mapping Through Register Set A" figure
Table 2-21	Added "GPIO_MUX1 Pin Assignments (M3 Primary Modes)" table
Table 2-22	Added "GPIO_MUX1 Pin Assignments (M3 Alternate Modes)" table
Table 2-23	Added "GPIO_MUX1 Pin Assignments (C28x Peripheral Modes)" table
Section 2.13.2	Updated "GPIO_MUX2" section
Table 2-24	Added "GPIO_MUX2 Pin Assignments (C28x Peripheral Modes)" table
Figure 2-11	Added "Pin Muxing on AIO_MUX1, AIO_MUX2, and GPIO_MUX2" figure
Section 2.13.3	Updated "AIO_MUX1" section
Table 2-25	Added "AIO_MUX1 Pin Assignments (C28x AIO Modes)" table
Section 2.13.4	Updated "AIO_MUX2" section
Table 2-26	Added "AIO_MUX2 Pin Assignments (C28x AIO Modes)" table
Figure 3-1	144-Pin RFP PowerPAD™ HTQFP (Top View): • Pin 135: Changed signal name from "ADC2V_{REFLO}" to "ADC2V_{REFLO}, V_{SSA2}"

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LOCATION	ADDITIONS, DELETIONS, AND MODIFICATIONS
Table 3-1	Terminal Functions: • Pin 118, ADC1V_{REFLO}, V_{SSA1}: Added "ADC1 Ground" to DESCRIPTION • Pin 135: Changed signal name from "ADC2V_{REFLO}" to "ADC2V_{REFLO}, V_{SSA2}" • Pin 135, ADC2V_{REFLO}, V_{SSA2}: Added "ADC2 Ground" to DESCRIPTION • Pin 23: Removed M_OFSD2N • Pin 104: Removed M_IID • Pin 103: Removed M_ISESSEND • Pin 82: Removed M_IAVALID • Pin 81: Removed M_IVBUSVALID. Added BOOT_2. • Pin 48: Removed M_IXRCV • Pin 51: Removed M_IDM • Pin 69: Removed M_IDP • Pin 50: Removed M_ODISCHRGVBUS • Pin 71: Removed M_OCHRGVBUS • Pin 78: – Removed M_ODMPULLDN – Added BOOT_0 • Pin 72: Removed M_OLSD2N • Pin 70: Removed M_OLSD1N • Pin 52: – Removed M_OIDPULLUP – Added BOOT_1 • Pin 41: Removed M_OSPEED • Pin 42: Removed M_OSUSPEND • Pin 36: Removed M_OOE • Pin 35: Removed M_ODMSE0 • Pin 46: Removed M_ODPDAT • Added "Boot Pins" group • Changed "FLASH" pin group heading to "Test Pins" • Added footnote about color-coding • Added footnote about output from the Concerto ePWM
Section 4	Added "Device Operating Conditions" section
Section 4.1	Added "Absolute Maximum Ratings" section
Section 4.2	Added "Recommended Operating Conditions" section
Section 4.3	Added "Electrical Characteristics" section
Section 5	Changed section title from "Peripheral and Electrical Specifications" to "Peripheral Information and Timings"
Section 5.1	Added "Master Subsystem Peripherals" section
Section 5.2	Added "Control Subsystem Peripherals" section
Figure 5-1	Added "ePWM, eQEP, eCAP" figure
Figure 5-2	Added "ePWM/HRPWM" figure
Section 5.3	Added "Analog/Shared Peripherals" section
Figure 5-3	Added "ADC" figure
Figure 5-4	Added "Comparator + DAC Units" figure
Figure 5-5	Added "Interprocessor Communications (IPC)" figure
Table 5-1	Updated "F28M35Hx Current Consumption at 150-MHz C28x SYSCLKOUT and 75-MHz M3SSCLK" table
Section 5.5	Added "Power Sequencing" section
Section 5.5.1	Added "Power Management and Supervisory Circuit Solutions" section
Table 5-2	Added "Power Management and Supervisory Circuit Solutions" table
Section 6	Added "Device and Documentation Support" section

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2 Device Overview

The Concerto™ microcontroller (MCU) comprises three subsystems: the Master Subsystem, the Control Subsystem, and the Analog Subsystem. While the Master and Control Subsystem each have dedicated local memories and peripherals, they can also share data and events through shared memories and peripherals. The Analog Subsystem has two ADC converters and six Analog Comparators. Both the Master and Control Subsystems access the Analog Subsystem through the Analog Common Interface Bus (ACIB). The NMI Blocks force communication of critical events to the Master and Control Subsystem processors and their Watchdog Timers. The Reset Block responds to Watchdog Timer NMI Reset, External Reset, and other events to initialize subsystem processors and the rest of the chip to a known state. The Clocking Blocks support multiple low-power modes where clocks to the processors and peripherals can be slowed down or stopped in order to manage power consumption.

NOTE

Throughout this document, the Master Subsystem is denoted by the color "blue"; the Control Subsystem is denoted by the color "green"; and the Analog Subsystem is denoted by the color "orange".

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2.1 Device Characteristics

Table 2-1 lists the features of the F28M35Hx devices.

Table 2-1. Hardware Features

FEATURE	TYPE(1)	H20B1	H20C1	H22B1	H22C1	H32B1	H32C1	H50B1	H50C1	H52B1	H52C1
Master Subsystem — ARM® Cortex™-M3											
Speed (MHz)	–	100(2)	100(2)	100(2)	100(2)	100(2)	100(2)	100(2)	100(2)	100(2)	100(2)
Flash (KB)	–	256	256	256	256	256	512	512	512	512	512
RAM ECC (KB)	–	16	16	16	16	16	16	16	16	16	16
RAM Parity (KB)	–	16	16	16	16	16	16	16	16	16	16
IPC Message RAM Parity (KB)	–	2	2	2	2	2	2	2	2	2	2
Security Zones	–	2	2	2	2	2	2	2	2	2	2
10/100 ENET 1588 MII	0	No	Yes	No	Yes	No	Yes	No	Yes	No	Yes
USB OTG FS	0	No	Yes	No	Yes	No	Yes	No	Yes	No	Yes
Synchronous Serial Interface (SSI)/ Serial Peripheral Interface (SPI)	0	4	4	4	4	4	4	4	4	4	4
Universal Asynchronous Receiver/Transmitter (UART)	0	5	5	5	5	5	5	5	5	5	5
Inter-integrated circuit (I2C)	0	2	2	2	2	2	2	2	2	2	2
Controller Area Network (CAN)	0	2	2	2	2	2	2	2	2	2	2
Direct Memory Access (µDMA)	0	32-ch	32-ch	32-ch	32-ch	32-ch	32-ch	32-ch	32-ch	32-ch	32-ch
External Peripheral Interface (EPI)	0	1	1	1	1	1	1	1	1	1	1
Micro Cyclic Redundancy Check (µCRC) Module	0	1	1	1	1	1	1	1	1	1	1
General-Purpose Timers	–	4	4	4	4	4	4	4	4	4	4
Watchdog Timer Modules	–	2	2	2	2	2	2	2	2	2	2
Control Subsystem — C28x Floating-Point Unit (FPU)/Viterbi, Complex Math, CRC Unit (VCU)											
Speed (MHz)		150	150	150	150	150	150	150	150	150	150
Flash (KB)		256	256	256	256	512	256	512	512	512	512
RAM ECC (KB)		20	20	20	20	20	20	20	20	20	20
RAM Parity (KB)		16	16	16	16	16	16	16	16	16	16
IPC Message RAM Parity (KB)		2	2	2	2	2	2	2	2	2	2
Security Zones		1	1	1	1	1	1	1	1	1	1
Enhanced Pulse Width Modulator (ePWM) modules	2	9: 18 outputs									
High-Resolution PWM outputs	2	16 outputs									
Enhanced Capture (eCAP) modules/ PWM outputs	0	6 (32-bit)									
Enhanced Quadrature Encoder (eQEP) modules	0	3 (32-bit)									
Fault Trip Zones	–	12 on any of 64 GPIO pins									

(1) A type change represents a major functional feature difference in a peripheral module. Within a peripheral type, there may be minor differences between devices that do not affect the basic functionality of the module. These device-specific differences are listed in the *TMS320x28xx, 28xxx DSP Peripheral Reference Guide* (literature number SPRU566) and in the peripheral reference guides.

(2) An integer divide ratio must be maintained between the C28x and Cortex™-M3 clock frequencies; thus, when the C28x is configured to run at maximum frequency of 150 MHz, the fastest allowable frequency for the Cortex™-M3 will be 75 MHz.

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Table 2-1. Hardware Features (continued)

FEATURE		TYPE[1]	H20B1	H20C1	H22B1	H22C1	H32B1	H32C1	H50B1	H50C1	H52B1	H52C1
Multi-Channel Buffered Serial Port (McBSP)/ Serial Peripheral Interface (SPI)		1	1	1	1	1	1	1	1	1	1	1
Serial Communications Interface (SCI)		0	1	1	1	1	1	1	1	1	1	1
Serial Peripheral Interface (SPI)		0	1	1	1	1	1	1	1	1	1	1
Inter-integrated circuit (I2C)		0	1	1	1	1	1	1	1	1	1	1
Direct Memory Access (DMA)		0	6-ch	6-ch	6-ch	6-ch	6-ch	6-ch	6-ch	6-ch	6-ch	6-ch
32-Bit Timers		–	3	3	3	3	3	3	3	3	3	3
Shared												
Supplemental RAM (KB)			0	0	64	64	64	64	0	0	64	64
12-Bit ADC 1	MSPS	3	2.88	2.88	2.88	2.88	2.88	2.88	2.88	2.88	2.88	2.88
	Conversion Time		350 ns	350 ns	350 ns	350 ns	350 ns	350 ns	350 ns	350 ns	350 ns	350 ns
	Channels		10	10	10	10	10	10	10	10	10	10
	Temperature Sensor		1	1	1	1	1	1	1	1	1	1
	Sample-and-Hold (S/H)		2	2	2	2	2	2	2	2	2	2
12-Bit ADC 2	MSPS	3	2.88	2.88	2.88	2.88	2.88	2.88	2.88	2.88	2.88	2.88
	Conversion Time		350 ns	350 ns	350 ns	350 ns	350 ns	350 ns	350 ns	350 ns	350 ns	350 ns
	Channels		10	10	10	10	10	10	10	10	10	10
	Sample-and-Hold (S/H)		2	2	2	2	2	2	2	2	2	2
Comparators with Integrated DACs		0	6	6	6	6	6	6	6	6	6	6
Voltage Regulator and Monitor			3.3-V Single Supply (3.3-V/1.2-V recommended for 125ºC)									
Clocking			4–20 MHz input, Clock fail or out-of-specification, 10-MHz/32-kHz Limp Mode									
Additional Safety												
Master Subsystem			2 Watchdogs, NMI Watchdog: CPU, Memory									
Control Subsystem			NMI Watchdog: CPU, Memory									
Shared			Critical Register and I/O Function Lock Protection; RAM Fetch Protection									
Packaging												
Package Type	144-Pin RFP PowerPAD™ HTQFP		Available at Prototype Sampling									
Temperature options	T: –40°C to 105°C	–	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	S: –40°C to 125°C	–	No 125ºC for ENET/USB									
	Q: –40°C to 125°C[3]	–	No 125ºC for ENET/USB									
Product status[4]		–	**x**F28M35...	**x**F28M35...	**x**F28M35...	**x**F28M35...	**x**F28M35...	**x**F28M35...	**x**F28M35...	**x**F28M35...	**x**F28M35...	**x**F28M35...

(3) "Q" refers to Q100 qualification for automotive applications.
(4) The "**x**F28M35..." product status denotes an experimental device that is not necessarily representative of the final device's electrical specifications. See Section 6.1.2, Device Nomenclature, for descriptions of device stages.

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2.2 Memory Maps

Section 2.2.1 shows the Control Subsystem Memory Map. Section 2.2.2 shows the Master Subsystem Memory Map.

2.2.1 Control Subsystem Memory Map

Table 2-2. Control Subsystem M0, M1 RAM

C DMA Access(1)	C Address (x16 Aligned)(1)	Control Subsystem M0, M1 RAM	Size (Bytes)
no	0000 0000 – 0000 03FF	M0 RAM (ECC)	2K
no	0000 0400 – 0000 07FF	M1 RAM (ECC)	2K

(1) The letter "C" refers to the Control Subsystem.

Table 2-3. Control Subsystem Peripheral Frame 0 (Includes Analog)

C DMA Access(1)	C Address (x16 Aligned)(1)	Control Subsystem Peripheral Frame 0 (Includes Analog)	Size (Bytes)
	0000 0800 – 0000 087F	Reserved	
no	0000 0880 – 0000 0890	Control Subsystem Device Configuration Registers (Read Only)	34
	0000 0891 – 0000 0ADF	Reserved	
no	0000 0AE0 – 0000 0AEF	C28x CSM Registers	32
	0000 0AF0 – 0000 0AFF	Reserved	
yes	0000 0B00 – 0000 0B0F	ADC1 Result Registers	32
	0000 0B10 – 0000 0B3F	Reserved	
yes	0000 0B40 – 0000 0B4F	ADC2 Result Registers	32
	0000 0B50 – 0000 0BFF	Reserved	
no	0000 0C00 – 0000 0C07	CPU Timer 0	16
no	0000 0C08 – 0000 0C0F	CPU Timer 1	16
no	0000 0C10 – 0000 0C17	CPU Timer 2	16
	0000 0C18 – 0000 0CDF	Reserved	
no	0000 0CE0 – 0000 0CFF	PIE Registers	64
no	0000 0D00 – 0000 0DFF	PIE Vector Table	512
no	0000 0E00 – 0000 0EFF	PIE Vector Table Copy (Read Only)	512
	0000 0F00 – 0000 0FFF	Reserved	
no	0000 1000 – 0000 11FF	C28x DMA Registers	1K
	0000 1200 – 0000 16FF	Reserved	
no	0000 1700 – 0000 177F	Analog Subsystem Control Registers	256
	0000 1780 – 0000 3FFF	Reserved	

(1) The letter "C" refers to the Control Subsystem.

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Table 2-4. Control Subsystem Peripheral Frame 3

C DMA Access(1)	C Address (x16 Aligned)(1)	Control Subsystem Peripheral Frame 3	Size (Bytes)	M Address (Byte-Aligned)(2)	µDMA Access
no	0000 4000 – 0000 4181	C28x Flash Control Registers	772		
	0000 4182 – 0000 42FF	Reserved			
no	0000 4300 – 0000 4323	C28x Flash ECC Error Log Registers	72		
	0000 4324 – 0000 43FF	Reserved			
no	0000 4400 – 0000 443F	M Clock Control Registers(2)	128	400F B800 – 400F B87F	no
	0000 4440 – 0000 48FF	Reserved			
no	0000 4900 – 0000 497F	RAM Configuration Registers	256	400F B200 – 400F B2FF	no
	0000 4980 – 0000 49FF	Reserved			
no	0000 4A00 – 0000 4A7F	RAM ECC/Parity/Access Error Log Registers	256	400F B300 – 400F B3FF	no
	0000 4A80 – 0000 4DFF	Reserved			
no	0000 4E00 – 0000 4E3F	CtoM and MtoC IPC Registers	128	400F B700 – 400F B77F	no
	0000 4E40 – 0000 4FFF	Reserved			
yes	0000 5000 – 0000 503F	McBSP-A	128		
	0000 5040 – 0000 50FF	Reserved			
yes	0000 5100 – 0000 517F	EPWM1 (Hi-Resolution)	256		
yes	0000 5180 – 0000 51FF	EPWM2 (Hi-Resolution)	256		
yes	0000 5200 – 0000 527F	EPWM3 (Hi-Resolution)	256		
yes	0000 5280 – 0000 52FF	EPWM4 (Hi-Resolution)	256		
yes	0000 5300 – 0000 537F	EPWM5 (Hi-Resolution)	256		
yes	0000 5380 – 0000 53FF	EPWM6 (Hi-Resolution)	256		
yes	0000 5400 – 0000 547F	EPWM7 (Hi-Resolution)	256		
yes	0000 5480 – 0000 54FF	EPWM8 (Hi-Resolution)	256		
yes	0000 5500 – 0000 557F	EPWM9	256		
	0000 5580 – 0000 57FF	Reserved			

(1) The letter "C" refers to the Control Subsystem.
(2) The letter "M" refers to the Master Subsystem.

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Table 2-5. Control Subsystem Peripheral Frame 1

C DMA Access(1)	C Address (x16 Aligned)(1)	Control Subsystem Peripheral Frame 1	Size (Bytes)
	0000 5800 – 0000 59FF	Reserved	
no	0000 5A00 – 0000 5A1F	ECAP1	64
no	0000 5A20 – 0000 5A3F	ECAP2	64
no	0000 5A40 – 0000 5A5F	ECAP3	64
no	0000 5A60 – 0000 5A7F	ECAP4	64
no	0000 5A80 – 0000 5A9F	ECAP5	64
no	0000 5AA0 – 0000 5ABF	ECAP6	64
	0000 5AC0 – 0000 5AFF	Reserved	
no	0000 5B00 – 0000 5B3F	EQEP1	128
no	0000 5B40 – 0000 5B7F	EQEP2	128
no	0000 5B80 – 0000 5BBF	EQEP3	128
	0000 5BC0 – 0000 5F7F	Reserved	
no	0000 5F80 – 0000 5FFF	C GPIO Group 1 Registers(1)	256
	0000 6000 – 0000 63FF	Reserved	
no	0000 6400 – 0000 641F	COMP1 Registers	64
no	0000 6420 – 0000 643F	COMP2 Registers	64
no	0000 6440 – 0000 645F	COMP3 Registers	64
no	0000 6460 – 0000 647F	COMP4 Registers	64
no	0000 6480 – 0000 649F	COMP5 Registers	64
no	0000 64A0 – 0000 64BF	COMP6 Registers	64
	0000 64C0 – 0000 6F7F	Reserved	
no	0000 6F80 – 0000 6FFF	C GPIO Group 2 Registers and AIO Mux Registers(1)	256

(1) The letter "C" refers to the Control Subsystem.

Table 2-6. Control Subsystem Peripheral Frame 2

C DMA Access(1)	C Address (x16 Aligned)(1)	Control Subsystem Peripheral Frame 2	Size (Bytes)
	0000 7000 – 0000 70FF	Reserved	
no	0000 7010 – 0000 702F	C28x System Control Registers	64
	0000 7030 – 0000 703F	Reserved	
no	0000 7040 – 0000 704F	SPI-A	32
no	0000 7050 – 0000 705F	SCI-A	32
no	0000 7060 – 0000 706F	NMI Watchdog Interrupt Registers	32
no	0000 7070 – 0000 707F	External Interrupt Registers	32
	0000 7080 – 0000 70FF	Reserved	
no	0000 7100 – 0000 717F	ADC1 Configuration Registers (Only 16-bit read/write access supported)	256
no	0000 7180 – 0000 71FF	ADC2 Configuration Registers (Only 16-bit read/write access supported)	256
	0000 7200 – 0000 78FF	Reserved	
no	0000 7900 – 0000 793F	I2C-A	128
	0000 7940 – 0000 7FFF	Reserved	

(1) The letter "C" refers to the Control Subsystem.

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Table 2-7. Control Subsystem RAMs

C DMA Access(1)	C Address (x16 Aligned)(1)	Control Subsystem RAMs	Size (Bytes)	M Address (Byte-Aligned)(2)	µDMA Access
no	0000 8000 – 0000 8FFF	L0 RAM (ECC, Secure)	8K		
no	0000 9000 – 0000 9FFF	L1 RAM (ECC, Secure)	8K		
yes	0000 A000 – 0000 AFFF	L2 RAM (Parity, Interleaving)	8K		
yes	0000 B000 – 0000 BFFF	L3 RAM (Parity, Interleaving)	8K		
yes	0000 C000 – 0000 CFFF	S0 RAM (Parity, Shared)	8K	2000 8000 – 2000 9FFF	yes
yes	0000 D000 – 0000 DFFF	S1 RAM (Parity, Shared)	8K	2000 A000 – 2000 BFFF	yes
yes	0000 E000 – 0000 EFFF	S2 RAM (Parity, Shared)	8K	2000 C000 – 2000 DFFF	yes
yes	0000 F000 – 0000 FFFF	S3 RAM (Parity, Shared)	8K	2000 E000 – 2000 FFFF	yes
yes	0001 0000 – 0001 0FFF	S4 RAM (Parity, Shared)	8K	2001 0000 – 2001 1FFF	yes
yes	0001 1000 – 0001 1FFF	S5 RAM (Parity, Shared)	8K	2001 2000 – 2001 3FFF	yes
yes	0001 2000 – 0001 2FFF	S6 RAM (Parity, Shared)	8K	2001 4000 – 2001 5FFF	yes
yes	0001 3000 – 0001 3FFF	S7 RAM (Parity, Shared)	8K	2001 6000 – 2001 7FFF	yes
	0001 4000 – 0003 F7FF	Reserved			
yes	0003 F800 – 0003 FBFF	CtoM MSG RAM (Parity)	2K	2007 F000 – 2007 F7FF	yes read only
yes read only	0003 FC00 – 0003 FFFF	MtoC MSG RAM (Parity)	2K	2007 F800 – 2007 FFFF	yes
	0004 0000 – 0004 7FFF	Reserved			
no	0004 8000 – 0004 8FFF	L0 RAM - ECC Bits	8K		
no	0004 9000 – 0004 9FFF	L1 RAM - ECC Bits	8K		
no	0004 A000 – 0004 AFFF	L2 RAM - Parity Bits	8K		
no	0004 B000 – 0004 BFFF	L3 RAM - Parity Bits	8K		
no	0004 C000 – 0004 CFFF	S0 RAM - Parity Bits	8K	2008 8000 – 2008 9FFF	no
no	0004 D000 – 0004 DFFF	S1 RAM - Parity Bits	8K	2008 A000 – 2008 BFFF	no
no	0004 E000 – 0004 EFFF	S2 RAM - Parity Bits	8K	2008 C000 – 2008 DFFF	no
no	0004 F000 – 0004 FFFF	S3 RAM - Parity Bits	8K	2008 E000 – 2008 FFFF	no
no	0005 0000 – 0005 0FFF	S4 RAM - Parity Bits	8K	2009 0000 – 2009 1FFF	no
no	0005 1000 – 0005 1FFF	S5 RAM - Parity Bits	8K	2009 2000 – 2009 3FFF	no
no	0005 2000 – 0005 2FFF	S6 RAM - Parity Bits	8K	2009 4000 – 2009 5FFF	no
no	0005 3000 – 0005 3FFF	S7 RAM - Parity Bits	8K	2009 6000 – 2009 7FFF	no
no	0005 4000 – 0007 EFFF	Reserved			
no	0007 F000 – 0007 F3FF	M0 RAM - ECC Bits	2K		
no	0007 F400 – 0007 F7FF	M1 RAM - ECC Bits	2K		
no	0007 F800 – 0007 FBFF	CtoM MSG RAM - Parity Bits	2K	200F F000 – 200F F7FF	no
no	0007 FC00 – 0007 FFFF	MtoC MSG RAM - Parity Bits	2K	200F F800 – 200F FFFF	no
	0008 0000 – 0009 FFFF	Reserved			

(1) The letter "C" refers to the Control Subsystem.
(2) The letter "M" refers to the Master Subsystem.

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Table 2-8. Control Subsystem Flash, ECC, OTP, Boot ROM

C DMA Access(1)	C Address (x16 Aligned)(1)	Control Subsystem Flash, ECC, OTP, Boot ROM	Size (Bytes)
no	0010 0000 – 0010 1FFF	Sector N (not available for 256KB Flash configuration)	16K
no	0010 2000 – 0010 3FFF	Sector M (not available for 256KB Flash configuration)	16K
no	0010 4000 – 0010 5FFF	Sector L (not available for 256KB Flash configuration)	16K
no	0010 6000 – 0010 7FFF	Sector K (not available for 256KB Flash configuration)	16K
no	0010 8000 – 0010 FFFF	Sector J (not available for 256KB Flash configuration)	64K
no	0011 0000 – 0011 7FFF	Sector I (not available for 256KB Flash configuration)	64K
no	0011 8000 – 0011 FFFF	Sector H (not available for 256KB Flash configuration)	64K
no	0012 0000 – 0012 7FFF	Sector G	64K
no	0012 8000 – 0012 FFFF	Sector F	64K
no	0013 0000 – 0013 7FFF	Sector E	64K
no	0013 8000 – 0013 9FFF	Sector D	16K
no	0013 A000 – 0013 BFFF	Sector C	16K
no	0013 C000 – 0013 DFFF	Sector B	16K
no	0013 E000 – 0013 FFFF	Sector A (CSM password in the high address)	16K
no	0014 0000 – 001F FFFF	Reserved	
no	0020 0000 – 0020 7FFF	Flash - ECC Bits (1/8 of Flash used = 64 KBytes)	64K
no	0020 8000 – 0024 01FF	Reserved	
no	0024 0200 – 0024 03FF	TI OTP	1K
no	0024 0400 – 003F 7FFF	Reserved	
no	003F 8000 – 003F FFFF	C28x Boot ROM (64 KBytes)	64K

(1) The letter "C" refers to the Control Subsystem.

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2.2.2 Master Subsystem Memory Map

Table 2-9. Master Subsystem Flash, ECC, OTP, Boot ROM

µDMA Access	M Address (Byte-Aligned)(1)	Master Subsystem Flash, ECC, OTP, Boot ROM	Size (Bytes)
no	0000 0000 – 0000 FFFF	Boot ROM - Dual-mapped to 0x0100 0000 (Both maps access same physical location.)	64K
	0001 0000 – 001F FFFF	Reserved	
no	0020 0000 – 0020 3FFF	Sector N (Zone 1 CSM password in the low address.)	16K
no	0020 4000 – 0020 7FFF	Sector M	16K
no	0020 8000 – 0020 BFFF	Sector L	16K
no	0020 C000 – 0020 FFFF	Sector K	16K
no	0021 0000 – 0021 FFFF	Sector J	64K
no	0022 0000 – 0022 FFFF	Sector I (not available for 256KB Flash configuration)	64K
no	0023 0000 – 0023 FFFF	Sector H (not available for 256KB Flash configuration)	64K
no	0024 0000 – 0024 FFFF	Sector G (not available for 256KB Flash configuration)	64K
no	0025 0000 – 0025 FFFF	Sector F (not available for 256KB Flash configuration)	64K
no	0026 0000 – 0026 FFFF	Sector E	64K
no	0027 0000 – 0027 3FFF	Sector D	16K
no	0027 4000 – 0027 7FFF	Sector C	16K
no	0027 8000 – 0027 BFFF	Sector B	16K
no	0027 C000 – 0027 FFFF	Sector A (Zone 2 CSM password in the high address.)	16K
	0028 0000 – 005F FFFF	Reserved	
no	0060 0000 – 0060 FFFF	Flash - ECC Bits (1/8 of Flash used = 64 KBytes)	64K
	0061 0000 – 0068 047F	Reserved	
no	0068 0480 – 0068 07FF	TI OTP	896
no	0068 0800	OTP – Security Lock	4
no	0068 0804	Reserved	
no	0068 0808	Reserved	
no	0068 080C	OTP – Zone 2 Flash Start Address	4
no	0068 0810	OTP – EMAC Address 0	4
no	0068 0814	OTP – EMAC Address 1	4
	0068 0818 – 0070 00FF	Reserved	
no	0070 0100 – 0070 0102	OTP – ECC Bits – Application Use (1/8 of OTP used = 3 Bytes)	3
	0070 0103 – 00FF FFFF	Reserved	
no	0100 0000 – 0100 FFFF	Boot ROM – Dual-mapped to 0x0000 0000 (Both maps access same physical location.)	64K
	0101 0000 – 03FF FFFF	Reserved	
no	0400 0000 – 07FF FFFF	ROM/Flash/OTP/Boot ROM – Mirror-mapped (Read cycles from this space cause the µCRC peripheral to continuously update data checksum inside a register, when reading a block of data.)	64M
	0800 0000 – 1FFF FFFF	Reserved	

(1) The letter "M" refers to the Master Subsystem.

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Table 2-10. Master Subsystem RAMs

µDMA Access	M Address (Byte-Aligned)(1)	Master Subsystem RAMs	Size (Bytes)	C Address (x16 Aligned)(2)	C DMA Access(2)
no	2000 0000 – 2000 1FFF	C0 RAM (ECC, Secure)	8K		
no	2000 2000 – 2000 3FFF	C1 RAM (ECC, Secure)	8K		
yes	2000 4000 – 2000 5FFF	C2 RAM (Parity)	8K		
yes	2000 6000 – 2000 7FFF	C3 RAM (Parity)	8K		
yes	2000 8000 – 2000 9FFF	S0 RAM (Parity, Shared)	8K	0000 C000 – 0000 CFFF	yes
yes	2000 A000 – 2000 BFFF	S1 RAM (Parity, Shared)	8K	0000 D000 – 0000 DFFF	yes
yes	2000 C000 – 2000 DFFF	S2 RAM (Parity, Shared)	8K	0000 E000 – 0000 EFFF	yes
yes	2000 E000 – 2000 FFFF	S3 RAM (Parity, Shared)	8K	0000 F000 – 0000 FFFF	yes
yes	2001 0000 – 2001 1FFF	S4 RAM (Parity, Shared)	8K	0001 0000 – 0001 0FFF	yes
yes	2001 2000 – 2001 3FFF	S5 RAM (Parity, Shared)	8K	0001 1000 – 0001 1FFF	yes
yes	2001 4000 – 2001 5FFF	S6 RAM (Parity, Shared)	8K	0001 2000 – 0001 2FFF	yes
yes	2001 6000 – 2001 7FFF	S7 RAM (Parity, Shared)	8K	0001 3000 – 0001 3FFF	yes
	2001 8000 – 2007 EFFF	Reserved			
yes read only	2007 F000 – 2007 F7FF	CtoM MSG RAM (Parity)	2K	0003 F800 – 0003 FBFF	yes
yes	2007 F800 – 2007 FFFF	MtoC MSG RAM (Parity)	2K	0003 FC00 – 0003 FFFF	yes read only
no	2008 0000 – 2008 1FFF	C0 RAM - ECC Bits	8K		
no	2008 2000 – 2008 3FFF	C1 RAM - ECC Bits	8K		
no	2008 4000 – 2008 5FFF	C2 RAM - Parity Bits	8K		
no	2008 6000 – 2008 7FFF	C3 RAM - Parity Bits	8K		
no	2008 8000 – 2008 9FFF	S0 RAM - Parity Bits	8K	0004 C000 – 0004 CFFF	no
no	2008 A000 – 2008 BFFF	S1 RAM - Parity Bits	8K	0004 D000 – 0004 DFFF	no
no	2008 C000 – 2008 DFFF	S2 RAM - Parity Bits	8K	0004 E000 – 0004 EFFF	no
no	2008 E000 – 2008 FFFF	S3 RAM - Parity Bits	8K	0004 F000 – 0004 FFFF	no
no	2009 0000 – 2009 1FFF	S4 RAM - Parity Bits	8K	0005 0000 – 0005 0FFF	no
no	2009 2000 – 2009 3FFF	S5 RAM - Parity Bits	8K	0005 1000 – 0005 1FFF	no
no	2009 4000 – 2009 5FFF	S6 RAM - Parity Bits	8K	0005 2000 – 0005 2FFF	no
no	2009 6000 – 2009 7FFF	S7 RAM - Parity Bits	8K	0005 3000 – 0005 3FFF	no
	2009 8000 – 200F EFFF	Reserved			
no	200F F000 – 200F F7FF	CtoM MSG RAM - Parity Bits	2K	0007 F800 – 0007 FBFF	no
no	200F F800 – 200F FFFF	MtoC MSG RAM - Parity Bits	2K	0007 FC00 – 0007 FFFF	no
	2010 0000 – 21FF FFFF	Reserved			
yes	2200 0000 – 23FF FFFF	Bit Banded RAM Zone (Dedicated address for each RAM bit of Cortex™-M3 RAM blocks above)	32M		
yes	2400 0000 – 27FF FFFF	All RAM Spaces – Mirror-Mapped (Read cycles from this space cause the µCRC peripheral to continuously update data checksum inside a register when reading a block of data.)	64M		
	2800 0000 – 3FFF FFFF	Reserved			

(1) The letter "M" refers to the Master Subsystem.
(2) The letter "C" refers to the Control Subsystem.

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Table 2-11. Master Subsystem Peripherals

µDMA Access	M Address (Byte-Aligned)(1)	Master Subsystem Peripherals	Size (Bytes)	C Address (x16 Aligned)(2)	C DMA Access(2)
yes	4000 0000 – 4000 0FFF	Watchdog Timer 0 Registers	4K		
yes	4000 1000 – 4000 1FFF	Watchdog Timer 1 Registers	4K		
	4000 2000 – 4000 3FFF	Reserved			
yes	4000 4000 – 4000 4FFF	M GPIO Port A (APB Bus)(1)	4K		
yes	4000 5000 – 4000 5FFF	M GPIO Port B (APB Bus)(1)	4K		
yes	4000 6000 – 4000 6FFF	M GPIO Port C (APB Bus)(1)	4K		
yes	4000 7000 – 4000 7FFF	M GPIO Port D (APB Bus)(1)	4K		
yes	4000 8000 – 4000 8FFF	SSI0	4K		
yes	4000 9000 – 4000 9FFF	SSI1	4K		
yes	4000 A000 – 4000 AFFF	SSI2	4K		
yes	4000 B000 – 4000 BFFF	SSI3	4K		
yes	4000 C000 – 4000 CFFF	UART0	4K		
yes	4000 D000 – 4000 DFFF	UART1	4K		
yes	4000 E000 – 4000 EFFF	UART2	4K		
yes	4000 F000 – 4000 FFFF	UART3	4K		
yes	4001 0000 – 4001 0FFF	UART4	4K		
	4001 1000 – 4001 FFFF	Reserved			
no	4002 0000 – 4002 07FF	I2C0 Master	2K		
no	4002 0800 – 4002 0FFF	I2C0 Slave	2K		
no	4002 1000 – 4002 17FF	I2C1 Master	2K		
no	4002 1800 – 4002 1FFF	I2C1 Slave	2K		
	4002 2000 – 4002 3FFF	Reserved			
yes	4002 4000 – 4002 4FFF	M GPIO Port E (APB Bus)(1)	4K		
yes	4002 5000 – 4002 5FFF	M GPIO Port F (APB Bus)(1)	4K		
yes	4002 6000 – 4002 6FFF	M GPIO Port G (APB Bus)(1)	4K		
yes	4002 7000 – 4002 7FFF	M GPIO Port H (APB Bus)(1)	4K		
	4002 8000 – 4002 FFFF	Reserved			
yes	4003 0000 – 4003 0FFF	GP Timer 0	4K		
yes	4003 1000 – 4003 1FFF	GP Timer 1	4K		
yes	4003 2000 – 4003 2FFF	GP Timer 2	4K		
yes	4003 3000 – 4003 3FFF	GP Timer 3	4K		
	4003 4000 – 4003 CFFF	Reserved			
yes	4003 D000 – 4003 DFFF	M GPIO Port J (APB Bus)(1)	4K		
	4003 E000 – 4003 FFFF	Reserved			
yes	4004 8000 – 4004 8FFF	ENET MAC0	4K		
	4004 9000 – 4004 FFFF	Reserved			
yes	4005 0000 – 4005 0FFF	USB MAC0	4K		
	4005 1000 – 4005 7FFF	Reserved			
yes	4005 8000 – 4005 8FFF	M GPIO Port A (AHB Bus)(1)	4K		
yes	4005 9000 – 4005 9FFF	M GPIO Port B (AHB Bus)(1)	4K		
yes	4005 A000 – 4005 AFFF	M GPIO Port C (AHB Bus)(1)	4K		
yes	4005 B000 – 4005 BFFF	M GPIO Port D (AHB Bus)(1)	4K		
yes	4005 C000 – 4005 CFFF	M GPIO Port E (AHB Bus)(1)	4K		
yes	4005 D000 – 4005 DFFF	M GPIO Port F (AHB Bus)(1)	4K		
yes	4005 E000 – 4005 EFFF	M GPIO Port G (AHB Bus)(1)	4K		

(1) The letter "M" refers to the Master Subsystem.
(2) The letter "C" refers to the Control Subsystem.

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Table 2-11. Master Subsystem Peripherals (continued)

µDMA Access	M Address (Byte-Aligned)(1)	Master Subsystem Peripherals	Size (Bytes)	C Address (x16 Aligned)(2)	C DMA Access(2)
yes	4005 F000 – 4005 FFFF	M GPIO Port H (AHB Bus)(1)	4K		
yes	4006 0000 – 4006 0FFF	M GPIO Port J (AHB Bus)(1)	4K		
	4006 1000 – 4006 FFFF	Reserved			
no	4007 0000 – 4007 3FFF	CAN0	16K		
no	4007 4000 – 4007 7FFF	CAN1	16K		
	4007 8000 – 400C FFFF	Reserved			
no	400D 0000 – 400D 0FFF	EPI0 (Registers only)	4K		
	400D 1000 – 400F 9FFF	Reserved			
no	400F A000 – 400F A303	M Flash Control Registers(1)	772		
	400F A304 – 400F A5FF	Reserved			
no	400F A600 – 400F A647	M Flash ECC Error Log Registers(1)	72		
	400F A648 – 400F B1FF	Reserved			
no	400F B200 – 400F B2FF	RAM Configuration Registers	256	0000 4900 – 0000 497F	no
no	400F B300 – 400F B3FF	RAM ECC/Parity/Access Error Log Registers	256	0000 4A00 – 0000 4A7F	no
no	400F B400 – 400F B5FF	M CSM Registers(1)	512		
no	400F B600 – 400F B67F	µCRC	128		
	400F B680 – 400F B6FF	Reserved			
no	400F B700 – 400F B77F	CtoM and MtoC IPC Registers	128	0000 4E00 – 0000 4E3F	no
	400F B780 – 400F B7FF	Reserved			
no	400F B800 – 400F B87F	M Clock Control Registers(1)	128	0000 4400 – 0000 443F	no
no	400F B880 – 400F B8BF	M LPM Control Registers(1)	64		
no	400F B8C0 – 400F B8FF	M Reset Control Registers(1)	64		
no	400F B900 – 400F B93F	Device Configuration Registers	64	0000 0880 – 0000 0890 (Read Only)	
	400F B940 – 400F B97F	Reserved			
no	400F B980 – 400F B9FF	M Write Protect Registers(1)	128		
no	400F BA00 – 400F BA7F	M NMI Registers(1)	128		
	400F BA80 – 400F EFFF	Reserved			
no	400F F000 – 400F FFFF	µDMA Registers	4K		
	4010 0000 – 41FF FFFF	Reserved			
yes	4200 0000 – 43FF FFFF	Bit Banded Peripheral Zone (Dedicated address for each register bit of Cortex™-M3 peripherals above.)	32M		
	4400 0000 – 4FFF FFFF	Reserved			

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Table 2-12. Master Subsystem Analog and EPI

µDMA Access	M Address (Byte-Aligned)(1)	Master Subsystem Analog and EPI	Size (Bytes)
	5000 0000 – 5000 15FF	Reserved	
yes	5000 1600 – 5000 161F	ADC1 Result Registers	32
	5000 1620 – 5000 167F	Reserved	
yes	5000 1680 – 5000 169F	ADC2 Result Registers	32
	5000 16A0 – 5FFF FFFF	Reserved	
yes	6000 0000 – DFFF FFFF	EPI0 (External Peripheral/Memory Interface)	2G

(1) The letter "M" refers to the Master Subsystem.

Table 2-13. Cortex™-M3 Private Bus

µDMA Access	Cortex™-M3 Address (Byte-Aligned)	Cortex™-M3 Private Bus	Size (Bytes)
no	E000 0000 – E000 0FFF	Reserved	
no	E000 1000 – E000 1FFF	DWT (Data Watchpoint and Trace)	4K
no	E000 2000 – E000 2FFF	FPB (Flash Patch and Breakpoint)	4K
	E000 3000 – E000 E007	Reserved	
no	E000 E008 – E000 E00F	System Control Block	8
no	E000 E010 – E000 E01F	System Timer	16
	E000 E020 – E000 E0FF	Reserved	
no	E000 E100 – E000 E4EF	Nested Vectored Interrupt Controller (NVIC)	1008
	E000 E4F0 – E000 ECFF	Reserved	
no	E000 ED00 – E000 ED3F	System Control Block	64
	E000 ED40 – E000 ED8F	Reserved	
no	E000 ED90 – E000 EDB8	Memory Protection Unit	41
	E000 EDB9 – E000 EEFF	Reserved	
no	E000 EF00 – E000 EF03	Nested Vectored Interrupt Controller (NVIC)	4
	E000 EF04 – FFFF FFFF	Reserved	

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2.3 Master Subsystem

The Master Subsystem includes the Cortex™-M3 CPU, µDMA, Nested Vectored Interrupt Controller (NVIC), Cortex™-M3 Peripherals, and Local Memory. Additionally, the Cortex™-M3 CPU and µDMA can access the Control Subsystem through Shared Resources (IPC, Message RAM, Shared RAM), and talk to the Analog Peripherals via the Analog Common Interface Bus. The Master Subsystem can also receive events from the NMI block and send events to the Resets block.

Figure 2-1 shows the Master Subsystem.

2.3.1 Cortex™-M3 CPU

The 32-bit Cortex™-M3 processor offers high performance, fast interrupt handling, and access to a variety of communication peripherals (including Ethernet and USB). The Cortex™-M3 features a Memory Protection Unit (MPU) to provide a privileged mode for protected operating system functionality. A bus bridge adjacent to the MPU can route program instructions and data on the I-CODE and D-CODE buses that connect to the Boot ROM and Flash. Other data is typically routed through the Cortex™-M3 System Bus connected to the local RAMs. The System Bus also goes to the Shared Resources block (also accessible by the Control Subsystem) and to the Analog Subsystem through the Analog Common Interface Bus (ACIB). Another bus bridge allows bus cycles from both the Cortex™-M3 System Bus and those of the µDMA bus to access the Master Subsystem peripherals (via the APB bus or the AHP bus).

Most of the interrupts to the Cortex™-M3 CPU come from the Nested Vectored Interrupt Controller (NVIC), which manages the interrupt requests from peripherals and assigns handling priorities. There are also several exceptions generated by Cortex™-M3 CPU that can return to the Cortex™-M3 as interrupts after being prioritized with other requests inside the NVIC. In addition to programmable priority interrupts, there are also three levels of fixed-priority interrupts of which the highest priority, level-3, is given to M3PORRST and M3SYSRST resets from the Resets block. The next highest priority, level-2, is assigned to the M3NMIINT, which originates from the NMI block. The M3HRDFLT (Hard Fault) interrupt is assigned to level-1 priority, and it is caused by one of the error condition exceptions (Memory Management, Bus Fault, Usage Fault) escalating to Hard Fault because they are not enabled or not properly serviced.

The Cortex™-M3 CPU has two low-power modes: Sleep and Deep Sleep.

2.3.2 Cortex™-M3 DMA and NVIC

The Cortex™-M3 direct memory access (µDMA) module provides a hardware method of transferring data between peripherals and/or memory without intervention from the Cortex™-M3 CPU. The Nested Vectored Interrupt Controller (NVIC) manages and prioritizes interrupt handling for the Cortex™-M3 CPU.

The Cortex™-M3 peripherals use REQ/DONE handshaking to coordinate data transfer requests with the µDMA. If a DMA channel is enabled for a given peripheral, REQ/DONE from the peripheral will trigger the data transfer, following which an IRQ request may be sent from the µDMA to the NVIC to announce to the Cortex™-M3 that the transfer has completed. If a DMA channel is not enabled for a given peripheral, REQ/DONE will directly drive IRQ to the NVIC so that the Cortex™-M3 CPU can transfer the data. For those peripherals that are not supported by the µDMA, IRQs are supplied directly to the NVIC, bypassing the DMA. This is the case for both Watchdogs, CANs, I2Cs, and the Analog-to-Digital Converters sending ADCINT[8:1] interrupts from the Analog Subsystem. The NMI Watchdog does not send any events to the µDMA or the NVIC (only to the Resets block).

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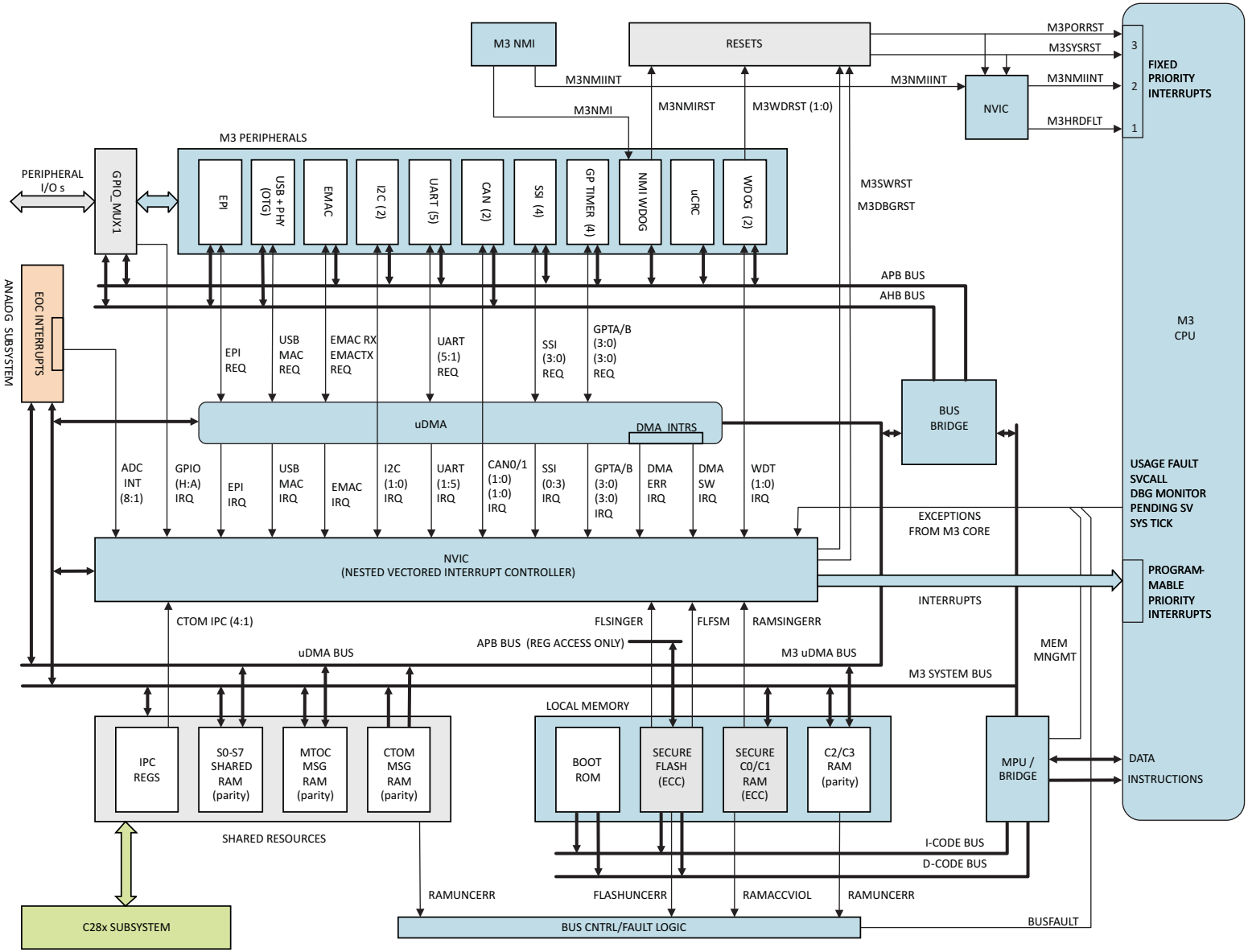

Figure 2-1. Master Subsystem

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2.3.3 Cortex™-M3 Interrupts

Table 2-14 shows all interrupt assignments for the Cortex™-M3 processor. Most interrupts (16–107) are associated with interrupt requests from Cortex™-M3 peripherals. The first 15 interrupts (1–15) are processor exceptions generated by the Cortex™-M3 core itself. These processor exceptions are detailed in Table 2-15.

Table 2-14. Interrupts from NVIC to Cortex™-M3

Interrupt Number (Bit in Interrupt Registers)	Vector Number	Vector Address or Offset	Description
–	0–15	0x0000.0000–0x0000.003C	Processor exceptions
0	16	0x0000.0040	GPIO Port A
1	17	0x0000.0044	GPIO Port B
2	18	0x0000.0048	GPIO Port C
3	19	0x0000.004C	GPIO Port D
4	20	0x0000.0050	GPIO Port E
5	21	0x0000.0054	UART0
6	22	0x0000.0058	UART1
7	23	0x0000.005C	SSI0
8	24	0x0000.0060	I2C0
9–17	25–33	–	Reserved
18	34	0x0000.0088	Watchdog Timers 0 and 1
19	35	0x0000.008C	Timer 0A
20	36	0x0000.0090	Timer 0B
21	37	0x0000.0094	Timer 1A
22	38	0x0000.0098	Timer 1B
23	39	0x0000.009C	Timer 2A
24	40	0x0000.00A0	Timer 2B
25–27	41–43	–	Reserved
28	44	0x0000.00B0	System Control
29	45	0x0000.00B4	Flash State Machine
30	46	0x0000.00B8	GPIO Port F
31	47	0x0000.00BC	GPIO Port G
32	48	0x0000.00C0	GPIO Port H
33	49	0x0000.00C4	UART2
34	50	0x0000.00C8	SSI1
35	51	0x0000.00CC	Timer 3A
36	52	0x0000.00D0	Timer 3B
37	53	0x0000.00D4	I2C1
38–41	54–57	–	Reserved
42	58	0x0000.00E8	Ethernet Controller
44	60	0x0000.00F0	USB
45	61	–	Reserved
46	62	0x0000.00F8	µDMA Software
47	63	0x0000.00FC	µDMA Error
48–52	64–68	–	Reserved
53	69	0x0000.0114	EPI
54	70	0x0000.0118	GPIO Port J
55–56	71–72	–	Reserved
57	73	0x0000.0124	SSI 2
58	74	0x0000.0128	SSI 3

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Table 2-14. Interrupts from NVIC to Cortex™-M3 (continued)

Interrupt Number (Bit in Interrupt Registers)	Vector Number	Vector Address or Offset	Description
59	75	0x0000.012C	UART3
60	76	0x0000.0130	UART4
61–63	77–79	–	Reserved
64	80	0x0000.0140	CAN1 INT0
65	81	0x0000.0144	CAN1 INT1
66	82	0x0000.0148	CAN1 INT0
67	83	0x0000.014C	CAN1 INT1
68–71	84–87	–	Reserved
72	88	0x0000.0160	ADCINT1
73	89	0x0000.0164	ADCINT2
74	90	0x0000.0168	ADCINT3
75	91	0x0000.016C	ADCINT4
76	92	0x0000.0170	ADCINT5
77	93	0x0000.0174	ADCINT6
78	94	0x0000.0178	ADCINT7
79	95	0x0000.017C	ADCINT8
80	96	0x0000.0180	CTOMIPC1
81	97	0x0000.0184	CTOMIPC2
82	98	0x0000.0188	CTOMIPC3
83	99	0x0000.018C	CTOMIPC4
84–87	100–103	–	Reserved
88	104	0x0000.01A0	RAM Single Error
89	1–5	0x0000.01A4	System / USB PLL Out of Lock
90	106	0x0000.01A8	M3 Flash Single Error
91	107	0x0000.01AC	Reserved

Table 2-15. Exceptions from Cortex™-M3 Core to NVIC

Exception Type	Priority(1)	Vector Number	Vector Address or Offset(2)	Activation
–	–	0	0x0000.0000	Stack top is loaded from the first entry of the vector table on reset.
Reset	–3 (highest)	1	0x0000.0004	Asynchronous
Non-Maskable Interrupt (NMI)	–2	2	0x0000.0008	Asynchronous On Concerto devices activated by clock fail condition, C28 PIE error, external M3GPIO NMI input signal, and C28 NMI WD timeout reset.
Hard Fault	–1	3	0x0000.000C	–
Memory Management	programmable(3)	4	0x0000.0010	Synchronous

(1) 0 is the default priority for all the programmable priorities
(2) See the "Vector Table" subsection of the "Exception Model" section in the *Cortex-M3 Processor* chapter of the *Concerto F28M35x Technical Reference Manual* (literature number SPRUH22).
(3) See SYSPRI1 in the *Cortex-M3 Peripherals* chapter of the *Concerto F28M35x Technical Reference Manual* (literature number SPRUH22).

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Table 2-15. Exceptions from Cortex™-M3 Core to NVIC (continued)

Exception Type	Priority(1)	Vector Number	Vector Address or Offset(2)	Activation
Bus Fault	programmable(3)	5	0x0000.0014	Synchronous when precise and asynchronous when imprecise. On Concerto devices activated by memory access errors and RAM and flash uncorrectable data errors.
Usage Fault	programmable(3)	6	0x0000.0018	Synchronous
–	–	7–10	–	Reserved
SVCall	programmable(3)	11	0x0000.002C	Synchronous
Debug Monitor	programmable(3)	12	0x0000.0030	Synchronous
–	–	13	–	Reserved
PendSV	programmable(3)	14	0x0000.0038	Asynchronous
SysTick	programmable(3)	15	0x0000.003C	Asynchronous
Interrupts	programmable (4)	16 and above	0x0000.0040 and above	Asynchronous

(4) See PRIn registers in the *Cortex-M3 Peripherals* chapter of the *Concerto F28M35x Technical Reference Manual* (literature number SPRUH22).

2.3.4 Cortex™-M3 Vector Table

Each peripheral interrupt of Table 2-14 is assigned an address offset containing the location of the peripheral interrupt handler (relative to the vector table base) for that particular interrupt (vector numbers 16–107).

Similarly, each exception interrupt of Table 2-15 (including Reset) is also assigned an address offset containing the location of the exception interrupt handler (relative to the vector table base) for that particular interrupt (vector numbers 1–15).

In addition to interrupt vectors, the vector table also contains the initial stack pointer value at table location 0.

Following system reset, the vector table base is fixed at address 0x0000.0000. Privileged software can write to the Vector Table Offset (VTABLE) register to relocate the vector table start address to a different memory location, in the range 0x0000 0200 to 0x3FFF FE00. Note that when configuring the VTABLE register, the offset must be aligned on a 512-byte boundary.

2.3.5 Cortex™-M3 Local Peripherals

The Cortex™-M3 local peripherals include two Watchdogs, an NMI Watchdog, four General-Purpose Timers, four SSI peripherals, two CAN peripherals, five UARTs, two I2C peripherals, Ethernet, USB + PHY, EPI, and µCRC (Cyclic Redundancy Check). The USB and EPI are accessible through the AHB Bus (Advanced High-Performance Bus). The remaining peripherals are accessible through the APB Bus (Advanced Peripheral Bus). The APB and AHB bus cycles originate from the CPU System Bus or the µDMA Bus via a bus bridge.

While the Cortex™-M3 CPU has access to all the peripherals, the µDMA has access to most, with the exception of the µCRC, Watchdogs, NMI Watchdog, CAN peripherals, and the I2C peripheral. The Cortex™-M3 peripherals connect to the Concerto™ device pins via GPIO_MUX1. Most of the peripherals also generate event signals for the µDMA and/or the NVIC. The Watchdogs receive M3SWRST from the NVIC (triggered by software) and send M3WDRST[1:0] reset requests to the Reset block. The NMI Watchdog receives the M3NMI event from the NMI block and sends the M3NMIRST request to the Resets block.

See Section 5.1 for more information on the Cortex™-M3 peripherals.

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2.3.6 Cortex™-M3 Local Memory

The Local Memory includes Boot ROM; Secure Flash with Error Correction Code (ECC); Secure C0/C1 RAM with ECC; and C2/C3 RAM with Parity Error Checking. The Boot ROM and Flash are both accessible through the I-CODE and D-CODE Buses. Flash registers can also be accessed by the Cortex™-M3 CPU through the APB Bus. All Local Memory is accessible from the Cortex™-M3 CPU; the C2/C3 RAM is also accessible by the µDMA.

Two types of error correction events can be generated during access of the Local Memory: uncorrectable errors and single errors. The uncorrectable errors (including one from the Shared Memories) generate a Bus Fault Exception to the Cortex™-M3 CPU. The less critical single errors go to the NVIC where they can result in maskable interrupts to the Cortex™-M3 CPU.

2.3.7 Cortex™-M3 Accessing Shared Resources and Analog Peripherals

There are several memories, digital peripherals, and analog peripherals that can be accessed by both the Master and Control Subsystems. They are grouped into Shared Resources block and the Analog Subsystem.

The Shared Resources block includes Inter-Processor Communications (IPC) registers, MTOC Message RAM, CTOM Message RAM, and eight individually configurable Shared RAM blocks. The RAMs of the Shared Resources block have Parity Error Checking.

The Message RAMs and the Shared RAMs can be accessed by the Cortex™-M3 CPU and µDMA. The MTOC Message RAM is intended for sending data from the Master Subsystem to the Control Subsystem, having r/w access for the Cortex™-M3/µDMA and read-only access for the C28x/DMA. The CTOM Message RAM is intended for sending data from the Control Subsystem to the Master Subsystem, having r/w access for the C28x/DMA and read-only access for the Cortex™-M3/µDMA.

The IPC registers provide up to 32 handshaking channels to coordinate the transfer of data through the Message RAMs by polling. Four of these channels are also backed up by four interrupts to PIE on the Control Subsystem side, and four interrupts to the NVIC on the Master Subsystem side (to reduce delays associated with polling).

The eight Shared RAM blocks are similar to the Message RAMs, in that the data flow is only one way; however, the direction of the data flow can be individually set for each block to be from Master to Control Subsystem or from Control to Master Subsystem.

The Analog Subsystem has ADC1, ADC2, and Analog Comparator peripherals that can be accessed by both the Cortex™-M3 and C28x Subsystems through the Analog Common Interface Bus. The Cortex™-M3 CPU accesses the ACIB through the System Bus, and the µDMA through the µDMA Bus. The ACIB arbitrates for access to the ADC and Analog Comparator registers between CPU/DMA bus cycles of the Master Subsystem with those of the Control Subsystem. In addition to managing bus cycles, the ACIB also transfers End-of-Conversion ADC interrupts to the Master Subsystem (as well as to the Control Subsystem). The eight EOC sources from ADC1 and the eight EOC sources from ADC2 are AND-ed together by the ACIB, with the resulting eight ADC interrupts going to destinations in both the Master Subsystem and the Control Subsystem.

See Section 5.3 for more information on shared resources and analog peripherals.

2.4 Control Subsystem

The Control Subsystem includes the C28x CPU/FPU/VCU, Peripheral Interrupt Expansion (PIE) block, DMA, C28x Peripherals, and Local Memory. Additionally, the C28x CPU and DMA have access to Shared Resources (IPC, Message RAM, Shared RAM), and to Analog Peripherals via the Analog Common Interface Bus.

Figure 2-2 shows the Control Subsystem.

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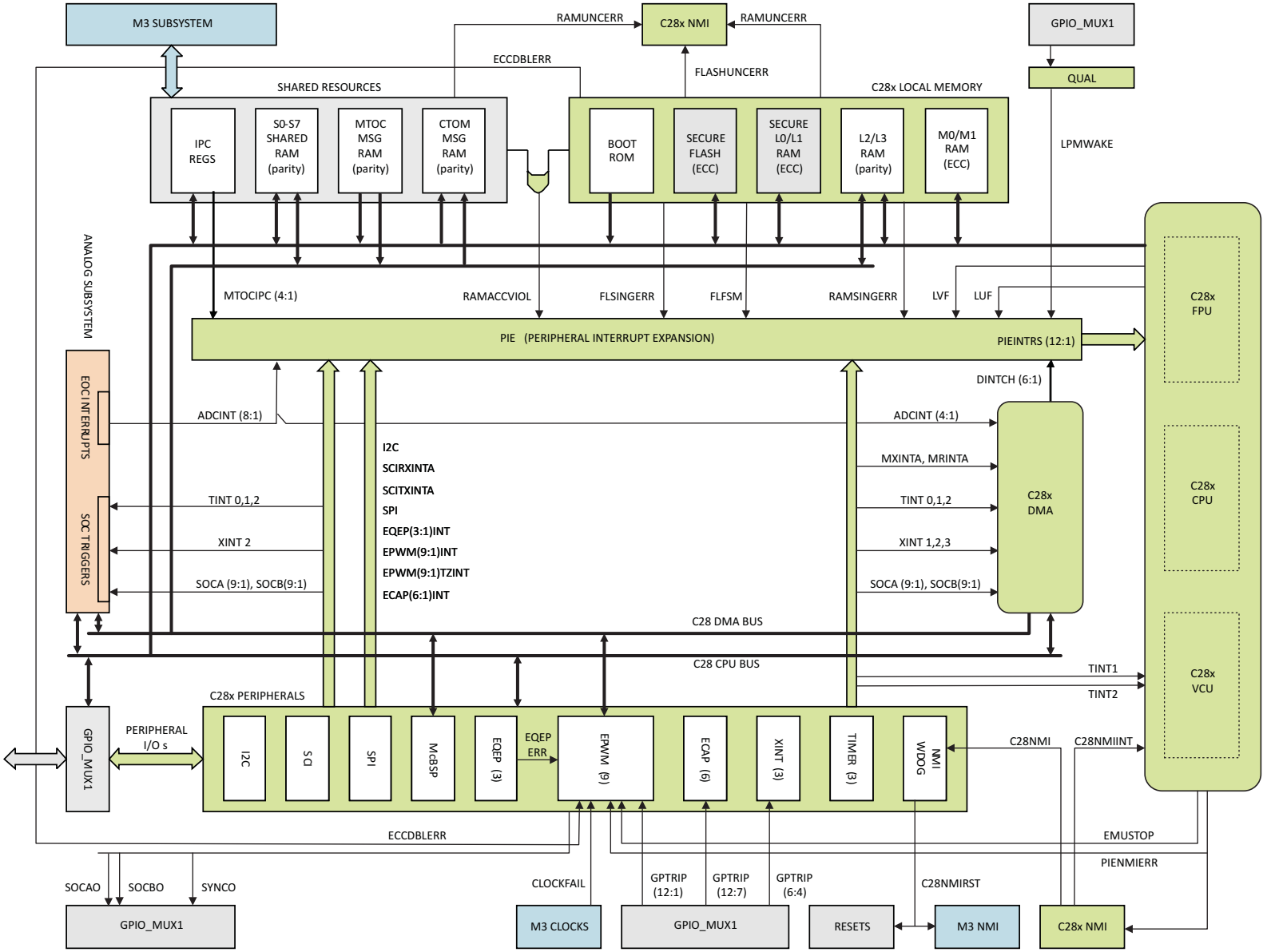

Figure 2-2. Control Subsystem

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2.4.1 C28x CPU/FPU/VCU

The F28M35x Concerto™ MCU family is a member of the TMS320C2000™ MCU platform. The Concerto™ C28x CPU/FPU has the same 32-bit fixed-point architecture as TI's existing Piccolo™ MCUs, combined with a single-precision (32-bit) IEEE 754 floating-point unit (FPU) of TI's existing Delfino™ MCUs. It is a very efficient C/C++ engine, enabling users to develop their system control software in a high-level language. It also enables math algorithms to be developed using C/C++. The device is as efficient at DSP math tasks as it is at system control tasks. The 32 x 32-bit MAC 64-bit processing capabilities enable the controller to handle higher numerical resolution problems efficiently. With the addition of the fast interrupt response with automatic context save of critical registers, the device is capable of servicing many asynchronous events with minimal latency. The device has an 8-level-deep protected pipeline with pipelined memory accesses. This pipelining enables it to execute at high speeds without resorting to expensive high-speed memories. Special branch-look-ahead hardware minimizes the latency for conditional discontinuities. Special conditional store operations further improve performance. The VCU extends the capabilities of the C28x CPU and C28x+FPU processors by adding additional instructions to accelerate Viterbi, Complex Arithmetic, 16-bit FFTs, and CRC algorithms. No changes have been made to existing instructions, pipeline, or memory bus architecture. Therefore, programs written for the C28x are completely compatible with the C28x+VCU.

There are two events generated by the FPU block that go to the C28x Peripheral Interrupt Expansion (PIE): LVF and LUV. Inside PIE, these and other events from C28x peripherals and memories result in 12 PIE interrupts PIEINTS[12:1] into the C28x CPU. The C28x CPU also receives three additional interrupts directly (instead of through PIE) from Timer 1 (TINT1), from Timer 2 (TINT2), and from the NMI block (C28uNMIINT).

The C28x has two low-power modes: Idle and Standby.

2.4.2 C28x Peripheral Interrupt Expansion (PIE)

The PIE block serves to multiplex numerous interrupt sources into a smaller set of interrupt inputs. The PIE block can support up to 96 peripheral interrupts. On the F28M35x, 70 of the possible 96 interrupts are used. The 96 interrupts are grouped into blocks of 8 and each group is fed into 1 of 12 CPU interrupt lines (INT1 to INT12). Each of 12 interrupt lines supports up to 8 simultaneously active interrupts. Each of the 96 interrupts has its own vector stored in a dedicated RAM block that can be overwritten by the user. The vector is automatically fetched by the CPU on servicing the interrupt. It takes eight CPU clock cycles to fetch the vector and save critical CPU registers. Hence, the CPU can quickly respond to interrupt events. Prioritization of interrupts is controlled in hardware and software. Each individual interrupt can be enabled or disabled within the PIE block.

See Table 2-16 for PIE interrupt assignments.

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Table 2-16. PIE Peripheral Interrupts(1)

CPU INTERRUPTS	PIE INTERRUPTS							
	INTx.8	INTx.7	INTx.6	INTx.5	INTx.4	INTx.3	INTx.2	INTx.1
INT1	C28.LPMWAKE (C28LPM) 0x0D4E	TINT0 (TIMER 0) 0x0D4C	Reserved – 0x0D4A	XINT2 – 0x0D48	XINT1 – 0x0D46	Reserved – 0x0D44	ADCINT2 (ADC) 0x0D42	ADCINT1 (ADC) 0x0D40
INT2	EPWM8_TZINT (ePWM8) 0x0D5E	EPWM7_TZINT (ePWM7) 0x0D5C	EPWM6_TZINT (ePWM6) 0x0D5A	EPWM5_TZINT (ePWM5) 0x0D58	EPWM4_TZINT (ePWM4) 0x0D56	EPWM3_TZINT (ePWM3) 0x0D54	EPWM2_TZINT (ePWM2) 0x0D52	EPWM1_TZINT (ePWM1) 0x0D50
INT3	EPWM8_INT (ePWM8) 0x0D6E	EPWM7_INT (ePWM7) 0x0D6C	EPWM6_INT (ePWM6) 0x0D6A	EPWM5_INT (ePWM5) 0x0D68	EPWM4_INT (ePWM4) 0x0D66	EPWM3_INT (ePWM3) 0x0D64	EPWM2_INT (ePWM2) 0x0D62	EPWM1_INT (ePWM1) 0x0D60
INT4	EPWM9_TZINT (ePWM9) 0x0D7E	Reserved – 0x0D7C	ECAP6_INT (eCAP6) 0x0D7A	ECAP5_INT (eCAP5) 0x0D78	ECAP4_INT (eCAP4) 0x0D76	ECAP3_INT (eCAP3) 0x0D74	ECAP2_INT (eCAP2) 0x0D72	ECAP1_INT (eCAP1) 0x0D70
INT5	EPWM9_INT (ePWM9) 0x0D8E	Reserved – 0x0D8C	Reserved – 0x0D8A	Reserved – 0x0D88	Reserved – 0x0D86	EQEP3_INT (eQEP3) 0x0D84	EQEP2_INT (eQEP2) 0x0D82	EQEP1_INT (eQEP1) 0x0D80
INT6	Reserved – 0x0D9E	Reserved – 0x0D9C	MXINTA (McBSPA) 0x0D9A	MRINTA (McBSPA) 0x0D98	Reserved – 0x0D96	Reserved – 0x0D94	SPITXINTA (SPIA) 0x0D92	SPIRXINTA (SPIA) 0x0D90
INT7	Reserved – 0x0DAE	Reserved – 0x0DAC	DINTCH6 (C28 DMA) 0x0DAA	DINTCH5 (C28 DMA) 0x0DA8	DINTCH4 (C28 DMA) 0x0DA6	DINTCH3 (C28 DMA) 0x0DA4	DINTCH2 (C28 DMA) 0x0DA2	DINTCH1 (C28 DMA) 0x0DA0
INT8	Reserved – 0x0DBE	Reserved – 0x0DBC	Reserved – 0x0DBA	Reserved – 0x0DB8	Reserved – 0x0DB6	Reserved – 0x0DB4	I2CINT2A (I2CA) 0x0DB2	I2CINT1A (I2CA) 0x0DB0
INT9	Reserved – 0x0DCE	Reserved – 0x0DCC	Reserved – 0x0DCA	Reserved – 0x0DC8	Reserved – 0x0DC6	Reserved – 0x0DC4	SCITXINTA (SCIA) 0x0DC2	SCIRXINTA (SCIA) 0x0DC0
INT10	ADCINT8 (ADC) 0x0DDE	ADCINT7 (ADC) 0x0DDC	ADCINT6 (ADC) 0x0DDA	ADCINT5 (ADC) 0x0DD8	ADCINT4 (ADC) 0x0DD6	ADCINT3 (ADC) 0x0DD4	ADCINT2 (ADC) 0x0DD2	ADCINT1 (ADC) 0x0DD0
INT11	Reserved – 0x0DEE	Reserved – 0x0DEC	Reserved – 0x0DEA	Reserved – 0x0DE8	MTOCIPCINT4 (IPC) 0x0DE6	MTOCIPCINT3 (IPC) 0x0DE4	MTOCIPCINT2 (IPC) 0x0DE2	MTOCIPCINT1 (IPC) 0x0DE0
INT12	LUF (C28FPU) 0x0DFE	LVF (C28FPU) 0x0DFC	Reserved – 0x0DFA	C28RAMACCVIOL (Memory) 0x0DF8	C28RAMSINGERR (Memory) 0x0DF6	C28FLFSM (Memory) 0x0DF4	C28FLSINGERR (Memory) 0x0DF2	XINT3 (Ext. Int. 3) 0x0DF0

(1) Out of the 96 possible interrupts, 66 interrupts are currently used. The remaining interrupts are reserved for future devices. These interrupts can be used as software interrupts if they are enabled at the PIEIFRx level, provided none of the interrupts within the group is being used by a peripheral. Otherwise, interrupts coming in from peripherals may be lost by accidentally clearing their flag while modifying the PIEIFR. To summarize, there are two safe cases when the reserved interrupts could be used as software interrupts:
1) No peripheral within the group is asserting interrupts.
2) No peripheral interrupts are assigned to the group (example PIE group 11).

2.4.3 C28x DMA

The C28x direct memory access (DMA) module provides a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up bandwidth for other system functions. Additionally, the DMA has the capability to orthogonally rearrange the data as it is transferred as well as “ping-pong” data between buffers. These features are useful for structuring data into blocks for optimal CPU processing. The interrupt trigger source for each of the six DMA channels can be configured separately and each channel contains its own independent PIE interrupt to let the CPU know when a DMA transfer has either started or completed. Five of the six channels are exactly the same, while Channel 1 has one additional feature: the ability to be configured at a higher priority than the others.

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2.4.4 C28x Local Peripherals

The C28x local peripherals include NMI Watchdog, three Timers, four Serial Port Peripherals (SCI, SPI, McBSP, I2C), and three types of Control Peripherals (ePWM, eQEP, eCAP). All peripherals are accessible by the C28x CPU via the C28x Memory Bus. Additionally, the McBSP and ePWM are accessible by the C28x DMA Bus. The Serial Port Peripherals and the Control Peripherals connect to Concerto's pins via the GPIO_MUX1 block. Internally, the C28x peripherals generate events to the PIE block, C28x DMA, and the Analog Subsystem. The C28x NMI Watchdog receives a C28NMI event from the NMI block and sends a counter timeout event to the Cortex™-M3 NMI block and the Resets block to flag a potentially critical condition.

The ePWM peripheral receives events that can be used to trip the ePWM outputs EPWMxA and EPWMxB. These events include ECCDBLERR event from the C28x Local Memory, PIENMIERR and EMUSTOP events from the C28x CPU, and up to 12 trips from GPIO_MUX1.

See Section 5.2 for more information on C28x peripherals.

2.4.5 C28x Local Memory

The C28x Local Memory includes Boot ROM; Secure Flash with Error Correction Code (ECC); Secure L0/L1 RAM with ECC; L2/L3 RAM with Parity Error Checking; and M0/M1 with ECC. All local memories are accessible from the C28x CPU; the L2/L3 RAM is also accessible by the C28x DMA. Two types of error correction events can be generated during access of the C28x Local Memory: uncorrectable errors and single errors. The uncorrectable errors propagate to the NMI block where they can become the C28NMI to the C28x NMI Watchdog and the C28NMIINT non-maskable interrupt to the C28x CPU. The less critical single errors go to the PIE block where they can become maskable interrupts to the C28x CPU.

2.4.6 C28x Accessing Shared Resources and Analog Peripherals

There are several memories, digital peripherals, and analog peripherals that can be accessed by both the Master and Control Subsystems. They are grouped into the Shared Resources block and the Analog Subsystem.

The Shared Resources block includes Inter-Processor Communications (IPC) registers, MTOC Message RAM, CTOM Message RAM, and eight individually configurable Shared RAM blocks.

The Message RAMs and the Shared RAMs can be accessed by the C28x CPU and DMA and have Parity-Error Checking. The MTOC Message RAM is intended for sending data from the Master Subsystem to the Control Subsystem, having r/w access for the Cortex™-M3/µDMA and read-only access for the C28x/DMA. The CTOM Message RAM is intended for sending data from the Control Subsystem to the Master Subsystem, having r/w access for the C28x/DMA and read-only access for the Cortex™-M3/µDMA.

The IPC registers provide up to 32 handshaking channels to coordinate transfer of data through the Message RAMs by polling. Four of these channels are also backed up by four interrupts to PIE on the Control Subsystem side, and four interrupts to the NVIC on the Master Subsystem side (to reduce delays associated with polling).

The eight Shared RAM blocks are similar to the Message RAMs, in that the data flow is only one way; however, the direction of the data flow can be individually set for each block to be from Master to Control Subsystem or from Control to Master Subsystem.

See Section 5.3 for more information on shared resources and analog peripherals.

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2.5 Analog Subsystem

The Analog Subsystem has ADC1, ADC2, and six Analog Comparator + DAC units that can be accessed by both the Master Subsystem and Control Subsystem via the Analog Common Interface Bus. The C28x CPU accesses the ACIB through the C28x Memory Bus, and the C28x DMA through the C28x DMA Bus. The ACIB arbitrates for access to ADC and Analog Comparator registers between CPU/DMA bus cycles of the C28x Subsystem with those of the Cortex™-M3 Subsystem. In addition to managing bus cycles, the ACIB also transfers Start-Of-Conversion triggers to the Analog Subsystem and returns End-Of-Conversion ADC interrupts to both the Master Subsystem and the Control Subsystem.

There are 22 possible SOC (Start-Of-Conversion) sources from the C28x Subsystem that are mapped to a total of 8 possible SOC triggers inside the Analog Subsystem (to ADC1 and ADC2).

Going the other way, eight EOC (End-Of-Conversion) sources from ADC1 and eight EOC sources from ADC2 are AND-ed together to form eight interrupts going to destinations in both the Master and Control Subsystems. Inside the C28x Subsystem, all eight EOC interrupts go to the PIE, but only four of the same eight go to the C28x DMA.

The Concerto™ MCU Analog Subsystem has two independent Analog-to-Digital Converters (ADC1, ADC2); six Analog Comparators + DAC units; and an Analog Common Interface Bus (ACIB) to facilitate analog data communications with Concerto's two digital subsystems (Cortex™-M3 and C28x).

Figure 2-3 shows the Analog Subsystem.

2.5.1 ADC1

The ADC1 consists of a 12-bit Analog-to-Digital converter with up to 16 analog input channels of which 10 are currently pinned out. One of the not-pinned-out channels is assigned to the internal temperature sensor. The analog channels are internally pre-assigned to two Sample-and-Hold (S/H) units A and B, both feeding an Analog Mux whose output is converted to a 12-bit digital value and stored in ADC1 result registers. The two S/H units enable simultaneous sampling of two analog signals at a time. Additional channels or channel pairs are converted sequentially. Start-of-Conversion (SOC) triggers from the Control Subsystem initiate analog-to-digital conversions. End-of-Conversion (EOC) interrupts from ADCs notify the Master and Control Subsystems that the conversion results are ready to be read from ADC1 result registers.

See Section 5.3.1 for more information on ADC peripherals.

2.5.2 ADC2

The ADC2 consists of a 12-bit Analog-to-Digital converter with up to 16 analog input channels of which 10 are currently pinned out. The analog channels are internally preassigned to two Sample-and-Hold (S/H) units A and B, both feeding an Analog Mux whose output is converted to a 12-bit digital value and stored in the ADC2 result registers. The two S/H units enable simultaneous sampling of two analog signals at a time. Additional channels or channel pairs are converted sequentially. Start-of-Conversion (SOC) triggers from the Control Subsystem initiate analog-to-digital conversions. End-of-Conversion (EOC) interrupts from ADCs notify the Master and Control Subsystems that the conversion results are ready to be read from ADC2 result registers.

See Section 5.3.1 for more information on ADC peripherals.

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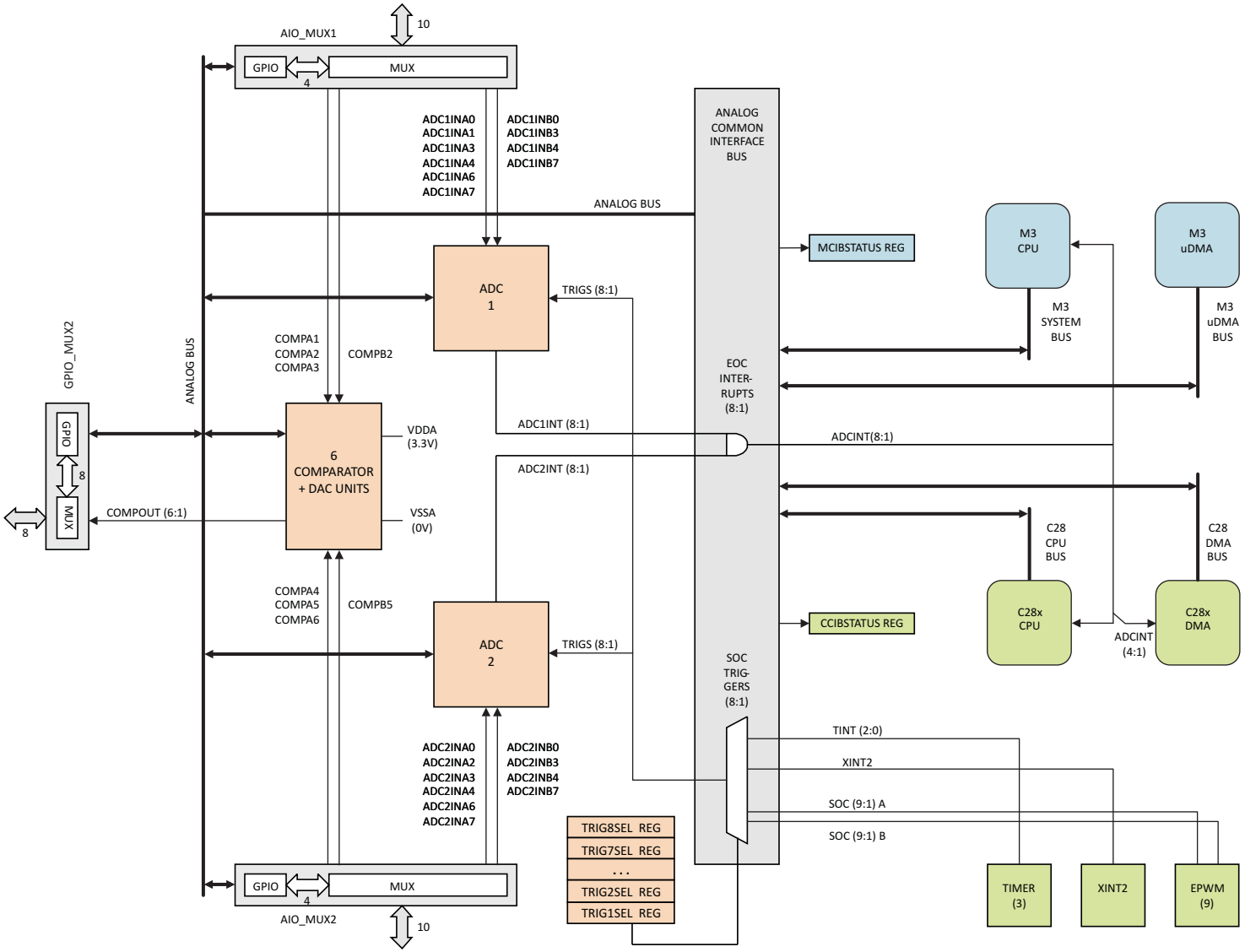

Figure 2-3. Analog Subsystem

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2.5.3 Analog Comparator + DAC

There are six Comparator blocks enabling simultaneous comparison of multiple pairs of analog inputs, resulting in six digital comparison outputs. The external analog inputs that are being compared in the comparators come from AIO_MUX1 and AIO_MUX2 blocks. These analog inputs can be compared against each other or the outputs of 10-bit DACs (Digital-to-Analog Converters) inside individual Comparator modules. The six comparator outputs go to the GPIO_MUX2 block where they can be mapped to six out of eight available pins.

Note that in order to use these comparator outputs to trip the C28x EPWMA/B outputs, they must be first routed externally from pins of the GPIO_MUX2 block to selected pins of the GPIO_MUX1 block before they can be assigned to selected 12 ePWM Trip Inputs.

See Section 5.3.2 for more information on the analog comparator + DAC.

2.5.4 Analog Common Interface Bus (ACIB)

The ACIB bus links the Master and Control Subsystems with the Analog Subsystem. It enables the Cortex™-M3 CPU/µDMA and C28x CPU/DMA to access Analog Subsystem registers, to send SOC Triggers to the Analog Subsystem, and to receive EOC Interrupts from the Analog Subsystem. The Cortex™-M3 uses its System Bus and the µDMA Bus to read from and write to Analog Subsystem registers. The C28x uses its Memory Bus and the DMA bus to access the same Analog Subsystem registers. The ACIB arbitrates between up to four possibly simultaneously occurring bus cycles on the Master/Control Subsystem side of ACIB to access the ADC and Analog Comparator registers on the Analog Subsystem side.

Additionally, ACIB maps up to 22 SOC trigger sources from the Control Subsystem to 8 SOC trigger destinations inside the Analog Subsystem (shared between ADC1 and ADC2), and up to 16 ADC EOC interrupt sources from the Analog Subsystem to 8 destinations inside the Master and Control Subsystems. The eight ADC interrupts are the result of AND-ing of eight EOC interrupts from ADC1 with 8 EOC interrupts from ADC2. The total of 16 possible ADC1 and ADC2 interrupts are sharing the 8 interrupt lines because it is unlikely that any application would need all 16 interrupts at the same time.

Eight registers (TRIG1SEL–TRIG8SEL) configure eight corresponding SOC triggers to assign 1 of 22 possible trigger sources to each SOC trigger.

There are two registers that provide status of ACIB to the Master Subsystem and to the Control Subsystem.

The Cortex™-M3 can read the MCIBSTATUS register to verify that the Analog Subsystem is properly powered up; the Analog System Clock (ASYSCLK) is present; and that the bus cycles, triggers, and interrupts are correctly propagating between the Master, Control, and Analog subsystems.

The C28x can read the CCIBSTATUS register to verify that the Analog Subsystem is properly powered up; the Analog System Clock (ASYSCLK) is present; and that the bus cycles, triggers, and interrupts are correctly propagating between the Master, Control, and Analog subsystems.

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2.6 Master Subsystem NMIs

The Cortex™-M3 NMI Block generates an M3NMIINT non-maskable interrupt to the Cortex™-M3 CPU and an M3NMI event to the NMI Watchdog in response to potentially critical conditions existing inside or outside the Concerto™ MCU. When able to respond to the M3NMIINT interrupt, the Cortex™-M3 CPU may address the NMI condition and disable the NMI Watchdog. Otherwise, the NMI Watchdog counts out and an M3NMIRST reset signal is sent to the Resets block.

The inputs to the Cortex™-M3 NMI block include the C28NMIRST, PIENMIERR, CLOCKFAIL, ACIBERR, VREGWARN and EXTGPIO signals. The C28NMIRST comes from the C28x NMI Watchdog and it indicates that the C28x was not able to prevent the C28x NMI Watchdog counter from counting out. PIENMIERR indicates that an error condition was generated during the NMI vector fetch from the C28x Peripheral Interrupt Expansion (PIE) block. The CLOCKFAIL input comes from the Master Clocks Block, announcing a missing clock source to the Main Oscillator. ACIBERR indicates an abnormal condition inside the Analog Common Interface Bus. The VREGWARN input communicates a power anomaly. EXTGPIO comes from the GPIO_MUX1 to announce an external emergency.

The Cortex™-M3 NMI block can be accessed via the Cortex™-M3 NMI configuration registers—including the MNMIFLG, MNMIFLGCLR, and MNMIFLGFRC registers—to examine flag bits for the NMI sources, clear the flags, and force the flags to active state, respectively.

Figure 2-4 shows the Cortex™-M3 NMI and C28x NMI.

2.7 Control Subsystem NMIs

The C28x NMI Block generates a C28NMIINT non-maskable interrupt to the C28x CPU and a C28NMI event to the C28x NMI Watchdog in response to potentially critical conditions existing inside the Concerto™ MCU. When able to respond to the C28NMIINT interrupt, the C28x CPU may address the NMI condition and disable the C28x NMI Watchdog. Otherwise, the C28x NMI Watchdog counts out and the C28NMIRST reset signal is sent to the Resets block and the Cortex™-M3 NMI Block, where it can generate an NMI to the Cortex™-M3 processor.

The inputs to the C28x NMI block include the CLOCKFAIL, ACIBERR, RAMUNCERR, FLASHUNCERR, and PIENMIERR signals. The CLOCKFAIL input comes from the Clocks Block, announcing a missing clock source to the Main Oscillator. ACIBERR indicates an abnormal condition inside the Analog Common Interface Bus. The RAMUCERR and FLASHUNCERR announce the occurrence of uncorrectable error conditions during access to the Flash or RAM (local or shared). PIENMIERR indicates that an error condition was generated during NMI vector fetch from the C28x Peripheral Interrupt Expansion (PIE) block.

The C28x NMI block can be accessed via the C28x NMI configuration registers—including the CNMIFLG, CNMIFLGCLR, and CNMIFLGFRC registers—to examine flag bits for the NMI sources, clear the flags, and force the flags to active state, respectively.

Figure 2-4 shows the Cortex™-M3 NMI and C28x NMI.

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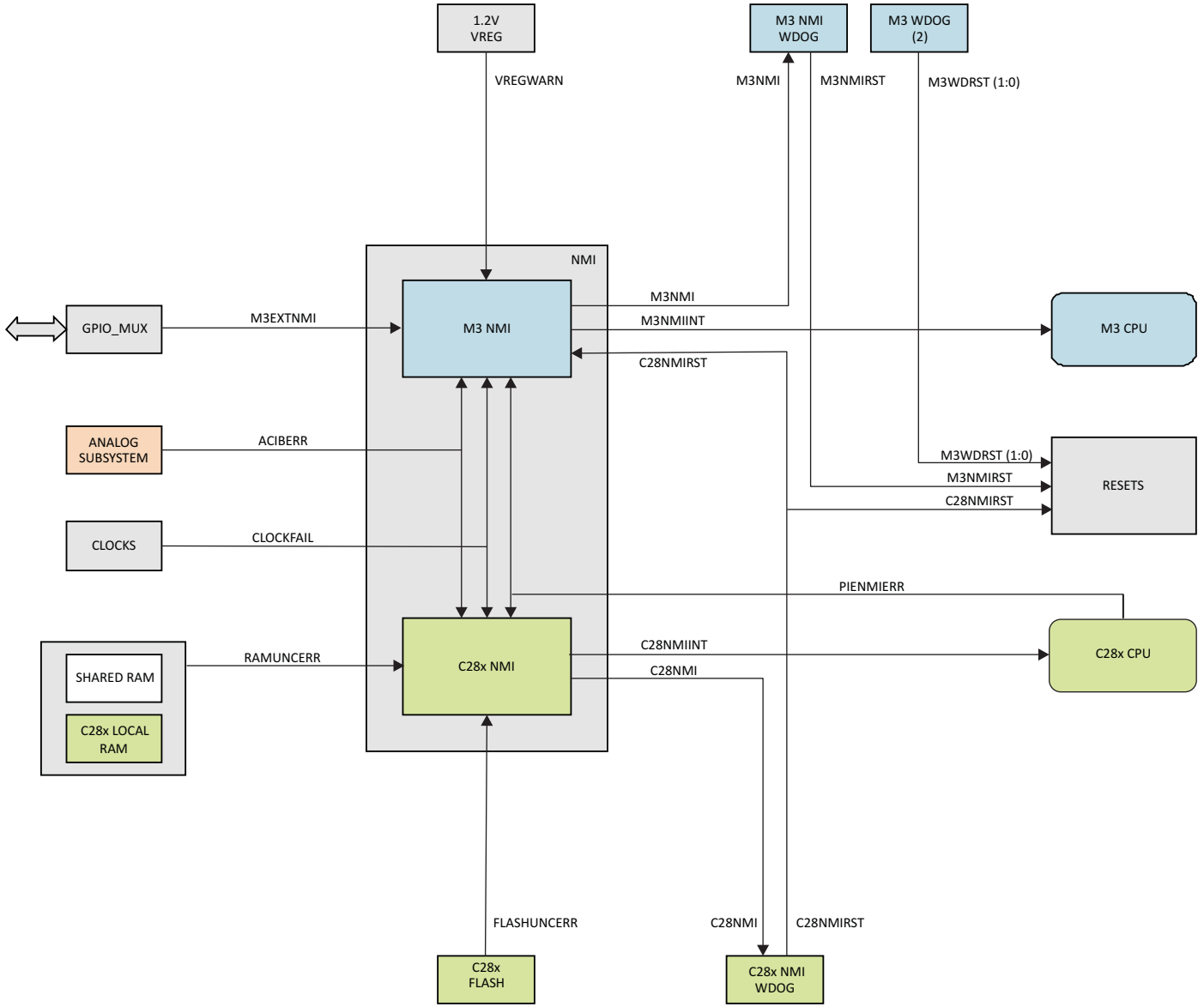

Figure 2-4. Cortex™-M3 NMI and C28x NMI

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2.8 Resets

The Concerto™ MCU has two external reset pins: $\overline{\text{XRS}}$ for the Master and Control Subsystems, and $\overline{\text{ARS}}$ for the Analog Subsystem. It is recommended that these two pins be externally tied together with a board signal trace.

The $\overline{\text{XRS}}$ pin can receive an external reset signal from outside into the chip, and it can drive a reset signal out from inside of the chip. A reset pulse driven into the $\overline{\text{XRS}}$ pin resets the Master and Control Subsystems. A reset pulse can also be driven out of the $\overline{\text{XRS}}$ pin by the voltage monitoring block of the Master and Control Subsystems. A reset pulse can be driven out of the $\overline{\text{XRS}}$ pin when the two Cortex™-M3 Watchdogs or the Cortex™-M3 NMI Watchdog time out.

The $\overline{\text{ARS}}$ pin can receive an external reset signal from outside into the chip, and it can drive a reset signal out from inside of the chip. A reset pulse driven into the $\overline{\text{ARS}}$ pin resets the Analog Subsystem. A reset pulse can be driven out of the $\overline{\text{ARS}}$ pin by the voltage monitoring block of the Analog Subsystem.

Figure 2-5 shows the resets.

2.8.1 Cortex™-M3 Resets

The Cortex™-M3 CPU and NVIC (Nested Vectored Interrupt Controller) are both reset by the POR (Power-On Reset) or the M3SYSRST reset signal. In both cases, the Cortex™-M3 CPU restarts program execution from the address provided by the reset entry in the vector table. A register can later be referenced to determine the source of the reset. The M3SYSRST signal also propagates to the Cortex™-M3 peripherals and the rest of the Cortex™-M3 Subsystem.

The $\overline{\text{M3SYSRST}}$ has four possible sources: $\overline{\text{XRS}}$, $\overline{\text{M3WDOGS}}$, $\overline{\text{M3SWRST}}$, and $\overline{\text{M3DBGRST}}$. The $\overline{\text{M3WDOGS}}$ is set in response to time-out conditions of the two Cortex™-M3 Watchdogs or the Cortex™-M3 NMI Watchdog. The $\overline{\text{M3SWRST}}$ is a software-generated reset output by the NVIC. The M3DBGRS is a debugger-generated reset that is also output by the NVIC. In addition to driving M3SYSRST, these two resets also propagate to the C28x Subsystem and the Analog Subsystem.

The M3RSNIN bit can be set inside the CRESCNF register to selectively reset the C28x Subsystem from the Cortex™-M3, and ACIBRST bit of the same register selectively resets the Analog Common Interface Bus. In addition to driving reset signals to other parts of the chip, the Cortex™-M3 can also detect a $\overline{\text{C28SYSRST}}$ reset being set inside the C28x Subsystem by reading the CRES bit of the CRESSTS register.

Cortex™-M3 software can also set bits in the SRCR register to selectively reset individual Cortex™-M3 peripherals, provided they are enabled inside the DC (Device Configuration) register. The Reset Cause register (MRESC) can be read to find out if the latest reset was caused by External Reset, VMON/POR/BOR, Watchdog Timer 0, Watchdog Timer 1, or Software Reset from NVIC.

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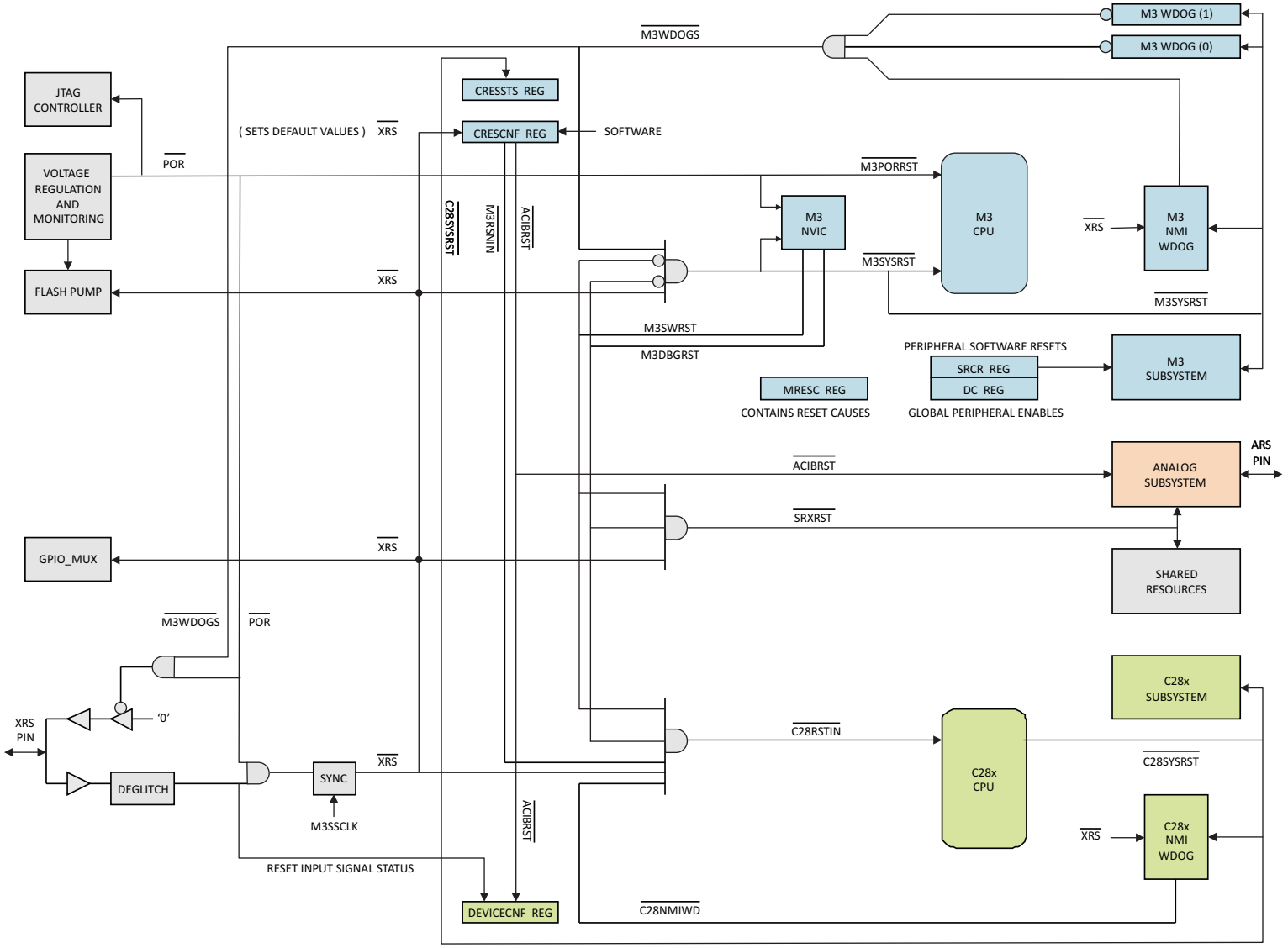

Figure 2-5. Resets

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2.8.2 C28x Resets

The C28x CPU is reset by the C28RSTIN signal, and the C28x CPU in turn resets the rest of the C28x Subsystem with the C28SYSRST signal. When reset, the C28x restarts program execution from the address provided at the top of the Boot ROM Vector Table.

The C28RSTIN has five possible sources: XRS, C28NMIWD, M3SWRST, M3DBGRST, and the M3RSNIN. The C28NMIWD is set in response to time-out conditions of the C28x NMI Watchdog. The M3SWRST is a software-generated reset output by the NVIC. The M3DBGRS is a debugger-generated reset that is also output by the NVIC. These two resets must be first enabled by the Cortex™-M3 processor in order to propagate to the C28x Subsystem. M3RSNIN reset comes from the Cortex™-M3 Subsystem to selectively reset the C28x Subsystem from Cortex™-M3 software.

The C28x processor can learn the status of the internal ACIBRST reset signal and the external XRS pin by reading the DEVICECNF register.

2.8.3 Analog Subsystem and Shared Resources Resets

Both the Analog Subsystem and the resources shared between the C28x and Cortex™-M3 subsystems (IPC, MSG RAM, Shared RAM) are reset by the SRXRST reset signal. Additionally, the Analog Subsystem is also reset by the internal ACIBRST signal from the Cortex™-M3 Subsystem and the external ARS pin (which should be externally tied to the XRS pin).

The SRXRST has three possible sources: XRS, M3SWRST, and M3DBGRST. The M3SWRST is a software-generated reset output by the NVIC. The M3DBGRS is a debugger-generated reset that is also output by the NVIC. These two resets must be first enabled by the Cortex™-M3 processor in order to propagate to the Analog Subsystem and the Shared Resources.

2.8.4 Device Boot Sequence

Concerto's boot sequence is used to configure the Master Subsystem and the Control Subsystem for execution of application code. It involves both internal resources, and resources external to the device. These resources include: Master Subsystem Bootloader code (M-Bootloader) factory-programmed inside the Master Subsystem Boot ROM (M-Boot ROM); Control Subsystem Bootloader code (C-Bootloader) factory-programmed inside the Control Subsystem Boot ROM (C-Boot ROM); three GPIO_MUX1 pins for Master boot mode selection; internal Flash and RAM memories; and selected Cortex™-M3 and C28x peripherals for loading the application code into the Master and Control Subsystems.

The boot sequence starts when the Master Subsystem comes out of reset. This can be caused by device power up, external reset, debugger reset, software reset, Cortex™-M3 watchdog reset, or Cortex™-M3 NMI watchdog reset. While the M-Bootloader starts executing first, the C-Bootloader starts soon after, and then both bootloaders work in tandem to configure the device, load application code for both processors (if not already in the Flash), and branch the execution of each processor to a selected location in the application code.

Execution of the M-Bootloader commences when an internal reset signal goes from active to inactive state. At that time, the Control Subsystem and the Analog Subsystem continue to be in reset state until the Master Subsystem takes them out of reset. The M-Bootloader first initializes some device-level functions, then it initializes the Master Subsystem. Next, the M-Bootloader takes the Control Subsystem and the Analog Subsystem/ACIB out of reset. When the Control Subsystem comes out of reset, its own C-Bootloader starts executing in parallel with the M-Bootloader. After initializing the Control Subsystem, the C-Bootloader enters the C28x processor into the idle mode (to wait for the M-Bootloader to wake it up later via the MTOCIPC1 interrupt). Next, the M-Bootloader reads three GPIO pins (see Table 2-17) to determine the boot mode for the rest of the M-Bootloader operation.

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Table 2-17. Master Subsystem Boot Mode Selection

Boot Mode #	Master Subsystem Boot Modes	PF3_GPIO35 (BOOT_2)	PG7_GPIO47 (BOOT_1)	PG3_GPIO43 (BOOT_0)
0	Boot from Parallel GPIO	0	0	0
1	Boot to Master Subsystem RAM	0	0	1
2	Boot from Master Subsystem serial peripherals (UART0/SSI0/I2C0)	0	1	0
3	Boot from Master Subsystem CAN interface	0	1	1
4	Boot from Master Subsystem Ethernet interface	1	0	0
5	Not supported (Defaults to Boot-to-Flash)	1	0	1
6	Not supported (Defaults to Boot-to-Flash)	1	1	0
7	Boot to Master Subsystem Flash memory	1	1	1

Boot Mode 7 causes the Master program to branch execution to the application in the Master Flash memory. This requires that the Master Flash be already programmed with valid code; otherwise, a hard fault exception is generated and the Cortex™-M3 goes back to the above reset sequence. (Therefore, for a factory-fresh device, the M-Bootloader will be in a continuous reset loop until the emulator is connected and a debug session started.) If the Master Subsystem Flash has already been programmed, the application code will start execution. Typically, the Master Subsystem application code will then establish data communication with the C28x [through the IPC (Interprocessor Communications peripheral)] to coordinate the rest of the boot process with the Control Subsystem. Boot Mode 7 typically does not require any external signals to drive the three boot mode pins, as by default, all three pins are internally pulled up to logic 1 (111b).

Boot Mode 1 causes the Master boot program to branch to Cortex™-M3 RAM, where it starts executing code that has been preloaded earlier. Typically, this mode is used during development of application code meant for Flash, but which has to be first tested running out of RAM. In this case, the user would typically load the application code into RAM using the debugger, and then issue a debugger reset, while setting the three boot pins to 001b. From that point on, the rest of the boot process on the Master Subsystem side is controlled by the application code.

Boot Modes 0, 2, 3, and 4 are used to load the Master application code from an external peripheral before branching to it. This is different from Boot Modes 7 and 1, where the application code was either already programmed in Flash or loaded into RAM by the emulator. If the boot mode selection pins are set to 000b, the M-Bootloader (running out of M-Boot ROM) will start uploading the Master application code from preselected Parallel GPIO_MUX1 pins. If the boot pins are set to 010b, the application code will be loaded from the Master Subsystem UART0, SSI0, or I2C0 peripheral. If the boot pins are set to 011b, the application code will be loaded from the Master Subsystem CAN interface. Furthermore, if the boot pins are set to 100b, the application code will be loaded through the Master Subsystem Ethernet interface.

Regardless of the type of boot mode selected, once the Master application code is resident in Master Flash or RAM, the next step for the M-Bootloader is to branch to it. At that point, the application code takes over control from the M-Bootloader, and the boot process continues as prescribed by the application code. At this stage, the Master application program typically establishes communication with the C-Bootloader, which by now, would have already initialized the Control Subsystem and forced the C28x to go into Idle mode. To wake the Control Subsystem out of Idle mode, the Master application issues the Master-to-Control-IPC-interrupt 1 (MTOCIPCINT1) . Once the data communication has been established through the IPC, the boot process can now also continue on the Control Subsystem side.

The rest of the Control Subsystem boot process is controlled by the Master Subsystem application issuing IPC instructions to the Control Subsystem, with the C-Bootloader interpreting the IPC commands and acting on them to continue the boot process. At this stage, a boot mode for the Control Subsystem can be established. The Control Subsystem boot modes are similar to the Master Subsystem boot modes, except for the mechanism by which they are selected. The Control Subsystem boot modes are chosen through the IPC commands from the Master application code to the C-Bootloader, which interprets them and acts

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accordingly. The choices are, as above, to branch to already existing Control application code in Flash, to branch to preloaded code in RAM (development mode), or to upload the Control application code from one of several available peripherals (see Table 2-18). As before, once the Control application is in place (in Flash or RAM), the C-Bootloader branches to it, and from that point on, the application code takes over.

Table 2-18. Control Subsystem Boot Mode Selection

Control Subsystem Boot Modes	MTOCIPCBOOTMODE Register Value	Description
BOOT_FROM_RAM	0x0000 0001	Upon receiving this command from the Master Subsystem, C-Boot ROM will branch to the Control Subsystem RAM entry point location and start executing code from there.
BOOT_FROM_FLASH	0x0000 0002	Upon receiving this command, C-Boot ROM will branch to the Control Subsystem FLASH entry point and start executing code from there.
BOOT_FROM_SCI	0x0000 0003	Upon receiving this command, C-Boot ROM will boot from the Control Subsystem SCI peripheral.
BOOT_FROM_SPI	0x0000 0004	Upon receiving this command, C-Boot ROM will boot from the Control Subsystem SPI interface.
BOOT_FROM_I2C	0x0000 0005	Upon receiving this command, C-Boot ROM will boot from the Control Subsystem I2C interface.
BOOT_FROM_PARALLEL	0x0000 0006	Upon receiving this command, C-Boot ROM will boot from the Control Subsystem GPIO.

The boot process can be considered completed once the Cortex™-M3 and C28x are both running out of their respective application programs. Note that following the boot sequence, the C-Bootloader is still available to interpret and act upon an assortment of IPC commands that can be issued from the Master Subsystem to perform a variety of configuration, housekeeping, and other functions. See the *Concerto F28M35x Technical Reference Manual* (literature number SPRUH22) for additional information on Concerto boot modes, IPC commands, and the underlying boot philosophy.

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2.9 Master Subsystem Clocking

The internal PLLSYSCLK clock, normally used as a source for all Master Subsystem clocks, is a divided-down output of the Main PLL or X1 external clock input, as defined by the SPLLCKEN bit of the SYSPLLCTL register.

There is also a second oscillator that internally generates two clocks: 32KHZCLK and 10MHZCLK. The 10MHZCLK is used by the Missing Clock Circuit to detect a possible absence of an external clock source to the Main Oscillator that drives the Main PLL. Detection of a missing clock results in a substitution of the 10MHZCLK for the PLLSYSCLK. CLKFAIL signal is also sent to the NMI Block and the Control Subsystem where it can trip the ePWM peripherals.

The 32KHZCLK and 10MMHZCLK clocks are also used by the Cortex™-M3 Subsystem as possible sources for the Deep Sleep Clock.

There are four registers associated with the Main PLL: SYSPLLCTL, SYSPLLMULT, SYSPLLSTAT and SYSDIVSEL. Typically, the Cortex™-M3 processor writes to these registers, while the C28x processor has read access. The C28x can request write access to the above registers through the CLKREQEST register. Cortex™-M3 can regain write ownership of these registers through the MCLKREQUEST register.

The Master Subsystem operates in one of three modes: Run Mode, Sleep Mode, or Deep Sleep Mode. Table 2-19 shows the Master Subsystem low-power modes and their effect on both CPUs, clocks, and peripherals. Figure 2-6 shows the Cortex™-M3 clocks and the Master Subsystem low-power modes.

Table 2-19. Master Subsystem Low-Power Modes

Cortex™-M3 Low-Power Mode	State of Cortex™-M3 CPU	Clock to Cortex™-M3 Peripherals	Register Used to Gate Clocks to Cortex™-M3 Peripherals	Main PLL	USB PLL	Clock to C28x	Clock to Shared Resources	Clock to Analog Subsystem
Run	Active	M3SSCLK(1)	RCGC	On	On	PLLSYSCLK(2)	PLLSYSCLK(2)	ASYSCLK(3)
Sleep	Stopped	M3SSCLK(1)	RCGC or SCGC(4)	On	On	PLLSYSCLK(2)	PLLSYSCLK(2)	ASYSCLK(3)
Deep Sleep	Stopped	M3DSDIVCLK(5)	RCGC or DCGC(4)	Off	Off	Off	Off	Off

(1) PLLSYSCLK or OSCCLK divided-down per the M3SSDIVSEL register. In case of a missing source clock, M3SSCLK becomes 10MHZCLK divided-down per the M3SSDIVSEL register.
(2) PLLSYSCLK normally refers to the output of the Main PLL divided-down per the SYSDIVSEL register. In case the PLL is bypassed, the PLLSYSCLK becomes the OSCCLK divided-down per the SYSDIVSEL register. In case of a missing source clock, the 10MHZCLK is substituted for the PLLSYSCLK.
(3) PLLSYSCLK or OSCCLK divided-down per the CCLKCTL register. In case of a missing source clock, ASYSCLK becomes 10MHZCLK.
(4) Depends on the ACG bit of the RCC register.
(5) 32KHZCLK or 10MHZCLK or OSCCLK chosen/divided-down per the DSLPCLKCFG register, then again divided by the M3SSDIVSEL register (source determined inside the DSLPCLKCFG register).

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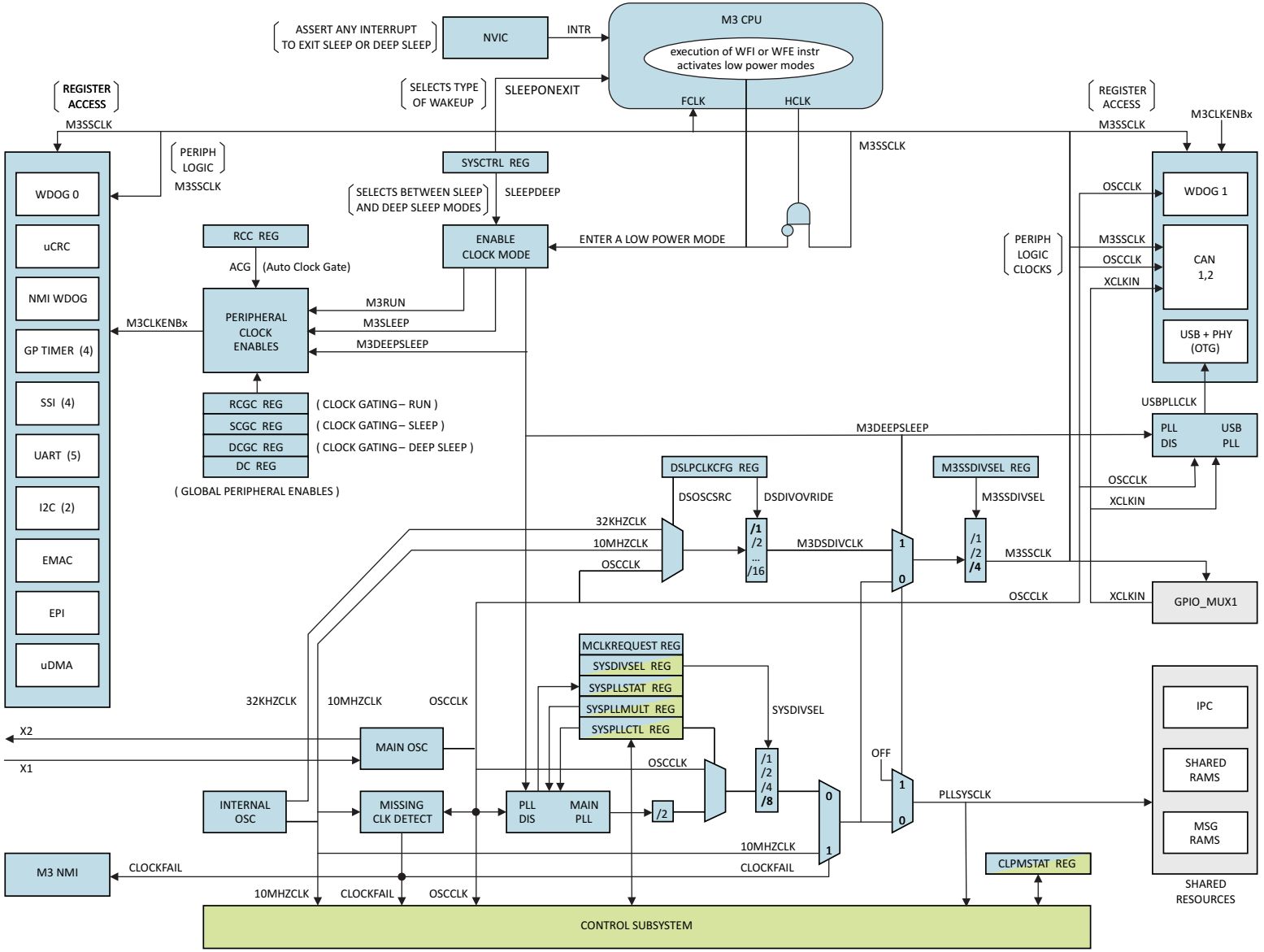

Figure 2-6. Cortex™-M3 Clocks and Low-Power Modes

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2.9.1 Cortex™-M3 Run Mode

In Run Mode, the Cortex™-M3 processor, memory, and most of the peripherals are clocked by the M3SSCLK, which is a divide-down version of the PLLSYSCLK (from Main PLL). The USB is clocked from a dedicated USB PLL, the CAN peripherals are clocked by M3SSCLK, OSCCLK, or XCLKIN, and one of two watchdogs (WDOG1) is also clocked by the OSCCLK. Clock selection for these peripherals is accomplished via corresponding peripheral configuration registers. Clock gating for individual peripherals is defined inside the RCGS register. RCGS, SCGS, and DCGS clock-gating settings only apply to peripherals that are enabled in a corresponding DC (Device Configuration) register.

Execution of the WFI instruction (Wait-for-Interrupt) shuts down the HCLK to the Cortex™-M3 CPU and forces the Cortex™-M3 Subsystem into Sleep or Deep Sleep low-power mode, depending on the state of the SLEEPDEEP bit of the Cortex™-M3 SYSCTRL register. To come out of a low-power mode, any properly configured interrupt event terminates the Sleep or Deep Sleep Mode and returns the Cortex™-M3 processor/subsystem to Run Mode.

2.9.2 Cortex™-M3 Sleep Mode

In Sleep Mode, the Cortex™-M3 processor and memory are prevented from clocking, and thus the code is no longer executing. The gating for the peripheral clocks may change based on the ACG bit of the RCC register. When ACG = 0, the peripheral clock gating is used as defined by the RCGS registers (same as in Run Mode); and when ASC = 1, the clock gating comes from the SCGS register. RCGS and SCGS clock-gating settings only apply to peripherals that are enabled in a corresponding DC register. Peripheral clock frequency for the enabled peripherals in Sleep Mode is the same as during the Run Mode.

Sleep Mode is terminated by any properly configured interrupt event. Exiting from the Sleep Mode depends on the Sleeponexit bit of the SYSCTRL register. When the Sleeponexit bit is 1, the processor will temporarily wake up only for the duration of the ISR of the interrupt causing the wake-up. After that, the processor goes back to Sleep Mode. When the Sleeponexit bit is 0, the processor wakes up permanently (for the ISR and thereafter).

2.9.3 Cortex™-M3 Deep Sleep Mode

In Deep Sleep Mode, the Cortex™-M3 processor and memory are prevented from clocking and thus the code is no longer executing. The Main PLL, USB PLL, ASYSCLK to the Analog Subsystem, and input clock to the C28x CPU and Shared Resources are turned off. The gating for the peripheral clocks may change based on the ACG bit of the RCC register. When ACG = 0, the peripheral clock gating is used as defined by the RCGS registers (same as in Run Mode); and when ASC = 1, the clock gating comes from the DCGS register. RCGS and DCGS clock gating settings only apply to peripherals that are enabled in a corresponding DC register.

Peripheral clock frequency for the enabled peripherals in Deep Sleep Mode is different from the Run Mode. One of three sources for the Deep Sleep clocks (32KHZCLK, 10MHZCLK, or OSCLK) is selected with the DSOSCSRC bits of the DSLPCLKCFG register. This clock is divided-down according to DSDIVOVRIDE bits of the DSLPCLKCFG register. The output of this Deep Sleep Divider is further divided-down per the M3SSDIVSEL bits of the D3SSDIVSEL register to become the Deep Sleep Clock. If 32KHXCLK or 10MHZCLK is selected in Deep Sleep mode, the internal oscillator circuit (that generates OSCCLK) is turned off.

The Cortex™-M3 processor should enter the Deep Sleep mode only after first confirming that the C28x is already in the Standby mode. Typically, just before entering the Standby mode, the C28x will record in the CLPMSTAT that it is about to do so. The Cortex™-M3 processor can read the CLPMSTAT register to check if the C28x is in Standby mode, and only then should it go into Deep Sleep. The reason for this is that the Deep Sleep mode shuts down the clock to C28x and its peripherals, and if this is not expected by the C28x, it could result in unintended consequences for some of its control peripherals.

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Deep Sleep Mode is terminated by any properly configured interrupt event. Exiting from the Deep Sleep Mode depends on the Sleeponexit bit of the SYSCTRL register. When the Sleeponexit bit is 1, the processor will temporarily wake up only for the duration of the ISR of the interrupt causing the wake-up. After that, the processor goes back to Deep Sleep Mode. When the Sleeponexit bit is 0, the processor wakes up permanently (for the ISR and thereafter).

2.10 Control Subsystem Clocking

The CLKIN input clock to the C28x processor is normally a divided-down output of the Main PLL or X1 external clock input. There are four registers associated with the Main PLL: SYSPLLCTL, SYSPLLMULT, SYSPLLSTAT and SYSDIVSEL. Typically, the Cortex™-M3 processor writes to these registers, while the C28x processor has read access. The C28x can request write access to the above registers through the CLKREQEST register. The Cortex™-M3 can regain write ownership of these registers through the MCLKREQUEST register.

Individual C28x peripherals can be turned on or off by gating C28SYSCLK to those peripherals. This is done via the CPCLKCR0,2,3 registers.

The C28x processor outputs two clocks: C28CPUCLK and C28SYSCLK.

The Control Subsystem operates in one of three modes: Normal Mode, Idle Mode, or Standby Mode. Table 2-20 shows the Control Subsystem low-power modes and their effect on the C28x CPU, clocks, and peripherals. Figure 2-7 shows the Control Subsystem clocks and low-power modes.

Table 2-20. Control Subsystem Low-Power Modes(1)

C28x Low-Power Mode	State of C28x CPU	C28CPUCLK(2)	C28SYSCLK(3)	Registers Used to Gate Clocks to C28x Peripherals
Normal	Active	On	On	CPCLKCR0,1,3
Idle	Stopped	Off	On	CPCLKCR0,1,3
Standby	Stopped	Off	Off	N/A

(1) The input clock to the C28x CPU is PLLSYSCLK from the Master Subsystem. This clock is turned off when the Master Subsystem enters the Deep Sleep mode.
(2) C28CPUCLK is an output from the C28x CPU and it clocks the C28x FPU, VCU, and PIE.
(3) C28SYSCLK is an output from the C28x CPU and it clocks C28x peripherals.

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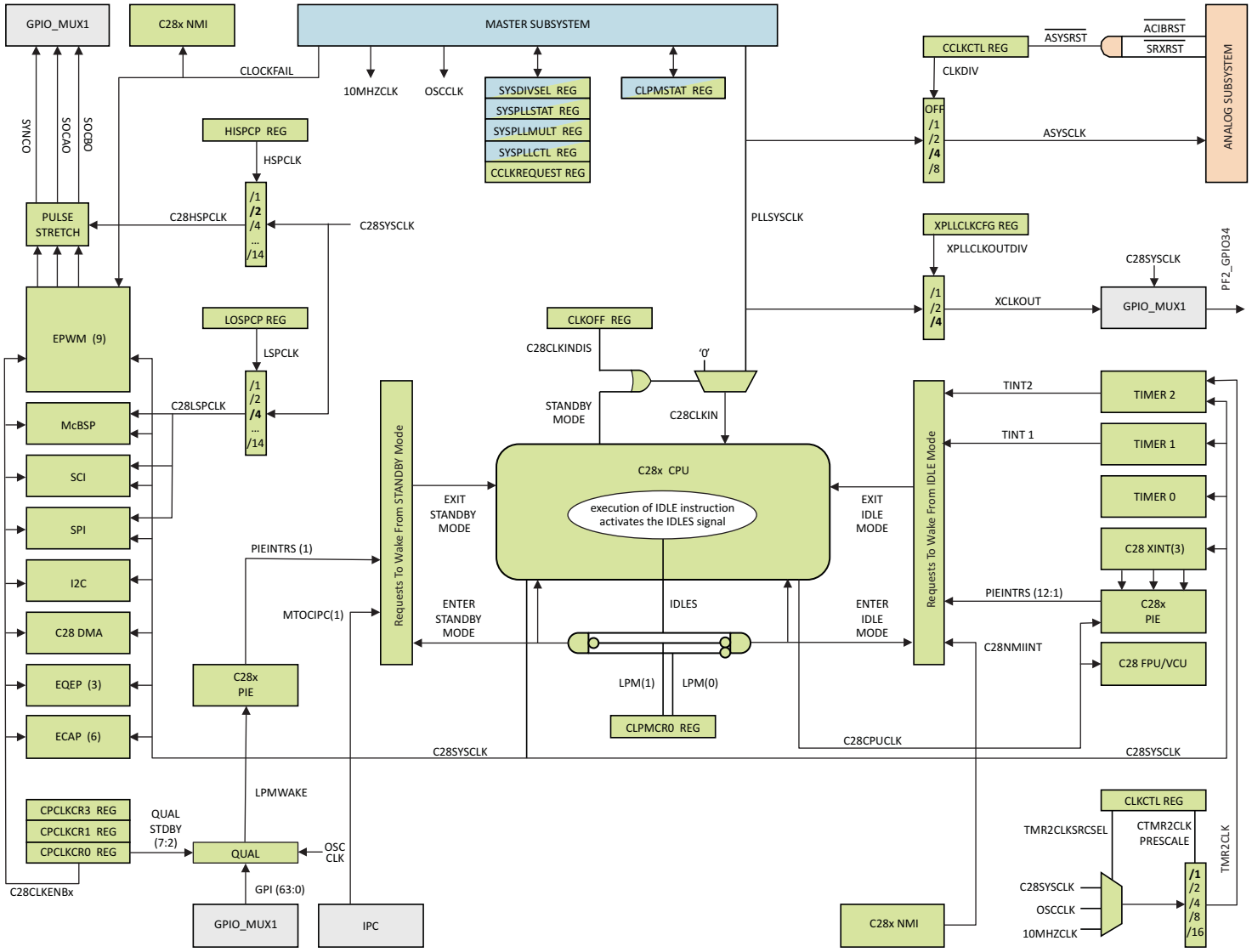

Figure 2-7. C28x Clocks and Low-Power Modes

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2.10.1 C28x Normal Mode

In Normal Mode, the C28x processor, Local Memory, and C28x peripherals are clocked by the C28SYSCLK, which is derived from the C28CLKIN input clock to the C28x processor. The FPU, VCU, and PIE are clocked by the C28CPUCLK, which is also derived from the C28CLKIN. Timer 2 can also be clocked by the TMR2CLK, which is a divided-down version of one of three source clocks—C28SYSCLK, OSCCLK, and 10MHZCLK—as selected by the CLKCTL register. Additionally, the LOSPCP register can be programmed to provide a dedicated clock (C28LSPCLK) to the SCI, SPI, and McBSP peripherals; and the HISPCP register can be programmed to provide a dedicated clock (C28HSPCLK) to stretch three outputs from ePWM peripherals.

Clock gating for individual peripherals is defined inside the CPCLKCR0,1,3 registers. Execution of the IDLE instruction stops the C28x processor from clocking and activates the IDLES signal. The IDLES signal is gated with two LPM bits of the CPCLKCR0 register to enter the C28x Subsystem into Idle mode or Standby Mode.

2.10.2 C28x Idle Mode

In Idle Mode, the C28x processor stops executing instructions and the C28CPUCLK is turned off. The C28SYSCLK continues to run. Exit from Idle Mode is accomplished by any enabled interrupt or the C28NMIINT (C28x non-maskable interrupt).

Upon exit from Idle Mode, the C28CPUCLK is restored. If LPMWAKE interrupt is enabled, the LPMWAKE ISR is executed. Next, the C28x processor starts fetching instructions from a location immediately following the IDLE instruction that originally triggered the Idle Mode.

2.10.3 C28x Standby Mode

In Standby Mode, the C28x processor stops executing instructions and the C28CLKIN, C28CPUCLK, and C28SYSCLK are turned off. Exit from Standby Mode is accomplished by one of 66 GPIOs from the GPIO_MUX1 block, or MTOCIPCINT1 (interrupt from MTOC IPC peripheral). The wakeup GPIO selected inside the GPIO_MUX block enters the Qualification Block as the LPMWAKE signal. Inside the Qualification Block, the LPMWAKE signal is sampled per the QUALSTDBY bits (bits [7:2] of the CPCLKCR0 register) before propagating into the wake request logic.

Cortex™-M3 should use CLPMSTAT register bits to tell the C28x to go into Standby mode before going into Deep Sleep mode. Otherwise, the clock to the C28x will be turned off suddenly when the control software is not expecting it to shut off. When the device is in Deep Sleep/Standby mode, wake-up should happen only from the Master Subsystem, since all C28x clocks are off (C28CLKIN, C28CPUCLK, C28SYSCLK), thus preventing the C28x from waking up first.

Upon exit from STANDBY Mode, the C28CLKIN, C28SYSCLK, and C28CPUCLK are restored. If the LPMWAKE interrupt is enabled, the LPMWAKE ISR is executed. Next, the C28x processor starts fetching instructions from a location immediately following the IDLE instruction that originally triggered the Standby Mode.

2.11 Analog Subsystem Clocking

The Analog Subsystem is clocked by ASYSCLK, which is a divided-down version of the PLLSYSCLK as defined by CLKDIV bits of the CCLKCTL register. The CCLKCTL register is exclusively accessible by the C28x processor, it is reset by $\overline{\text{ASYSRST}}$, which is derived from two Analog Subsystem resets—$\overline{\text{ACIBRST}}$ and $\overline{\text{SRXRST}}$. Therefore, while normally the C28x controls the frequency of ASYSCLK, it is possible for the Cortex™-M3 software to restore the ASYSCLK to its default value by resetting the Analog Subsystem.

The ASYSCLK is shut down when the Cortex™-M3 processor enters the Deep Sleep mode.

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2.12 Shared Resources Clocking

All Shared Resources (IPC, Shared RAMs, and Message RAMs) are clocked by PLLSYSCLK. The PLLSYSCLK normally refers to the output of the Main PLL divided-down per the SYSDIVSEL register. In case the PLL is bypassed, the PLLSYSCLK becomes the OSCCLK divided-down per the SYSDIVSEL register. In case of a missing source clock, the 10MHZCLK is substituted for the PLLSYSCLK.

2.13 GPIOs and Other Pins

Most Concerto external pins are shared among many internal peripherals. This is accomplished through several I/O muxes where a specific physical pin can be assigned to selected signals of internal peripherals.

Most of the I/O pins of the Concerto™ MCU can also be configured as programmable GPIOs. Exceptions include the X1 and X2 oscillator inputs; the $\overline{\text{XRS}}$ digital reset and $\overline{\text{ARS}}$ analog reset; the $\overline{\text{VREG12EN}}$ and $\overline{\text{VREG18EN}}$ internal voltage regulator enables; and five JTAG pins. The 74 primary GPIOs are grouped in 2 programmable blocks: GPIO_MUX1 block (66 pins) and GPIO_MUX2 block (8 pins). Additionally, eight secondary GPIOs are available through the AIO_MUX1 block (four pins) and AIO_MUX2 block (four pins). Figure 2-8 shows the GPIOs and other pins.

2.13.1 GPIO_MUX1

The 66 pins of the GPIO_MUX1 block can be selectively mapped through corresponding sets of registers to all Cortex™-M3 peripherals, all C28x peripherals, 12 ePWM Trip Inputs, 6 eCAP inputs, 3 External Interrupts to the C28x PIE, the C28x Standby Mode Wakeup signal (LMPWAKE), 64 General-Purpose Inputs or 64 General-Purpose Outputs, or a mixture of all of the above. Additionally, each GPIO_MUX1 pin can have a pullup enabled or disabled. By default, all pullups and outputs are disabled on reset, and all pins of the GPIO_MUX1 block are mapped to Cortex™-M3 peripherals (and not to C28x peripherals).

Figure 2-9 shows the internal structure of GPIO_MUX1. The blue blocks represent the Master Subsystem side of GPIO_MUX1, and the green blocks are the Control Subsystem side. The grey block in the center, Pin-Level Mux, is where the 66 GPIO_MUX1 pins are individually assigned between the two subsystems, based on how the configuration registers are programmed in the blue and green blocks (see Figure 2-10 for the configuration registers).

Pin-Level Mux assigns Master Subsystem peripheral signals, Control Subsystem peripheral signals, or GPIOs to the 66 Concerto pins. In addition to connecting peripheral I/Os of the two subsystems to pins, the Pin-Level Mux also provides other signals to the subsystems: XCLKIN and GPIO[H:A] IRQ signals to the Master Subsystem, plus GPTRIP[12:1] and GPI[63:0] signals to the Control Subsystem. XCLKIN carries a clock from an external pin to USB PLL and CAN modules. The eight GPIO[H:A] IRQ signals are interrupt requests from selected external pins to the NVIC interrupt controller. The 12 GPTRIP[12:1] signals carry trip events from selected external pins to C28x control peripherals—ePWM, eCAP, and eQEP. The 64 GPI[63:0] signals go to the C28x QUAL block, where any one of them can be selected and qualified to wake up the C28x CPU from Standby Low-Power Mode.

The configuration registers for the muxing of Master Subsystem peripherals are organized in nine sets (A–J), with each set being responsible for up to eight pins. These registers are programmable by the Cortex™-M3 CPU via the AHB bus or the APB bus. The configuration register for the muxing of Control Subsystem peripherals are organized in three sets (A–C), with each set being responsible for up to 32 pins. These registers are programmable by the C28x CPU via the C28x CPU bus. Figure 2-10 shows set A of the Master Subsystem GPIO configuration registers, set A of the Control Subsystem registers, and the muxing logic for one GPIO pin as driven by these registers.

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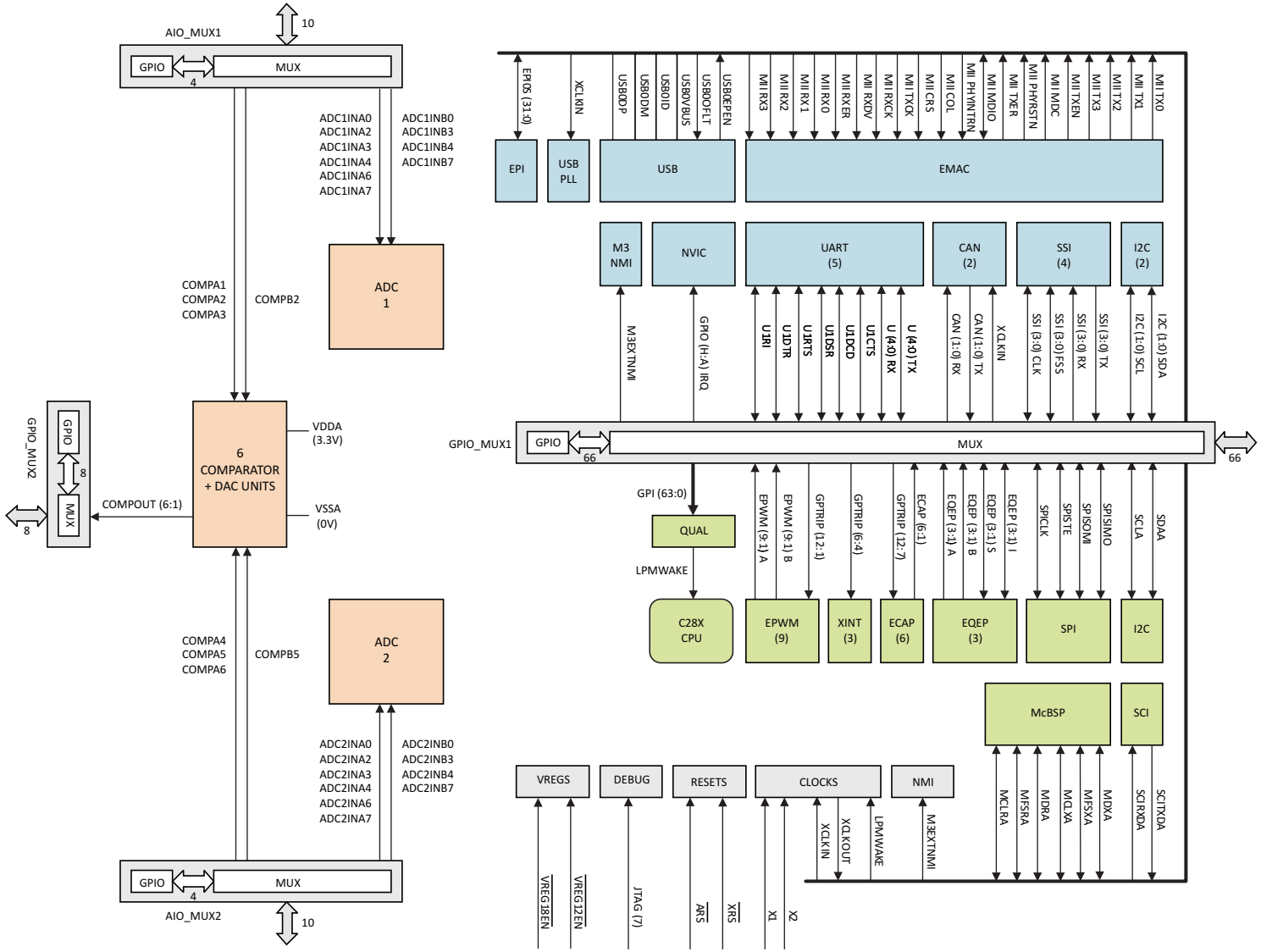

Figure 2-8. GPIOs and Other Pins

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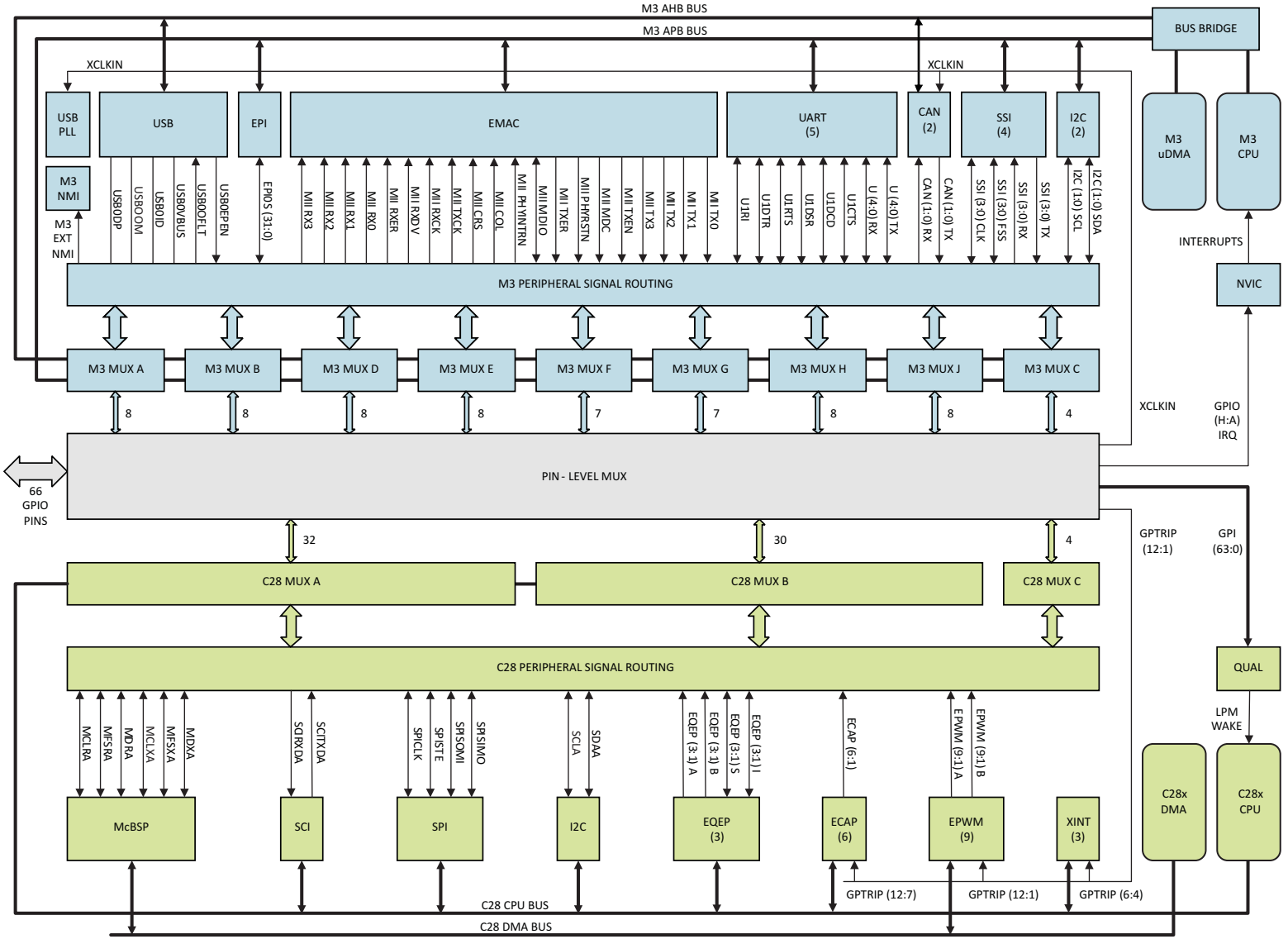

Figure 2-9. GPIO_MUX1 Block

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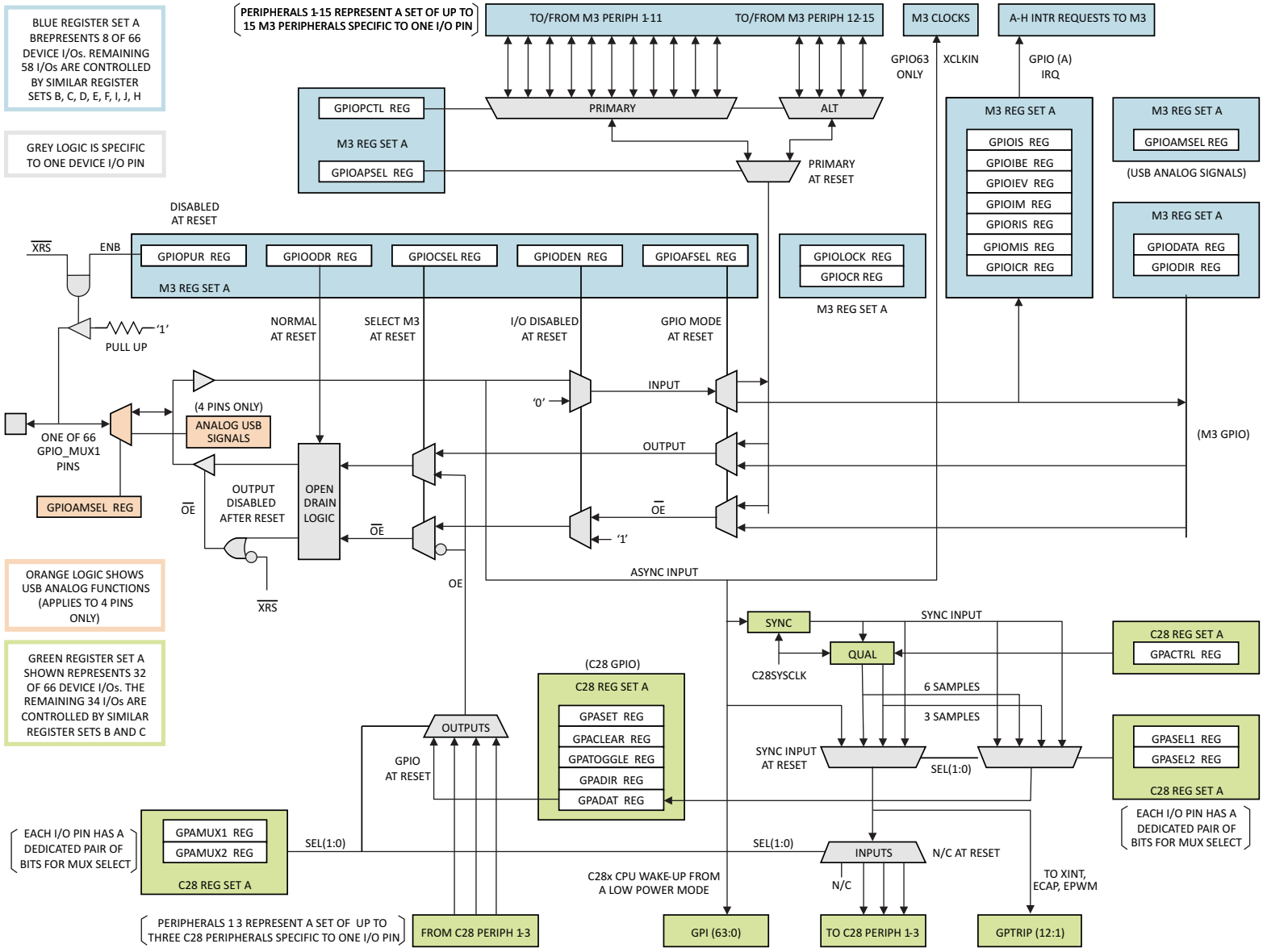

Figure 2-10. GPIO_MUX1 Pin Mapping Through Register Set A

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For each of the 8 pins in set A of the Cortex™-M3 GPIO registers, register GPIOPCTL selects between 1 of 11 possible primary Cortex™-M3 peripheral signals, or 1 of 4 possible alternate peripheral signals. Register GPIOAPSEL then picks one output to propagate further along the muxing chain towards a given pin. The input takes the reverse path. See Table 2-21 and Table 2-22 for the mapping of Cortex™-M3 peripheral pins to the 66 pins of GPIO_MUX1.

Similarly, on the C28x side, GPAMUX1 and GPAMUX2 registers select 1 of 4 possible C28x peripheral signals for each of 32 pins of set A. The selected C28x peripheral output then propagates further along the muxing chain towards a given pin. The input takes the reverse path. See Table 2-23 for the mapping of C28x peripheral pins to the 66 pins of GPIO_MUX1.

In addition to passing mostly digital signals, a few GPIO_MUX1 pins can also be assigned to analog signals. The GPIO Analog Mode Select (GPIOAMSEL) Register is used to assign four pins to analog USB signals. PF6_GPIO38 becomes USB0VBUS, PG2_GPIO42 becomes USB0DM, PG5_GPIO45 becomes USB0DP, and PG6_GPIO46 becomes USB0ID. When analog mode is selected, the corresponding pins are not available for digital GPIO_MUX1 options as described above.

Another special case is the External Oscillator Input signal (XCLKIN). This signal, available through pin PJ7_GPIO63, is directly tied to USBPLLCLK (clock input to USB PLL) and two CAN modules. It is always available at these modules where it can be selected through local registers.

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Table 2-21. GPIO_MUX1 Pin Assignments (M3 Primary Modes)(1)

Analog Mode (USB Pins)	Device Pin Name	M3 Primary Mode 1	M3 Primary Mode 2	M3 Primary Mode 3	M3 Primary Mode 4	M3 Primary Mode 5	M3 Primary Mode 6	M3 Primary Mode 7	M3 Primary Mode 8	M3 Primary Mode 9	M3 Primary Mode 10	M3 Primary Mode 11
–	PA0_GPIO0	U0RX	–	–	–	–	–	–	I2C1SCL	U1RX	–	–
–	PA1_GPIO1	U0TX	–	–	–	–	–	–	I2C1SDA	U1TX	–	–
–	PA2_GPIO2	SSI0CLK	–	MMI_TXD2	–	–	–	–	–	–	–	–
–	PA3_GPIO3	SSI0FSS	–	MMI_TXD1	–	–	–	–	–	–	–	–
–	PA4_GPIO4	SSI0RX	–	MMI_TXD0	–	CAN0RX	–	–	–	–	–	–
–	PA5_GPIO5	SSI0TX	–	MMI_RXDV	–	CAN0TX	–	–	–	–	–	–
–	PA6_GPIO6	I2C1SCL	CCP1	MMI_RXCK	–	–	CAN0RX	–	USB0EPEN	U1CTS	–	–
–	PA7_GPIO7	I2C1SDA	CCP4	MMI_RXER	–	–	CAN0TX	CCP3	USB0PFLT	U1DCD	–	–
–	PB0_GPIO8	CCP0	–	–	–	U1RX	–	–	–	–	–	–
–	PB1_GPIO9	CCP2	–	–	CCP1	U1TX	–	–	–	–	–	–
–	PB2_GPIO10	I2C0SCL	–	–	CCP3	CCP0	–	–	USB0EPEN	–	–	–
–	PB3_GPIO11	I2C0SDA	–	–	–	–	–	–	USB0PFLT	–	–	–
–	PB4_GPIO12	–	–	–	U2RX	CAN0RX	–	U1RX	EPI0S23	–	–	–
–	PB5_GPIO13	–	CCP5	CCP6	CCP0	CAN0TX	CCP2	U1TX	EPI0S22	–	–	–
–	PB6_GPIO14	CCP1	CCP7	–	–	–	CCP5	–	–	–	–	–
–	PB7_GPIO15	–	–	–	NMI	–	–	MII_RXD1	–	–	–	–
–	PD0_GPIO16	PWM0	CAN0RX	–	U2RX	U1RX	CCP6	MII_RXDV	–	U1CTS	–	–
–	PD1_GPIO17	PWM1	CAN0TX	–	U2TX	U1TX	CCP7	MII_TXER	–	U1DCD	CCP2	–
–	PD2_GPIO18	U1RX	CCP6	–	CCP5	–	–	–	EPI0S20	–	–	–
–	PD3_GPIO19	U1TX	CCP7	–	CCP0	–	–	–	EPI0S21	–	–	–
–	PD4_GPIO20	CCP0	CCP3	–	MII_TXD3	–	–	–	–	U1RI	EPI0S19	–
–	PD5_GPIO21	CCP2	CCP4	–	MII_TXD2	–	–	–	–	U2RX	EPI0S28	–
–	PD6_GPIO22	Fault0	–	–	MII_TXD1	–	–	–	–	U2TX	EPI0S29	–
–	PD7_GPIO23	IDX0	–	CCP1	MII_TXD0	–	–	–	–	U1DTR	EPI0S30	–
–	PE0_GPIO24	PWM4	SSI1CLK	CCP3	–	–	–	–	EPI0S8	USB0PFLT	–	–
–	PE1_GPIO25	PWM5	SSI1FSS	–	CCP2	CCP6	–	–	EPI0S9	–	–	–
–	PE2_GPIO26	CCP4	SSI1RX	–	–	CCP2	–	–	EPI0S24	–	–	–
–	PE3_GPIO27	CCP1	SSI1TX	–	–	CCP7	–	–	EPI0S25	–	–	–
–	PE4_GPIO28	CCP3	–	–	–	U2TX	CCP2	MII_RXD0	–	–	–	–
–	PE5_GPIO29	CCP5	–	–	–	–	–	–	–	–	–	–
–	PE6_GPIO30	–	–	–	–	–	–	–	–	U1CTS	–	–
–	PE7_GPIO31	–	–	–	–	–	–	–	–	U1DCD	–	–

(1) Blank fields represent Reserved functions.

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Table 2-21. GPIO_MUX1 Pin Assignments (M3 Primary Modes)[(1)] (continued)

Analog Mode (USB Pins)	Device Pin Name	M3 Primary Mode 1	M3 Primary Mode 2	M3 Primary Mode 3	M3 Primary Mode 4	M3 Primary Mode 5	M3 Primary Mode 6	M3 Primary Mode 7	M3 Primary Mode 8	M3 Primary Mode 9	M3 Primary Mode 10	M3 Primary Mode 11
–	PF0_GPIO32	CAN1RX	–	–	MII_RXCK	–	–	–	–	U1DSR	–	–
–	PF1_GPIO33	CAN1TX	–	–	MII_RXER	–	–	–	–	U1RTS	CCP3	–
–	PF2_GPIO34	–	–	$\overline{\text{MII\_PHYINTR}}$	–	–	–	–	–	SSI1CLK	–	–
–	PF3_GPIO35	–	–	MII_MDC	–	–	–	–	–	SSI1FSS	–	–
–	PF4_GPIO36	CCP0	–	MII_MDIO	–	–	–	–	EPI0S12	SSI1RX	–	–
–	PF5_GPIO37	CCP2	–	MII_RXD3	–	–	–	–	EPI0S15	SSI1TX	–	–
USB0VBUS	PF6_GPIO38	CCP1	–	MII_RXD2	–	–	–	–	–	–	U1RTS	–
–	PF7_GPIO39 (no pin)	–	–	–	–	–	–	–	–	–	–	–
–	PG0_GPIO40	U2RX	–	I2C1SCL	–	–	–	USB0EPEN	EPI0S13	–	–	–
–	PG1_GPIO41	U2TX	–	I2C1SDA	–	–	–	–	EPI0S14	–	–	–
USB0DM	PG2_GPIO42	–	–	MII_COL	–	–	–	–	–	–	–	–
–	PG3_GPIO43	–	–	MII_CRS	–	–	–	–	–	–	–	–
–	PG4_GPIO44 (no pin)	–	–	–	–	–	–	–	–	–	–	–
USB0DP	PG5_GPIO45	CCP5	–	MII_TXEN	–	–	–	–	–	–	U1DTR	–
USB0ID	PG6_GPIO46	–	–	MII_TXCK	–	–	–	–	–	–	U1RI	–
–	PG7_GPIO47	–	–	MII_TXER	–	–	–	–	CCP5	EPI0S31	–	–
–	PH0_GPIO48	CCP6	–	$\overline{\text{MII\_PHYRST}}$	–	–	–	–	EPI0S6	–	–	–
–	PH1_GPIO49	CCP7	–	–	–	–	–	–	EPI0S7	–	–	–
–	PH2_GPIO50	–	–	–	–	–	–	–	EPI0S1	MII_TXD3	–	–
–	PH3_GPIO51	–	–	–	USB0EPEN	–	–	–	EPI0S0	MII_TXD2	–	–
–	PH4_GPIO52	–	–	–	USB0PFLT	–	–	–	EPI0S10	MII_TXD1	–	SSI1CLK
–	PH5_GPIO53	–	–	–	–	–	–	–	EPI0S11	MII_TXD0	–	SSI1FSS
–	PH6_GPIO54	–	–	–	–	–	–	–	EPI0S26	MII_RXDV	–	SSI1RX
–	PH7_GPIO55	–	–	MII_RXCK	–	–	–	–	EPI0S27	–	–	SSI1TX
–	PJ0_GPIO56	–	–	MII_RXER	–	–	–	–	EPI0S16	–	–	I2C1SCL
–	PJ1_GPIO57	–	–	–	–	–	–	–	EPI0S17	USB0PFLT	–	I2C1SDA
–	PJ2_GPIO58	–	–	–	–	–	–	–	EPI0S18	CCP0	–	–
–	PJ3_GPIO59	–	–	–	–	–	–	–	EPI0S19	U1CTS	CCP6	–
–	PJ4_GPIO60	–	–	–	–	–	–	–	EPI0S28	U1DCD	CCP4	–
–	PJ5_GPIO61	–	–	–	–	–	–	–	EPI0S29	U1DSR	CCP2	–
–	PJ6_GPIO62	–	–	–	–	–	–	–	EPI0S30	U1RTS	CCP1	–
–	PJ7_GPIO63/ XCLKIN	–	–	–	–	–	–	–	–	U1DTR	CCP0	–

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Table 2-21. GPIO_MUX1 Pin Assignments (M3 Primary Modes)[(1)] (continued)

Analog Mode (USB Pins)	Device Pin Name	M3 Primary Mode 1	M3 Primary Mode 2	M3 Primary Mode 3	M3 Primary Mode 4	M3 Primary Mode 5	M3 Primary Mode 6	M3 Primary Mode 7	M3 Primary Mode 8	M3 Primary Mode 9	M3 Primary Mode 10	M3 Primary Mode 11
–	PC0_GPIO64 (no pin)	–	–	–	–	–	–	–	–	–	–	–
–	PC1_GPIO65 (no pin)	–	–	–	–	–	–	–	–	–	–	–
–	PC2_GPIO66 (no pin)	–	–	–	–	–	–	–	–	–	–	–
–	PC3_GPIO67 (no pin)	–	–	–	–	–	–	–	–	–	–	–
–	PC4_GPIO68	CCP5	–	MII_TXD3	–	CCP2	CCP4	–	EPI0S2	CCP1	–	–
–	PC5_GPIO69	CCP1	–	–	–	CCP3	USB0EPEN	–	EPI0S3	–	–	–
–	PC6_GPIO70	CCP3	–	–	–	U1RX	CCP0	USB0PFLT	EPI0S4	–	–	–
–	PC7_GPIO71	CCP4	–	–	CCP0	U1TX	USB0PFLT	–	EPI0S5	–	–	–

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Table 2-22. GPIO_MUX1 Pin Assignments (M3 Alternate Modes)(1)

Analog Mode (USB Pins)	Device Pin Name	M3 Alternate Mode 12	M3 Alternate Mode 13	M3 Alternate Mode 14	M3 Alternate Mode 15
–	PA0_GPIO0	–	–	–	–
–	PA1_GPIO1	–	–	–	SSI1FSS
–	PA2_GPIO2	–	–	U1CTS	–
–	PA3_GPIO3	–	–	U1DCD	SSI1CLK
–	PA4_GPIO4	–	–	U1DSR	–
–	PA5_GPIO5	–	–	U1RTS	–
–	PA6_GPIO6	–	–	U1DTR	–
–	PA7_GPIO7	MII_RXD1	–	U1RI	–
–	PB0_GPIO8	–	SSI2TX	CAN1TX	U4TX
–	PB1_GPIO9	–	SSI2RX	–	–
–	PB2_GPIO10	–	SSI2CLK	CAN1RX	U4RX
–	PB3_GPIO11	–	SSI2FSS	U1RX	–
–	PB4_GPIO12	–	–	CAN1TX	SSI1TX
–	PB5_GPIO13	–	–	CAN1RX	SSI1RX
–	PB6_GPIO14	MII_CRS	I2C0SDA	U1TX	SSI1CLK
–	PB7_GPIO15	–	I2C0SCL	U1RX	SSI1FSS
–	PD0_GPIO16	MII_RXD2	SSI0TX	CAN1TX	USB0EPEN
–	PD1_GPIO17	MII_COL	SSI0RX	CAN1RX	USB0PFLT
–	PD2_GPIO18	–	SSI0CLK	U1TX	CAN0RX
–	PD3_GPIO19	–	SSI0FSS	U1RX	CAN0TX
–	PD4_GPIO20	–	–	U3TX	CAN1TX
–	PD5_GPIO21	–	–	U3RX	CAN1RX
–	PD6_GPIO22	–	–	I2C1SDA	U1TX
–	PD7_GPIO23	–	–	I2C1SCL	U1RX
–	PE0_GPIO24	–	SSI3TX	CAN0RX	SSI1TX
–	PE1_GPIO25	–	SSI3RX	CAN0TX	SSI1RX
–	PE2_GPIO26	–	SSI3CLK	U2RX	SSI1CLK
–	PE3_GPIO27	–	SSI3FSS	U2TX	SSI1FSS
–	PE4_GPIO28	–	U0RX	–	USB0EPEN
–	PE5_GPIO29	MII_TXER	U0TX	–	USB0PFLT
–	PE6_GPIO30	MII_MDIO	CAN0RX	–	–
–	PE7_GPIO31	MII_RXD3	CAN0TX	–	–
–	PF0_GPIO32	–	I2C0SDA	–	–
–	PF1_GPIO33	–	I2C0SCL	–	–
–	PF2_GPIO34	–	–	–	XCLKOUT
–	PF3_GPIO35	–	U0TX	–	–
–	PF4_GPIO36	–	U0RX	–	–
–	PF5_GPIO37	–	–	–	–
USB0VBUS	PF6_GPIO38	–	–	–	–
–	PF7_GPIO39 (no pin)	–	–	–	–

(1) Blank fields represent Reserved functions.

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Table 2-22. GPIO_MUX1 Pin Assignments (M3 Alternate Modes)[(1)] (continued)

Analog Mode (USB Pins)	Device Pin Name	M3 Alternate Mode 12	M3 Alternate Mode 13	M3 Alternate Mode 14	M3 Alternate Mode 15
–	PG0_GPIO40	MII_RXD2	U4RX	–	–
–	PG1_GPIO41	MII_RXD1	U4TX	–	–
USB0DM	PG2_GPIO42	–	–	–	–
–	PG3_GPIO43	MII_RXDV	–	–	–
–	PG4_GPIO44 (no pin)	–	–	–	–
USB0DP	PG5_GPIO45	–	–	–	–
USB0ID	PG6_GPIO46	–	–	–	–
–	PG7_GPIO47	–	–	–	–
–	PH0_GPIO48	–	SSI3TX	–	–
–	PH1_GPIO49	MII_RXD0	SSI3RX	–	–
–	PH2_GPIO50	–	SSI3CLK	–	–
–	PH3_GPIO51	–	SSI3FSS	–	–
–	PH4_GPIO52	–	U3TX	–	–
–	PH5_GPIO53	–	U3RX	–	–
–	PH6_GPIO54	MII_TXEN	SSI0TX	–	–
–	PH7_GPIO55	MII_TXCK	SSI0RX	–	–
–	PJ0_GPIO56	–	SSI0CLK	–	–
–	PJ1_GPIO57	MII_RXDV	SSI0FSS	–	–
–	PJ2_GPIO58	MII_RXCK	SSI0CLK	U0TX	–
–	PJ3_GPIO59	MII_MDC	SSI0FSS	U0RX	–
–	PJ4_GPIO60	MII_COL	SSI1CLK	–	–
–	PJ5_GPIO61	MII_CRS	SSI1FSS	–	–
–	PJ6_GPIO62	$\overline{\text{MII\_PHYINTR}}$	U2RX	–	–
–	PJ7_GPIO63/ XCLKIN	$\overline{\text{MII\_PHYRST}}$	U2TX	–	–
–	PC0_GPIO64 (no pin)	–	–	–	–
–	PC1_GPIO65 (no pin)	–	–	–	–
–	PC2_GPIO66 (no pin)	–	–	–	–
–	PC3_GPIO67 (no pin)	–	–	–	–
–	PC4_GPIO68	–	–	–	–
–	PC5_GPIO69	–	–	–	–
–	PC6_GPIO70	–	–	–	–
–	PC7_GPIO71	–	–	–	–

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Table 2-23. GPIO_MUX1 Pin Assignments (C28x Peripheral Modes)(1)

Analog Mode (USB Pins)	Devices Pin Name	C28x Peripheral Mode 0	C28x Peripheral Mode 1	C28x Peripheral Mode 2	C28x Peripheral Mode 3
–	PA0_GPIO0	GPIO0	EPWM1A	–	–
–	PA1_GPIO1	GPIO1	EPWM1B	ECAP6	–
–	PA2_GPIO2	GPIO2	EPWM2A	–	–
–	PA3_GPIO3	GPIO3	EPWM2B	ECAP5	–
–	PA4_GPIO4	GPIO4	EPWM3A	–	–
–	PA5_GPIO5	GPIO5	EPWM3B	MFSRAO	ECAP1
–	PA6_GPIO6	GPIO6	EPWM4A	–	EPWMSYNCO
–	PA7_GPIO7	GPIO7	EPWM4B	MCLKRAO	ECAP2
–	PB0_GPIO8	GPIO8	EPWM5A	–	$\overline{\text{ADCSOCAO}}$
–	PB1_GPIO9	GPIO9	EPWM5B	–	ECAP3
–	PB2_GPIO10	GPIO10	EPWM6A	–	$\overline{\text{ADCSOCBO}}$
–	PB3_GPIO11	GPIO11	EPWM6B	–	ECAP4
–	PB4_GPIO12	GPIO12	EPWM7A	–	–
–	PB5_GPIO13	GPIO13	EPWM7B	–	–
–	PB6_GPIO14	GPIO14	EPWM8A	–	–
–	PB7_GPIO15	GPIO15	EPWM8B	–	–
–	PD0_GPIO16	GPIO16	SPISIMOAO	–	–
–	PD1_GPIO17	GPIO17	SPISOMIAO	–	–
–	PD2_GPIO18	GPIO18	SPICLKAO	–	–
–	PD3_GPIO19	GPIO19	SPISTEAO	–	–
–	PD4_GPIO20	GPIO20	EQEP1A	MDXA	–
–	PD5_GPIO21	GPIO21	EQEP1B	MDRA	–
–	PD6_GPIO22	GPIO22	EQEP1SO	MCLKXAO	–
–	PD7_GPIO23	GPIO23	EQEP1IO	MFSXAO	–
–	PE0_GPIO24	GPIO24	ECAP1	EQEP2A	–
–	PE1_GPIO25	GPIO25	ECAP2	EQEP2B	–
–	PE2_GPIO26	GPIO26	ECAP3	EQEP2IO	–
–	PE3_GPIO27	GPIO27	ECAP4	EQEP2SO	–
–	PE4_GPIO28	GPIO28	SCIRXDA	–	–
–	PE5_GPIO29	GPIO29	SCITXDA	–	–
–	PE6_GPIO30	GPIO30	–	–	EPWM9A
–	PE7_GPIO31	GPIO31	–	–	EPWM9B
–	PF0_GPIO32	GPIO32	SDAAOC	SCIRXDA	$\overline{\text{ADCSOCAO}}$
–	PF1_GPIO33	GPIO33	SCLAOC	EPWMSYNCO	$\overline{\text{ADCSOCBO}}$
–	PF2_GPIO34	GPIO34	ECAP1	SCIRXDA	XCLKOUT
–	PF3_GPIO35	GPIO35	SCITXDA	–	–
–	PF4_GPIO36	GPIO36	SCIRXDA	–	–
–	PF5_GPIO37	GPIO37	ECAP2	–	–
USB0VBUS	PF6_GPIO38	GPIO38	–	–	–
–	PF7_GPIO39 (no pin)	GPIO39	–	–	–

(1) Blank fields represent Reserved functions.

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Table 2-23. GPIO_MUX1 Pin Assignments (C28x Peripheral Modes)[(1)] (continued)

Analog Mode (USB Pins)	Devices Pin Name	C28x Peripheral Mode 0	C28x Peripheral Mode 1	C28x Peripheral Mode 2	C28x Peripheral Mode 3
–	PG0_GPIO40	GPIO40	–	–	–
–	PG1_GPIO41	GPIO41	–	–	–
USB0DM	PG2_GPIO42	GPIO42	–	–	–
–	PG3_GPIO43	GPIO43	–	–	–
–	PG4_GPIO44 (no pin)	GPIO44	–	–	–
USB0DP	PG5_GPIO45	GPIO45	–	–	–
USB0ID	PG6_GPIO46	GPIO46	–	–	–
–	PG7_GPIO47	GPIO47	–	–	–
–	PH0_GPIO48	GPIO48	ECAP5	–	–
–	PH1_GPIO49	GPIO49	ECAP6	–	–
–	PH2_GPIO50	GPIO50	EQEP1A	–	–
–	PH3_GPIO51	GPIO51	EQEP1B	–	–
–	PH4_GPIO52	GPIO52	EQEP1SO	–	–
–	PH5_GPIO53	GPIO53	EQEP1IO	–	–
–	PH6_GPIO54	GPIO54	SPISIMOAO	–	EQEP3A
–	PH7_GPIO55	GPIO55	SPISOMIAO	–	EQEP3B
–	PJ0_GPIO56	GPIO56	SPICLKAO	–	EQEP3SO
–	PJ1_GPIO57	GPIO57	SPISTEAO	–	EQEP3IO
–	PJ2_GPIO58	GPIO58	MCLKRAO	–	EPWM7A
–	PJ3_GPIO59	GPIO59	MFSRAO	–	EPWM7B
–	PJ4_GPIO60	GPIO60	–	–	EPWM8A
–	PJ5_GPIO61	GPIO61	–	–	EPWM8B
–	PJ6_GPIO62	GPIO62	–	–	EPWM9A
–	PJ7_GPIO63/ XCLKIN	GPIO63/XCLKIN	–	–	EPWM9B
–	PC0_GPIO64 (no pin)	GPIO64	–	–	–
–	PC1_GPIO65 (no pin)	GPIO65	–	–	–
–	PC2_GPIO66 (no pin)	GPIO66	–	–	–
–	PC3_GPIO67 (no pin)	GPIO67	–	–	–
–	PC4_GPIO68	GPIO68	–	–	–
–	PC5_GPIO69	GPIO69	–	–	–
–	PC6_GPIO70	GPIO70	–	–	–
–	PC7_GPIO71	GPIO71	–	–	–

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2.13.2 GPIO_MUX2

The eight pins of the GPIO_MUX2 block can be selectively mapped to eight General-Purpose Inputs, eight General-Purpose Outputs, or six COMPOUT outputs from the Analog Comparator peripheral. Each GPIO_MUX2 pin can have a pullup enabled or disabled. On reset, all pins of the GPIO_MUX2 block are configured as analog inputs, and the GPIO function is disabled. The GPIO_MUX2 block is programmed through a separate set of registers from those used to program GPIO_MUX1.

The multiple registers responsible for configuring the GPIO_MUX2 pins are organized in register set E. They are accessible by the C28x CPU only. The middle portion of Figure 2-11 shows set E of Control Subsystem registers, plus muxing logic for the associated eight GPIO pins. The GPEMUX1 register selects one of six possible digital output signals from analog comparators, or one of eight general-purpose GPIO digital outputs. The GPEPUD register disables pullups for the GPIO_MUX2 pins when a corresponding bit of that register is set to “1”. Other registers of set E allow reading and writing of the eight GPIO bits, as well as setting the direction for each of the bits (read or write). See Table 2-24 for the mapping of comparator outputs and GPIO to the eight pins of GPIO_MUX2.

Peripheral Modes 0, 1, 2, and 3 are chosen by setting selected bit pairs of GPIOEMUX1 register to “00”, “01”, “10”, and “11”, respectively. For example, setting bits 5–4 of the GPIOEMUX1 register to “00” (Peripheral Mode 0) assigns pin GPIO130 to internal signal GPIO130 (digital GPIO). Setting bits 5–4 of the GPIOEMUX1 register to “11” (Peripheral Mode 3) assigns pin GPIO130 to internal signal COMP6OUT coming from Analog Comparator 6. Peripheral Modes 1 and 2 are reserved and are not currently available.

Table 2-24. GPIO_MUX2 Pin Assignments (C28x Peripheral Modes)(1)

Device Pin Name	C28x Peripheral Mode 0	C28x Peripheral Mode 1	C28x Peripheral Mode 2	C28x Peripheral Mode 3
GPIO128	GPIO128	–	–	–
GPIO129	GPIO129	–	–	COMP1OUT
GPIO130	GPIO130	–	–	COMP6OUT
GPIO131	GPIO131	–	–	COMP2OUT
GPIO132	GPIO132	–	–	COMP3OUT
GPIO133	GPIO133	–	–	COMP4OUT
GPIO134	GPIO134	–	–	–
GPIO135	GPIO135	–	–	COMP5OUT

(1) Blank fields represent Reserved functions.

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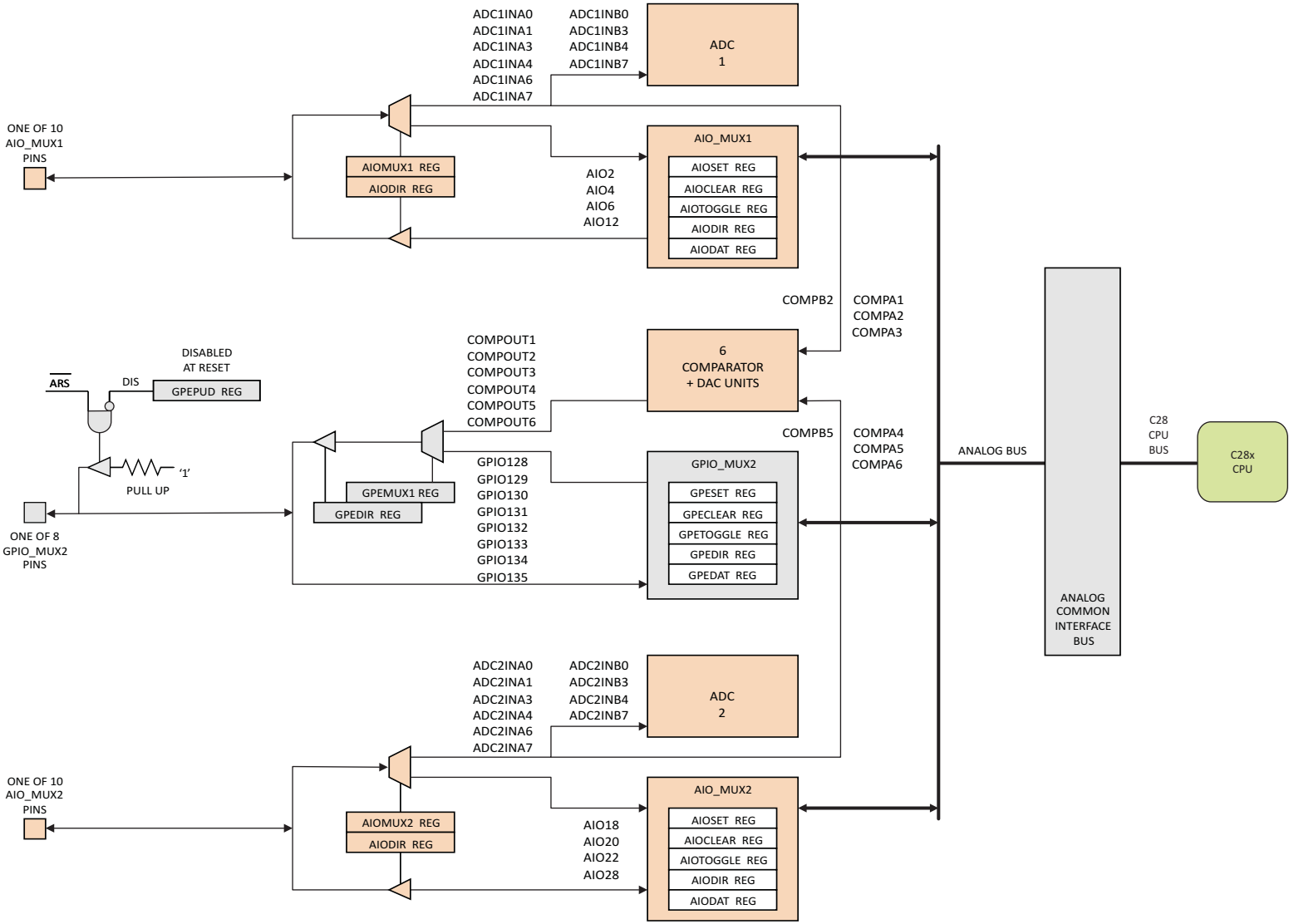

Figure 2-11. Pin Muxing on AIO_MUX1, AIO_MUX2, and GPIO_MUX2

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2.13.3 AIO_MUX1

The ten pins of AIO_MUX1 can be selectively mapped through a dedicated set of registers to ten analog inputs for ADC1 peripheral, six analog inputs for Comparator peripherals, four General-Purpose Inputs, or four General-Purpose Outputs. Note that while AIO_MUX1 has been named after the analog signals passing through it, the GPIOs (here called AIOs) are still digital, although with fewer features than those in the GPIO_MUX1 and GPIO_MUX2 blocks—for example, they do not offer pullups. On reset, all pins of the AIO_MUX1 block are configured as analog inputs and the GPIO function is disabled. The AIO_MUX1 block is programmed through a separate set of registers from those used to program AIO_MUX2.

The multiple registers responsible for configuring the AIO_MUX1 pins are accessible by the C28x CPU only. The top portion of Figure 2-11 shows Control Subsystem registers and muxing logic for the associated ten AIO pins. The AIOMUX1 register selects one of ten possible analog input signals or one of four general-purpose AIO inputs. Other registers allow reading and writing of the four AIO bits, as well as setting the direction for each of the bits (read or write). See Table 2-25 for the mapping of analog inputs and AIOs to the ten pins of AIO_MUX1.

AIO Mode 0 is chosen by setting selected odd bits of the AIOMUX1 register to '0'. AIO Mode 1 is chosen by setting selected odd bits of the AIOMUX1 register to '1'. For example, setting bit 5 of the AIOMUX1 register to '0' assigns pin ADC1INA2 to internal signal AIO2 (digital GPIO). Setting bit 5 of the AIOMUX1 register to '1' assigns pin ADC1INA2 to analog inputs ADC1INA2 or COMPA1 (only one should be enabled at a time in the respective analog module). Currently, all even bits of the AIOMUX1 register are "don't cares".

Table 2-25. AIO_MUX1 Pin Assignments (C28x AIO Modes)[1][2]

Device Pin Name	C28x AIO Mode 0[3]	C28x AIO Mode 1[4]
ADC1INA0	–	ADC1INA0
ADC1INA2	AIO2	ADC1INA2, COMPA1
ADC1INA3	–	ADC1INA3
ADC1INA4	AIO4	ADC1INA4, COMPA2
ADC1INA6	AIO6	ADC1INA6, COMPA3
ADC1INA7	–	ADC1INA7
ADC1INB0	–	ADC1INB0
ADC1INB3	–	ADC1INB3
ADC1INB4	AIO12	ADC1INB4, COMPB2
ADC1INB7	–	ADC1INB7

(1) Blank fields represent Reserved functions.
(2) For each field with two pins (e.g., ADC1INA2, COMPA1), only one pin should be enabled at a time; the other pin should be disabled. Use registers inside the respective destination analog peripherals to enable or disable these inputs.
(3) AIO Mode 0 represents digital general-purpose inputs or outputs.
(4) AIO Mode 1 represents analog inputs for ADC1 or the Comparator module.

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2.13.4 AIO_MUX2

The ten pins of AIO_MUX2 can be selectively mapped through a dedicated set of registers to ten analog inputs for ADC2 peripheral, six analog inputs for Comparator peripherals, four General-Purpose Inputs, or four General-Purpose Outputs. Note that while AIO_MUX2 has been named after the analog signals passing through it, the GPIOs (here called AIOs) are still digital, although with fewer features than those in the GPIO_MUX1 and GPIO_MUX2 blocks—for example, they do not offer pullups. On reset, all pins of the AIO_MUX2 block are configured as analog inputs and the GPIO function is disabled. The AIO_MUX2 block is programmed through a separate set of registers from those used to program AIO_MUX1.

The multiple registers responsible for configuring the AIO_MUX2 pins are accessible by the C28x CPU only. The bottom portion of Figure 2-11 shows Control Subsystem registers and muxing logic for the associated ten AIO pins. The AIOMUX2 register selects one of ten possible analog input signals or one of four general-purpose AIO inputs. Other registers allow reading and writing of the four AIO bits, as well as setting the direction for each of the bits (read or write). See Table 2-26 for the mapping of analog inputs and AIOs to the ten pins of AIO_MUX2. Peripheral Modes 1 and 2 are currently not available.

AIO Mode 0 is chosen by setting selected odd bits of the AIOMUX2 register to '0'. AIO Mode 1 is chosen by setting selected odd bits of the AIOMUX2 register to '1'. For example, setting bit 9 of the AIOMUX2 register to '0' assigns pin ADC2INA4 to internal signal AIO20 (digital GPIO). Setting bit 9 of the AIOMUX2 register to '1' assigns pin ADC2INA4 to analog inputs ADC2INA4 or COMPA5 (only one should be enabled at a time in the respective analog module). Currently, all even bits of the AIOMUX2 register are "don't cares".

Table 2-26. AIO_MUX2 Pin Assignments (C28x AIO Modes)(1)(2)

Device Pin Name	C28x AIO Mode 0(3)	C28x AIO Mode 1(4)
ADC2INA0	–	ADC2INA0
ADC2INA2	AIO18	ADC2INA2, COMPA4
ADC2INA3	–	ADC2INA3
ADC2INA4	AIO20	ADC2INA4, COMPA5
ADC2INA6	AIO22	ADC2INA6, COMPA6
ADC2INA7	–	ADC2INA7
ADC2INB0	–	ADC2INB0
ADC2INB3	–	ADC2INB3
ADC2INB4	AIO28	ADC2INB4, COMPB5
ADC2INB7	–	ADC2INB7

(1) Blank fields represent Reserved functions.
(2) For each field with two pins (e.g., ADC2INA6, COMPA6), only one pin should be enabled at a time; the other pin should be disabled. Use registers inside the respective destination analog peripherals to enable or disable these inputs.
(3) AIO Mode 0 represents digital general-purpose inputs or outputs.
(4) AIO Mode 1 represents analog inputs for ADC2 or the Comparator module.

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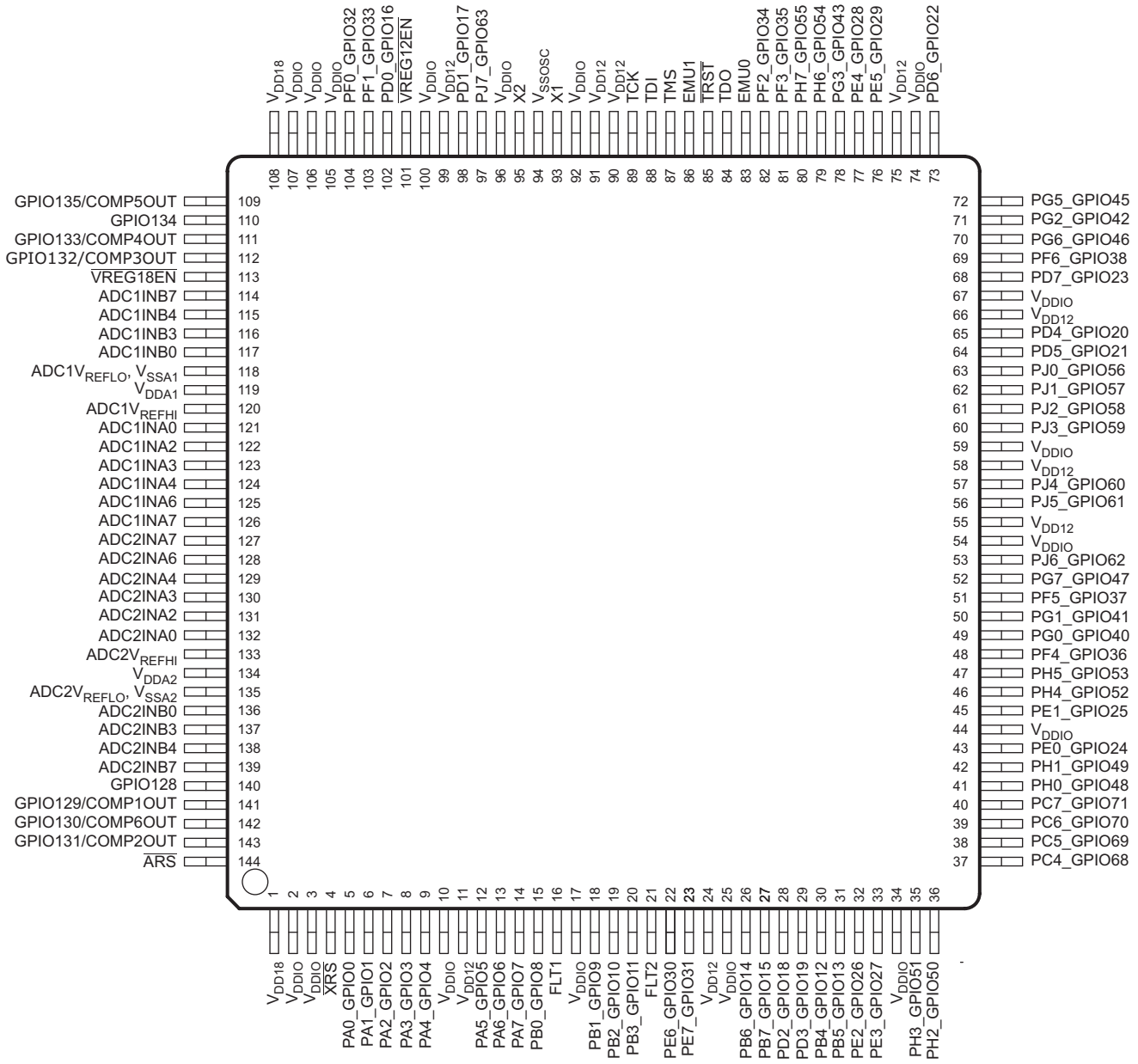
3 Device Pins

3.1 Pin Assignments

Figure 3-1 shows the 144-pin RFP PowerPAD™ Thermally Enhanced Thin Quad Flatpack (HTQFP) pin assignments.



A. See Table 3-1, Terminal Functions, for the complete multiplexed signal names.

Figure 3-1. 144-Pin RFP PowerPAD™ HTQFP (Top View)

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3.2 Terminal Functions

Table 3-1 describes the signals.

Table 3-1. Terminal Functions(1)

TERMINAL		I/O/Z(2)	DESCRIPTION
NAME	RFP PIN #		
ADC 1 Inputs, Analog Comparator Inputs, AIO Group 1			
$ADC1V_{REFHI}$	120	I	ADC1 External High Reference – only used when in ADC external reference mode.
$ADC1V_{REFLO}$, V_{SSA1}	118	I	ADC1 External Low Reference – only used when in ADC external reference mode, ADC1 Ground.
ADC1INA0	121	I	ADC1 Group A, Channel 0 input
ADC1INA2	122	I	ADC1 Group A, Channel 2 input
COMPA1		I	Comparator Input A1
AIO2		I/O	Digital AIO2
ADC1INA3	123	I	ADC1 Group A, Channel 3 input
ADC1INA4	124	I	ADC1 Group A, Channel 4 input
COMPA2		I	Comparator Input A2
AIO4		I/O	Digital AIO4
ADC1INA6	125	I	ADC1 Group A, Channel 6 input
COMPA3		I	Comparator Input A3
AIO6		I/O	Digital AIO6
ADC1INA7	126	I	ADC1 Group A, Channel 7 input
ADC1INB0	117	I	ADC1 Group B, Channel 0 input
ADC1INB3	116	I	ADC1 Group B, Channel 3 input
ADC1INB4	115	I	ADC1 Group B, Channel 4 input
COMPB2		I	Comparator Input B2
AIO12		I/O	Digital AIO12
ADC1INB7	114	I	ADC1 Group B, Channel 7 input
ADC 2 Inputs, Analog Comparator Inputs, AIO Group 2			
$ADC2V_{REFHI}$	133	I	ADC2 External High Reference – only used when in ADC external reference mode.
$ADC2V_{REFLO}$, V_{SSA2}	135	I	ADC2 External Low Reference – only used when in ADC external reference mode, ADC2 Ground.
ADC2INA0	132	I	ADC2 Group A, Channel 0 input
ADC2INA2	131	I	ADC2 Group A, Channel 2 input
COMPA4		I	Comparator Input A4
AIO18		I/O	Digital AIO18
ADC2INA3	130	I	ADC2 Group A, Channel 3 input
ADC2INA6	128	I	ADC2 Group A, Channel 6 input
COMPA6		I	Comparator Input A6
AIO22		I/O	Digital AIO22
ADC2INA4	129	I	ADC2 Group A, Channel 4 input
COMPA5		I	Comparator Input A5
AIO20		I/O	Digital AIO20

(1) Throughout this table, Master Subsystem signals are denoted by the color "blue"; Control Subsystem signals are denoted by the color "green"; and Analog Subsystem signals are denoted by the color "orange".
(2) I = Input, O = Output, Z = High Impedance, OD = Open Drain, ↑ = Pullup, ↓ = Pulldown

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Table 3-1. Terminal Functions[1] (continued)

TERMINAL		I/O/Z[2]	DESCRIPTION
NAME	RFP PIN #		
ADC2INA7	127	I	ADC2 Group A, Channel 7 input
ADC2INB0	136	I	ADC2 Group B, Channel 0 input
ADC2INB3	137	I	ADC2 Group B, Channel 3 input
ADC2INB4	138	I	ADC2 Group B, Channel 4 input
COMPB5		I	Comparator Input B5
AIO28		I/O	Digital AIO28
ADC2INB7	139	I	ADC2 Group B, Channel 7 input
Analog Comparator Results (Digital) and GPIO Group 2 (C28x Access Only)			
GPIO128	140	I/O	General-purpose input/output 128
GPIO129	141	I/O	General-purpose input/output 129
COMP1OUT		O	Compare result from Analog Comparator 1
GPIO130	142	I/O	General-purpose input/output 130
COMP6OUT		O	Compare result from Analog Comparator 6
GPIO131	143	I/O	General-purpose input/output 131
COMP2OUT		O	Compare result from Analog Comparator 2
GPIO132	112	I/O	General-purpose input/output 132
COMP3OUT		O	Compare result from Analog Comparator 3
GPIO133	111	I/O	General-purpose input/output 133
COMP4OUT		O	Compare result from Analog Comparator 4
GPIO134	110	I/O	General-purpose input/output 134
GPIO135	109	I/O	General-purpose input/output 135
COMP5OUT		O	Compare result from Analog Comparator 5
GPIO Group 1 and Peripheral Signals			
PA0_GPIO0	5	I/O/Z	General-purpose input/output 0
M_U0RX		I	UART-0 receive data
M_I2C1SCL		I/OD	I2C-1 clock open-drain bidirectional port
M_U1RX		I	UART-1 receive data
C_EPWM1A		O	Enhanced PWM-1 output A
PA1_GPIO1	6	I/O/Z	General-purpose input/output 1
M_U0TX		O	UART-0 transmit data
M_I2C1SDA		I/OD	I2C-1 data open-drain bidirectional port
M_U1TX		O	UART-1 data transmit
M_SSI1FSS		I/O	SSI-1 frame
C_EPWM1B		O	Enhanced PWM-1 output B
C_ECAP6		I/O	Enhanced Capture-6 input/output
PA2_GPIO2	7	I/O/Z	General-purpose input/output 2
M_SSI0CLK		I/O	SSI-0 clock
M_MIITXD2		O	EMAC MII transmit data bit 2
M_U1CTS		I	UART-1 clear-to-send modem status
C_EPWM2A		O	Enhanced PWM-2 output A

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Table 3-1. Terminal Functions[1] (continued)

TERMINAL		I/O/Z[2]	DESCRIPTION
NAME	RFP PIN #		
PA3_GPIO3	8	I/O/Z	General-purpose input/output 3
M_SSI0FSS		I/O	SSI-0 frame
M_MIITXD1		O	EMAC MII transmit data bit 1
M_U1DCD		I	UART-1 data carrier detect
M_SSI1CLK		I/O	SSI-1 clock
C_EPWM2B		O	Enhanced PWM-2 output B
C_ECAP5		I/O	Enhanced Capture-5 input/output
PA4_GPIO4	9	I/O/Z	General-purpose input/output 4
M_SSI0RX		I/O	SSI-0 clock
M_MIITXD0		O	EMAC MII transmit data bit 0
M_CAN0RX		I	CAN-0 receive data
M_U1DSR		I	UART-1 data set ready
C_EPWM3A		O	Enhanced PWM-3 output A
PA5_GPIO5	12	I/O/Z	General-purpose input/output 5
M_SSI0TX		O	SSI-0 transmit data
M_MIIRXDV		I	EMAC MII receive data valid
M_CAN0TX		O	CAN-0 transmit data
M_U1RTS		O	UART-1 request-to-send
C_EPWM3B		O	Enhanced PWM-3 output B
C_MFSRA		I	McBSP-A receive frame sync
C_ECAP1		I/O	Enhanced Capture-1 input/output
PA6_GPIO6	13	I/O/Z	General-purpose input/output 6
M_I2C1SCL		I/OD	I2C-1 clock open-drain bidirectional port
M_CCP1		I/O	Capture/Compare/PWM-1 (General-purpose Timer)
M_MIIRXCK		I	EMAC MII receive clock
M_CAN0RX		I	CAN-0 receive data
M_USB0EPEN		O	USB-0 external power enable (optionally used in host mode
M_U1CTS		I	UART-1 clear-to-send modem status
M_U1DTR		O	UART-1 data terminal ready
C_EPWM4A		O	Enhanced PWM-4 output A
C_EPWMSYNCO		O	Enhanced PWM-4 external sync pulse
PA7_GPIO7	14	I/O/Z	General-purpose input/output 7
M_I2C1SDA		I/OD	I2C-1 data open-drain bidirectional port
M_CCP4		I/O	Capture/Compare/PWM-4 (General-purpose Timer)
M_MIIRXER		I	EMAC MII receive error
M_CAN0TX		O	CAN-0 transmit data
M_CCP3		I/O	Capture/Compare/PWM-3 (General-purpose Timer)
M_USB0PFLT		I	USB-0 external power error state (optionally used in the host mode)
M_U1DCD		I	UART-1 data carrier detect
M_MII_RXD1		I	EMAC MII receive data 1
M_U1RI		I	UART-1 ring indicator status
C_EPWM4B		O	Enhanced PWM-4 output B
C_MCLKRA		I	McBSP-A receive clock
C_ECAP2		I/O	Enhanced Capture-1 input/output

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Table 3-1. Terminal Functions[1] (continued)

TERMINAL		I/O/Z[2]	DESCRIPTION
NAME	RFP PIN #		
PB0_GPIO8	15	I/O/Z	General-purpose input/output 8
M_CCP0		I/O	Capture/Compare/PWM-0 (General-purpose Timer)
M_U1RX		I	UART-1 data receive data
M_SSI2TX		O	SSI-2 transmit data
M_CAN1TX		O	CAN-1 transmit data
M_U4TX		O	UART-4 transmit data
C_EPWM5A		O	Enhanced PWM-5 output A
C_ADCSOCAO		O	ADC start-of-conversion A
PB1_GPIO9	18	I/O/Z	General-purpose input/output 9
M_CCP2		I/O	Capture/Compare/PWM-2 (General-purpose Timer)
M_CCP1		I/O	Capture/Compare/PWM-1 (General-purpose Timer)
M_U1TX		O	UART-1 transmit data
M_SSI2RX		I	SSI-2 receive data
C_EPWM5B		O	Enhanced PWM-5 output B
C_ECAP3		I/O	Enhanced Capture-3 input/output
PB2_GPIO10	19	I/O/Z	General-purpose input/output 10
M_I2C0SCL		I/OD	I2C-0 clock open-drain bidirectional port
M_CCP3		I/O	Capture/Compare/PWM-3 (General-purpose Timer)
M_CCP0		I/O	Capture/Compare/PWM-0 (General-purpose Timer)
M_USB0EPEN		O	USB-0 external power enable (optionally used in the host mode)
M_SSI2CLK		I/O	SSI-2 clock
M_CAN1RX		I	CAN-1 receive data
M_U4RX		I	UART-4 receive data
C_EPWM6A		O	Enhanced PWM-6 output A
C_ADCSOCBO		O	ADC start-of-conversion B
PB3_GPIO11	20	I/O/Z	General-purpose input/output 11
M_I2C0SDA		I/OD	I2C-0 data open-drain bidirectional port
M_USB0PFLT		I	USB-0 external power error state (optionally used in the host mode)
M_SSI2FSS		I/O	SSI-2 frame
M_U1RX		I	UART-1 receive data
C_EPWM6B		O	Enhanced PWM-6 output B
C_ECAP4		I/O	Enhanced Capture-4 input/output
PB4_GPIO12	30	I/O/Z	General-purpose input/output 12
M_U2RX		I	UART-2 receive data
M_CAN0RX		I	CAN-0 receive data
M_U1RX		I	UART-1 receive data
M_EPIOS23		I/O	EPI-0 signal 23
M_CAN1TX		O	CAN-1 transmit data
M_SSI1TX		O	SSI-1 transmit data
C_EPWM7A		O	Enhanced PWM-7 output A

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Table 3-1. Terminal Functions[1] (continued)

TERMINAL		I/O/Z[2]	DESCRIPTION
NAME	RFP PIN #		
PB5_GPIO13	31	I/O/Z	General-purpose input/output 13
M_CCP5		I/O	Capture/Compare/PWM-5 (General-purpose Timer)
M_CCP6		I/O	Capture/Compare/PWM-6 (General-purpose Timer)
M_CCP0		I/O	Capture/Compare/PWM-0 (General-purpose Timer)
M_CAN0TX		O	CAN-0 transmit data
M_CCP2		I/O	Capture/Compare/PWM-2 (General-purpose Timer)
M_U1TX		O	UART-1 transmit data
M_EPI0S22		I/O	EPI-0 signal 22
M_CAN1RX		I	CAN-1 receive data
M_SSI1RX		I	SSI-1 receive data
C_EPWM7B		O	Enhanced PWM-7 output B
PB6_GPIO14	26	I/O/Z	General-purpose input/output 14
M_CCP1		I/O	Capture/Compare/PWM-1 (General-purpose Timer)
M_CCP7		I/O	Capture/Compare/PWM-7 (General-purpose Timer)
M_CCP5		I/O	Capture/Compare/PWM-5 (General-purpose Timer)
M_MIICRS		I	EMAC MII carrier sense
M_I2C0SDA		I/OD	I2C-0 data open-drain bidirectional port
M_U1TX		O	UART-1 transmit data
M_SSI1CLK		I/O	EMAC MII carrier sense
C_EPWM8A		O	Enhanced PWM-8 output A
PB7_GPIO15	27	I/O/Z	General-purpose input/output 15
M_EXTNMI		I	Cortex™-M3 external non-maskable interrupt
M_MIIRXD1		I	EMAC MII receive data 1
M_I2C0SCL		I/OD	I2C-0 clock open-drain bidirectional port
M_U1RX		I	UART-1 receive data
M_SSI1FSS		I/O	SSI-1 frame
C_EPWM8B		O	Enhanced PWM-8 output B
PD0_GPIO16	102	I/O/Z	General-purpose input/output 16
M_CAN0RX		I	CAN-0 receive data
M_U2RX		I	UART-2 receive data
M_U1RX		I	UART-1 receive data
M_CCP6		I/O	Capture/Compare/PWM-6 (General-purpose Timer)
M_MIIRXDV		I	EMAC MII receive data valid
M_U1CTS		I	UART-1 clear-to-send modem status
M_MIIRXD2		I	EMAC MII receive data 2
M_SSI0TX		O	SSI-0 transmit data
M_CAN1TX		O	CAN-1 transmit data
M_USB0EPEN		O	USB-0 external power enable (optionally used in the host mode)
C_SPISIMOA		I/O	SPI-A slave in, master out

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Table 3-1. Terminal Functions[1] (continued)

TERMINAL		I/O/Z[2]	DESCRIPTION
NAME	RFP PIN #		
PD1_GPIO17	98	I/O/Z	General-purpose input/output 17
M_CAN0TX		O	CAN-0 transmit data
M_U2TX		O	UART-2 transmit data
M_U1TX		O	UART-1 transmit data
M_CCP7		I/O	Capture/Compare/PWM-7 (General-purpose Timer)
M_MIITXER		O	EMAC MII transmit error
M_U1DCD		I	UART-1 data carrier detect
M_CCP2		I/O	Capture/Compare/PWM-2 (General-purpose Timer)
M_MIICOL		I	EMAC MII collision detect
M_SSI0RX		I	SSI-0 receive data
M_CAN1RX		I	CAN-1 receive data
M_USB0PFLT		I	USB-0 external power error state (optionally used in the host mode)
C_SPISOMIA		I/O	SPI-A master in, slave out
PD2_GPIO18	28	I/O/Z	General-purpose input/output 18
M_U1RX		I	UART-1 receive data
M_CCP6		I/O	Capture/Compare/PWM-6 (General-purpose Timer)
M_CCP5		I/O	Capture/Compare/PWM-5 (General-purpose Timer)
M_EPI0S20		I/O	EPI-0 signal 20
M_SSI0CLK		I/O	SSI-0 clock
M_U1TX		O	UART-1 transmit data
M_CAN0RX		I	CAN-0 receive data
C_SPICLKA		I/O	SPI-A clock
PD3_GPIO19	29	I/O/Z	General-purpose input/output 19
M_U1TX		O	UART-1 transmit data
M_CCP7		I/O	Capture/Compare/PWM-7 (General-purpose Timer)
M_CCP0		I/O	Capture/Compare/PWM-0 (General-purpose Timer)
M_EPI0S21		I/O	EPI-0 signal 21
M_SSI0FSS		I/O	SSI-0 frame
M_U1RX		I	UART-1 receive data
M_CAN0TX		O	CAN-0 transmit data
C_SPISTEA		I/O	SPI-A slave transmit enable
PD4_GPIO20	65	I/O/Z	General-purpose input/output 20
M_CCP0		I/O	Capture/Compare/PWM-0 (General-purpose Timer)
M_CCP3		I/O	Capture/Compare/PWM-3 (General-purpose Timer)
M_MIITXD3		O	EMAC MII transmit data 3
M_U1RI		I	UART-1 receive data
M_EPI0S19		I/O	EPI-0 signal 19
M_U3TX		O	UART-3 transmit data
M_CAN1TX		O	CAN-1 transmit data
C_EQEP1A		I	Enhanced QEP-1 input A
C_MDXA		O	McBSP-A transmit data

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Table 3-1. Terminal Functions[1] (continued)

TERMINAL		I/O/Z[2]	DESCRIPTION
NAME	RFP PIN #		
PD5_GPIO21	64	I/O/Z	General-purpose input/output 21
M_CCP2		I/O	Capture/Compare/PWM-2 (General-purpose Timer)
M_CCP4		I/O	Capture/Compare/PWM-4 (General-purpose Timer)
M_MIITXD2		O	EMAC MII transmit data 2
M_U2RX		I	UART-2 receive data
M_EPI0S28		I/O	EPI-0 signal 28
M_U3RX		I	UART-3 receive data
M_CAN1RX		I	CAN-1 receive data
C_EQEP1B		I	Enhanced QEP-1 input B
C_MDRA		I	McBSP-A receive data
PD6_GPIO22	73	I/O/Z	General-purpose input/output 22
M_MIITXD1		O	EMAC MII transmit data 1
M_U2TX		O	UART-2 transmit data
M_EPI0S29		I/O	EPI-0 signal 29
M_I2C1SDA		I/OD	I2C-0 data open-drain bidirectional port
M_U1TX		O	UART-1 transmit data
C_EQEP1S		I/O	Enhanced QEP-1 strobe
C_MCLKXA		O	McBSP-A transmit clock
PD7_GPIO23	68	I/O/Z	General-purpose input/output 23
M_CCP1		I/O	Capture/Compare/PWM-1 (General-purpose Timer)
M_MIITXD0		O	EMAC MII transmit data 0
M_U1DTR		O	UART-1 data terminal ready
M_EPI0S30		I/O	EPI-0 signal 30
M_I2C1SCL		I/OD	I2C-1 clock open-drain bidirectional port
M_U1RX		I	UART-1 receive data
C_EQEP1I		I/O	Enhanced QEP-1 index
C_MFSXA		O	McBSP-A transmit frame sync
PE0_GPIO24	43	I/O/Z	General-purpose input/output 24
M_SSI1CLK		I/O	SSI-1 clock
M_CCP3		I/O	Capture/Compare/PWM-3 (General-purpose Timer)
M_EPI0S8		I/O	EPI-0 signal 8
M_USB0PFLT		I	USB-0 external power error state (optionally used in the host mode)
M_SSI3TX		O	SSI-3 transmit data
M_CAN0RX		I	CAN-1 receive data
M_SSI1TX		O	SSI-1 transmit data
C_ECAP1		I/O	Enhanced Capture-1 input/output
C_EQEP2A		I	Enhanced QEP-2 input A

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Table 3-1. Terminal Functions[1] (continued)

TERMINAL		I/O/Z[2]	DESCRIPTION
NAME	RFP PIN #		
PE1_GPIO25	45	I/O/Z	General-purpose input/output 25
M_SSI1FSS		I/O	SSI-1 frame
M_CCP2		I/O	Capture/Compare/PWM-2 (General-purpose Timer)
M_CCP6		I/O	Capture/Compare/PWM-6 (General-purpose Timer)
M_EPI0S9		I/O	EPI-0 signal 9
M_SSI3RX		I	SSI-3 receive data
M_CAN0TX		O	CAN-1 transmit data
M_SSI1RX		O	SSI-1 transmit data
C_ECAP2		I/O	Enhanced Capture-2 input/output
C_EQEP2B		I	Enhanced QEP-2 input B
PE2_GPIO26	32	I/O/Z	General-purpose input/output 26
M_CCP4		I/O	Capture/Compare/PWM-4 (General-purpose Timer)
M_SSI1RX		I	SSI-1 receive data
M_CCP2		I/O	Capture/Compare/PWM-2 (General-purpose Timer)
M_EPI0S24		I/O	EPI-0 signal 24
M_SSI3CLK		I/O	SSI-3 clock
M_U2RX		I	UART-2 receive data
M_SSI1CLK		I/O	SSI-1 clock
C_ECAP3		I/O	Enhanced Capture-3 input/output
C_EQEP2I		I/O	Enhanced QEP-2 index
PE3_GPIO27	33	I/O/Z	General-purpose input/output 27
M_CCP1		I/O	Capture/Compare/PWM-1 (General-purpose Timer)
M_SSI1TX		O	SSI-1 transmit data
M_CCP7		I/O	Capture/Compare/PWM-7 (General-purpose Timer)
M_EPI0S25		I/O	EPI-0 signal 25
M_SSI3FSS		I/O	SSI-3 frame
M_U2TX		O	UART-2 transmit data
M_SSI1FSS		I/O	SSI-1 frame
C_ECAP4		I/O	Enhanced Capture-4 input/output
C_EQEP2S		I/O	Enhanced QEP-2 strobe
PE4_GPIO28	77	I/O/Z	General-purpose input/output 28
M_CCP3		I/O	Capture/Compare/PWM-3 (General-purpose Timer)
M_U2TX		O	UART-2 transmit data
M_CCP2		I/O	Capture/Compare/PWM-2 (General-purpose Timer)
M_MIIRXD0		I	EMAC MII receive data 0
M_U0RX		I	UART-0 receive data
M_USB0EPEN		O	USB-0 external power enable (optionally used in the host mode)
C_SCIRXDA		I	SCI-A receive data
PE5_GPIO29	76	I/O/Z	General-purpose input/output 29
M_CCP5		I/O	Capture/Compare/PWM-5 (General-purpose Timer)
M_MIITXER		O	EMAC MII transmit error
M_U0TX		O	UART-0 transmit data
M_USB0PFLT		I	USB-0 external power error state (optionally used in the host mode)
C_SCITXDA		O	SCI-A transmit data

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Table 3-1. Terminal Functions[1] (continued)

TERMINAL		I/O/Z[2]	DESCRIPTION
NAME	RFP PIN #		
PE6_GPIO30	22	I/O/Z	General-purpose input/output 30
M_U1CTS		I	UART-1 clear-to-send modem status
M_MIIMDIO		I/O	EMAC MII MDIO
M_CAN0RX		I	CAN-0 receive data
C_EPWM9A		O	Enhanced PWM-9 output A
PE7_GPIO31	23	I/O/Z	General-purpose input/output 31
M_U1DCD		I	UART-1 data carrier detect
M_MIIRXD3		I	EMAC MII receive data 3
M_CAN0TX		O	CAN-0 transmit data
C_EPWM9B		O	Enhanced PWM-9 output B
PF0_GPIO32	104	I/O/Z	General-purpose input/output 32
M_CAN1RX		I	CAN-1 receive data
M_MIIRXCK		I	EMAC MII receive clock
M_U1DSR		I	UART-1 data set ready
M_I2C0SDA		I/OD	I2C-0 data open-drain bidirectional port
C_SDAA		I/OD	I2C-A data open-drain bidirectional port
C_SCIRXDA		I	SCI-A receive data
$\overline{\text{C\_ADCSOCAO}}$		O	ADC start-of-conversion A[1]
PF1_GPIO33	103	I/O/Z	General-purpose input/output 33
M_CAN1TX		O	CAN-1 transmit data
M_MIIRXER		I	EMAC MII receive error
M_U1RTS		O	UART-1 request-to-send
M_CCP3		I/O	Capture/Compare/PWM-3 (General-purpose Timer)
M_I2C0SCL		I/OD	I2C-0 clock open-drain bidirectional port
C_SCLA		I/OD	I2C-A clock open-drain bidirectional port
C_EPWMSYNCO		O	Enhanced PWM sync out
$\overline{\text{C\_ADCSOCBO}}$		O	ADC start-of-conversion B[1]
PF2_GPIO34	82	I/O/Z	General-purpose input/output 34
$\overline{\text{M\_MIIPHYINTR}}$		I	EMAC PHY MII interrupt
M_SSI1CLK		I/O	SSI-1 clock
M_XCLKOUT		O	Main PLL clock (divided by 1, 2 or 4)
C_ECAP1		I/O	Enhanced Capture-1 input/output
C_SCIRXDA		I	SCI-A receive data
C_XCLKOUT		O	Main PLL clock (divided by 1, 2 or 4)

(1) Output from the Concerto ePWM is meant for the external ADC (if present).

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Table 3-1. Terminal Functions[1] (continued)

TERMINAL		I/O/Z[2]	DESCRIPTION
NAME	RFP PIN #		
PF3_GPIO35	81	I/O/Z	General-purpose input/output 35
M_MIIMDC		I	EMAC PHY MII MDC
M_SSI1FSS		I/O	SSI-1 frame
M_U0TX		O	UART-0 transmit data
C_SCITXDA		O	SCI-A transmit data
BOOT_2		I	Boot pin 2
PF4_GPIO36	48	I/O/Z	General-purpose input/output 36
M_CCP0		I/O	Capture/Compare/PWM-0 (General-purpose Timer)
M_MIIMDIO		I/O	EMAC MII MDIO
M_EPI0S12		I/O	EPI-0 signal 12
M_SSI1RX		I	SSI-1 receive data
M_U0RX		I	UART-0 receive data
C_SCIRXDA		I	SCI-A receive data
PF5_GPIO37	51	I/O/Z	General-purpose input/output 37
M_CCP2		I/O	Capture/Compare/PWM-2 (General-purpose Timer)
M_MIIRXD3		I	EMAC MII receive data 3
M_EPI0S15		I/O	EPI-0 signal 15
M_SSI1TX		O	SSI-1 transmit data
C_ECAP2		I/O	Enhanced Capture-2 input/output
PF6_GPIO38	69	I/O/Z	General-purpose input/output 38
M_USB0VBUS		Analog	USB0 VBUS power
M_CCP1		I/O	Capture/Compare/PWM-1 (General-purpose Timer)
M_MIIRXD2		I	EMAC MII receive data 2
M_U1RTS		O	UART-1 request-to-send
PF7_GPIO39	No Pin	No Pin	General-purpose input/output 39 is not pinned out.
PG0_GPIO40	49	I/O/Z	General-purpose input/output 40
M_U2RX		I	UART-2 receive data
M_I2C1SCL		I/OD	I2C-1 clock open-drain bidirectional port
M_USB0EPEN		O	USB-0 external power enable (optionally used in the host mode)
M_EPI0S13		I/O	EPI-0 signal 13
M_MIIRXD2		I	EMAC MII receive data 2
M_U4RX		I	UART-4 receive data
PG1_GPIO41	50	I/O/Z	General-purpose input/output 41
M_U2TX		O	UART-2 transmit data
M_I2C1SDA		I/OD	I2C-1 data open-drain bidirectional port
M_EPI0S14		I/O	EPI-0 signal 14
M_MIIRXD1		I	EMAC MII receive data 1
M_U4TX		O	UART-4 transmit data

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Table 3-1. Terminal Functions[1] (continued)

TERMINAL		I/O/Z[2]	DESCRIPTION
NAME	RFP PIN #		
PG2_GPIO42	71	I/O/Z	General-purpose input/output 42
M_USB0DM		Analog	USB0 data minus
M_MIICOL		I	EMAC MII collision detect
PG3_GPIO43	78	I/O/Z	General-purpose input/output 43
M_MIICRS		I	EMAC MII carrier sense
M_MIIRXDV		I	EMAC MII receive data valid
BOOT_0		I	Boot pin 0
PF7_GPIO44	No Pin	No Pin	General-purpose input/output 44 is not pinned out.
PG5_GPIO45	72	I/O/Z	General-purpose input/output 45
M_USB0DP		Analog	USB0 data plus
M_CCP5		I/O	Capture/Compare/PWM-5 (General-purpose Timer)
M_MIITXEN		O	EMAC MII transmit enable
M_U1DTR		O	UART-1 data terminal ready
PG6_GPIO46	70	I/O/Z	General-purpose input/output 46
M_USB0ID		Analog	USB0 ID
M_MIITCK		I	EMAC MII transmit clock
M_U1RI		I	UART-1 receive data
PG7_GPIO47	52	I/O/Z	General-purpose input/output 47
M_MIITXER		O	EMAC MII transmit error
M_EPI0S31		I/O	EPI-0 signal 31
BOOT_1		I	Boot pin 1
PH0_GPIO48	41	I/O/Z	General-purpose input/output 48
M_CCP6		I/O	Capture/Compare/PWM-6 (General-purpose Timer)
$\overline{\text{M\_MIIPHYRST}}$		O	EMAC PHY MII reset
M_EPI0S6		I/O	EPI-0 signal 6
M_SSI3TX		O	SSI-3 transmit data
C_ECAP5		I/O	Enhanced Capture-5 input/output
PH1_GPIO49	42	I/O/Z	General-purpose input/output 49
M_CCP7		I/O	Capture/Compare/PWM-7 (General-purpose Timer)
M_EPI0S7		I/O	EPI-0 signal 7
M_MIIRXD0		I	EMAC MII receive data 0
M_SSI3RX		I	SSI-3 receive data
C_ECAP6		I/O	Enhanced Capture-6 input/output
PH2_GPIO50	36	I/O/Z	General-purpose input/output 50
M_EPI0S1		I/O	EPI-0 signal 1
M_MIITXD3		O	EMAC MII transmit data 3
M_SSI3CLK		I/O	SSI-3 clock
C_EQEP1A		I	Enhanced QEP-2 input B

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Table 3-1. Terminal Functions[1] (continued)

TERMINAL		I/O/Z[2]	DESCRIPTION
NAME	RFP PIN #		
PH3_GPIO51	35	I/O/Z	General-purpose input/output 51
M_USB0EPEN		O	USB-0 external power enable (optionally used in the host mode)
M_EPI0S0		I/O	EPI-0 signal 0
M_MIITXD2		O	EMAC MII transmit data 2
M_SSI3FSS		I/O	SSI-3 frame
C_EQEP1B		I	Enhanced QEP-1 input B
PH4_GPIO52	46	I/O/Z	General-purpose input/output 52
M_USB0FLT		I	USB-0 external power error state (optionally used in the host mode)
M_EPI0S10		I/O	EPI-0 signal 10
M_MIITXD1		O	EMAC MII transmit data 1
M_SSI1CLK		I/O	SSI-1 clock
M_U3TX		O	UART-3 transmit data
C_EQEP1S		I/O	Enhanced QEP-1 strobe
PH5_GPIO53	47	I/O/Z	General-purpose input/output 53
M_EPI0S11		I/O	EPI-0 signal 11
M_MIITXD0		O	EMAC MII transmit data 0
M_SSI1FSS		I/O	SSI-1 frame
M_U3RX		I	UART-3 receive data
C_EQEP1I		I/O	Enhanced QEP-1 index
PH6_GPIO54	79	I/O/Z	General-purpose input/output 54
M_EPI0S26		I/O	EPI-0 signal 26
M_MIIRXDV		I	EMAC MII receive data valid
M_SSI1RX		I	SSI-1 receive data
M_MIITXEN		O	EMAC MII transmit enable
M_SSI0TX		O	SSI-0 transmit data
C_SPISIMOA		I/O	SPI-A slave in, master out
C_EQEP3A		I	Enhanced QEP-1 input A
PH7_GPIO55	80	I/O/Z	General-purpose input/output 55
M_MIIRXCK		I	EMAC MII receive clock
M_EPI0S27		I/O	EPI-0 signal 27
M_SSI1TX		O	SSI-1 transmit data
M_MIITXCK		I	EMAC MII transmit clock
M_SSI0RX		I	SSI-0 receive data
C_SPISOMIA		I/O	SPI-A master in, slave out
C_EQEP3B		I	Enhanced QEP-3 input B
PJ0_GPIO56	63	I/O/Z	General-purpose input/output 56
M_MIIRXER		I	EMAC MII receive error
M_EPI016		I/O	EPI-0 signal 16
M_I2C1SCL		I/OD	I2C-1 clock open-drain bidirectional port
M_SSI0CLK		I/O	SSI-0 clock
C_SPICLKA		I/O	SPI-A clock
C_EQEP3S		I/O	Enhanced QEP-3 strobe

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Table 3-1. Terminal Functions[1] (continued)

TERMINAL		I/O/Z[2]	DESCRIPTION
NAME	RFP PIN #		
PJ1_GPIO57	62	I/O/Z	General-purpose input/output 57
M_EPI0S17		I/O	EPI-0 signal 17
M_USB0PFLT		I	USB-0 external power error state (optionally used in the host mode)
M_I2C1SDA		I/OD	I2C-1 data open-drain bidirectional port
M_MIIRXDV		I	EMAC MII receive data valid
M_SSI0FSS		I/O	SSI-0 frame
C_SPISTEA		I/O	SPI-A slave transmit enable
C_EQEP3I		I/O	Enhanced QEP-3 index
PJ2_GPIO58	61	I/O/Z	General-purpose input/output 58
M_EPI0S18		I/O	EPI-0 signal 18
M_CCP0		I/O	Capture/Compare/PWM-0 (General-purpose Timer)
M_MIIRXCK		I	EMAC MII receive clock
M_SSI0CLK		I/O	SSI-0 clock
M_U0TX		O	UART-0 transmit data
C_MCLKRA		I	McBSP-A receive clock
C_EPWM7A		O	Enhanced PWM-7 output A
PJ3_GPIO59	60	I/O/Z	General-purpose input/output 59
M_EPI0S19		I/O	EPI-0 signal 19
M_U1CTS		I	UART-1 clear-to-send
M_CCP6		I/O	Capture/Compare/PWM-6 (General-purpose Timer)
M_MIIMDC		O	EMAC PHY MII MDC
M_SSI0FSS		I/O	SSI-0 frame
M_U0RX		I	UART-0 receive data
C_MFSRA		I	McBSP-A receive frame sync
C_EPWM7B		O	Enhanced PWM-7 output B
PJ4_GPIO60	57	I/O/Z	General-purpose input/output 60
M_EPI0S28		I/O	EPI-0 signal 28
M_U1DCD		I	UART-1 data carrier detect
M_CCP4		I/O	Capture/Compare/PWM-4 (General-purpose Timer)
M_MIICOL		I	EMAC MII collision detect
M_SSI1CLK		I/O	SSI-1 clock
C_EPWM8A		O	Enhanced PWM-8 output A
PJ5_GPIO61	56	I/O/Z	General-purpose input/output 61
M_EPI0S29		I/O	EPI-0 signal 29
M_U1DSR		I	UART-1 data set ready
M_CCP2		I/O	Capture/Compare/PWM-2 (General-purpose Timer)
M_MIICRS		I	EMAC PHY MII CRS
M_SSI1FSS		I/O	SSI-1 frame
C_EPWM8B		O	Enhanced PWM-8 output B

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Table 3-1. Terminal Functions[1] (continued)

TERMINAL		I/O/Z[2]	DESCRIPTION
NAME	RFP PIN #		
PJ6_GPIO62	53	I/O/Z	General-purpose input/output 62
M_EPI0S30		I/O	EPI-0 signal 30
M_U1RTS		O	UART-1 request-to-send
M_CCP1		I/O	Capture/Compare/PWM-1 (General-purpose Timer)
M_MIIPHYINTR		I	EMAC PHY MII interrupt
M_U2RX		I	UART-2 receive data
C_EPWM9A		O	Enhanced PWM-9 output A
PJ7_GPIO63	97	I/O/Z	General-purpose input/output 63
M_U1DTR		O	UART-1 data terminal ready
M_CCP0		I/O	Capture/Compare/PWM-0 (General-purpose Timer)
M_MIIPHYRST		O	EMAC PHY MII reset
M_U2TX		O	UART-2 transmit data
C_EPWM9B		O	Enhanced PWM-9 output B
PC0_GPIO64	No Pin	No Pin	General-purpose input/output 64 is not pinned out
PC1_GPIO65	No Pin	No Pin	General-purpose input/output 65 is not pinned out
PC2_GPIO66	No Pin	No Pin	General-purpose input/output 66 is not pinned out
PC3_GPIO67	No Pin	No Pin	General-purpose input/output 67 is not pinned out
PC4_GPIO68	37	I/O/Z	General-purpose input/output 68
M_CCP5		I	Capture/Compare/PWM-5 (General-purpose Timer)
M_MIITXD3		O	EMAC MII transmit data 3
M_CCP2		I	Capture/Compare/PWM-2 (General-purpose Timer)
M_CCP4		I	Capture/Compare/PWM-4 (General-purpose Timer)
M_EPI0S2		I/O	EPI-0 signal 2
M_CCP1		I	Capture/Compare/PWM-1 (General-purpose Timer)
PC5_GPIO69	38	I/O/Z	General-purpose input/output 69
M_CCP1		I	Capture/Compare/PWM-1 (General-purpose Timer)
M_CCP3		I	Capture/Compare/PWM-3 (General-purpose Timer)
M_USB0EPEN		O	USB-0 external power enable (optionally used in the host mode)
M_EPI0S3		I/O	EPI-0 signal 3
PC6_GPIO70	39	I/O/Z	General-purpose input/output 70
M_CCP3		I	Capture/Compare/PWM-3 (General-purpose Timer)
M_U1RX		I	UART-1 receive data
M_CCP0		I	Capture/Compare/PWM-0 (General-purpose Timer)
M_USB0PFLT		I	USB-0 external power error state (optionally used in the host mode)
M_EPI0S4		I/O	EPI-0 signal 4
PC7_GPIO71	40	I/O/Z	General-purpose input/output 71
M_CCP4		I	Capture/Compare/PWM-4 (General-purpose Timer)
M_CCP0		I	Capture/Compare/PWM-0 (General-purpose Timer)
M_U1TX		O	UART-1 transmit data
M_USB0PFLT		I	USB-0 external power error state (optionally used in the host mode)
M_EPI0S5		I/O	EPI-0 signal 5

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Table 3-1. Terminal Functions[1] (continued)

TERMINAL		I/O/Z[2]	DESCRIPTION
NAME	RFP PIN #		
Reset			
$\overline{\text{XRS}}$	4	I/OD	Digital Subsystem Reset (in) and Watchdog/Brown-out Reset (out). In most applications, it is recommended that the $\overline{\text{XRS}}$ pin be tied with the $\overline{\text{ARS}}$ pin. The Digital Subsystem has a built-in power-on-reset (POR) and brown-out-reset (BOR) circuitry. As such, no external circuitry is needed to generate a reset pulse. During a power-on or brown-out condition, this pin is driven low by the Digital Subsystem. This pin is also driven low by the Digital Subsystem when a watchdog reset occurs. During watchdog reset, the $\overline{\text{XRS}}$ pin is driven low for the watchdog reset duration of 512 OSCCLK cycles. If need be, an external circuitry may also drive this pin to assert device reset. In this case, it is recommended that this pin be driven by an open-drain device. An R-C circuit must be connected to this pin for noise immunity reasons. Regardless of the source, a device reset causes the Digital Subsystem to terminate execution. The Cortex™-M3 program counter points to the address contained at the location 0x00000004. The C28 program counter points to the address contained at the location 0x3FFFC0. When reset is deactivated, execution begins at the location designated by the program counter. The output buffer of this pin is an open-drain with an internal pullup.
$\overline{\text{ARS}}$	144	I/OD	Analog Subsystem Reset (in) and Brown-out Reset (out).In most applications, it is recommended that the $\overline{\text{ARS}}$ pin be tied with the $\overline{\text{XRS}}$ pin. The Digital Subsystem has a built-in brown-out-reset (BOR) circuitry. As such, no external circuitry is needed to generate a reset pulse. During a power-on or brown-out condition, this pin is driven low by the Analog Subsystem. If need be, an external circuitry may also drive this pin to assert a device reset. In this case, it is recommended that this pin be driven by an open-drain device. An R-C circuit must be connected to this pin for noise immunity reasons. Regardless of the source, the Analog Subsystem reset causes the digital logic associated with the Analog Subsystem, to enter reset state. The output buffer of this pin is an open-drain with an internal pullup.
Clocks			
X1	93	I	On-chip crystal-oscillator input. To use this oscillator, a quartz crystal or a ceramic resonator must be connected across X1 and X2. If this pin is not used, it must be tied to GND.
X2	95	O	On-chip crystal-oscillator output. A quartz crystal or a ceramic resonator must be connected across X1 and X2. If X2 is not used, it must be left unconnected.
XCLKIN	see PJ7_GPIO63	I	External oscillator input. This pin feeds a clock from an external 3.3-V oscillator to internal USB PLL module and to the CAN peripherals.
XCLKOUT	see PF2_GPIO34	O/Z	External oscillator output. This pin outputs a clock divided-down from the internal PLL System Clock. The divide ratio is defined in the XCLKCFG register.
Boot Pins			
BOOT_0	see PG3_GPIO43	I	One of three boot mode pins. It selects a specific configuration source from which the Concerto device boots on start-up.
BOOT_1	see PG7_GPIO47	I	One of three boot mode pins. It selects a specific configuration source from which the Concerto device boots on start-up.
BOOT_2	see PG3_GPIO35	I	One of three boot mode pins. It selects a specific configuration source from which the Concerto device boots on start-up.

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Table 3-1. Terminal Functions[1] (continued)

TERMINAL		I/O/Z[2]	DESCRIPTION
NAME	RFP PIN #		
JTAG			
$\overline{\text{TRST}}$	85	I	JTAG test reset with internal pulldown. $\overline{\text{TRST}}$, when driven high, gives the scan system control of the operations of the device. If this signal is not connected or driven low, the device operates in its functional mode, and the test reset signals are ignored. **NOTE:** $\overline{\text{TRST}}$ is an active-high test pin and must be maintained low during normal device operation. An external pull-down resistor is required on this pin. The value of this resistor should be based on drive strength of the debugger pods applicable to the design. A 2.2-kΩ resistor generally offers adequate protection. Since this is application-specific, it is recommended that each target board be validated for proper operation of the debugger and the application. (↓)
TCK	89	I	JTAG test clock with internal pullup (↑)
TMS	87	I	JTAG test-mode select (TMS) with internal pullup. This serial control input is clocked into the TAP controller on the rising edge of TCK. (↑)
TDI	88	I	JTAG test data input (TDI) with internal pullup. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK. (↑)
TDO	84	O/Z	JTAG scan out, test data output (TDO). The contents of the selected register (instruction or data) are shifted out of TDO on the falling edge of TCK. (8-mA drive)
EMU0	83	I/O/Z	Emulator pin 0. When $\overline{\text{TRST}}$ is driven high, this pin is used as an interrupt to or from the emulator system and is defined as input/output through the JTAG scan. This pin is also used to put the device into boundary-scan mode. With the EMU0 pin at a logic-high state and the EMU1 pin at a logic-low state, a rising edge on the $\overline{\text{TRST}}$ pin would latch the device into boundary-scan mode. (I/O/Z, 8 mA drive ↑) **NOTE:** An external pullup resistor is required on this pin. The value of this resistor should be based on the drive strength of the debugger pods applicable to the design. A 2.2-kΩ to 4.7-kΩ resistor is generally adequate. Since this is application-specific, it is recommended that each target board be validated for proper operation of the debugger and the application. **NOTE:** If EMU0 is 0 and EMU1 is 1 when coming out of reset, the device enters Wait-in-Reset mode. WIR suspends bootloader execution, allowing the Emulator to connect to the device and to modify FLASH contents.
EMU1	86	I/O/Z	Emulator pin 1. When $\overline{\text{TRST}}$ is driven high, this pin is used as an interrupt to or from the emulator system and is defined as input/output through the JTAG scan. This pin is also used to put the device into boundary-scan mode. With the EMU0 pin at a logic-high state and the EMU1 pin at a logic-low state, a rising edge on the $\overline{\text{TRST}}$ pin would latch the device into boundary-scan mode. (I/O/Z, 8 mA drive ↑) **NOTE:** An external pullup resistor is required on this pin. The value of this resistor should be based on the drive strength of the debugger pods applicable to the design. A 2.2-kΩ to 4.7-kΩ resistor is generally adequate. Since this is application-specific, it is recommended that each target board be validated for proper operation of the debugger and the application. **NOTE:** If EMU0 is 0 and EMU1 is 1 when coming out of reset, the device enters Wait-in-Reset mode. WIR suspends bootloader execution, allowing the Emulator to connect to the device and to modify FLASH contents.

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Table 3-1. Terminal Functions[1] (continued)

TERMINAL		I/O/Z[2]	DESCRIPTION
NAME	RFP PIN #		
Test Pins			
FLT1	16	I/O	FLASH Test Pin 1. Reserved for TI. Must be left unconnected.
FLT2	21	I/O	FLASH Test Pin 2. Reserved for TI. Must be left unconnected.
Internal Voltage Regulator Control			
$\overline{\text{VREG18EN}}$	113		Internal 1.8-V VREG Enable/Disable for V_{DD18}. Pull low to enable the internal 1.8-V voltage regulator (VREG18), pull high to disable VREG18.
$\overline{\text{VREG12EN}}$	101		Internal 1.2-V VREG Enable/Disable for V_{DD12}. Pull low to enable the internal 1.2-V voltage regulator (VREG12), pull high to disable VREG12.
Analog, Digital, and I/O Power			
V_{DDA1}	119		3.3-V Analog Module 1 Power Pin. Tie with a 2.2-µF capacitor (typical) close to the pin.
V_{DDA2}	134		3.3-V Analog Module 2 Power Pin. Tie with a 2.2-µF capacitor (typical) close to the pin.
V_{DDIO}	107		3.3-V Digital I/O and FLASH Power Pin. Tie with a 0.1-µF capacitor (typical) close to the pin.
V_{DDIO}	10		3.3-V Digital I/O and FLASH Power Pin. Tie with a 0.1-µF capacitor (typical) close to the pin.
V_{DDIO}	25		3.3-V Digital I/O and FLASH Power Pin. Tie with a 0.1-µF capacitor (typical) close to the pin.
V_{DDIO}	34		3.3-V Digital I/O and FLASH Power Pin. Tie with a 0.1-µF capacitor (typical) close to the pin.
V_{DDIO}	44		3.3-V Digital I/O and FLASH Power Pin. Tie with a 0.1-µF capacitor (typical) close to the pin.
V_{DDIO}	54		3.3-V Digital I/O and FLASH Power Pin. Tie with a 0.1-µF capacitor (typical) close to the pin.
V_{DDIO}	59		3.3-V Digital I/O and FLASH Power Pin. Tie with a 0.1-µF capacitor (typical) close to the pin.
V_{DDIO}	105		3.3-V Digital I/O and FLASH Power Pin. Tie with a 0.1-µF capacitor (typical) close to the pin.
V_{DDIO}	3		3.3-V Digital I/O and FLASH Power Pin. Tie with a 0.1-µF capacitor (typical) close to the pin.
V_{DDIO}	67		3.3-V Digital I/O and FLASH Power Pin. Tie with a 0.1-µF capacitor (typical) close to the pin.
V_{DDIO}	74		3.3-V Digital I/O and FLASH Power Pin. Tie with a 0.1-µF capacitor (typical) close to the pin.
V_{DDIO}	92		3.3-V Digital I/O and FLASH Power Pin. Tie with a 0.1-µF capacitor (typical) close to the pin.
V_{DDIO}	100		3.3-V Digital I/O and FLASH Power Pin. Tie with a 0.1-µF capacitor (typical) close to the pin.
V_{DDIO}	96		3.3-V Digital I/O and FLASH Power Pin. Tie with a 0.1-µF capacitor (typical) close to the pin.
V_{DDIO}	17		3.3-V Digital I/O and FLASH Power Pin. Tie with a 0.1-µF capacitor (typical) close to the pin.
V_{DDIO}	2		3.3-V Digital I/O and FLASH Power Pin. Tie with a 0.1-µF capacitor (typical) close to the pin.
V_{DDIO}	106		3.3-V Digital I/O and FLASH Power Pin. Tie with a 0.1-µF capacitor (typical) close to the pin.
V_{DD18}	1		1.8-V Digital Logic Power Pins (associated with the Analog Subsytem) - no supply needed when using internal VREG18. Tie with 1.2-µF (minimum) ceramic capacitor (10% tolerance) to ground when using internal VREG. Higher value capacitors may be used but could impact supply-rail ramp-up time.

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Table 3-1. Terminal Functions[1] (continued)

TERMINAL		I/O/Z[2]	DESCRIPTION
NAME	RFP PIN #		
V_{DD18}	108		1.8-V Digital Logic Power Pins (associated with the Analog Subsytem) - no supply needed when using internal VREG18. Tie with 1.2-µF (minimum) ceramic capacitor (10% tolerance) to ground when using internal VREG. Higher value capacitors may be used but could impact supply-rail ramp-up time.
V_{DD12}	24		1.2-V Digital Logic Power Pins - no supply needed when using internal VREG12. Tie with 422- nF (minimum) ceramic capacitor (10% tolerance) to ground when using internal VREG. Higher value capacitors may be used but could impact supply-rail ramp-up time.
V_{DD12}	55		1.2-V Digital Logic Power Pins - no supply needed when using internal VREG12. Tie with 422- nF (minimum) ceramic capacitor (10% tolerance) to ground when using internal VREG. Higher value capacitors may be used but could impact supply-rail ramp-up time.
V_{DD12}	66		1.2-V Digital Logic Power Pins - no supply needed when using internal VREG12. Tie with 422- nF (minimum) ceramic capacitor (10% tolerance) to ground when using internal VREG. Higher value capacitors may be used but could impact supply-rail ramp-up time.
V_{DD12}	99		1.2-V Digital Logic Power Pins - no supply needed when using internal VREG12. Tie with 422- nF (minimum) ceramic capacitor (10% tolerance) to ground when using internal VREG. Higher value capacitors may be used but could impact supply-rail ramp-up time.
V_{DD12}	75		1.2-V Digital Logic Power Pins - no supply needed when using internal VREG12. Tie with 422- nF (minimum) ceramic capacitor (10% tolerance) to ground when using internal VREG. Higher value capacitors may be used but could impact supply-rail ramp-up time.
V_{DD12}	58		1.2-V Digital Logic Power Pins - no supply needed when using internal VREG12. Tie with 422- nF (minimum) ceramic capacitor (10% tolerance) to ground when using internal VREG. Higher value capacitors may be used but could impact supply-rail ramp-up time.
V_{DD12}	11		1.2-V Digital Logic Power Pins - no supply needed when using internal VREG12. Tie with 422- nF (minimum) ceramic capacitor (10% tolerance) to ground when using internal VREG. Higher value capacitors may be used but could impact supply-rail ramp-up time.
V_{DD12}	91		1.2-V Digital Logic Power Pins - no supply needed when using internal VREG12. Tie with 422- nF (minimum) ceramic capacitor (10% tolerance) to ground when using internal VREG. Higher value capacitors may be used but could impact supply-rail ramp-up time.
V_{DD12}	90		1.2-V Digital Logic Power Pins - no supply needed when using internal VREG12. Tie with 422- nF (minimum) ceramic capacitor (10% tolerance) to ground when using internal VREG. Higher value capacitors may be used but could impact supply-rail ramp-up time.
V_{SS}	PWR PAD		Analog and Digital Ground Power Pad (located on the bottom of the chip).
V_{SSOSC}	94		Clock Oscillator Ground Pin

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4 Device Operating Conditions

4.1 Absolute Maximum Ratings(1) (2)

Supply voltage range, V_{DDIO} (I/O and Flash)	with respect to V_{SS}	–0.3 V to 4.6 V
Supply voltage range, V_{DD18}	with respect to V_{SS}	–0.3 V to 2.5 V
Supply voltage range, V_{DD12}	with respect to V_{SS}	–0.3 V to 1.5 V
Analog voltage range, V_{DDA}	with respect to V_{SSA}	–0.3 V to 4.6 V
Input voltage range, V_{IN} (3.3 V)		–0.3 V to 4.6 V
Output voltage range, V_O		–0.3 V to 4.6 V
Input clamp current, I_{IK} (V_{IN} < 0 or V_{IN} > V_{DDIO})(3)		±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DDIO})		±20 mA
Junction temperature range, T_J (4)		–40°C to 150°C
Storage temperature range, T_{stg} (4)		–65°C to 150°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Section 4.2 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to V_{SS}, unless otherwise noted.
(3) Continuous clamp current per pin is ± 2 mA.
(4) Long-term high-temperature storage and/or extended use at maximum temperature conditions may result in a reduction of overall device life. For additional information, see *IC Package Thermal Metrics Application Report* (literature number SPRA953) and *Reliability Data for TMS320LF24xx and TMS320F28xx Devices Application Report* (literature number SPRA963).

4.2 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Device supply voltage, I/O, V_{DDIO}(1)		3.14	3.3	3.46	V
Device supply voltage, Analog Subsystem, V_{DD18} (when internal VREG is disabled and 1.8 V is supplied externally)		1.71	1.8	1.89	V
Device supply voltage, Master and Control Subsystems, V_{DD12} (when internal VREG is disabled and 1.2 V is supplied externally)		1.14	1.2	1.26	V
Supply ground, V_{SS}			0		V
Analog supply voltage, V_{DDA}(1)		3.14	3.3	3.47	V
Analog ground, V_{SSA}			0		V
Device clock frequency (system clock)		2		60	MHz
High-level input voltage, V_{IH} (3.3 V)		V_{DDIO} * 0.7		V_{DDIO} + 0.3	V
Low-level input voltage, V_{IL} (3.3 V)		V_{SS} – 0.3		V_{DDIO} * 0.3	V
High-level output source current, V_{OH} = $V_{OH(MIN)}$, I_{OH}	All GPIO/AIO pins			–4	mA
	Group 2(2)			–8	mA
Low-level output sink current, V_{OL} = $V_{OL(MAX)}$, I_{OL}	All GPIO/AIO pins			4	mA
	Group 2(2)			8	mA
Junction temperature, T_J (3)	T version	–40		105	°C
	S version	–40		125	
	Q version (Q100 qualification)	–40		125	

(1) V_{DDIO} and V_{DDA} should be maintained within ~0.3 V of each other.
(2) Group 2 pins are as follows: PD3_GPIO19, PE2_GPIO26, PE3_GPIO27, PH6_GPIO54, PH7_GPIO55, EMU0, TDO, EMU1, PD0_GPIO16, AIO7, AIO4.
(3) T_A (Ambient temperature) is product- and application-dependent and can go up to the specified T_J max of the device.

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4.3 Electrical Characteristics(1)

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = I_{OH} MAX		V_{DDIO} * 0.8			V
			I_{OH} = 50 µA		V_{DDIO} – 0.2			
V_{OL}	Low-level output voltage		I_{OL} = I_{OL} MAX				V_{DDIO} * 0.2	V
I_{IL}	Input current (low level)	Pin with pullup enabled	V_{DDIO} = 3.3 V, V_{IN} = 0 V	All GPIO/AIO		–140		µA
				$\overline{XRS}$ pin and $\overline{ARS}$ pin		–300		
		Pin with pulldown enabled	V_{DDIO} = 3.3 V, V_{IN} = 0 V			±2		
I_{IH}	Input current (high level)	Pin with pullup enabled	V_{DDIO} = 3.3 V, V_{IN} = V_{DDIO}			±2		µA
		Pin with pulldown enabled	V_{DDIO} = 3.3 V, V_{IN} = V_{DDIO}			50		
I_{OZ}	Output current, pullup or pulldown disabled		V_O = V_{DDIO} or 0 V			±2		µA
C_I	Input capacitance					2		pF
	V_{DDIO} BOR trip point		Falling V_{DDIO}			2.78		V
	V_{DDIO} BOR hysteresis					35		mV
	Supervisor reset release delay time		Time after BOR/POR/OVR event is removed to $\overline{XRS}$ release			600		µs
	VREG V_{DD18} output		Internal VREG18 on			1.8		V
	VREG V_{DD12} output		Internal VREG12 on			1.2		V

(1) When the on-chip VREG is used, its output is monitored by the POR/BOR circuit, which will reset the device should the core voltage (V_{DD}) go out of range.

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5 Peripheral Information and Timings

5.1 Master Subsystem Peripherals

Master Subsystem peripherals are located on the APB Bus and AHB Bus, and are accessible from the Cortex™-M3 CPU/µDMA. The AHB peripherals include EPI, USB, and two CAN modules. The APB peripherals include EMAC, two I2Cs, five UARTs, four SSIs, four GPTIMERs, two WDOGs, NMI WDOG, and a µCRC module (Cyclic Redundancy Check).

5.1.1 External Peripheral Interface (EPI)

The External Peripheral Interface (EPI) is a high-speed parallel bus for external peripherals or memory. It has several modes of operation to interface gluelessly to many types of external devices. The EPI is similar to a standard microprocessor address/data bus, except that it must typically be connected to just one type of external device. Enhanced capabilities include µDMA support, clocking control, and support for external FIFO buffers.

The EPI supports three primary functional modes: Synchronous Dynamic Random-Access Memory (SDRAM) mode, Traditional Host-Bus mode, and General-Purpose mode. The EPI module also provides custom GPIOs; however, unlike regular GPIOs, the EPI module uses a FIFO in the same way as a communication mechanism and is speed-controlled using clocking.

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5.2 Control Subsystem Peripherals

Control Subsystem peripherals are accessible from the C28x CPU via the C28x Memory Bus, and from the C28x DMA via the C28x DMA Bus. They include one NMI Watchdog, three Timers, four Serial Port Peripherals (SCI, SPI, McBSP, I2C), and three types of Control Peripherals (ePWM, eQEP, eCAP).

5.2.1 Pulse Width Modulator (PWM) Modules

There are nine PWM modules in the Concerto device. Eight of these are of the High-Resolution PWM (HRPWM) type, and one is of the Enhanced PWM (ePWM) type. The HRPWM modules have all the features of the ePWM plus they offer significantly higher PWM resolution (time granularity). Figure 5-1 shows the eight HRPWM modules (PWM 1–8) and the single ePWM module (PWM 9).

The synchronization inputs to the PWM modules include the SYNCI signal from the GPTRIP1 output of GPIO_MUX1, and the TBCLKSYNC signal from the CPCLKCR0 register. Synchronization output SYNCO1 comes from the HRPWM1 module and is stretched by 8 HSPCLK cycles before entering GPIO_MUX1. There are two groups of trip signal inputs to PWM modules. TRIP1–15 inputs come from GPTRIP1–12 (from GPIO_MUX1), ECCDBLERR signal (from C28x Local and Shared RAM), and PIEERR signal from the C28x CPU. TZ1–6 (Trip Zone) inputs come from GPTRIP 1–3 (from GPIO_MUX1), EQEPERR (from the eQEP peripheral), CLOCKFAIL (from M3 CLOCKS), and EMUSTOP (from the C28x CPU).

There are nine SOCA PWM outputs and nine SOCB PWM outputs—a pair from each PWM module. The nine SOCA outputs are OR-ed together and stretched by 32 HSPCLK cycles before entering GPIO_MUX1 as a single SOCAO signal. The nine SOCB outputs are OR-ed together and stretched by 32 HSPCLK cycles before entering GPIO_MUX1 as a single SOCBO signal. The 18 SOCA/B outputs also go to the Analog Subsystem, where they can be selected to become conversion triggers to ADC modules.

The nine PWM modules also drive two other sets of outputs which can interrupt the C28x CPU via the C28x PIE block. These are nine EPWMINT interrupts and nine EPWMTZINT trip-zone interrupts. See Figure 5-2 for the internal structure of the ePWM and HRPWM modules. The green-colored blocks are common to both ePWM and HRPWM modules, but only the HRPWMs have the grey-colored hi-resolution blocks.

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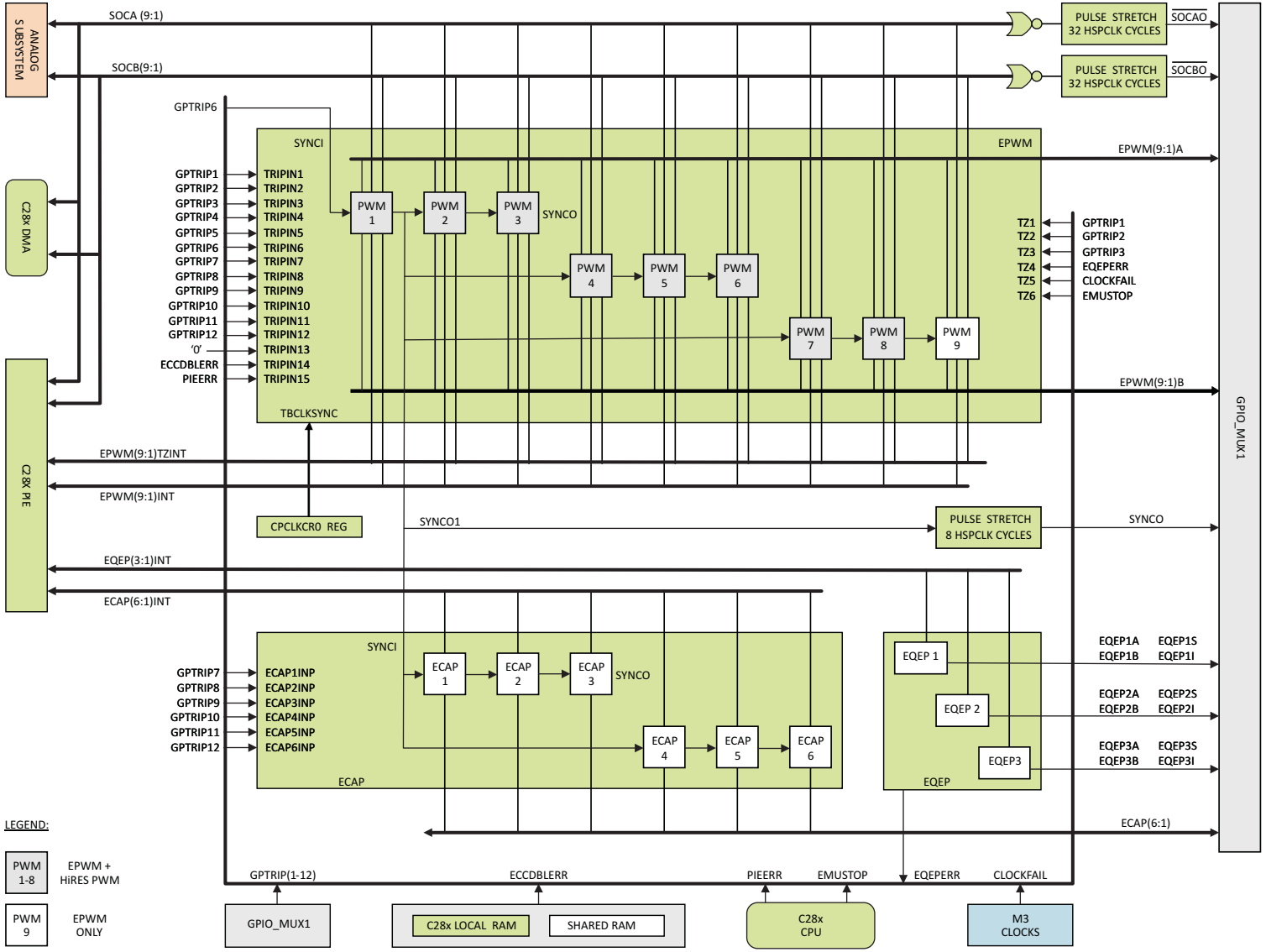

Figure 5-1. ePWM, eQEP, eCAP

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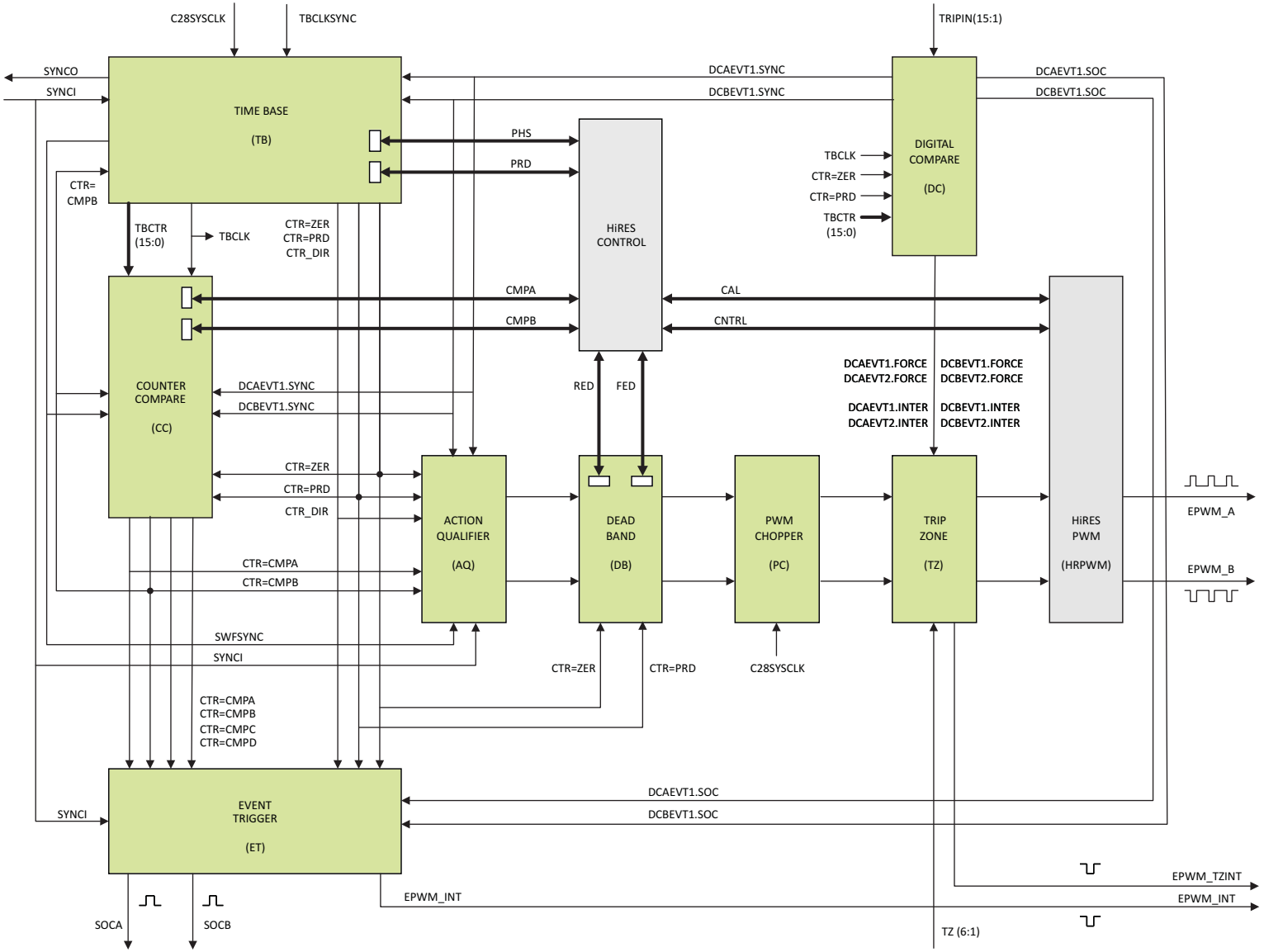

Figure 5-2. ePWM/HRPWM

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5.3 Analog/Shared Peripherals

Concerto Shared Peripherals are accessible from both the Master Subsystem and the Control Subsystem. The Analog Shared Peripherals include two 12-bit ADCs (Analog-to-Digital Converters), and six Comparator + DAC (10-bit) modules. All ADC and Comparator registers are accessible by the Cortex™-M3 CPU and C28x CPU, while ADC results registers are also accessible by the respective DMAs of the two processors.

The Inter-Processor Communications (IPC) Peripheral is only accessible by the Cortex™-M3 CPU and by the C28x CPU (not accessible by DMAs). IPC is used for sending and receiving synchronization events between Master and Control subsystems to coordinate execution of software running on both processors, or exchanging of data between the two processors.

5.3.1 Analog-to-Digital Converter (ADC)

Figure 5-3 shows the internal structure of each of the two ADC peripherals that are present on Concerto. Each ADC has 16 channels that can be programmed to select analog inputs, select start-of-conversion trigger, set the sampling window, and select end-of-conversion interrupt to prompt a CPU or DMA to read 16 result registers. The 16 ADC channels can be used independently or in pairs, based on the assignments inside the SAMPLEMODE register. Pairing up the channels allows two analog inputs to be sampled simultaneously—thereby, increasing the overall conversion performance.

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5.3.1.1 Sample Mode

Each ADC has 16 programmable channels that can be independently programmed for analog-to-digital conversion when corresponding bits in the SAMPLEMODE register are set to Sequential Mode. For example, if bit 2 in the SAMPLEMODE register is set to 0, ADC channels 4 and 5 are set to sequential mode. This means that the SOC4CTL and SOC5CTL registers can both be programmed to configure channels 4 and 5 to independently perform analog-to-digital conversions with results being stored in the RESULT4 and RESULT5 registers. "Independently" means that channel 4 may use a different Start-Of-Conversion (SOC) trigger, different analog input, and different sampling window than the trigger, input, and window assigned to channel 5.

The 16 programmable channels for each ADC may also be grouped in 8 channel pairs when corresponding bits in the SAMPLEMODE register are set to Simultaneous Mode. For example, if bit 2 in the SAMPLEMODE register is set to 1, ADC channels 4 and 5 are set to Simultaneous Mode. This means that the SOC4CTL register now contains configuration parameters for both channel 4 and channel 5, and the SOC5CTL register is ignored. This means that while channel 4 and channel 5 are still using dedicated analog inputs (now selected as pairs in the CHSEL field of SOC4CTL), they both share the same SOC trigger and Sampling Window, with the results being stored in the RESULT4 and RESULT5 registers.

The Simultaneous mode is made possible by two sample-and-hold units present in each ADC. Each sample-and-hold unit has its own mux for selecting analog inputs (see Figure 5-3). By programming the SAMPLEMODE register, the 16 available channels can be configured as 16 independent channels, 8 channel pairs, or any combination thereof (for example, 10 sequential channels and 3 simultaneous pairs).

5.3.1.2 Start-of-Conversion (SOC) Triggers

There are eight external SOC triggers that go to each of the two ADC modules (from the Control Subsystem). In addition to the eight external SOC triggers, there are also two internal SOC triggers derived from End-Of-Conversion (EOC) interrupts inside each ADC module (ADCINT1 and ADCINT2). Registers INTSOCSEL1 and 2 are used to configure each of the 16 ADC channels for internal or external SOC sources. If internal SOC is chosen for a given channel, the INTSOCSEL1 and 2 registers also select whether the internal source is ADCINT1 or ADCINT2. If external SOC is chosen for a given ADC channel, the TRIGSEL field of the corresponding SOCxCTL register selects which of the eight external triggers is used for SOC in that channel. One analog-to-digital conversion can be performed at a time by the 12-bit ADC. The analog-to-digital conversion priority is managed according to the state of the PRICTL register.

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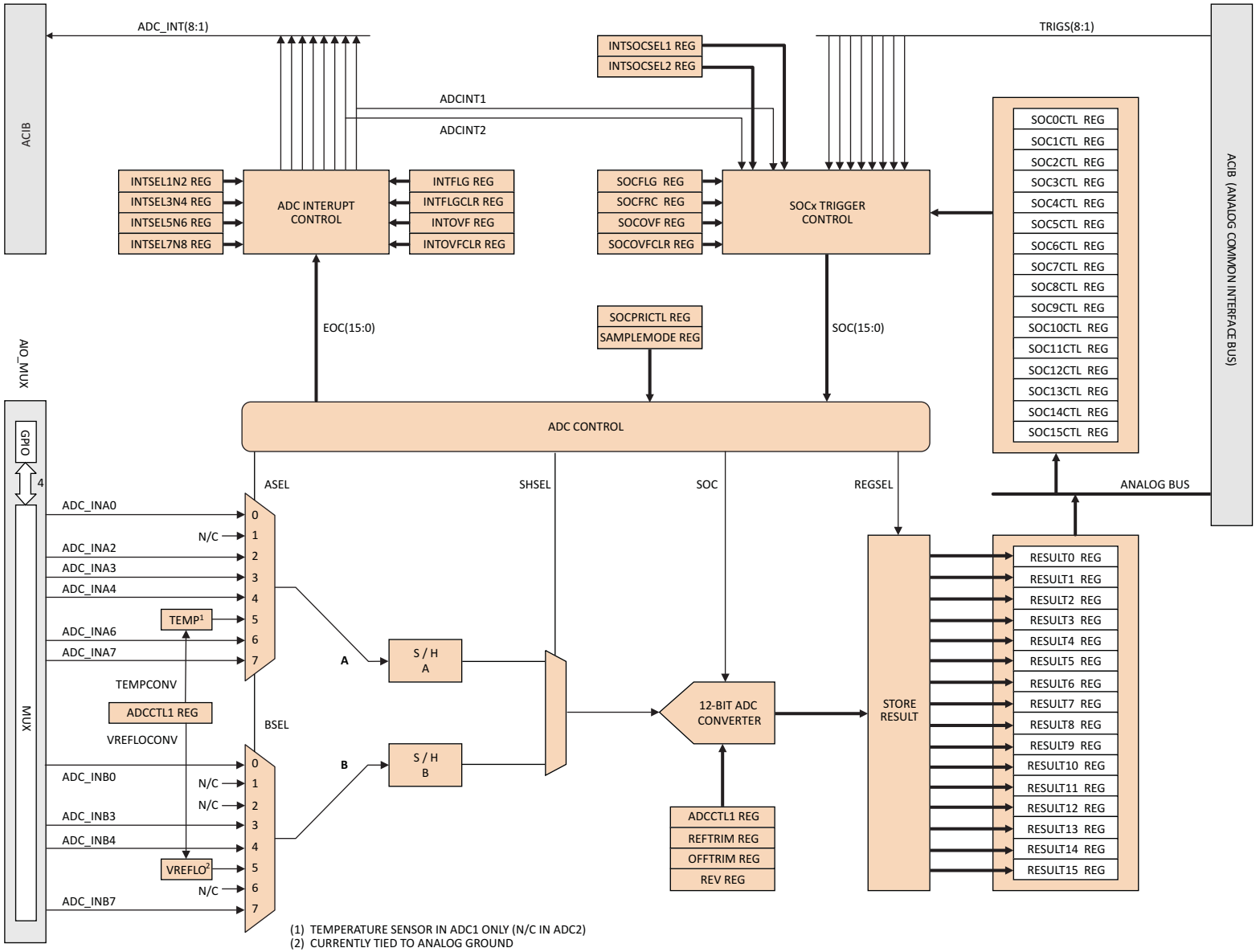

Figure 5-3. ADC

PRODUCT PREVIEW

5.3.1.3 Analog Inputs

Analog inputs to each of the two ADC modules are organized in two groups—A and B, with each group having a dedicated mux and sample-and-hold unit (see Figure 5-3). Mux A selects one of seven possible analog inputs—six external inputs via AIO MUX, and one from the internal temperature sensor (present on ADC1 only). Mux B selects one of five possible analog inputs—four external inputs via AIO MUX, and one from the internal VREFLO signal, which is currently tied to the Analog Ground. The Mux A and Mux B inputs can be simultaneously or sequentially sampled by the two sample-and-hold units according to the sampling window chosen in the SOCxCTL register for the corresponding channel.

5.3.1.4 ADC Result Registers and EOC Interrupts

Concerto analog-to-digital conversion results are stored in 32 Results Registers (16 for ADC1 and 16 for ADC2). The 16 ADCx channels can be programmed via the INTSELxNy registers to trigger up to eight ADCINT interrupts per ADC module, when their results are ready to be read. The eight ADCINT interrupts from ADC1 and the eight ADCINT interrupts from ADC2 are AND-ed together before propagating to both the Master Subsystem and the Control Subsystem, announcing that the Result Registers are ready to be read by a CPU or DMA (see Figure 2-3).

5.3.2 Comparator + DAC Units

Figure 5-4 shows the internal structure of the six analog Comparator + DAC units present in Concerto devices. Each unit compares two analog inputs (A and B) and assigns a value of ‘1’ when the voltage of the A input is greater than that of the B input, or a value of ‘0’ when the opposite is true. The A inputs come from AIO_MUX1 and AIO_MUX2, as do two of the six B inputs. The remaining four of the B inputs are provided by 10-bit digital-to-analog units that are present in each comparator. In fact, all six B inputs can be provided by the DACs, if so desired. The 10-bit value for each DAC unit is programmed in the respective DACVAL register. Another comparator register, COMPCTL, can be programmed to select the source of the B input, to enable/disable the comparator circuit, to invert comparator output, to synchronize comparator output to C28x SYSCLK, and to select the qualification period (number of clock cycles). All six output signals from the six comparators can be routed out to the device pins via GPIO_MUX2 pin mux.

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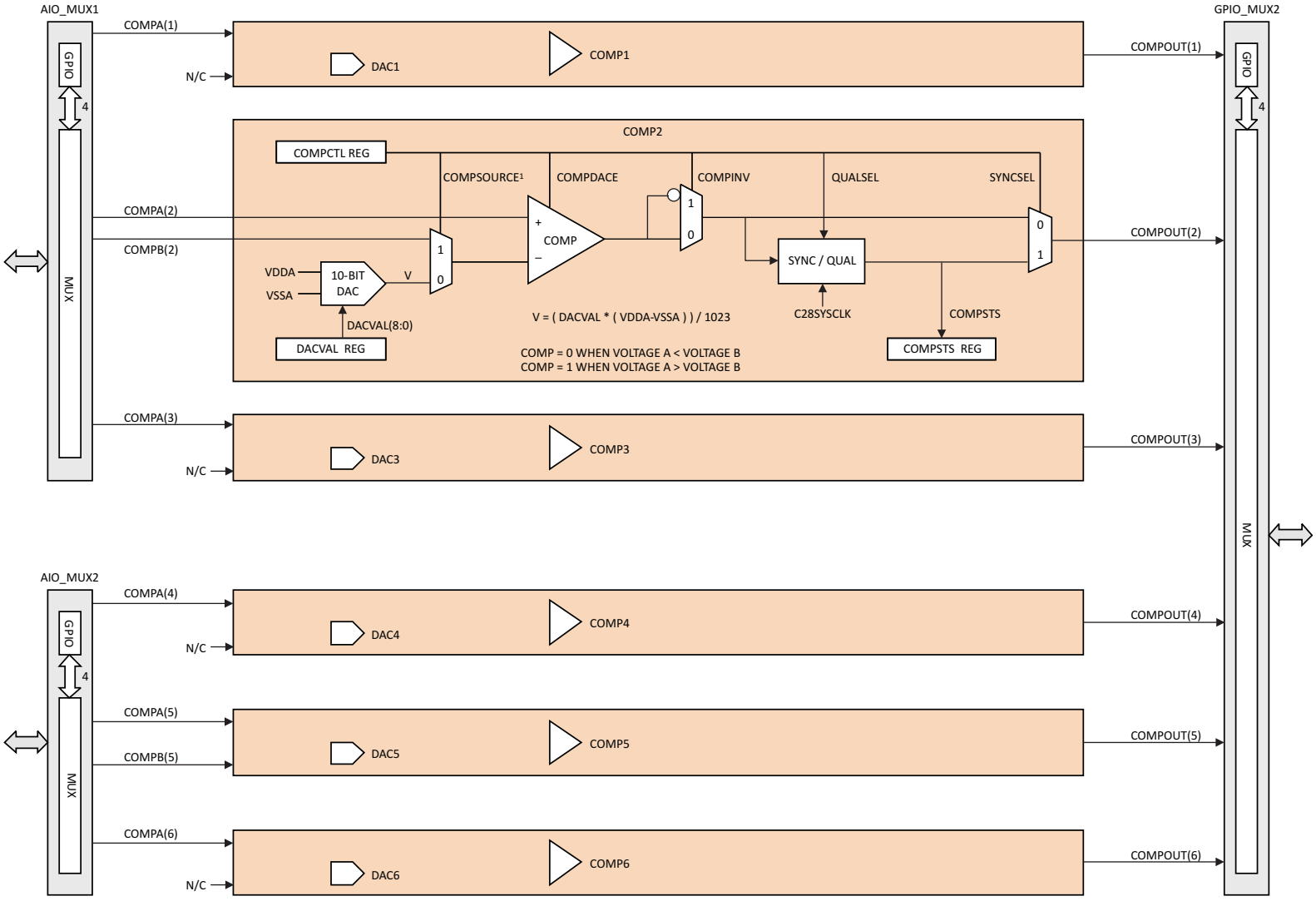

(1) COMPSOURCE BIT MUST BE SET TO "DAC" FOR COMP 1, 3, 4, AND 6 , AS THE CORRESPONDING COMPB INPUTS ARE NOT CONNECTED

Figure 5-4. Comparator + DAC Units

PRODUCT PREVIEW

5.3.3 Inter-Processor Communications (IPC)

Figure 5-5 shows the internal structure of the IPC peripheral used to synchronize program execution and exchange of data between the Cortex™-M3 and the C28x CPU. IPC can be used by itself when synchronizing program execution or it can be used in conjunction with Message RAMs when coordinating data transfers between processors. In either case, the operation of the IPC is the same. There are two independent sides to the IPC peripheral—MTOC (Master to Control) and CTOM (Control to Master).

The MTOC IPC is used by the Master Subsystem to send events to the Control Subsystem. This is typically accomplished using the following three registers: MTOCIPCSET, MTOCIPCFLG, and MTOCIPCACK. Each of the 32 bits of these registers represents 32 independent channels through which the Cortex™-M3 CPU can send up to 32 events to the C28x CPU via software handshaking. Additionally, the first 4 bits of the MTOCIPC registers are supplemented with interrupts. To send an event via channel 2, for example, the Cortex™-M3 and C28x CPUs write to, and read from bit 2 of the MTOCIPCSET, MTOCIPCFLG, MTOCIPCACK registers. The handshake starts with the Cortex™-M3 polling bit 2 of the MTOCIPCFLG register to make sure it is ‘0’. Next, the Cortex™-M3 writes a ‘1’ into bit 2 of the MTOCIPCSET register to start the handshake. In the mean time, the C28x is continually polling the MTOCIPCFLG register while waiting for the message. As soon as the Cortex™-M3 writes ‘1’ to bit 2 of the MTOCIPCSET register, bit 2 of MTOCIPCFLG also turns ‘1’, thus announcing the event to the C28x. As soon as the C28x CPU reads a ‘1’ from the MTOCIPCFLG register, it should acknowledge by writing a ‘1’ to bit 2 of the MTOCIPCACK register. This, in turn, clears bit 2 of the MTOCIPCFLG register, enabling the Cortex™-M3 to send another message. Since the first four channels (bits 0, 1, 2, 3) are backed up by interrupts, both processors in the above example can use IPC interrupt 2 instead of polling to increase performance.

A similar handshake is also used when sending data (not just event) from the Master Subsystem to the Control Subsystem, but with two additional steps. Before setting a bit in the MTOCIPCSET register, the Cortex™-M3 should first load the MTOC Message RAM with a block of data that it wants to make available to the C28x. In the second additional step, the C28x should read the data before setting a bit in the MTOCIPCACK register. This way, no data gets lost during multiple data transfers through a given block of the message RAM.

The CTOM IPC is used by the Control Subsystem to send events to the Master Subsystem. This is typically accomplished using the following three registers: CTOMIPCSET, CTOMIPCFLG and CTOMIPCACK. The process is exactly the same as that for the MTOC IPC communication above.

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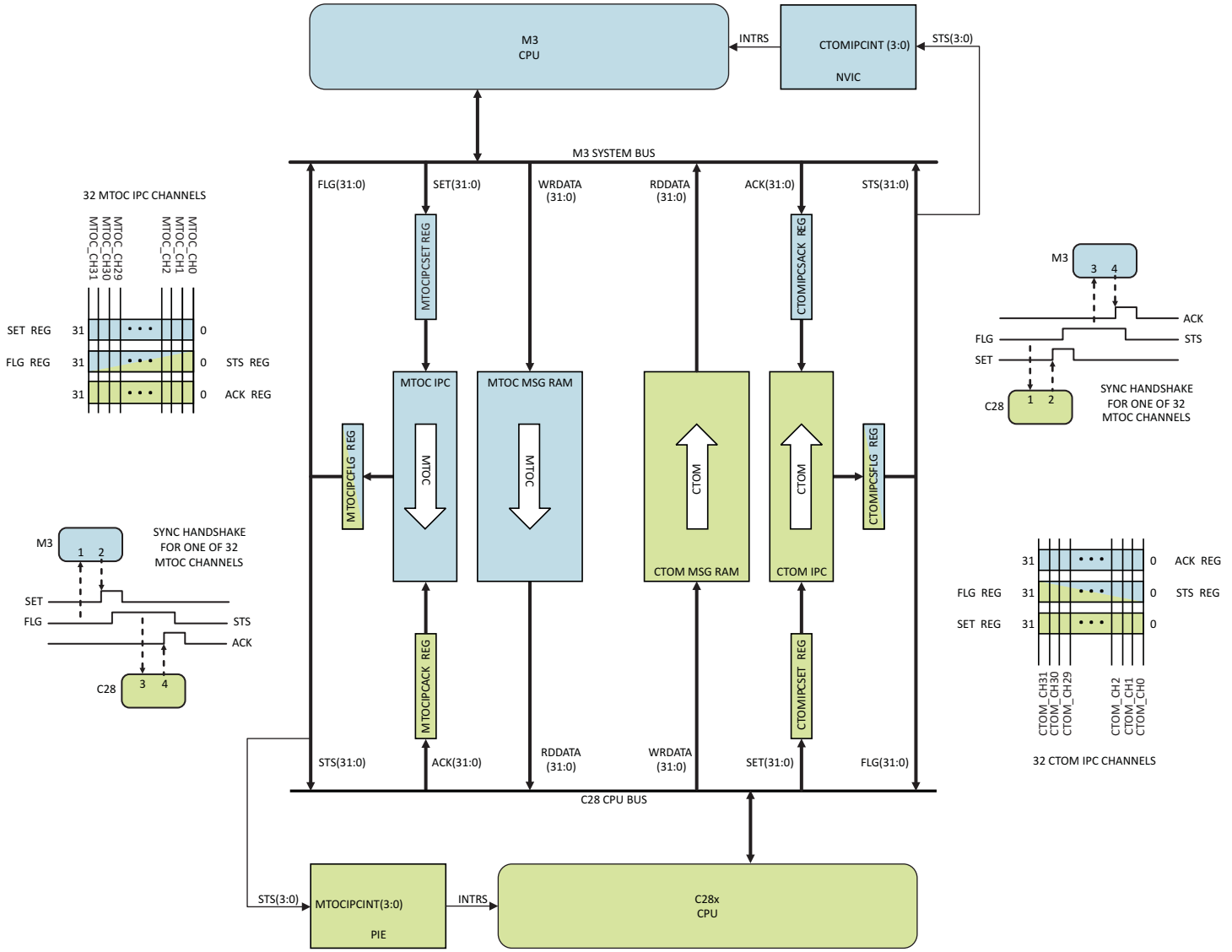

Figure 5-5. Interprocessor Communications (IPC)

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5.4 Current Consumption

Table 5-1. F28M35Hx Current Consumption at 150-MHz C28x SYSCLKOUT and 75-MHz M3SSCLK(1)(2)

MODE	TEST CONDITIONS(3)	VREG ENABLED				VREG DISABLED							
		I_{DDIO}(4)		I_{DDA}		I_{DD18}		I_{DD12}		I_{DDIO}(4)		I_{DDA}	
		TYP(5)	MAX	TYP(5)	MAX	TYP(5)	MAX	TYP(5)	MAX	TYP(5)	MAX	TYP(5)	MAX
Operational (RAM)	The following Cortex™-M3 peripherals are exercised: • I2C1 • SSI1/2 • UART0/1/2 • CAN0 • USB • µDMA • Timer0/1 • µCRC • WDOG0/1 • Flash • Internal Oscillators 1 and 2 The following C28x peripherals are exercised: • ePWM1/2/3/4/7/8 • McBSP • eQEP1/2 • eCAP1/2/3/4 • SCI-A • SPI-A • I2C • DMA • VCU • FPU • Flash The following Analog peripherals are exercised: • ADC1/2 • Comparator1/2/3/4/5/6	217 mA	–	30 mA	–	20 mA	–	121 mA	–	74 mA	–	30 mA	–
SLEEP IDLE	• PLL is on. • Cortex™-M3 CPU is not executing. • M3SSCLK is on. • C28CLKIN is on. • C28x™ CPU is not executing. • C28CPUCLK is off. • C28SYSCLK is on.	TBD	–	TBD	–	TBD	–	TBD	–	TBD	–	TBD	–

(1) Currently only typical current consumption data is available, maximum numbers will come in another release of this data sheet.
(2) The numbers in Table 5-1 are not assured at this time, and are subject to change.
(3) The following is done in a loop:
- Code is running out of RAM.
- All I/O pins are left unconnected.
- All the communication peripherals are exercised in loop-back mode.
- USB – Only logic is exercised by loading and unloading FIFO.
- µDMA does memory-to-memory transfer.
- DMA does memory-to-memory transfer.
- VCU – CRC calculated and checked.
- FPU – Float operations performed.
- ePWM – 6 enabled and generates 20-MHz PWM output on 12 pins, HRPWM clock enabled.
- Timers and Watchdog serviced.
- eCAP in APWM mode generates 36.6-kHz output on 4 pins.
- ADC performs continuous conversion.
- FLASH is continuously read and in active state.
- XCLKOUT is turned off.

(4) I_{DDIO} current is dependent on the electrical loading on the I/O pins.
(5) The TYP numbers are applicable over room temperature and nominal voltage.

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Table 5-1. F28M35Hx Current Consumption at 150-MHz C28x SYSCLKOUT and 75-MHz M3SSCLK[1][2] (continued)

MODE	TEST CONDITIONS[3]	VREG ENABLED				VREG DISABLED							
		I_{DDIO}[4]		I_{DDA}		I_{DD18}		I_{DD12}		I_{DDIO}[4]		I_{DDA}	
		TYP[5]	MAX	TYP[5]	MAX	TYP[5]	MAX	TYP[5]	MAX	TYP[5]	MAX	TYP[5]	MAX
SLEEP STANDBY	• PLL is on. • Cortex™-M3 CPU is not executing. • M3SSCLK is on. • C28CLKIN is off. • C28x™ CPU is not executing. • C28CPUCLK is off. • C28SYSCLK is off.	TBD	–	TBD	–	TBD	–	TBD	–	TBD	–	TBD	–
DEEP SLEEP STANDBY	• PLL is off. • Cortex™-M3 CPU is not executing. • M3SSCLK is 32 kHz. • C28CLKIN is off. • C28x™ CPU is not executing. • C28CPUCLK is off. • C28SYSCLK is off.	TBD	–	TBD	–	TBD	–	TBD	–	TBD	–	TBD	–

NOTE

The peripheral - I/O multiplexing implemented in the device prevents all available peripherals from being used at the same time. This is because more than one peripheral function may share an I/O pin. It is, however, possible to turn on the clocks to all the peripherals at the same time, although such a configuration is not useful. If this is done, the current drawn by the device will be more than the numbers specified in the current consumption table.

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5.5 Power Sequencing

5.5.1 Power Management and Supervisory Circuit Solutions

Table 5-2 lists the power management and supervisory circuit solutions for F28M35x devices. LDO selection depends on the total power consumed in the end application. Go to www.ti.com and click on *Power Management* for a complete list of TI power ICs or select the *Power Management Selection Guide* link for specific power reference designs.

Table 5-2. Power Management and Supervisory Circuit Solutions

SUPPLIER	TYPE	PART	DESCRIPTION
Texas Instruments	LDO	TPS767D301	Dual 1-A low-dropout regulator (LDO) with supply voltage supervisor (SVS)
Texas Instruments	LDO	TPS70202	Dual 500/250-mA LDO with SVS
Texas Instruments	LDO	TPS766xx	250-mA LDO with PG
Texas Instruments	SVS	TPS3808	Open Drain SVS with programmable delay
Texas Instruments	SVS	TPS3803	Low-cost Open-drain SVS with 5 µS delay
Texas Instruments	LDO	TPS799xx	200-mA LDO in WCSP package
Texas Instruments	LDO	TPS736xx	400-mA LDO with 40 mV of V_{DO}
Texas Instruments	DC/DC	TPS62110	High V_{in} 1.2-A dc/dc converter in 4x4 QFN package
Texas Instruments	DC/DC	TPS6230x	500-mA converter in WCSP package
Texas Instruments	EVM	TPS62290	6-V input, 1.8-V output, 1-A evaluation module
Texas Instruments	DC/DC	TPS62291	1-A step-down dc/dc converter in 2x2 SON package

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6 Device and Documentation Support

6.1 Device Support

6.1.1 Development Support

TI offers an extensive line of development tools, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules. The tool's support documentation is electronically available within the Code Composer Studio™ Integrated Development Environment (IDE).

The following products support development of processor applications:

Software Development Tools: Code Composer Studio™ Integrated Development Environment (IDE): including Editor C/C++/Assembly Code Generation, and Debug plus additional development tools Scalable, Real-Time Foundation Software (SYS/BIOS), which provides the basic run-time target software needed to support any processor application.

Hardware Development Tools: Extended Development System (XDS™) Emulator

For a complete listing of development-support tools for the processor platform, visit the Texas Instruments website at www.ti.com. For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

6.1.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all Concerto™ MCU devices and support tools. Each Concerto™ MCU commercial family member has one of three prefixes: x, p, or no prefix (e.g., **x**F28M35H52C1RFPT). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (with prefix **x**/TMDX) through fully qualified production devices/tools (no prefix/TMDS).

xF28M35...	Experimental device that is not necessarily representative of the final device's electrical specifications
pF28M35...	Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification
F28M35...	Fully qualified production device

Support tool development evolutionary flow:

TMDX	Development-support product that has not yet completed Texas Instruments internal qualification testing
TMDS	Fully qualified development-support product

Devices with prefix **x** or **p** and TMDX development-support tools are shipped against the following disclaimer:
"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

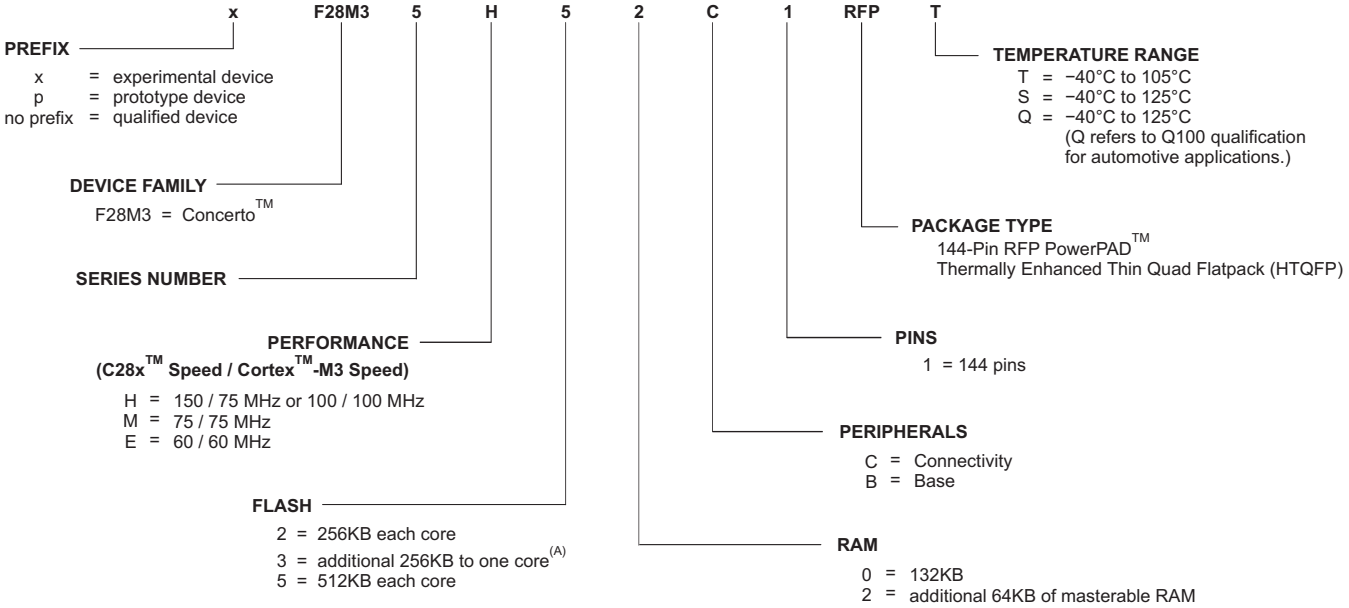
Predictions show that prototype devices with prefix of **x** or **p** have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, RFP) and temperature range (for example, T).

PRODUCT PREVIEW

For device part numbers and further ordering information of F28M35x devices in the RFP package type, see the TI website (www.ti.com) or contact your TI sales representative.

For additional description of the device nomenclature markings on the die, see the *F28M35H20B1, F28M35H20C1, F28M35H22B1, F28M35H22C1, F28M35H32B1, F28M35H32C1, F28M35H50B1, F28M35H50C1, F28M35H52B1, F28M35H52C1 Concerto MCU Silicon Errata* (literature number SPRZ357).



A. The additional 256KB is added to the Cortex™-M3 core (Connectivity Devices) or to the C28x™ core (Base Devices).

Figure 6-1. Device Nomenclature

6.2 Documentation Support

The following documents describe the MCU. Copies of these documents are available on the Internet at www.ti.com. Tip: Enter the literature number in the search box.

SPRUH22 ***Concerto F28M35x Technical Reference Manual***

SPRZ357 ***F28M35H20B1, F28M35H20C1, F28M35H22B1, F28M35H22C1, F28M35H32B1, F28M35H32C1, F28M35H50B1, F28M35H50C1, F28M35H52B1, F28M35H52C1 Concerto MCU Silicon Errata***

6.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

TI Embedded Processors Wiki ***Texas Instruments Embedded Processors Wiki.*** Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

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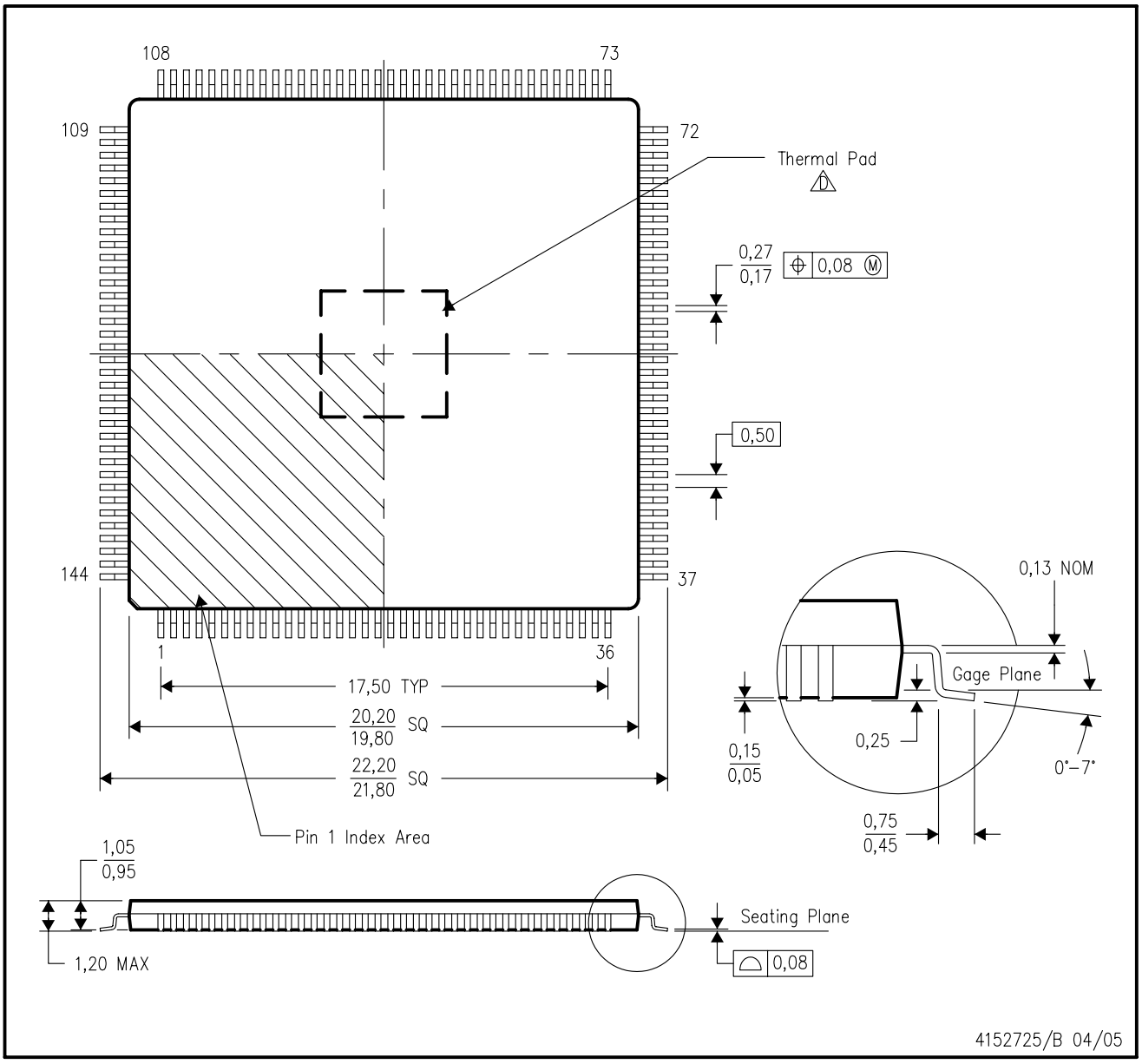
7 Mechanical Packaging and Orderable Information

7.1 Packaging Information

The following packaging information and addendum reflect the most current data available for the designated device(s). This data is subject to change without notice and without revision of this document.

PRODUCT PREVIEW

RFP (S–PQFP–G144) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments.

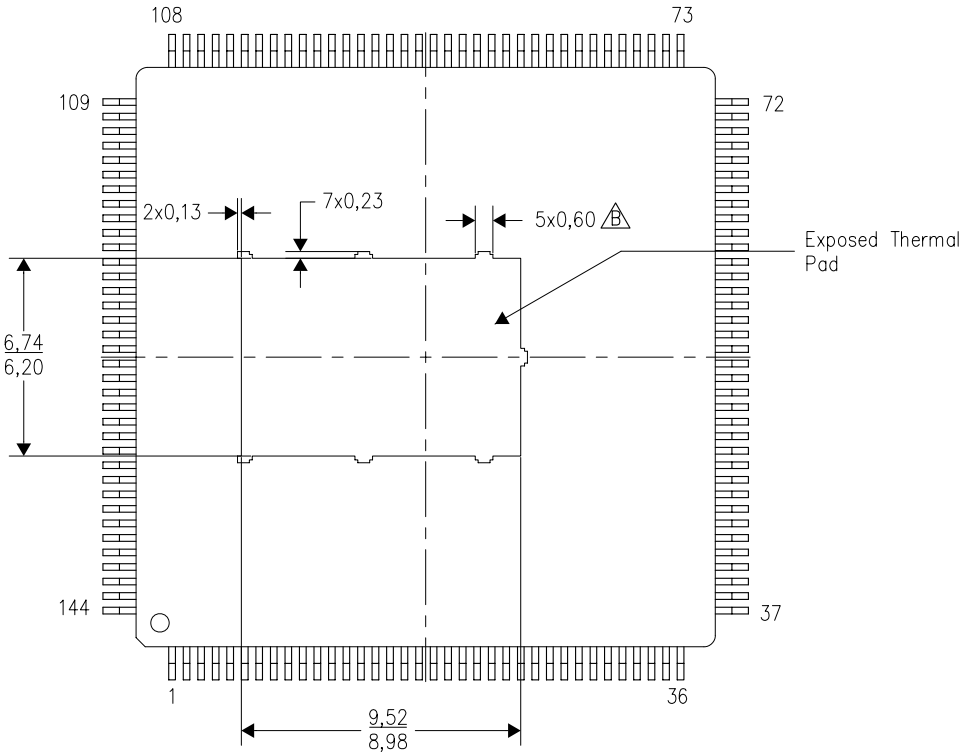
RFP (S–PQFP–G144) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206900–12/D 09/10

NOTES: A. All linear dimensions are in millimeters

B. Tie strap features may not be present

PowerPAD is a trademark of Texas Instruments.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
F28M35H20B1RFPQ	PREVIEW	HTQFP	RFP	144	1000	TBD	Call TI	Call TI	
F28M35H20B1RFPS	PREVIEW	HTQFP	RFP	144	1000	TBD	Call TI	Call TI	
F28M35H20B1RFPT	PREVIEW	HTQFP	RFP	144	1000	TBD	Call TI	Call TI	
F28M35H20C1RFPQ	PREVIEW	HTQFP	RFP	144	1000	TBD	Call TI	Call TI	
F28M35H20C1RFPS	PREVIEW	HTQFP	RFP	144	1000	TBD	Call TI	Call TI	
F28M35H20C1RFPT	PREVIEW	HTQFP	RFP	144	1000	TBD	Call TI	Call TI	
F28M35H22B1RFPQ	PREVIEW	HTQFP	RFP	144	1000	TBD	Call TI	Call TI	
F28M35H22B1RFPS	PREVIEW	HTQFP	RFP	144	1000	TBD	Call TI	Call TI	
F28M35H22B1RFPT	PREVIEW	HTQFP	RFP	144	1000	TBD	Call TI	Call TI	
F28M35H22C1RFPQ	PREVIEW	HTQFP	RFP	144	1000	TBD	Call TI	Call TI	
F28M35H22C1RFPS	PREVIEW	HTQFP	RFP	144	1000	TBD	Call TI	Call TI	
F28M35H22C1RFPT	PREVIEW	HTQFP	RFP	144	1000	TBD	Call TI	Call TI	
F28M35H32B1RFPQ	PREVIEW	HTQFP	RFP	144	1000	TBD	Call TI	Call TI	
F28M35H32B1RFPS	PREVIEW	HTQFP	RFP	144	1000	TBD	Call TI	Call TI	
F28M35H32B1RFPT	PREVIEW	HTQFP	RFP	144	1000	TBD	Call TI	Call TI	
F28M35H32C1RFPQ	PREVIEW	HTQFP	RFP	144	1000	TBD	Call TI	Call TI	
F28M35H32C1RFPS	PREVIEW	HTQFP	RFP	144	1000	TBD	Call TI	Call TI	
F28M35H32C1RFPT	PREVIEW	HTQFP	RFP	144	1000	TBD	Call TI	Call TI	
F28M35H50B1RFPQ	PREVIEW	HTQFP	RFP	144	1000	TBD	Call TI	Call TI	
F28M35H50B1RFPS	PREVIEW	HTQFP	RFP	144	1000	TBD	Call TI	Call TI	
F28M35H50B1RFPT	PREVIEW	HTQFP	RFP	144	1000	TBD	Call TI	Call TI	
F28M35H50C1RFPQ	PREVIEW	HTQFP	RFP	144	1000	TBD	Call TI	Call TI	
F28M35H50C1RFPS	PREVIEW	HTQFP	RFP	144	1000	TBD	Call TI	Call TI	
F28M35H50C1RFPT	PREVIEW	HTQFP	RFP	144	1000	TBD	Call TI	Call TI	
F28M35H52B1RFPQ	PREVIEW	HTQFP	RFP	144	1000	TBD	Call TI	Call TI	
F28M35H52B1RFPS	PREVIEW	HTQFP	RFP	144	1000	TBD	Call TI	Call TI	
F28M35H52B1RFPT	PREVIEW	HTQFP	RFP	144	1000	TBD	Call TI	Call TI	
F28M35H52C1RFPQ	PREVIEW	HTQFP	RFP	144	1000	TBD	Call TI	Call TI	
F28M35H52C1RFPS	PREVIEW	HTQFP	RFP	144	1000	TBD	Call TI	Call TI	
F28M35H52C1RFPT	PREVIEW	HTQFP	RFP	144	1000	TBD	Call TI	Call TI	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
XF28M35H52C1RFPT	ACTIVE	HTQFP	RFP	144	1	TBD	Call TI	Call TI	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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