TPS75005 Advanced Information: LDO+SVS Combined Accuracy

Masashi Nogawa *Power Management Products*

1 OVERVIEW

The TPS75005 is a complete power management solution for C2000™ controllers from Texas Instruments. This document is a supplimental advanced information to the TPS75005 data sheet.

In this advanced information document, the concept of low dropout (LDO) and supply voltage supervisor (SVS) combined accuracy is described in detail.

2 TRUE 5% SOLUTION FOR C2000 CONTROLLERS

All target C2000 controllers specify nominal power-supply input voltages to be accurate within ±5%. To monitor the power rails correctly, both the accuracy of the supply voltage and the accuracy window of the voltage monitor are forced to fit within the overall ±5% requirement. Until now, this requirement has been very difficult to achive. By integrating voltage regulators and voltage supervisors together, the TPS75005 offers a true 5% accuracy solution for C2000 controllers. This feature is very important for mission-critical applications.

Figure 1 and Figure 2 illustrate the primary differences between the TPS75005 and traditional solutions. In Figure 1, the V_{LDO1} and V_{LDO2} waveforms are shown as green during the active power-good (PG) = H period. The green-colored sections are within a ±5% window because the supervisor thresholds V_{SVS1} and V_{SVS2} are within that ±5% window, assuring that the TPS75005 supplies the correct voltage.

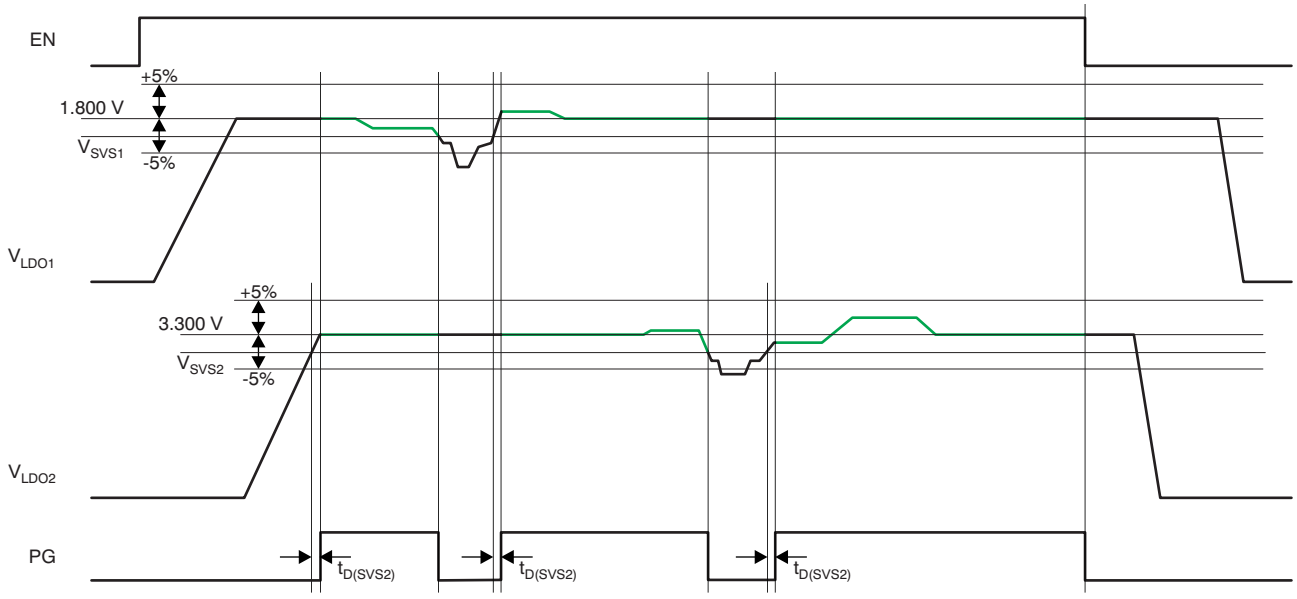

Figure 1. Output Voltage Accuracy and Power-Good with the TPS75005

By contrast, a traditional C2000 solution is shown in Figure 2. Here, everything is the same as Figure 1 except that the supervisor thresholds V_{th18} and V_{th33} are outside the ±5% window because of the poor accuracy of the typical supervisor circuit. In a traditional approach, the power-good signal outputs high, even though three red-colored sections of the V18 and V33 waveforms are outside of the ±5% window. These false power-good events occur when the output voltage rails exceed the respective supervisor thresholds, but the individual values do not reach the –5% line. False power-good events cause the C2000 controllers to operate beyond the recommended operating conditions.

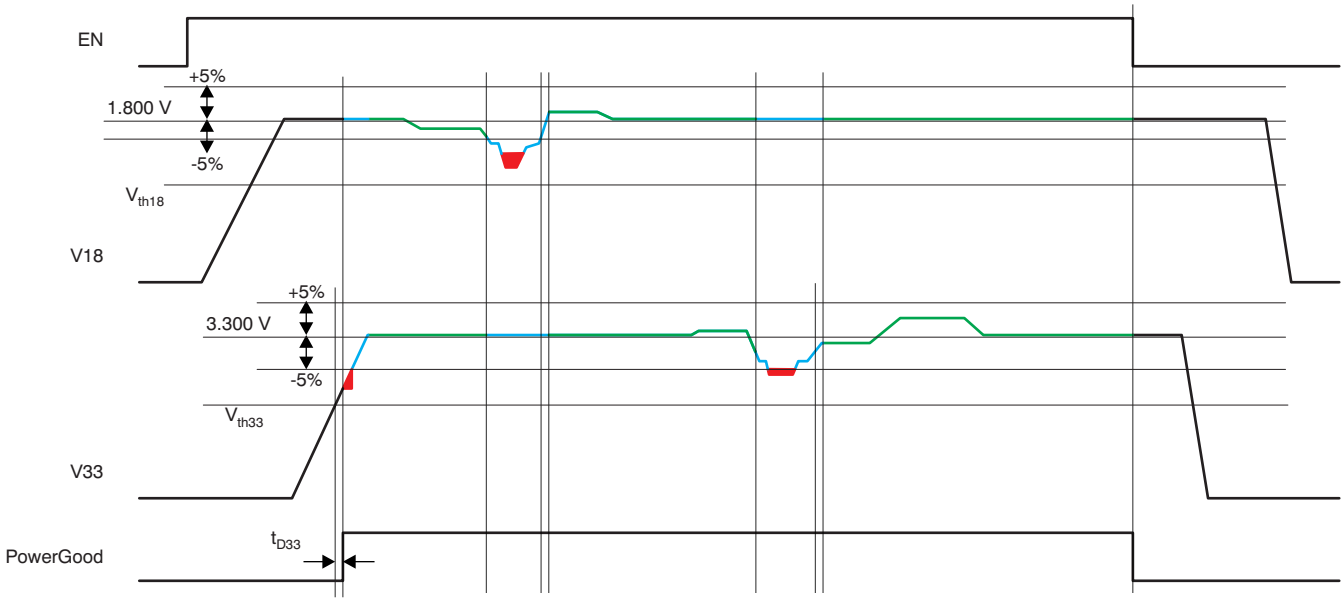

Figure 2. Output Voltage Accuracy and Power-Good with a Traditional Solution

The TPS75005 is designed to offer this accurate power-good (PG) over all operating conditions. Figure 3 shows, in more detail, the concept of the TPS75005 tolerance design. For a 3.3-V rail, the output of LDO2 is designed, characterized, and tested to fit within the V_{OUT2} tolerance region across all input voltage, output current, and temperature range conditions. Simultaneously, the supervisor SVS2 window fits within the V_{SVS2} tolerance region over all input voltage and temperature range conditions.

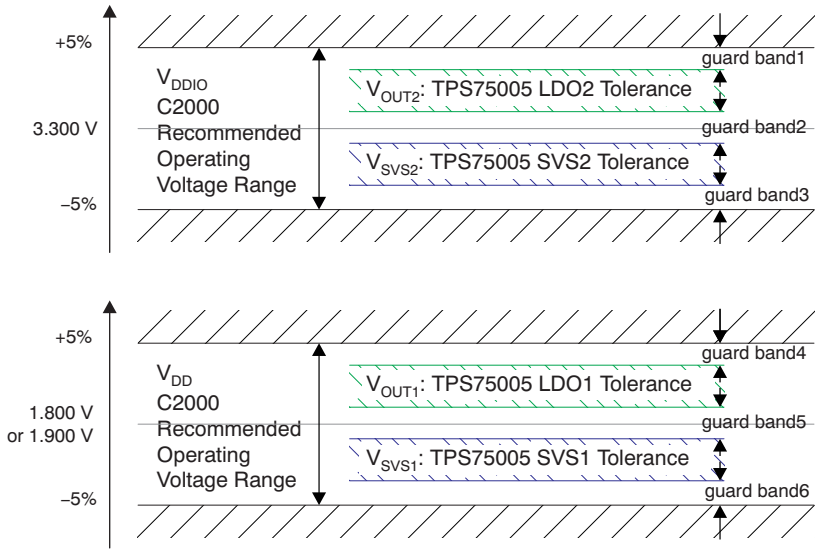

Figure 3. TPS75005 Tolerance Design Concept

As illustrated in Figure 3, both tolerance regions are surrounded by guard band 1, guard band 2, and guard band 3. The *first and third guard bands* indicate the limits of the ±5% limit. The *second guard band* shows the limit of the LDO2 and SVS2 tolerances. If the LDO2 and SVS2 tolerances overlap (that is, there is no guard band 2), there is a chance that LDO2 will not trigger the SVS2 threshold. In this situation, PG never reaches a *good* condition.
The same description applies to the 1.8-V rail for guard band 4, guard band 5, and guard band 6. The LDO1 and SVS1 tolerances are designed in the same manner.

Typical characteristic curves Figure 4 through Figure 7 from the TPS75005 data sheet show the corresponding measurement curves and confirm the following test results:

- The LDO1 output remains greater than 1.8 V (guard band 5) and does not exceed +5% of 1.8 V (guard band 4)
- The LDO2 output remains greater than 3.3 V (guard band 2) and does not exceed +5% of 3.3 V (guard band 1)
- The SVS1 threshold remains less than 1.8 V (guard band 5) and does not underrun –5% of 1.8 V (guard band 6)
- The SVS2 threshold remains less than 3.3 V (guard band 2) and does not underrun –5% of 3.3 V (guard band 3)

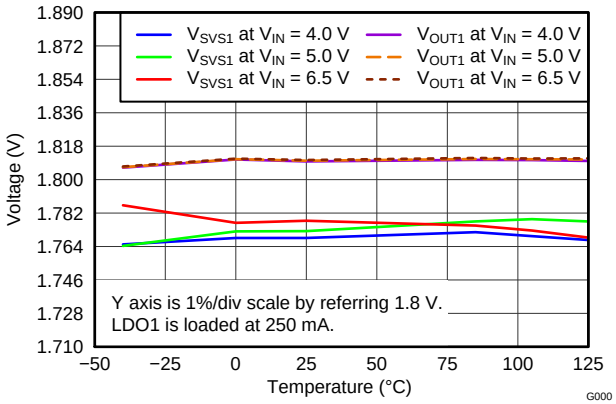

Figure 4. LDO1 (Output and Supervisor Threshold) Voltage vs Temperature

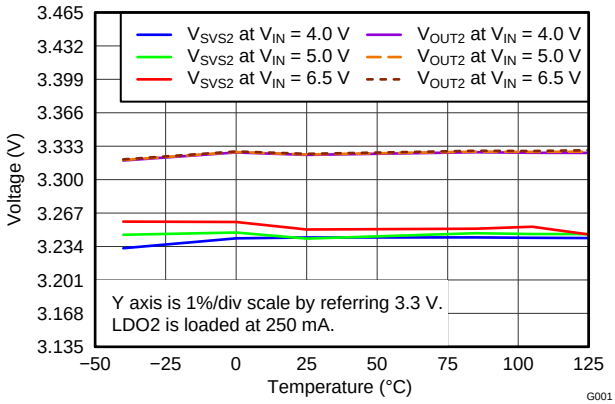

Figure 5. LDO2 (Output and Supervisor Threshold) Voltage vs Temperature

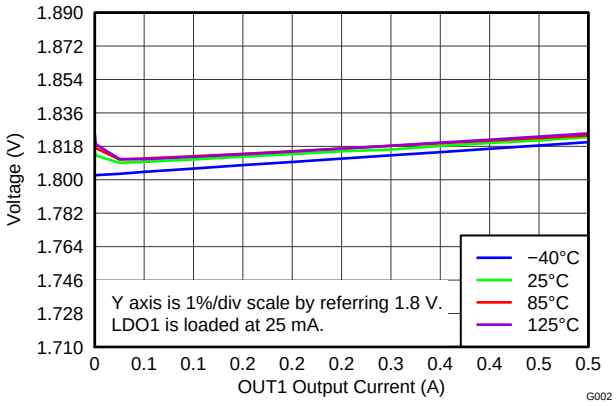

Figure 6. LDO1 Load Regulation

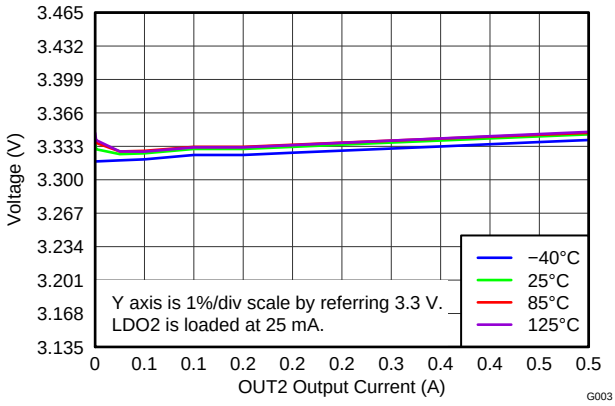

Figure 7. LDO2 Load Regulation

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