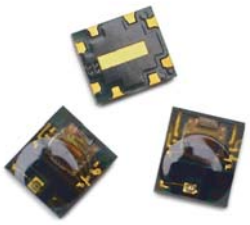
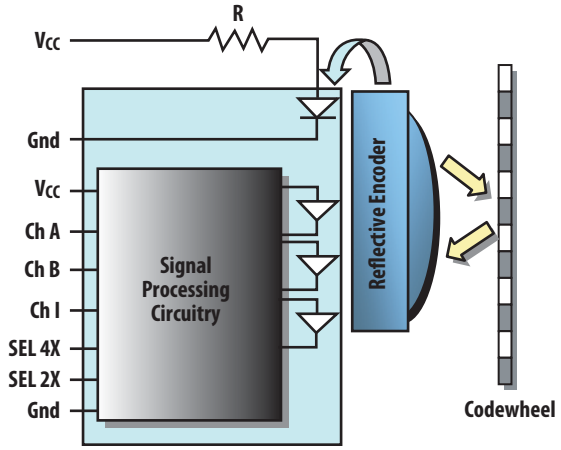
AEDR-850x
Reflective Three-Channel Encoder

Application Note 5500



Introduction

The AEDR-850x encoder is the smallest three-channel optical encoder with digital outputs in the market, employing reflective technology for motion control purposes. This article describes the recommended resistor biasing needed, the codewheel design for the special index track, and the proper mounting orientation and positioning with respect to the codewheel to achieve the desired performance.



Note: Drawing not to scale.

Figure 1. AEDR-850x Schematic Diagram

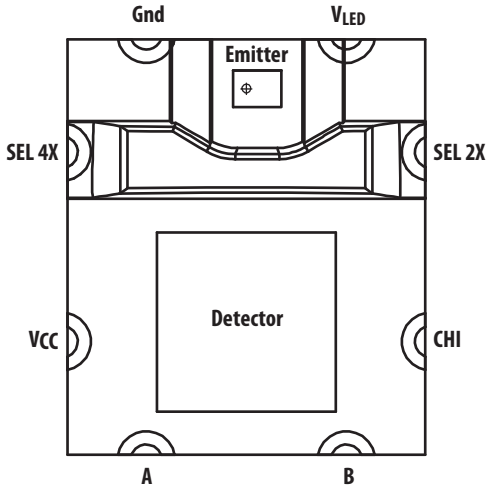


Figure 2. AEDR-850x pin layout

LED current limiting resistor, R

A resistor is required to limit current to the LED. The recommended value is 180 Ω (±1%) and the resistor should be placed in series between the Vcc supply (5 V) and pin V_{LED}. This will produce an LED current of approximately 15 mA for optimal encoder performance.

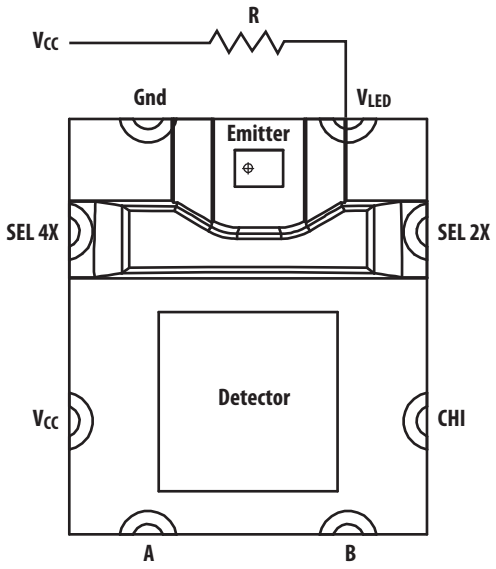


Figure 3. Resistor, R is required for biasing

Gap setting

The recommended operating gap setting for the encoder is 0.5 mm to 1 mm from the surface of the encoder to that of the codewheel.

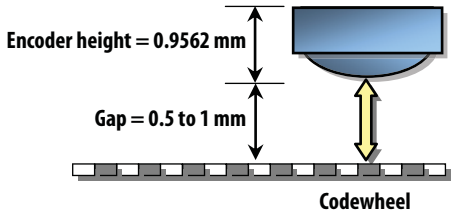
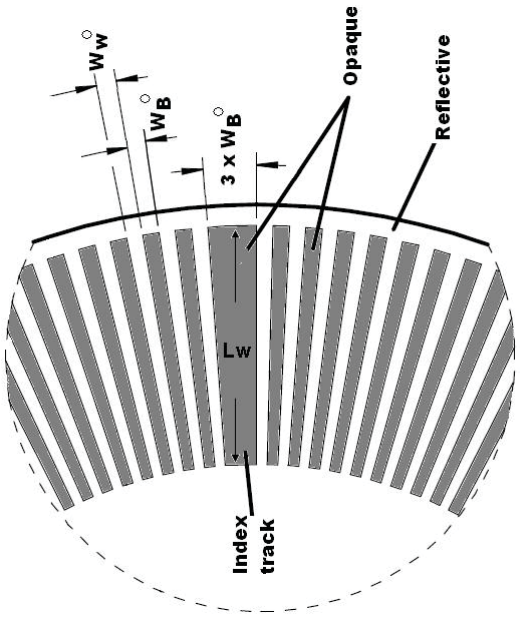


Figure 4. Recommended gap distance between codewheel and encoder

Codewheel Design

The most important dimension to consider for codewheel design is the width angle for the index (I) channel pattern, which should be 3 x W_B°. The dimension Lw should be at least 1.8 mm.



Index track design : Patent granted

L_W = 1.8 mm (minimum)

Figure 5. The Index track width angle should equal 3 x W_B°

Codewheel Design Example

The following two codewheel design examples – the first a two-channel design and the second a three-channel design – both employ an operating radius (Rop) of 1.70 mm @ 128 CPR. The index track design uses two tracks for the special track (index), hence reducing the overall physical track count but not the counts per revolution (CPR). The **CPR remains the same** because the count during this index transition is generated by an intelligent signal processing circuit.

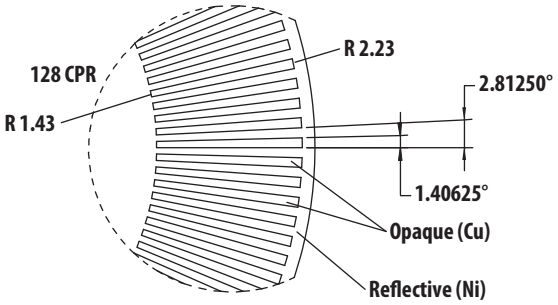


Figure 6. Codewheel pattern for a two-channel encoder

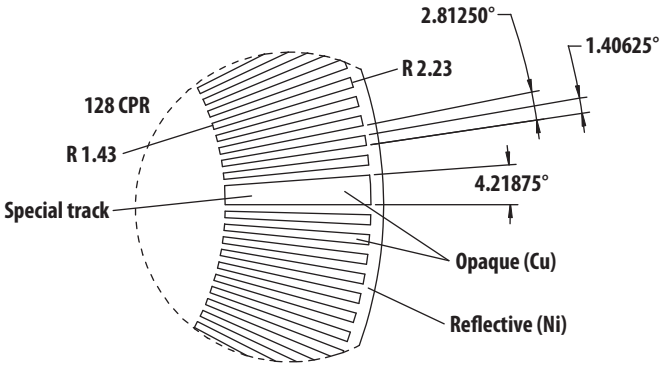


Figure 7. Patented codewheel pattern for a three-channel encoder

Notes:

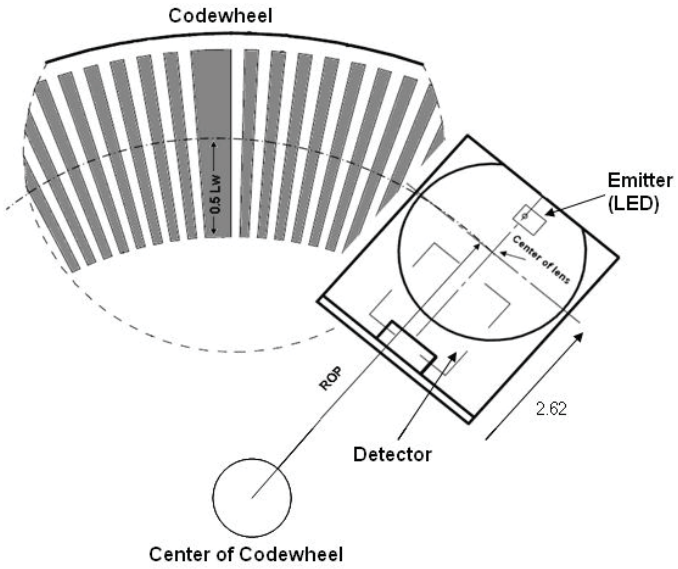
a). Two tracks from the original 128 CPR two-channel codewheel design have been utilized for the special track (Index), but CPR remains the same.

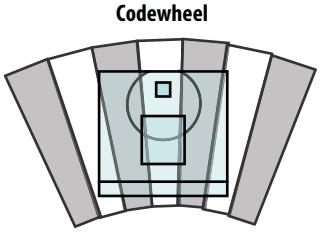
b) This is due to the nature of the design for the index track.

Encoder Placement Orientation and Positioning

The AEDR-850X is designed such that both the emitter and detector IC should be placed parallel to the window/ bar orientation *with the encoder mounted on top of the codewheel* (as shown in the picture below right).

When properly oriented the detector side will be closer to the center of codewheel than the emitter. Most importantly, **the center of the lens** of the encoder unit must be aligned with the codewheel (R_{OP}), or more specifically tangent to the center point of Lw (½ of the Length of Window). For best results it is recommended that Lw be 1.8 mm or greater.





Placement orientation of the encoder's emitter and detector on the codewheel

Figure 8. Center of the lens should be aligned with the Rop of the codewheel

AEDR-850x Alignment Step

The below steps are highly recommended for fine tuning of the mechanical alignment or may be adopted as a means for the final verification that optimal alignment has been achieved; for optimal signal performance.

It is hence recommended to include these external oscilloscope probing points (for encoder's signal "A" and "I") in the PCB design to allow for this final alignment verification feature. The AEDR-850x module SEL 2X and SEL 4X pins, must also be able to be set to "factory use" mode too; to perform this alignment process. In this mode, both SEL 2X and SEL 4X are set to logic "H".

A two channel oscilloscope would be required, with triggering channel set for the Index signal "I" and the other channel for signal "A" of the encoder output.

Step 1. Set the encoder's built-in interpolator pins to "factory use" (SEL 2X and SEL 4X pins - both at "H" state) as shown in Table 1.

Table 1. Interpolator setting for alignment mode Figure 9.

Encoder's Built-in Interpolation

Pin (Interpolation)		Interpolation
SEL 4X	SEL 2X	Factor
L	L	1X
L	H	2X
H	L	4X
H	H	Factory use

H = HIGH Logic Level

L = LOW Logic Level

Step 2. Make X, Y and Z alignment where applicable on the mechanical setup; to ensure that signal "A" is centered with respect to signal "I" index, as much as possible (refer Figure 9), with the help of an oscilloscope.

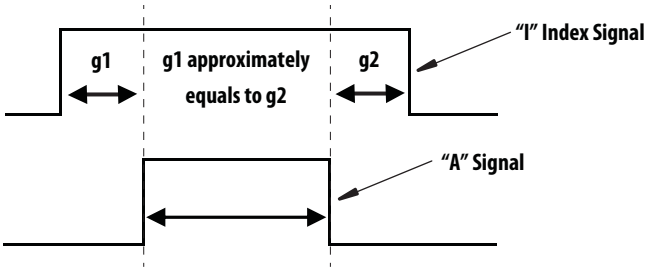


Figure 9. Centering signal "A" relative to "I" index signal, aided by an oscilloscope.

Step 3. Revert back the SEL 2X and SEL 4X to the original desired logic state setting, once the signal "A" is satisfactorily centered to "I" index signal.

Physical dimensions

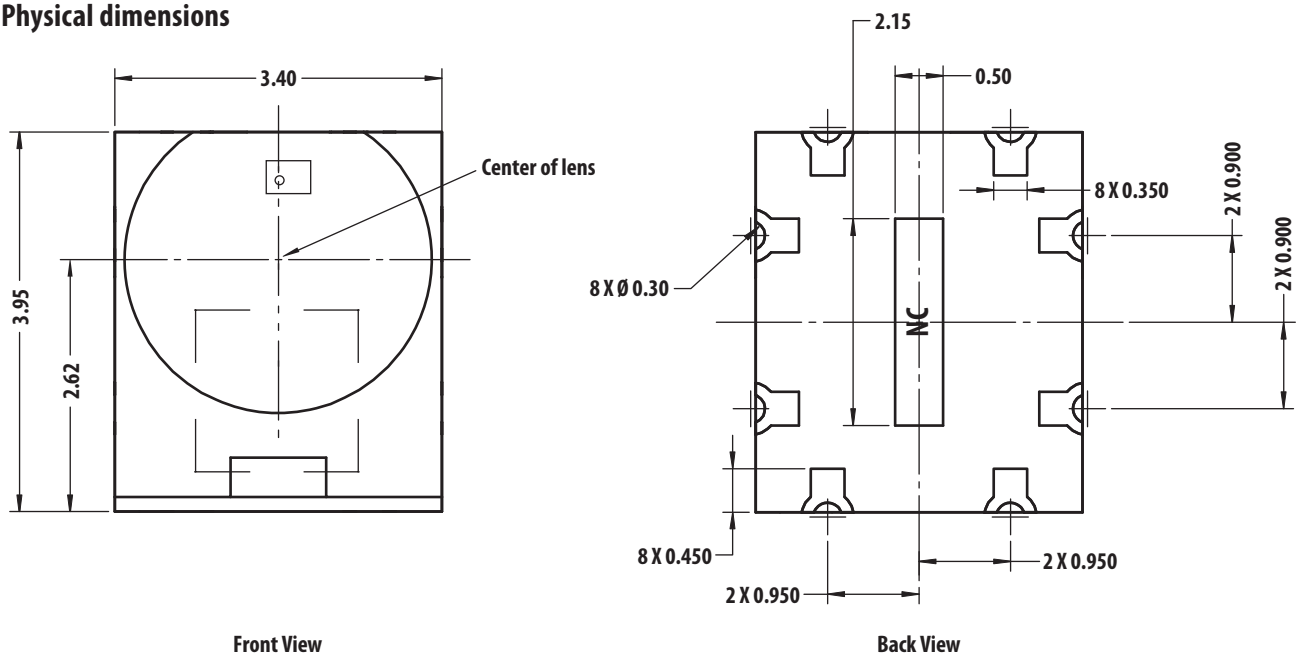


Figure 10. Physical dimensions

Recommended PCB layout pattern

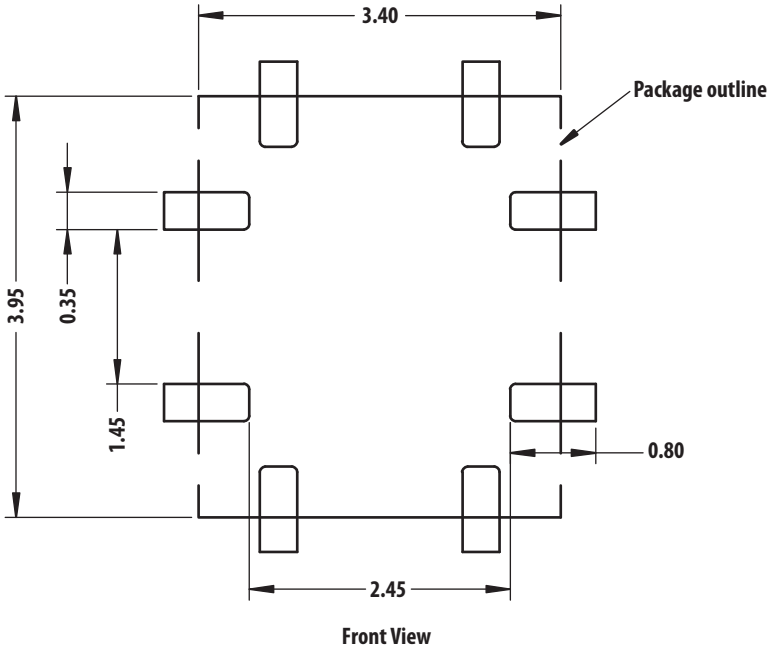


Figure 11. Recommended PCB layout pattern

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