

# AN11148

## BGU7003 1900 MHz to 2100 MHz LNA application

Rev. 1 — 1 March 2012

Application note

### Document information

Info	Content
<b>Keywords</b>	LNA, 1900 MHz to 2100 MHz, BGU7003, GSM, W-CDMA
<b>Abstract</b>	This application note provides circuit, layout, BOM and performance information for 1900 MHz to 2100 MHz LNA equipped with NXP Semiconductors BGU7003



## Revision history

Rev	Date	Description
v.1	20120301	initial version

## Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

## 1. Introduction

The BGU7003 is a wideband Silicon Germanium Amplifier MMIC intended for high speed, low noise applications. It is used for LNA applications up to 6 GHz such as GPS, satellite radio, cordless phone and China Mobile Multimedia Broadcasting (CMMB). The BGU7003 contains one RF stage and internal bias that is temperature stabilized. It also contains a power down function to shut down the amplifier with a logic signal on the enable pin.

The BGU7003 is ideal for use in portable electronic devices, such as mobile phones, Personal Digital Assistants (PDAs), Personal Navigation Devices (PNDs) etc.

The 1900 MHz to 2100 MHz LNA evaluation board (EVB) is designed to evaluate the performance of the BGU7003 applied as a GSM/W-CDMA LNA. In this document, the application diagram, board layout, bill of material, and some typical results are given.

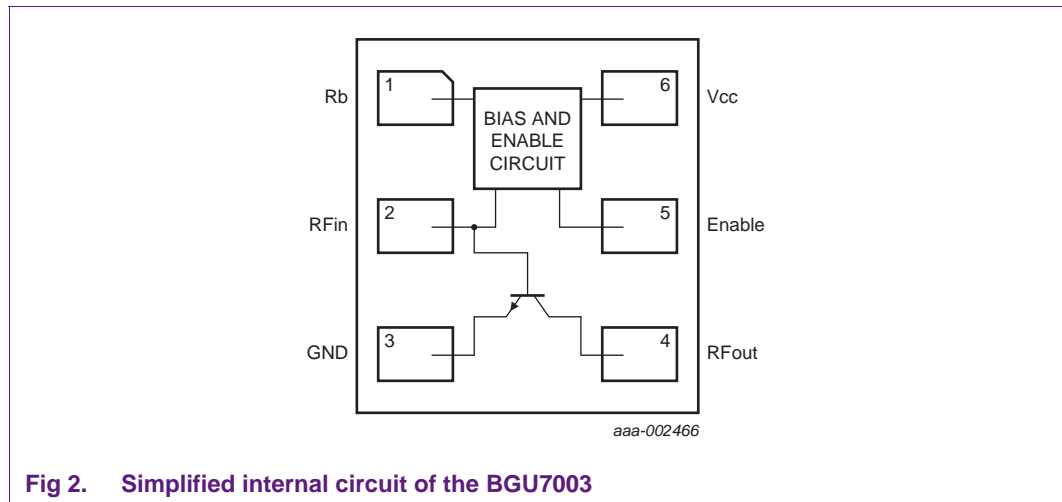
[Figure 1](#) shows the evaluation board



Fig 1. BGU7003, 1900 MHz to 2100 MHz LNA evaluation board

## 2. General description

The BGU7003 design is a wideband Silicon Germanium (SiGe) transistor with internal bias circuit. This bias circuit is temperature stabilized, which keeps the current constant over temperature. The bias current for the RF stage can be set via an external bias resistor in order to give the designer flexibility in choosing the bias current. The MMIC is also supplied with a power down function that allows the designer to control the MMIC via a logic signal. This power down mode only consumes 0.4  $\mu$ A. In [Figure 2](#) the simplified internal circuit of the BGU7003 is given.



**Fig 2. Simplified internal circuit of the BGU7003**

The BGU7003 is not internally matched so for both input and output a matching circuit needs to be designed. The fact that no internal matching is available makes the product suitable for different application areas.

In the following Sections the BGU7003 is described applied as a 1900 MHz to 2100 MHz LNA.

### 3. Application board

The BGU7003 1900 MHz ~ 2100 MHz LNA EVB simplifies the evaluation of the BGU7003 wideband amplifier MMIC, for the GSM / W-CDMA application area. The EVB enables testing of the device performance and requires no additional support circuitry. The board is fully assembled with the BGU7003 IC, including input and output matching, to optimize the performance. The board is supplied with two SMA connectors for input and output connection to RF test equipment:

This document describes the EVBs functionality when operated from a 2.5 V DC supply voltage

#### 3.1 Application circuit

The application diagram as supplied on the evaluation board is shown in [Figure 3](#).

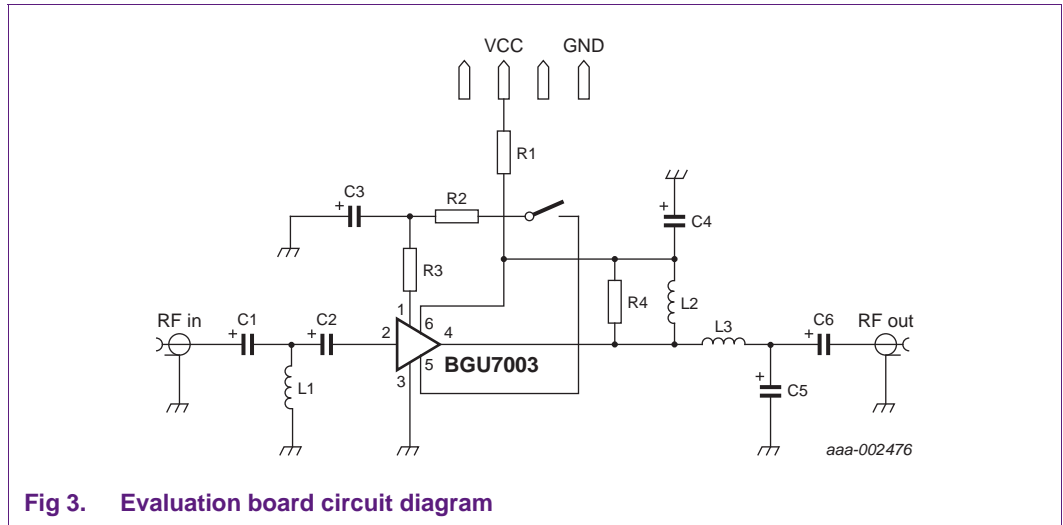


Fig 3. Evaluation board circuit diagram

### 3.2 Board layout

Figure 4 shows the board layout with components.

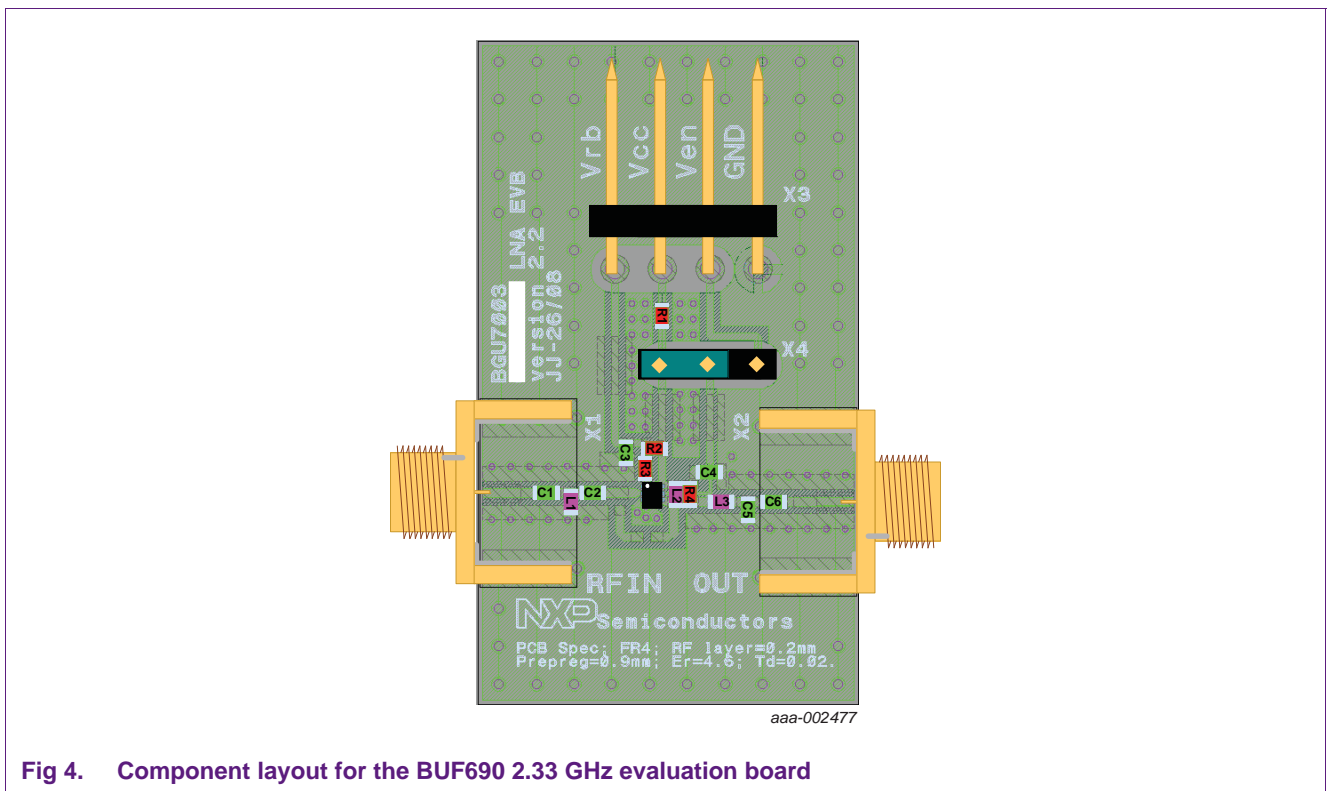


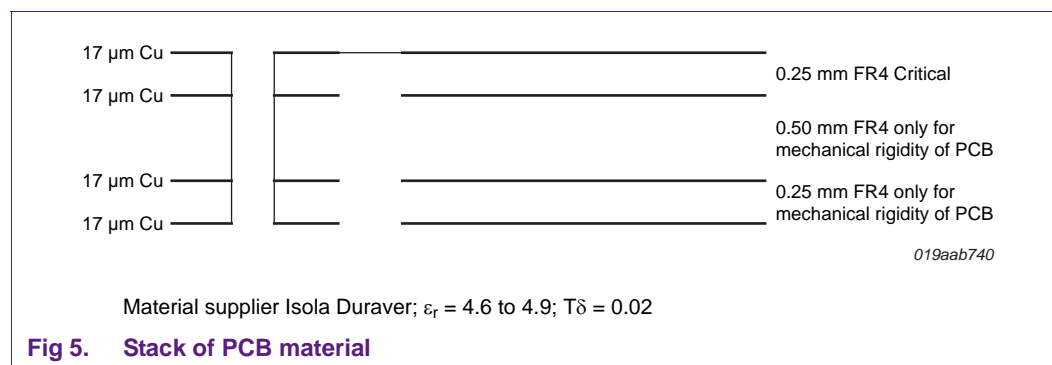
Fig 4. Component layout for the BGU7003 1900 MHz to 2100 MHz LNA evaluation board

### 3.3 PCB layout

A good PCB Layout is an essential part of an RF circuit design. The EVB of the BGU7003 can serve as a guideline for laying out a board using either the BGU7003. Use controlled impedance lines for all high frequency inputs and outputs. Bypass supply voltage  $V_{CC}$  with decoupling capacitors, preferable located as close as possible to the device. For long bias

lines it may be necessary to add decoupling capacitors along the line further away from the device. Proper grounding of the GND pin is also essential for the performance. Either connect the GND pin directly to the ground plane or through vias, or do both.

The EVB is made of FR4 material using the stack shown in [Figure 5](#)



### 3.4 Bill of materials

**Table 1. Bill of materials**

Component	Description	Footprint	Value	Manufacturer	Comment
C1	capacitor	0402	10 pF	Murata GRM1555	input matching
C2, C6	capacitor	0402	100 pF	Murata GRM1555	DC blocking
C3, C4	capacitor	0402	0.1 $\mu$ F	Murata GRM1555	LF decoupling
C5	capacitor	0402	1 pF	Murata GRM1555	output matching
L1	inductor	0402	4.3 nH	Murata/LQW15A; high Q, low Rs	input matching
L2	inductor	0402	18 nH	Murata/LQG15A; high Q, low Rs	DC bias
L3	inductor	0402	4.3 nH	Murata/LQG15A	output matching
R1, R2	resistor	0402	0 $\Omega$	various	backup tune pads
R3	resistor	0402	3.9 k $\Omega$	various	bias setting
R4	resistor	0402	120 $\Omega$	various	stability
X1, X2	SMA RF connector	-	-	Johnson, End Launch SMA 142-0701-841	RF input/ RF output
X3	DC header	-	-	Molex, PCB header, Right angle, 1 row, 3 way, Part no: 90121-0763	bias connector

## 4. Required equipment

In order to measure the evaluation board the following are necessary:

- DC power supply up to 5 mA at 2.5 V (up to 15 V for bias Control)
- RF signal generator capable of generating an RF signal at the 1900 MHz to 2100 MHz operating frequency
- RF spectrum analyzer covering as a minimum the 1900 MHz to 2100 MHz operating frequency and some of the harmonics (up to 6 GHz should be sufficient). Optional: a version with the capability of measuring noise figure is convenient
- Amp meter to measure the supply current (optional)

- NetWork analyzer for measuring gain, return loss and reverse isolation
- Noise figure analyzer.

## 5. Connections and setup

The BFU690, 1900 MHz to 2100 MHz EVB is fully assembled and tested. To operate the EVB and test the device functions follow this step-by-step guide:

1. Connect the DC power supply to the  $V_{CC}$  and GND terminals and set to 2.5 V.
2. Connect the RF signal generator and the spectrum analyzer to the RF input and the RF output of the EVB respectively. Do not yet turn on the RF output of the signal generator. Set it to  $-30$  dBm output power at 2000 MHz and set the spectrum analyzer to 2000 MHz center frequency with a reference level of 0 dBm.
3. Turn on the DC power supply and it should read approximately 5 mA.
4. Enable the RF output of the generator; the spectrum analyzer displays a tone of 2000 MHz at approximately  $-14$  dBm.
5. In order to evaluate the board using different bias currents through RF stage of the MMIC, the voltage on Rb (VRb) can be connected to a separate power supply. This is enabling the control of the bias current.
6. To evaluate the enable function, the Ven terminal of the board can also be connected to a separate DC power supply that either gives a voltage  $>0.6$  V (amplifier on) or  $<0.5$  V amplifier off.
7. A NetWork Analyzer (NWA) can be used instead of a signal generator and spectrum analyzer in order to measure both gain and input and output return losses.
8. For noise figure evaluation use either a noise figure analyzer or a spectrum analyzer with noise option. The use of a 5 dB noise source, such as the Agilent 364A is recommended. When measuring the noise figure of the evaluation board, any kind of adaptors, cables etc, between the noise source and the EVB should be avoided, since this affects the noise performance.

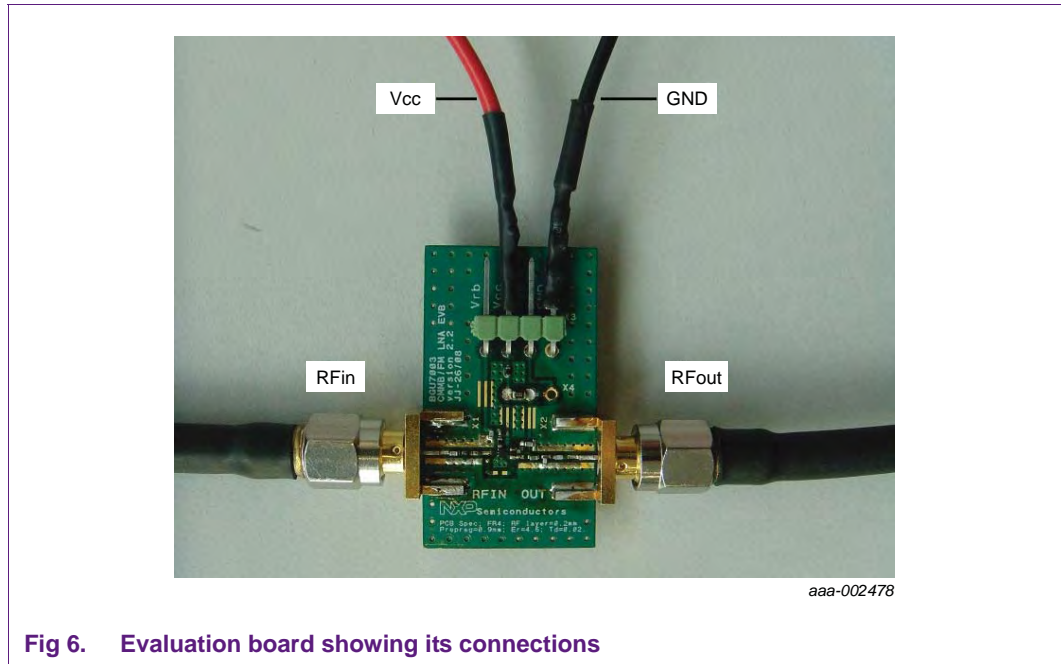


Fig 6. Evaluation board showing its connections

## 6. Typical EVB results

**Table 2. Typical results measured on the evaluation board**  
*T = 25 °C; f = 2.33 GHz unless otherwise specified*

Symbol	Parameter	BGU7003 EVB	Unit
NF	noise figure	1.2 <sup>[1]</sup>	dB
G <sub>p</sub>	power gain	15.3 <sup>[2]</sup>	dB
RL <sub>in</sub>	input return loss	8.0 <sup>[2]</sup>	dB
RL <sub>out</sub>	output return loss	19.5 <sup>[2]</sup>	dB
S <sub>21</sub>   <sup>2</sup>	isolation	23.0 <sup>[2]</sup>	dB
P <sub>i(1dB)</sub>	input power at 1 dB gain compression	-18.1	dBm
P <sub>L(1dB)</sub>	output power at 1 dB gain compression	-3.8	dBm
IP3 <sub>i</sub>	input third-order intercept point	-10.3 <sup>[2][3]</sup>	dBm
IP3 <sub>o</sub>	output third-order intercept point	5.0 <sup>[2][3]</sup>	dBm

[1] The NF and gain figures are measured at the SMA connectors of the EVB, so the connector and PCB losses are not subtracted. If subtracted the NF will improve by approximately 0.1 dB.

[2] Pin = -30 dBm.

[3] 2-Tone test with F1 = 1999.5 MHz, F2 = 2000.5 MHz (spacing 1 MHz). Highest spurious recordings used for calculations.



### 6.1 Noise figure



**Table 3. Noise figure tabular data**  
From Rohde & Schwarz FSU

Frequency list results			
RF (GHz)	NF (dB)	Noise temp (K)	Gain (dB)
1.900	1.192	91.588	16.278
1.920	1.198	92.109	16.212
1.940	1.197	91.992	16.212
1.960	1.214	93.552	16.153
1.980	1.184	90.882	16.021
2.020	1.248	96.557	15.846
2.000	1.182	90.728	15.712
2.040	1.198	92.149	15.650
2.060	1.182	90.738	15.605
2.080	1.234	95.262	15.614
2.100	1.175	90.113	15.534

### 6.2 Stability performance

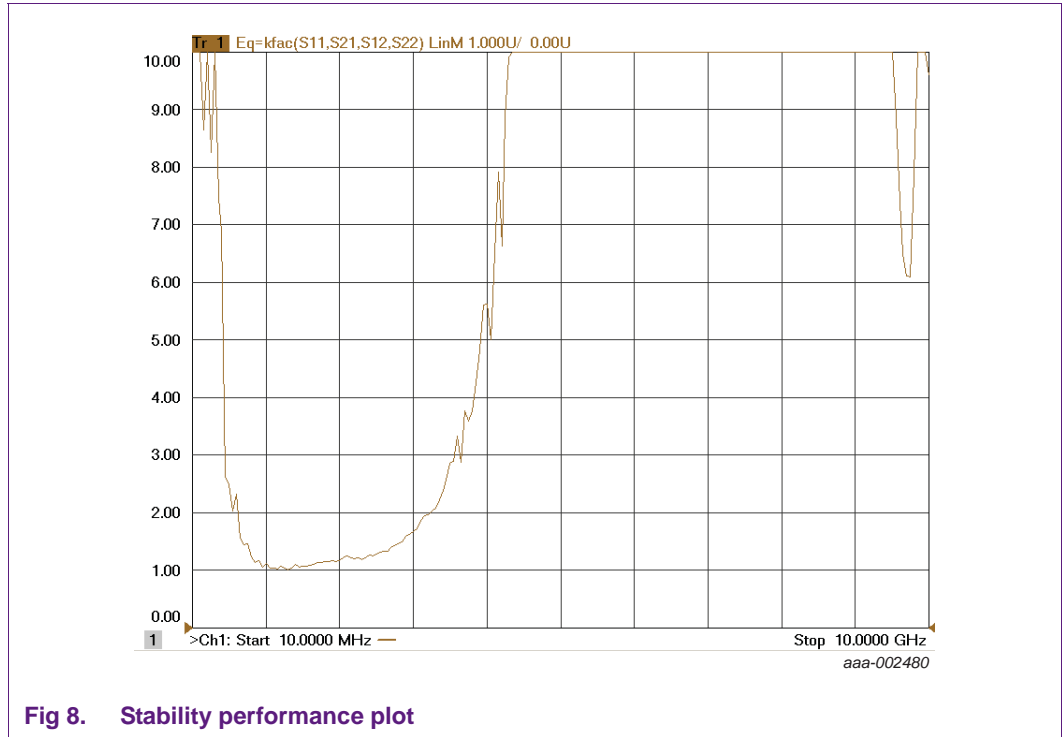
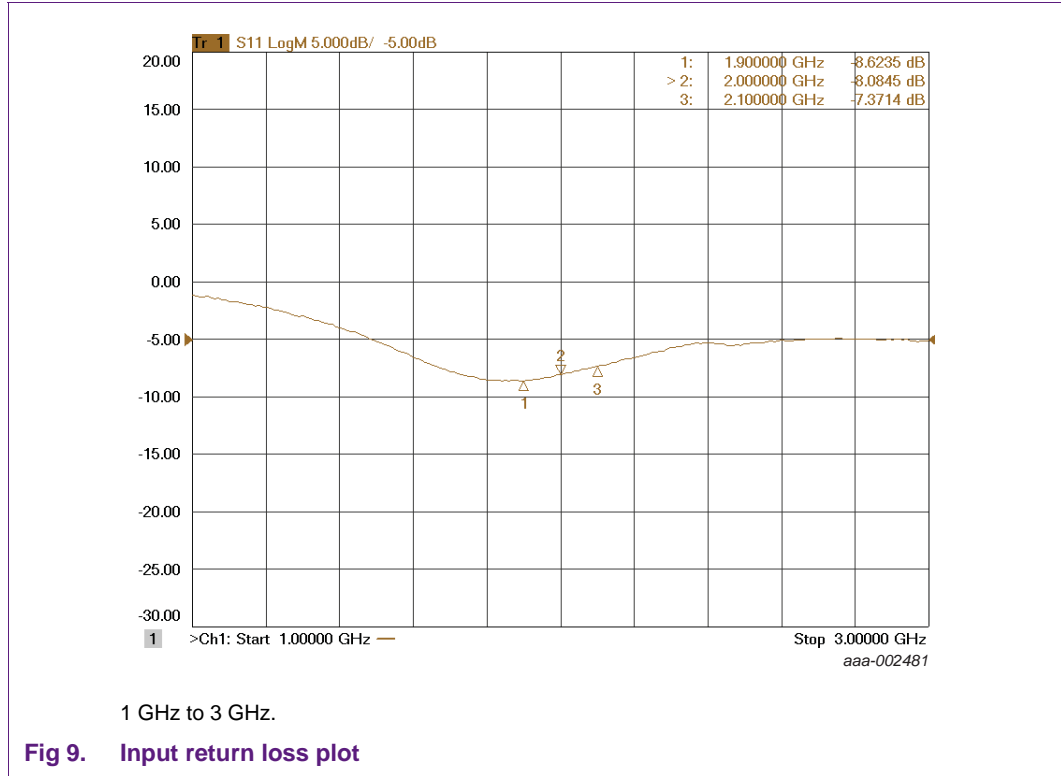


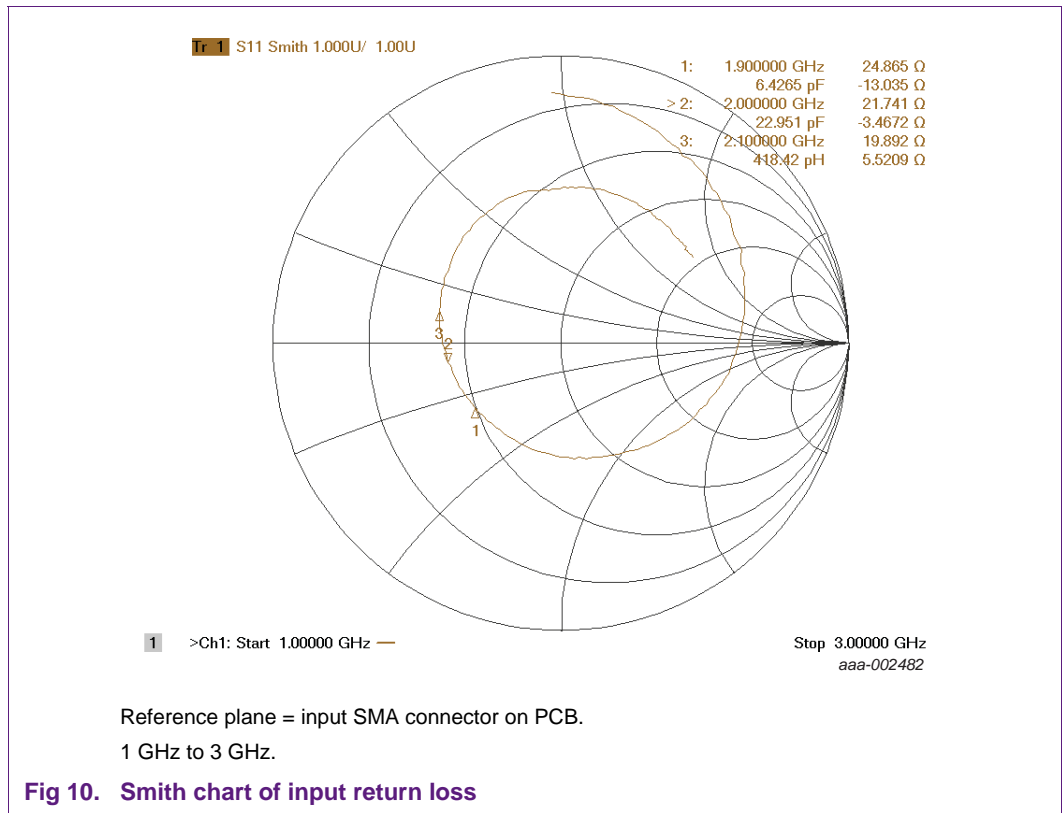
Fig 8. Stability performance plot

### 6.3 Input return losses

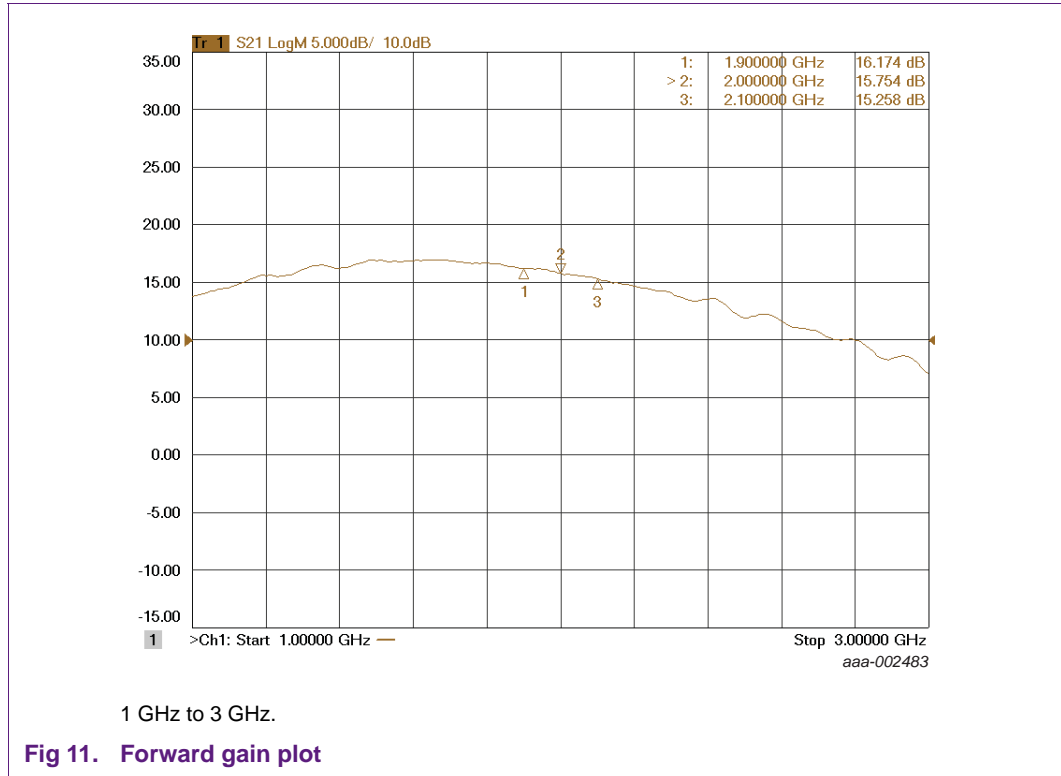
#### 6.3.1 Log Mag



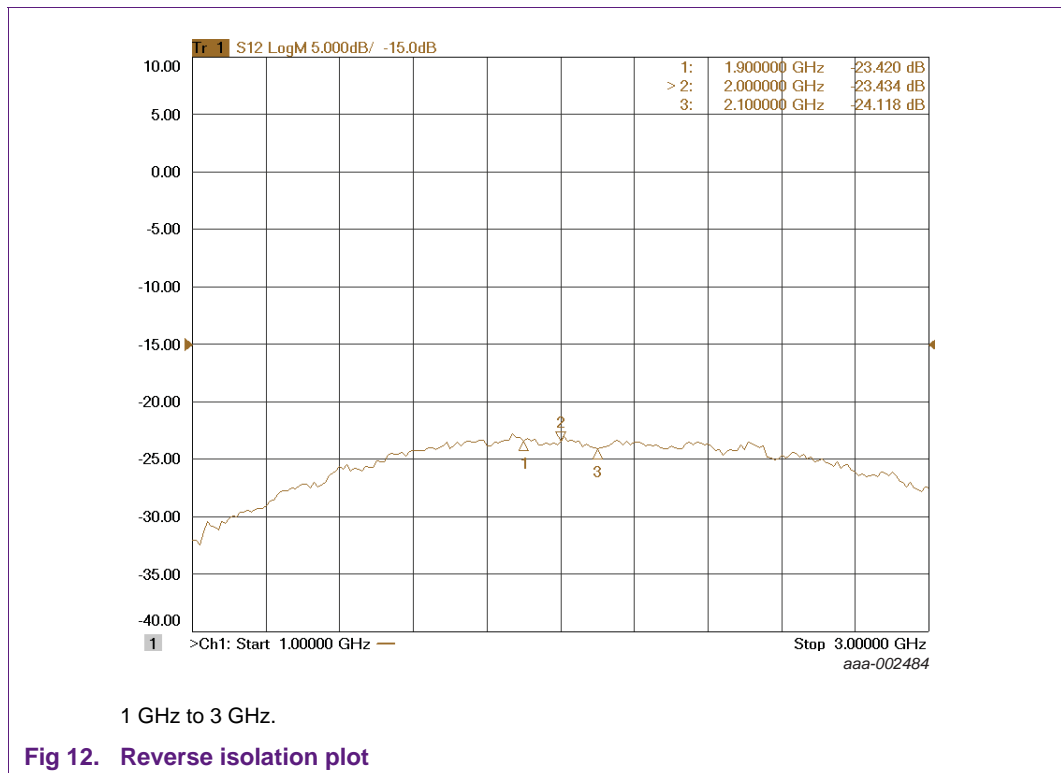
6.3.2 Smith chart



6.4 Forward gain, wide sweep

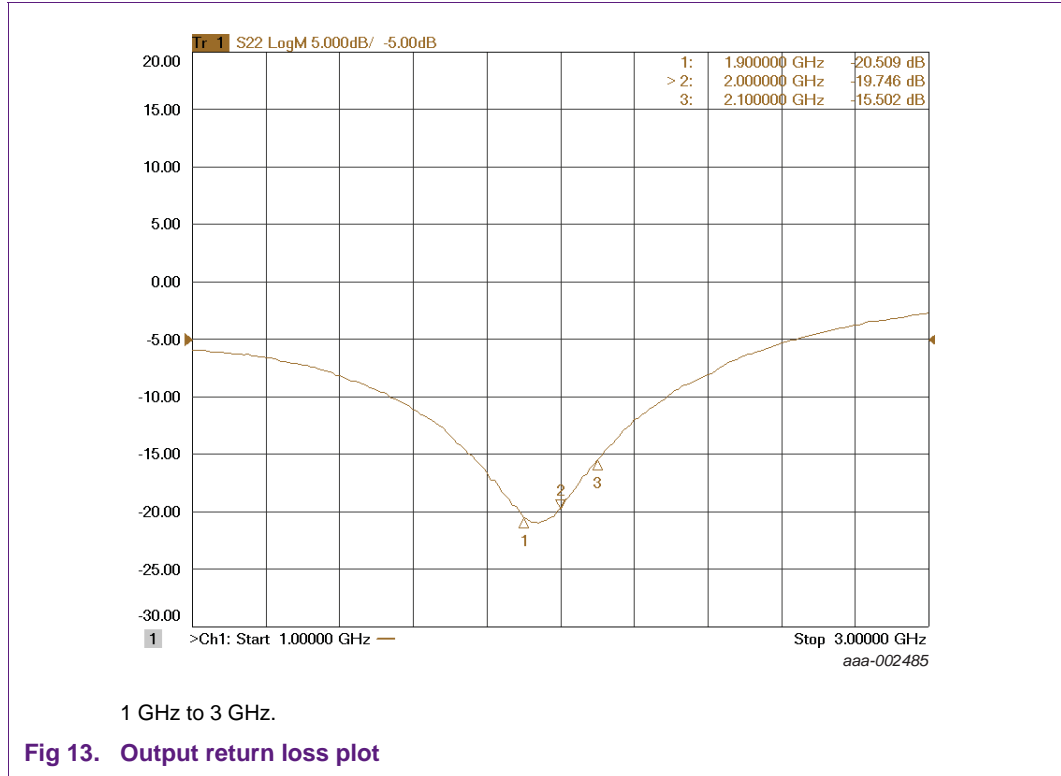


6.5 Reverse isolation

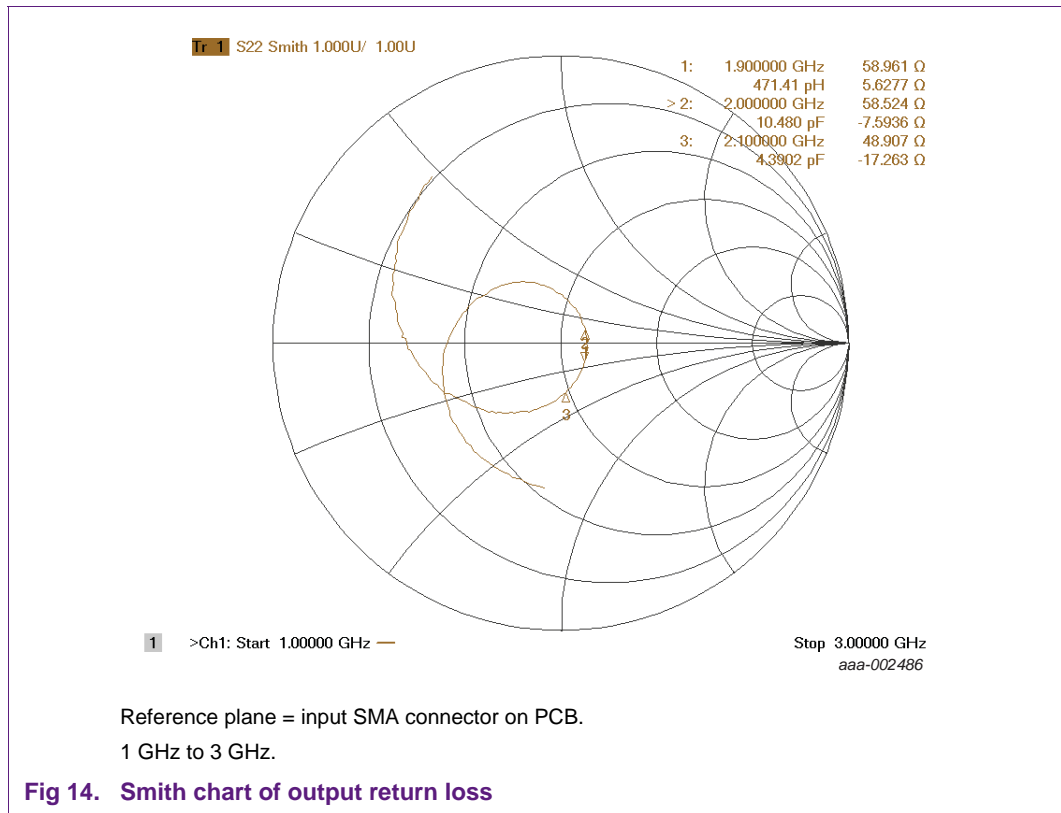


6.6 Output return losses

6.6.1 Log Mag



6.6.2 Smith chart



7. Abbreviations

Table 4. Abbreviations

Acronym	Description
EVB	Evaluation Board
GPS	Global Positioning System
LNA	Low Noise Amplifier
MMIC	Monolithic Microwave Integrated Circuit
NWA	NetWork Analyzer
RF	Radio Frequency

## 8. Legal information

### 8.1 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

### 8.2 Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product

design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

**Evaluation products** — This product is provided on an "as is" and "with all faults" basis for evaluation purposes only. NXP Semiconductors, its affiliates and their suppliers expressly disclaim all warranties, whether express, implied or statutory, including but not limited to the implied warranties of non-infringement, merchantability and fitness for a particular purpose. The entire risk as to the quality, or arising out of the use or performance, of this product remains with customer.

In no event shall NXP Semiconductors, its affiliates or their suppliers be liable to customer for any special, indirect, consequential, punitive or incidental damages (including without limitation damages for loss of business, business interruption, loss of use, loss of data or information, and the like) arising out of the use of or inability to use the product, whether or not based on tort (including negligence), strict liability, breach of contract, breach of warranty or any other theory, even if advised of the possibility of such damages.

Notwithstanding any damages that customer might incur for any reason whatsoever (including without limitation, all damages referenced above and all direct or general damages), the entire liability of NXP Semiconductors, its affiliates and their suppliers and customer's exclusive remedy for all of the foregoing shall be limited to actual damages incurred by customer based on reasonable reliance up to the greater of the amount actually paid by customer for the product or five dollars (US\$5.00). The foregoing limitations, exclusions and disclaimers shall apply to the maximum extent permitted by applicable law, even if any remedy fails of its essential purpose.

**Translations** — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

### 8.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.



## 9. Contents

<b>1</b>	<b>Introduction</b>	<b>3</b>
<b>2</b>	<b>General description</b>	<b>3</b>
<b>3</b>	<b>Application board</b>	<b>4</b>
3.1	Application circuit	4
3.2	Board layout	5
3.3	PCB layout	5
3.4	Bill of materials	6
<b>4</b>	<b>Required equipment</b>	<b>6</b>
<b>5</b>	<b>Connections and setup</b>	<b>7</b>
<b>6</b>	<b>Typical EVB results</b>	<b>8</b>
6.1	Noise figure	9
6.2	Stability performance	10
6.3	Input return losses	11
6.3.1	Log Mag	11
6.3.2	Smith chart	12
6.4	Forward gain, wide sweep	13
6.5	Reverse isolation	13
6.6	Output return losses	14
6.6.1	Log Mag	14
6.6.2	Smith chart	15
<b>7</b>	<b>Abbreviations</b>	<b>15</b>
<b>8</b>	<b>Legal information</b>	<b>16</b>
8.1	Definitions	16
8.2	Disclaimers	16
8.3	Trademarks	16
<b>9</b>	<b>Contents</b>	<b>17</b>

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2012.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: 1 March 2012

Document identifier: AN11148