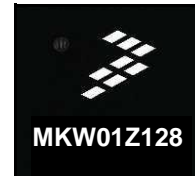


# MKW01Z128



Package Information

Ordering Information

Device	Device Marking	Package
MKW01Z128CHN	MKW01Z128CHN	LGA-60

# MKW01Z128

Highly-integrated, cost-effective single-package solution for sub-1 GHz applications

## 1 Introduction

The MKW01Z device is highly-integrated, cost-effective, smart radio, sub-1 GHz wireless node solution composed of a transceiver supporting FSK, GFSK, MSK, or OOK modulations with a low-power ARM® Cortex M0+ CPU. The highly integrated RF transceiver operates over a wide frequency range including 315 MHz, 433 MHz, 470 MHz, 868 MHz, 915 MHz, 928 MHz, and 955 MHz in the license-free Industrial, Scientific and Medical (ISM) frequency bands. This configuration allows users to minimize the use of external components.

The MKW01Z128 is targeted for the following low-power wireless applications:

- Automated Meter Reading
- Wireless Sensor Networks
- Home and Building Automation
- Wireless Alarm and Security Systems
- Industrial Monitoring and Control

Freescale supplements the MKW01Z128 with tools and software that include hardware evaluation and

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development boards, software development IDE and applications, drivers, custom PHY usable with Freescale's IEEE 802.15.4 compatible MAC and SMAC.

## 2 Features

This section provides a simplified block diagram and highlights MKW01Z128 features.

### 2.1 Block Diagram

Figure 1 shows a simplified block diagram of the MKW01Z128.

MKW01 Block Diagram

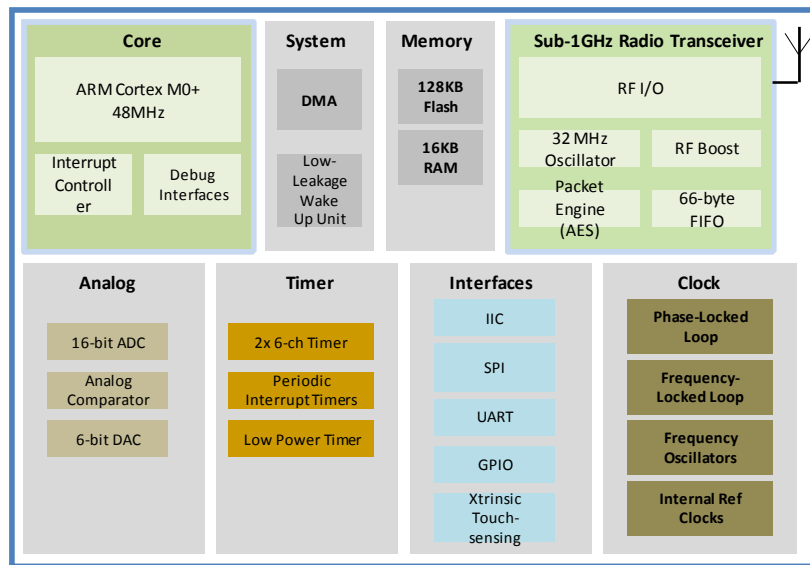


Figure 1. MKW01Z128 Simplified Block Diagram

### 2.2 Features Summary

- **RF Transceiver Features**
  - Operating Voltage from 1.8V to 3.6V.
  - Programmable bit rate up to 600kbps (FSK)
  - High Sensitivity: down to -120 dBm at 1.2 kbps
  - High Selectivity: 16-tap FIR Channel Filter
  - Bullet-proof front end: IIP3 = -18 dBm, IIP2 = +35 dBm, 80 dB Blocking Immunity, no Image Frequency response
  - Low current: Rx = 16mA, 100nA register retention

- Programmable Pout : -18 to +17 dBm in 1 dB steps
- Constant RF performance over voltage range of chip
- Fully integrated synthesizer with a resolution of 61 Hz
- FSK, GFSK, MSK, GMSK and OOK modulations
- Built-in Bit Synchronizer performing Clock recovery
- Incoming Sync Word Recognition
- Automatic RF Sense with ultra-fast AFC
- Packet engine with CRC, AES-128 encryption and 66-byte FIFO
- Built-in temperature sensor and Low battery indicator
- 32 MHz crystal oscillator clock source
- Dedicated I/O's for connection with an external 32 kHz crystal

- **MCU Features**

**System:**

- 48 MHz Max. Central Processor Unit (CPU) frequency
- 24 MHz Max. Bus frequency
- Vectored Interrupt Controller (NVIC) with 36 vectored interrupts with 4 programmable interrupt priority levels
- Wake-up Interrupt Controller (WIC)
- 4 channel Direct Memory Access (DMA)
- DMA request multiplex
- Non Maskable Interrupt (NMI)
- Software COP
- Low leakage Wake-up Unit (LLWU)
- Debug and Trace
  - 2-pin Serial Wire Debug (SWD)
  - Basic Branch Buffering (BBB)
- Boundary scan
- 80-bit wide ID number

**Memory:**

- 128 KB P-Flash with 64 byte flash cache
- 16 KB RAM
- Low Leakage Standby Memory:
  - 8KB in VLLS2 mode
  - 32 Register File Bytes in VLLS1 mode
  - Register File and PMC lose control and others in TBD in VLLS0
- 16-bit or 32-bit Cyclic Redundancy Check (CRC) with programmable generator polynomial

#### Clocks:

- External crystal oscillator or resonator:
  - 32 - 40 kHz low range, low power or full swing
  - 3 MHz - 32 MHz high range, low power or full swing
- DC - 48 MHz external square wave input clock
- Internal clock references:
  - 31.25 kHz to 39.063 kHz oscillator with +/- 2% max. deviation across temperature
  - 4 MHz oscillator with +/- 5% max. deviation across temperature
  - 1 kHz oscillator
- Phase Locked Loop (PLL) with up to 100 MHz VCO
- Frequency Locked Loop (FLL):
  - Range 1: 20 - 25 MHz
  - Range 2: 40 - 48 MHz

#### Analog:

- Power Management Controller (PMC) with low voltage warning (LVW) and detect with selectable trip points.
- 16-bit analog to digital converter
  - 16 single ended channels
  - 2 status, control and results registers
  - DMA support
- 1 High Speed Comparator (HSCMP) with internal 6-bit digital to analog converters (DAC)
- One 12-bit DAC with DMA support and 2 x 16 bit data buffer

#### Timers:

- Six channel Timer/PWM (TPM)
- Two 2-channel Timer/PWM (TPM)
- Periodic interrupt timers
- 16-bit low-power timer (LPTMR)
- Real-time clock 2 channel 32-bit Programmable Input Timer (PIT)
- 24-bit counter System Tick Timer (SYSTICK)
- Independent Real Time Clock (SRTC) supporting an auxiliary supply, 32 kHz external oscillator and 32 Byte register file
- Low Power Timer (LPTMR) supporting 1 channel 16-bit pulse counter or periodic interrupt functional in any low-power mode

#### Communication Interface:

- Two Serial Peripheral Interfaces (SPIs)

- Two Inter-Integrated Circuits (IICs) with DMA support
- One Universal Asynchronous Receiver / Transmitter 0 (UART0) / (LPSCIO) that supports standard features plus:
  - Tx pin true open drain with enable / disable programmable
  - x4, x8, x16 oversampling
  - Functional in STOP / VLPS modes
  - DMA support
  - UART0 is clocked by the bus clock
- UART1 (SCI) that supports standard features with DMA support
  - UART1 is clocked by the core clock

#### Human Machine Interface (HMI)

- General Purpose Input/Output (GPIO) supporting:
  - 5 V Tolerant I/O
  - Default to disabled (no leakage)
  - 4 pins with 18 mA high current drive capability
  - Hysteresis and configurable pull up device on all input pins
  - Slew rate and drive strength fixed on all output pins
  - Single cycle GPIO control via IOPORT
- Touch Sensor Inputs (TSI)
  - 9-channel
  - Selectable single channel wakeup source available in all modes
  - DMA support
- Pin Interrupt

1.8 V to 3.6 V operating voltage with on-chip voltage regulators

Temperature range of  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$

60-pin LGA (8x8 mm) package

## 3 Software Solutions

Freescale will support the MKW01x128 platform with several software solutions:

- A radio utility GUI will be available that allows testing of various features and setting registers. A connectivity test firmware will allow a limited set of testing controlled with a terminal emulator on any computer.
- SMAC (Simple Media Access Controller) — This codebase provides simple communication and test apps based on drivers/PHY utilities available as source code. This environment is useful for hardware and RF debug, hardware standards certification, and developing proprietary applications.
- Additional software will be available through 3rd party providers.

## 4 Smart Radio Sub-1 GHz Wireless Node

The MKW01Z128 brings together a transceiver chip and an MCU chip on a single substrate to provide a small footprint, cost-effective sub-1 GHz wireless node. The transceiver is controlled by the MCU through a dedicated SPI interface. The SPI bus interface and some status signals are connected onboard the substrate to eliminate the need for external connections. The SPI supports bit order swapping providing hardware support for bit endianness reducing processing overhead.

### 4.1 RF Transceiver

The transceiver (see Figure 2) is a single-chip integrated circuit ideally suited for today's high performance ISM band RF applications. Its advanced features set, including state of the art packet engine, greatly simplifies system design while the high level of integration reduces the external RF component bill of material (BOM) to a handful of passive de-coupling and matching components. It is intended for use as a high-performance, low-cost FSK, GFSK, MSK, GMSK, and OOK RF transceiver for robust, frequency agile, half-duplex bi-directional RF links.

The MKW01Z128 is intended for applications over a wide frequency range, including the 433 MHz, the 868 MHz European, and the 902-928 MHz North American ISM bands. Coupled with a link budget in excess of 135 dB, the transceiver advanced system features include a 66 byte TX/RX FIFO, configurable automatic packet handler, listen mode, temperature sensor and configurable DIO's which greatly enhance system flexibility while at the same time significantly reducing MCU requirements. The transceiver complies with both ETSI and FCC regulatory requirements.

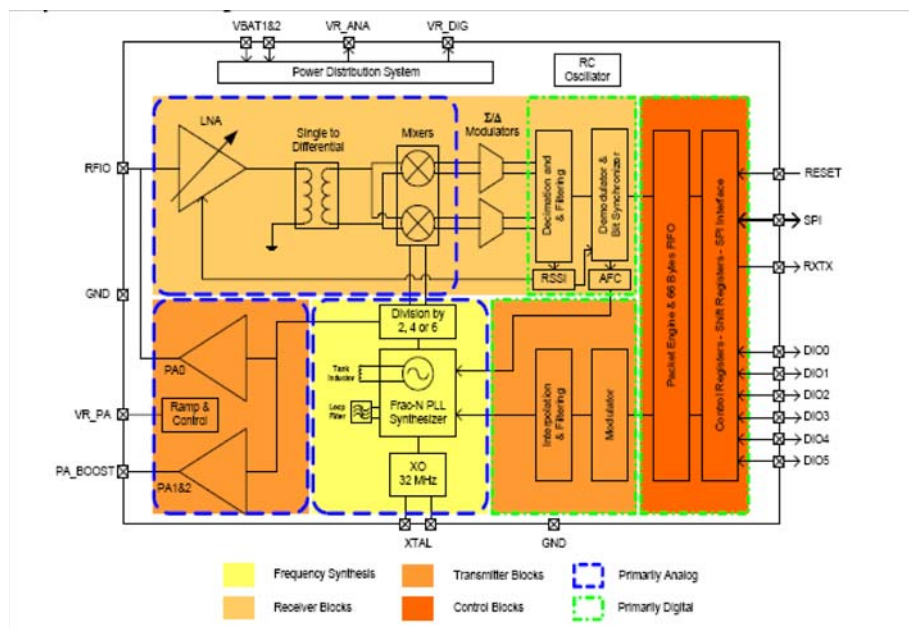


Figure 2. MKW01Z128 Transceiver Block Diagram

The major RF communication parameters of the MKW01Z128 transceiver are programmable and most can be dynamically set. This feature offers the unique advantage of programmable narrow-band and

wide-band communication modes without the need to modify external components. The transceiver is also optimized for low power consumption while offering high RF output power and channelized operation.

## 4.2 ARM® 32-bit Cortex M0+ CPU

The onboard MCU integrated circuit features an ARM® Cortex M0+ CPU, up to 16 KB RAM, 128 KB Flash memory, and a rich set of peripherals (see [Section 2.2, “Features Summary”](#)). The RF transceiver is controlled through the MCU SPI port which is dedicated to the RF device interface. Two of the transceiver status IO lines are also directly connected to the MCU GPIO to monitor the transceiver operation. In addition, the transceiver reset and additional status can be connected to the MCU through external connections.

Operational modes of the MKW01Z128 are determined by the software running on the MCU. The MCU itself has a run mode as well as an array of low power modes that are coordinated by the PMC. The MCU in turn set the operational modes of the transceiver which include sleep, standby, and radio operational modes.

Two common application scenarios are:

- Low power, battery-operated standalone wireless node - a common example of this configuration would be a remote sensor monitor. The wireless node programmed for standalone operation, typically has a low active-mode duty cycle, and is designed for long battery life, i.e., lowest power.
- Communication channel to a higher level controller - in this example, the wireless node implements the lower levels of a communications stack and is subordinate to the primary controller. Typically the MKW01Z128 is connected to the controller through a command channel implemented via a UART/SCI port or other serial communication port.

## 4.3 System Clock Configuration

The MKW01Z128 device allows for various system clock configurations:

- Pins 46 & 47 are provided to input a 32 or 30 MHz crystal for the transceiver reference clock source (required) as shown in [Figure 3](#).
- The transceiver can be programmed to provide a programmable frequency clock output (ClkOut Pin #54) that can be used as an external source to the CPU (see [Figure 3](#) and [Figure 4](#)). As a result, a single crystal system clock solution is possible where the transceiver reference clock source can be divided by 2, 4, 8, 16 and 32.
- The MCU provides a trimmable internal reference clock and also supports an external clock source. An optional onboard frequency locked loop (FLL) can be used with either clock source to support a CPU clock as high as 48 MHz at 3.6 V.
- Pins 16 and 15 are available to provide an external 32.768 kHz external clock source for the MCU.

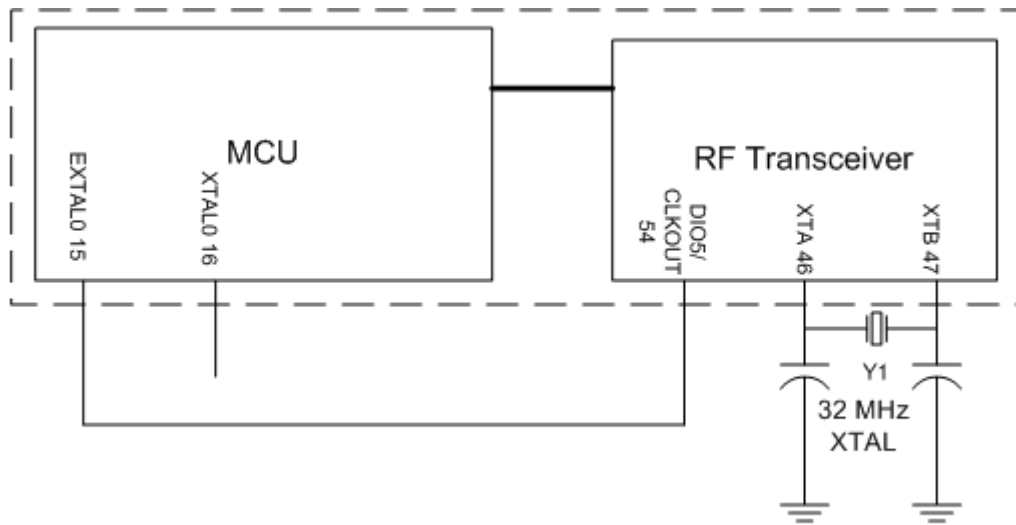


Figure 3. MKW01Z128 Single Crystal System Clock Connection

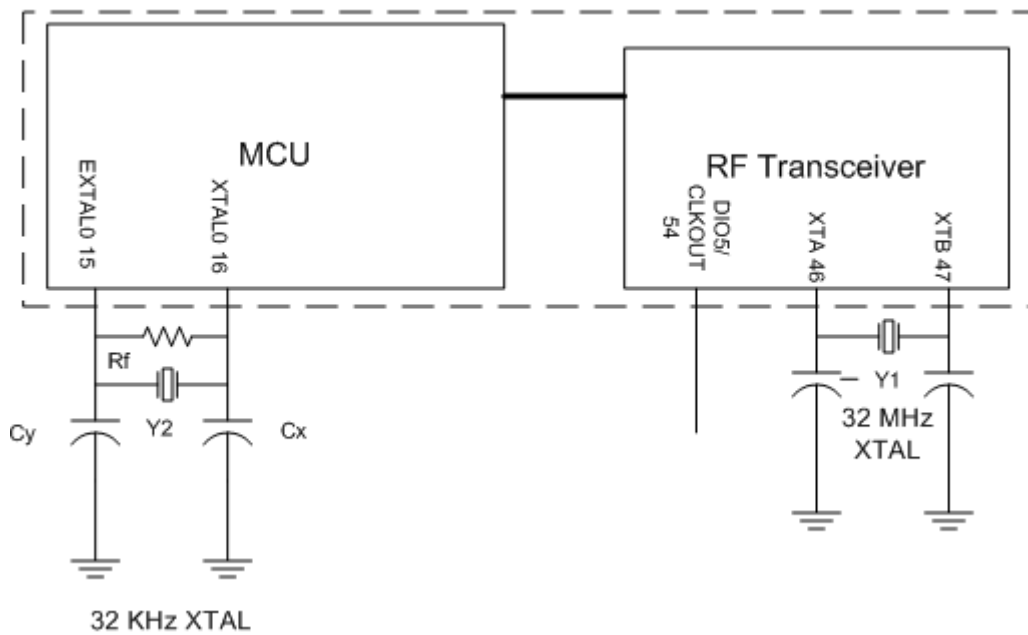


Figure 4. MKW01Z128 Two Crystal System Clock Connection



# 5 MKW01Z128 Pin Assignments and Connections

Figure 5 shows the MKW01Z128 pinout.

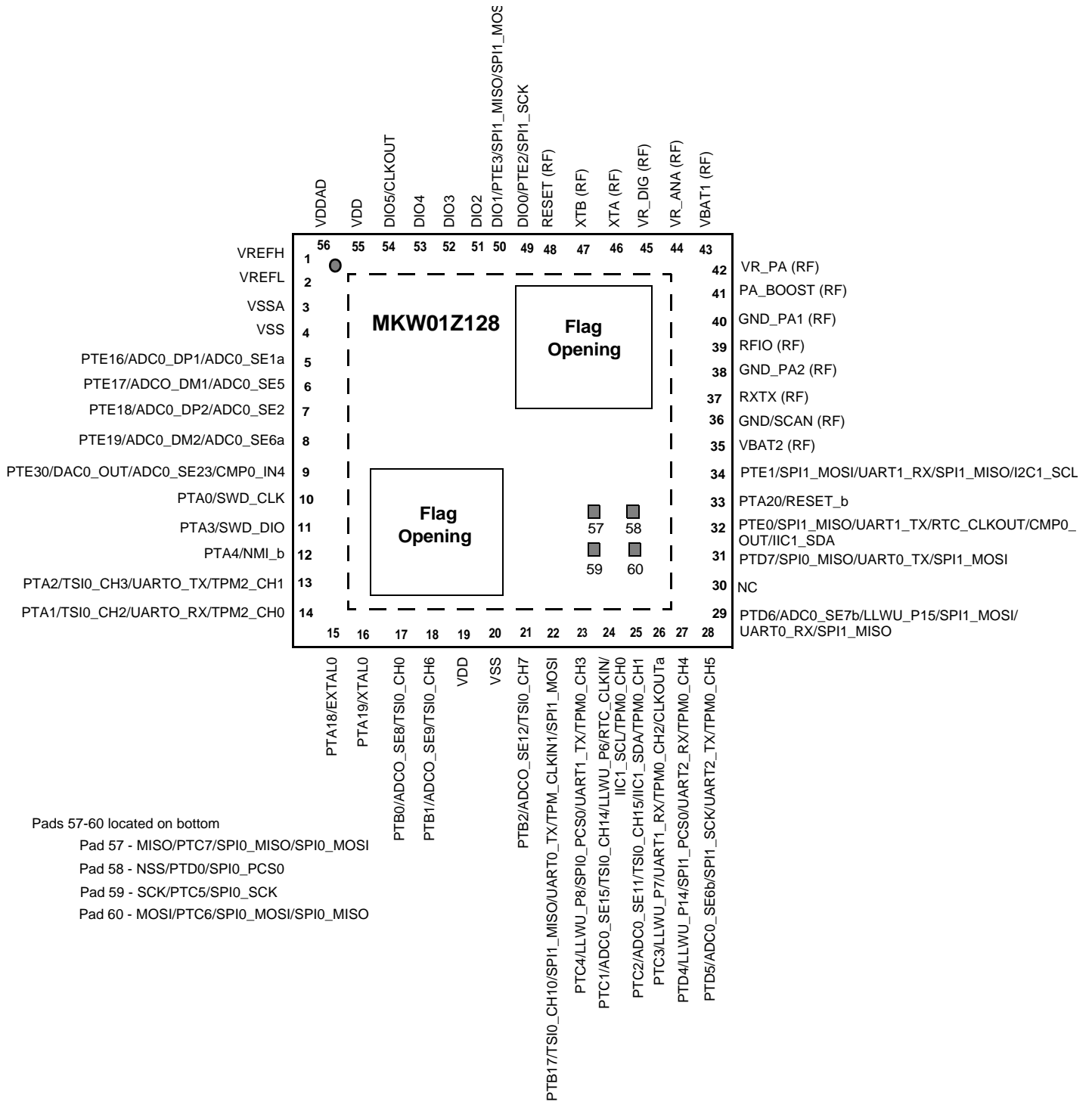


Figure 5. MKW01Z128 Pinout (Top View)

## 5.1 Pin Definitions

Table 1 details the MKW01Z128 pinout and functionality.

**Table 1. Pin Function Description (Sheet 1 of 5)**

Pin #	Pin Name <sup>1</sup>	Type	Description	Functionality
1	VREFH	Input	MCU high reference voltage for ADC	
2	VREFL	Input	MCU low reference voltage for ADC	
3	VSSA	Power Input	MCU ADC Ground	Connect to ground
4	VSS	Power Input	MCU Ground	Connect to ground
5	PTE16/ADC0_DP1/ADC0_SE1/SPI0_PCS0/TPM/UART2_TX	Digital Input / Output	MCU Port E Bit 16 / ADC0 Single Ended analog channel input DP1/ ADC0 Single Ended analog channel input SE1 / SPI module 0 PCS0 / TPM module Clock In 0 / UART2_TX	
6	PTE17/ADC0_DM1/ADC0_SE5a/SPI0_SCK/TPM_CLKIN1/UART2_RX/LPTMR0_ALT3	Digital Input / Output	MCU Port E Bit 17 / ADC0 Single Ended analog channel input DM1/ ADC0 Single Ended analog channel input 5a / SPI module 0 SCK / TPM module Clock In 1 / UART2_RX / Low Power Timer Module 0 ALT3	
7	PTE18/ADC0_DP2/ADC0_SE2/SPI0_MOSI/IIC0_SDA/SPI0_MISO	Digital Input / Output	MCU Port E Bit 18 / ADC0 Single Ended analog channel input DP2/ ADC0 Single Ended analog channel input 2 / SPI module 0 MOSI / IIC0 Bus Data / SPI module 0 MISO	
8	PTE19/ADC0_DM2/ADC0_SE6a/SPI0_MISO/IIC0_SCL/ SPI0_MOSI	Digital Input / Output	MCU Port E Bit 19 / ADC0 Single Ended analog channel input DM2/ ADC0 Single Ended analog channel input 6a / SPI module 0 MISO / IIC0 Bus Clock / SPI module 0 MOSI	
9	PTE30/DAC0_OUT/ADC0_SE23/CMP0_IN4/TPM0_CH3/TPM_CLKIN1	Digit-I Input / Output	MCU Port E Bit 30 / DAC0 Output/ ADC0 Single Ended analog channel input 23 / Comparator 0 Analog Voltage Input 4/ TPM Timer module 0 Channel 3 / TPM module Clock In 1	
10	PTA0/SWD_CLK/TSI0_CH1/TPM0_CH5	Digital Input / Output	MCU Port A Bit 0 / Serial Wire Data Clock / Touch Screen Interface Channel 1/ TPM module 0 Channel 5	
11	PTA3/SWD_DIO/TSI0_CH4/IIC1_SCL/TPM0_CH0	Digital Input / Output	MCU Port A Bit 3 / Serial Wire Data DIO / Touch Screen Interface Channel 4 / IIC1 Bus Clock / TPM module 0 Channel 0	
12	PTA4/NMI_b/TSI0_CH5/IIC1_SDA/TPM0_CH1	Digital Input / Output	MCU Port A Bit 4 / Non Maskable Interrupt_b/Touch Screen Interface Channel 5 / IIC1 Bus Data / TPM module 0 Channel 1	

**Table 1. Pin Function Description (Sheet 2 of 5)**

Pin #	Pin Name <sup>1</sup>	Type	Description	Functionality
13	PTA2/TSI0_CH3/UART0_TX/TPM2_CH1	Digital Input / Output	MCU Port A Bit 2/Touch Screen Interface Channel 3/UART module 0 Transmit / TPM module 2 Channel 1	
14	PTA1/TSI0_CH2/UART0_RX/TPM2_CH0	Digital Input / Output	MCU Port A Bit 1/Touch Screen Interface Channel 2/UART module 0 Receive / TPM module Channel 0	
15	PTA18/EXTAL0/UART1_RX/TPM_CLKIN0	Digital Input / Output	MCU Port A Bit 18 / EXTAL0/ UART module 1 Receive / TPM module Clock In 0	
16	PTA19/XTAL0/UART1_TX/TPM_CLKIN1/LPTMR0_ALT1	Digital Input / Output	MCU Port A Bit 19 / XTAL0/ UART module 1 Transmit / TPM module Clock In 1 /Low Power Timer module 0 ALT1	
17	PTB0/ADC0_SE8/TSI0_CH0/LLWU_P5/IIC0_SCL/TPM1_CH0	Digital Input / Output	MCU Port B Bit 0 / ADC0 Single Ended analog channel input SE8 / Touch Screen Interface Channel 0/ Low Leakage Wake Up Port 5 / IIC0 Bus Clock / TPM module 1 Channel 0	
18	PTB1/ADC0_SE9/TSI0_CH6/IIC0_SDA/TPM1_CH1	Digital Input / Output	MCU Port B Bit 1 / ADC0 Single Ended analog channel input SE9 / Touch Screen Interface Channel 6 / IIC0 Bus Data / TPM module 1 Channel 1	
19	VDD	Power Input	MCU VDD supply input	Connect to system VDD supply
20	VSS	Power Input	MCU Ground	Connect to ground
21	PTB2/ADC0_SE12/TSI0_CH7/IIC0_SCL/TPM2_CH0	Digital Input/Output	MCU Port B Bit 2 / ADC0 Single Ended analog channel input SE12 / Touch Screen Interface Channel 7 / IIC0 Bus Clock / TPM Timer module 2 Channel 0	
22	PTB17/TSI0_CH10/SPI1_MISO/UART0_TX/TPM_CLKIN1/SPI1_MOSI	Digital Input/Output	MCU Port B Bit 17 / Touch Screen Interface Channel 10/SPI1 MOSI or MISO/UART0 TX / TPM timer clock	
23	PTC4/LLWU_P8/SPI0_PCS0/UART1_TX/TPM0_CH3	Digital Input / Output	MCU Port C bit 4 / Low leakage Wake Up port 8 / SPI0 Chip Select / UART1 TX / TPM Timer module 0 channel 3	
24	PTC1/ADC0_SE15/TSI0_CH14/LLWU_P6/RTC_CLKIN/IIC1_SCL/TPM0_CH0	Digital Input / Output / Analog Input	MCU Port C Bit 1 /ADC0 Single Ended analog channel input SE15/ Touch Screen Interface Channel 14/ Low Leakage Wake Up Port 6 / Real Time Counter Clock Input/ IIC1 Bus Clock/ TPM module 0 Channel 0	
25	PTC2/ADC0_SE11/TSI0_CH15/IIC1_SDA/TPM0_CH1	Digital Input / Output / Analog Input	MCU Port C Bit 2 / ADC0 Single Ended analog channel input SE11// Touch Screen Interface Channel 15 / IIC1 Bus Data / TPM module 0 Channel 1	

**Table 1. Pin Function Description (Sheet 3 of 5)**

Pin #	Pin Name <sup>1</sup>	Type	Description	Functionality
26	PTC3/LLWU_P7/UART1_RX/TPM0_CH2/CLKOUTa	Digital Input / Output	MCU Port C Bit 3 / Low Leakage Wake Up Port 7 / UART module 1 Receive / TPM module 0 Channel 2/ Clock OutA	
27	PTD4/LLWU_P14/SPI1_PCS0 /UART2_RX/TPM0_CH4	Digital Input / Output	MCU Port D Bit 4 / Low Leak Wake Up Port 14/ SPI module 1 PCS0 / UART2 Receiver input / TPM module 0 Channel 4	
28	PTD5/ADC0_SE6b/SPI1_SCK/UART2_TX/TPM0_CH5	Digital Input / Output / Analog Input	MCU Port D bit 5 / ADC0 Single Ended analog channel input SE6b / SPI1 clock / UART2 TX / TPM module 0 Channel 5	
29	PTD6/ADC0_SE7b/LLWU_P15/SPI1_MOSI/UART0_RX/SPI1_MISO	Digital Input / Output / Analog Input	MCU Port D bit 6 / ADC0 Single Ended analog channel input SE7b / Low leakage Wake Up port 15 / SPI1 MOSI / UART0 RX / SPI module 1 MISO	
30	NC		No Connect	
31	PTD7/SPI0_MISO/UART0_TX/SPI1_MOSI	Digital Input/Output	MCU Port D Bit 7 / SPI module 0 MISO / UART module 0 Transmit / SPI module 1 MOSI	
32	PTE0/SPI1_MISO/UART1_TX /RTC_CLKOUT/CMP0_OUT/ IIC1_SDA	Digital Input/Output	MCU Port E Bit 0 / SPI module 1 MISO / UART module 1 Transmit / Real Time Counter Clock Output / Comparator 0 Analog voltage Output / IIC1 Bus Data	
33	PTA20/RESETB	Digital Input/Output	MCU Port A Bit 20/MCU $\overline{\text{RESET}}$	
34	PTE1 / SPI1_MOSI / UART1_RX /SPI1_MISO / IIC1_SCL	Digital Input/Output	MCU Port E Bit 1 / SPI module 1 MOSI / UART module 1 RX / SPI1_MISO / IIC1_SCL	
35	VBAT2 (RF)	Power Input	Transceiver VDD	Connect to system VDD supply
36	GND/SCAN (RF)	Power Input	Transceiver Ground	Connect to ground
37	RXTX (RF)	Digital Output	Transceiver Rx / Tx RF Switch Control Output; high when in TX	
38	GND_PA2 (RF)	Power Input	Transceiver RF Ground	Connect to ground
39	RFIO (RF)	RF Input / Output	Transceiver RF Input / Output	
40	GND_PA1 (RF)	Power Input	Transceiver RF Ground	Connect to ground
41	PA_BOOST (RF)	RF Output	Transceiver Optional High-Power PA Output	
42	VR_PA (RF)	Power Output	Transceiver regulated output voltage for VR_PA use.	De-coupling cap suggested.
43	VBAT1 (RF)	Power Input	Transceiver VDD for RF circuitry	Connect to system VDD supply

**Table 1. Pin Function Description (Sheet 4 of 5)**

Pin #	Pin Name <sup>1</sup>	Type	Description	Functionality
44	VR_ANA (RF)	Power Output	Transceiver regulated output voltage for analog circuitry.	Decouple to ground with 100 nF capacitor
45	VR_DIG (RF)	Power Output	Transceiver regulated output voltage for digital circuitry.	Decouple to ground with 100 nF capacitor
46	XTA (RF)	Xtal Osc	Transceiver crystal reference oscillator	Connect to 32 MHz crystal and load capacitor
47	XTB (RF)	Xtal Osc	Transceiver crystal reference oscillator	Connect to 32 MHz crystal and load capacitor
48	RESET (RF)	Digital Input	Transceiver hardware reset input	Typically driven from MCU GPIO
49	DIO0/PTE2/SPI1_SCK	Digital Input/Output	Internally connected to Transceiver GPIO bit 0 and MCU Port E bit 2 / SPI1 clock	MCU IO and Transceiver IO connected onboard
50	DIO1/PTE3/SPI1_MISO/SPI1_MOSI	Digital Input/Output	Internally connected to Transceiver GPIO bit 1 and MCU Port E bit 3 / SPI1 in or out	MCU IO and Transceiver IO connected onboard
51	DIO2	Digital Input/Output	Transceiver GPIO Bit 2	
52	DIO3	Digital Input/Output	Transceiver GPIO Bit 3	
53	DIO4	Digital Input/Output	Transceiver GPIO Bit 4	
54	DIO5/CLKOUT	Digital Input/Output	Transceiver GPIO Bit 5 / ClkOut	Commonly programmed as ClkOut to supply MCU clock; connect to Pin 5
55	VDD	Power Input	MCU VDD supply	Connect to VDD supply
56	VDDAD	Power Input	MCU Analog supply	Connect to Analog supply
57	MISO/PTC7/SPI0_MISO/SPI0_MOSI	Digital Input/Output	Internal SPI data connection from Transceiver MISO bit 1 to MCU SPI0 (Port C bit 7 )	<ul style="list-style-type: none"> <li>MCU IO and Transceiver IO connected onboard</li> <li>MCU IO must be configured for this connection</li> </ul>
58	NSS/PTD0/SPI0_PCS0	Digital Input/Output	Internal SPI select connection between Transceiver NSS and MCU SPI0 (Port D bit 0)	<ul style="list-style-type: none"> <li>MCU IO and Transceiver IO connected onboard</li> <li>MCU IO must be configured for this connection</li> </ul>
59	SCK/PTC5/SPI0_SCK	Digital Input/Output	Internal SPI clock connection between Transceiver SCK and MCU SPI0 (port C bit 5)	<ul style="list-style-type: none"> <li>MCU IO and Transceiver IO connected onboard</li> <li>MCU IO must be configured for this connection</li> </ul>

**Table 1. Pin Function Description (Sheet 5 of 5)**

Pin #	Pin Name <sup>1</sup>	Type	Description	Functionality
60	MOSI/PTC6/SPI0_MOSI/ SPI0_MISO	Digital Input/Output	Internal SPI data connection to Transceiver MOSI bit 1 to MCU SPI0 (Port C bit 6 )	<ul style="list-style-type: none"> <li>MCU IO and Transceiver IO connected onboard</li> <li>MCU IO must be configured for this connection</li> </ul>
FLAG	VSS	Power input	External package flag. Common VSS	Connect to ground.

<sup>1</sup> Refer to ADD Table 1-3 for additional pin-out information on default and alternate setting selections.

## 5.2 Internal Functional Interconnects

The MCU provides control to the transceiver through the SPI Port and receives status from the transceiver from the DIOx pins. Certain interconnects between the devices are routed onboard the SiP. In addition, the signals are brought out to external pads.

**Table 2. MKW01Z128 Internal Functional Interconnects**

Pin #	MCU Signal	Transceiver Signal	Description
49	DIO0/PTE2/SPI1_ SCK	DIO0	Transceiver DIO0 can be programmed to provide status to the MCU
50	DIO1/PTE3/SPI1_ MISO/SPI1_MOSI	DIO1	Transceiver DIO1 can be programmed to provide status to the MCU
57	MISO/PTC7/SPI0_ MISO/SPI0_MOSI	MISO	SPI data from transceiver to MCU
58	NSS/PTD0/SPI0_ PCS0	NSS	SPI chip select
59	SCK/PTC5/SPI0_ SCK	SCK	SPI Clock
60	MOSI/PTC6/SPI0_ MOSI/SPI0_MISO	MOSI	SPI data from MCU to transceiver

### NOTE

- As shown in [Table 2](#), the MCU SPI Port pin selection must be configured by software.
- The transceiver DIO pins must be programmed to provide desired status

## 5.3 External Functional Interconnects

In addition to the onboard device interconnection, other external connections between the MCU and the transceiver are common:

- Freescall recommends driving/controlling the transceiver reset from an MCU GPIO - This allows over-riding control of the transceiver from the system application.

- The other DIO2-DIO4 status and RXTX signals can prove useful for monitoring the transceiver operation - the DIO2-DIO4 signals must be programmed to provide operational status. All signals must be connected externally to appropriate MCU GPIO for this function.

## 6 System and Power Management

The MKW01Z128 consists of an independent transceiver and MCU. The MCU controls the transceiver through programming of the SPI Port, and sets its operational mode through this control channel. Total current draw for the MKW01Z128 is dependent on the operation mode of both devices where different modes allow for different levels of power-down. Some additional features supported are:

- Transceiver Sleep with MCU set at the lowest power state.
- The transceiver mode selection being independent of the MCU's mode selection.
- The transceiver uses/powers-up the transmitter or receiver only as required.
- MCU peripheral control clock gating being disabled on a module-by-module basis to provide lowest power.
- RTC can be used as wake-up timer.
- LLWU (Low Leakage Wake-up Unit) available.

### 6.1 MCU Power Modes

The MCU has 9 different modes of operation to allow the user to optimize power consumption for the level of functionality needed. Depending on the STOP requirements of the user application, a variety of STOP modes are available that provide state retention, partial power down or full power down of certain logic and/or memory. I/O states are held in all modes of operation. [Table 3](#) outlines the various available power modes of MCU operation.

For each RUN mode there is a corresponding WAIT and STOP mode. WAIT modes are similar to ARM sleep modes. STOP modes (VLPS, STOP) are similar to ARM sleep deep mode. The very low power run (VLPR) operating mode can greatly reduce runtime power when the maximum bus frequency is not required to handle application needs. The 3 primary modes of operation are RUN, WAIT and STOP. The WFI instruction invokes both WAIT and STOP modes for the MCU. The primary modes are augmented in a number of ways to provide lower power based on application needs.

**Table 3. MCU power modes**

Chip Power Mode	Description	Core Mode	Normal Recovery Method
Normal run	Allows maximum performance of chip. Default mode out of reset; onchip voltage regulator is on.	Run	—
Normal Wait - via WFI	Allows peripherals to function while the core is in sleep mode, reducing power. NVIC remains sensitive to interrupts; peripherals continue to be clocked.	Sleep	Interrupt

**Table 3. MCU power modes**

Chip Power Mode	Description	Core Mode	Normal Recovery Method
Normal Stop - via WFI	Places chip in static state. Lowest power mode that retains all registers while maintaining LVD protection. NVIC is disabled; AWIC is used to wake up from interrupt; peripheral clocks are stopped.	Sleep Deep	Interrupt
VLPR (Very Low Power Run)	On-chip voltage regulator is in a low power mode that supplies only enough power to run the chip at a reduced frequency. Reduced frequency Flash access mode (1 MHz); LVD off; in BLPI clock mode, the fast internal reference oscillator is available to provide a low power nominal 4 MHz source for the core with the nominal bus and flash clock required to be <800 kHz; alternatively, BLPE clock mode can be used with an external clock or the crystal oscillator providing the clock source.	Run	—
VLPW (Very Low Power Wait) -via WFI	Same as VLPR but with the core in sleep mode to further reduce power; NVIC remains sensitive to interrupts (FCLK = ON). On-chip voltage regulator is in a low power mode that supplies only enough power to run the chip at a reduced frequency.	Sleep	Interrupt
VLPS (Very Low Power Stop)-via WFI	Places chip in static state with LVD operation off. Lowest power mode with ADC and pin interrupts functional. Peripheral clocks are stopped, but OSC, LPTMR, RTC, CMP, TSI can be used. TPM and UART can optionally be enabled if their clock source is enabled. NVIC is disabled (FCLK = OFF); AWIC is used to wake up from interrupt. On-chip voltage regulator is in a low power mode that supplies only enough power to run the chip at a reduced frequency. All SRAM is operating (content retained and I/O states held).	Sleep Deep	Interrupt
LLS (Low Leakage Stop)	State retention power mode. Most peripherals are in state retention mode (with clocks stopped), but OSC, LLWU, LPTMR, RTC, CMP,, TSI can be used. NVIC is disabled; LLWU is used to wake up.  <b>NOTE:</b> The LLWU interrupt must not be masked by the interrupt controller to avoid a scenario where the system does not fully exit stop mode on an LLS recovery.  All SRAM is operating (content retained and I/O states held).	Sleep Deep	Wakeup Interrupt <sup>1</sup>
VLLS3 (Very Low Leakage Stop3)	Most peripherals are disabled (with clocks stopped), but OSC, LLWU, LPTMR, RTC, CMP, TSI can be used. NVIC is disabled; LLWU is used to wake up.  SRAM_U and SRAM_L remain powered on (content retained and I/O states held).	Sleep Deep	Wakeup Reset <sup>2</sup>



**Table 3. MCU power modes**

<b>Chip Power Mode</b>	<b>Description</b>	<b>Core Mode</b>	<b>Normal Recovery Method</b>
VLLS1 (Very Low Leakage Stop1)	Most peripherals are disabled (with clocks stopped), but OSC, LLWU, LPTMR, RTC, CMP, TSI can be used. NVIC is disabled; LLWU is used to wake up. All of SRAM_U and SRAM_L are powered off.	Sleep Deep	Wakeup Reset <sup>2</sup>
VLLS0 (Very Low Leakage Stop 0)	Most peripherals are disabled (with clocks stopped), but LLWU, LPTMR, RTC, TSI can be used. NVIC is disabled; LLWU is used to wake up. All of SRAM_U and SRAM_L are powered off. LPO disabled, optional POR brown-out detection	Sleep Deep	Wakeup Reset <sup>2</sup>

<sup>1</sup> Resumes normal run mode operation by executing the LLWU interrupt service routine.

<sup>2</sup> Follows the reset flow with the LLWU interrupt flag set for the NVIC.

## 6.1.1 Power mode transitions

Figure 6 shows power mode transitions. Any reset always brings the MCU back to normal state run. In RUN, WAIT and STOP modes active power regulation is enabled. The VLPx modes are limited in frequency but offer a lower power operating power mode than normal modes. The LLS and VLLSx modes are the lowest power stop modes based on the amount of logic or memory that is required to be retained by the application.

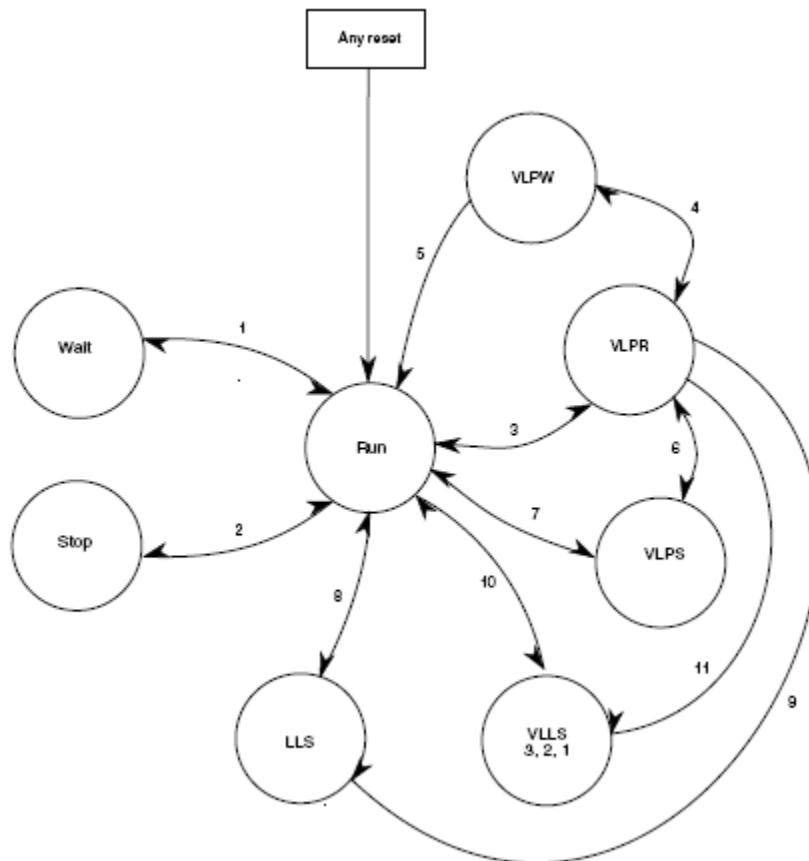


Figure 6. Power mode state transition diagram

## 6.2 Transceiver modes of operation.

The transceiver can be set in numerous modes of operation as described in Table 4. By default, when switching from one mode to another various features are selectively turned on coordinated by a pre-defined optimized sequence using the automatic sequencer. Alternatively, these operating modes can be selected directly by disabling the automatic sequencer.

Table 4. Basic Transceiver modes

Selected Mode	Enabled blocks
Sleep	None
Stand-by	Main regulator and crystal osillator

**Table 4. Basic Transceiver modes**

Selected Mode	Enabled blocks
Idle	Main regulator and RC oscillator
FS	Frequency synthesizer
Transmit	Frequency synthesizer and transmitter
Receive	Frequency synthesizer and receiver
Listen	Periodical receive wake-up from Idle operation

An overview of the transceiver modes of operation is described below:

- Sleep - provides lowest power consumption and is the full power down state.
- Idle - provides very low standby power consumption and has the main voltage regulator and the RC oscillator enabled.
- Standby - similar to Idle with low standby power consumption but has the main voltage regulator and the crystal oscillator enabled.
- FS (Frequency synthesizer) - the frequency synthesizer is alive to shorten startup time to transmit or receive states.
- Transmit - transmitter is active.
- Receive - receiver is active.

## 6.3 System Protection

The MKW01Z128 provides numerous vehicles to maintain security or a high level of system robustness:

- Standard COP Watchdog reset with option to run from dedicated 1 kHz internal clock source or bus clock. The COP watchdog is intended to force a system reset when the application software fails to execute as expected.
- LVD protection with reset or interrupt; selectable trip points.
- HardFault exception on attempts to execute undefined instructions or access to undefined memory space.
- LOCKUP reset resource from core.
- Flash protection

## 7 Development Environment

Development support for the ARM® Cortex M0+ MCU on the MKW01Z128 is configured to provide maximum flexibility as allowed by the restrictions of the pinout and other available resources. One debug interface is supported:

- Two-wire Serial Wire Debug (SWD) interface

[Table 5](#) presents a brief description of the serial wire debug description.

## NOTE

Electrical specifications for the SWD lines can be found in the appendix.

**Table 5. Debug Components Description**

Module	Type	Description
SWCLK	Input	Serial Wire Clock. This pin is the clock for debug logic when in the Serial Wire Debug mode. This pin is pulled down internally.
SWDIO	Input /Output	Serial Wire debug data input / output. The SWDIO pin is used by an external debug tool for communication and device control. This pin is pulled up internally.

## 8 System Electrical Specification

This section details maximum ratings for the 60 pin LGA package and recommended operating conditions, DC characteristics, and AC characteristics for the modem, and the MCU.

### 8.1 LGA Package Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maximum rating is not guaranteed. Stress beyond the limits specified in [Table 6](#) may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either  $V_{SS}$  or  $V_{DD}$ ) or the programmable pull-up resistor associated with the pin is enabled.

[Table 6](#) shows the maximum ratings for the 60 Pin LGA package.

**Table 6. LGA Package Maximum Ratings**

Rating	Symbol	Value	Unit
Maximum Junction Temperature	$T_J$	95	°C
Storage Temperature Range	$T_{stg}$	-55 to 115	°C
Power Supply Voltage	$V_{BATT}, V_{DDINT}$	-0.3 to 3.8	Vdc
Digital Input Voltage	$V_{in}$	-0.3 to ( $V_{DDINT} + 0.3$ )	
RF Input Power	$P_{max}$	6	dBm

**Note:** Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics or Recommended Operating Conditions tables.

**Note:** Meets Human Body Model (HBM) = 2 kV. RF input/output pins have no ESD protection.

## 8.2 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with the JESD22 Stress Test Qualification for Commercial Grade Integrated Circuits. During the device qualification ESD stresses were performed for the human body model (HBM), the machine model (MM) and the charge device model (CDM).

All latchup testing is in conformity with the JESD78 IC Latch-Up Test.

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification.

**Table 7. ESD and Latch-up Test Conditions**

Model	Description	Symbol	Value	Unit
Human Body	Series resistance	R1	1500	$\Omega$
	Storage capacitance	C	100	pF
	Number of pulses per pin <sup>1</sup>	—	1	
Machine	Series resistance	R1	0	$\Omega$
	Storage capacitance	C	200	pF
	Number of pulses per pin <sup>1</sup>	—	1	
Latch-up	Minimum input voltage limit		-1.8	V
	Maximum input voltage limit		4.32	V

<sup>1</sup> This number represents a minimum number for both positive pulse(s) and negative pulse(s)

**Table 8. ESD and Latch-Up Protection Characteristics**

No.	Rating <sup>1</sup>	Symbol	Min	Max	Unit
1	Human body model (HBM)	$V_{HBM}$	$\pm 2000$	—	V
2	Machine model (MM)	$V_{MM}$	$\pm 200$	—	V
3	Charge device model (CDM)	$V_{CDM}$	$\pm 500$	—	V
4	Latch-up current at $T_A = 85^\circ\text{C}$	$I_{LAT}$	$\pm 100$	—	mA

<sup>1</sup> Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

## 8.3 Transceiver Electrical Characteristics

The tables below give the electrical specifications of the transceiver under the following conditions: Supply voltage  $V_{BAT1} = V_{BAT2} = V_{DD} = 3.3$  V, temperature =  $25^\circ\text{C}$ ,  $FXOSC = 32$  MHz,  $FRF = 915$  MHz,  $P_{out} = +13$  dBm, 2-level FSK modulation without pre-filtering,  $FDA = 5$  kHz, Bit Rate = 4.8 kb/s and terminated in a matched 50 Ohm impedance, unless otherwise specified.

## NOTE

Unless otherwise specified, the performances in the other frequency bands are similar or better.

### 8.3.1 Transceiver Recommended Operating Conditions

Table 9. Recommended Operating Conditions

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage ( $V_{BATT}$ )		1.8		3.6	Vdc
Operating Temperature Range	$T_A$	-40	25	85	°C
Logic Input Voltage Low	$V_{IL}$	0	-	20% $V_{BATT}$	V
Logic Input Voltage High	$V_{IH}$	80% $V_{BATT}$	-	$V_{BATT}$	V
Logic Output Voltage Low ( $I_{max} = -1$ mA)	$V_{OL}$	0	-	10% $V_{BATT}$	V
Logic Output Voltage High ( $I_{max} = 1$ mA)	$V_{OH}$	90% $V_{BATT}$	-	$V_{BATT}$	V
Load capacitance on digital ports	$C_L$			25	pF
SPI Clock Rate	$f_{SPI}$	-	-	8.0	MHz
RF Input Power	$P_{max}$	-	-	0	dBm
Crystal Reference Oscillator Frequency	$f_{ref}$	32 MHz Only (Some variants may use 30 MHz instead)			

## 8.3.2 Transceiver Power Consumption

Table 10. Power Supply Current

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Supply current in Sleep mode		IDDSL	-	0.1	1	μA
Supply current in Idle mode	RC oscillator enabled	IDDIDLE	-	1.2	-	μA
Supply current in Standby mode	Crystal oscillator enabled	IDDST	-	1.25	1.5	mA
Supply current in Synthesizer mode		IDDFS	-	9	-	mA
Supply current in Receive mode		IDDR	-	16	-	mA
Supply current in Transmit mode with appropriate matching, stable across VDD range	RFOP = +17 dBm, on PA_BOOST	IDDT	-	95	-	mA
	RFOP = +13 dBm, on RFIO pin		-	45	-	mA
	RFOP = +10 dBm, on RFIO pin		-	33	-	mA
	RFOP = 0 dBm, on RFIO pin		-	20	-	mA
	RFOP = -1 dBm, on RFIO pin		-	16	-	mA

## 8.3.3 Transceiver Frequency Synthesis

Table 11. Frequency Synthesizer Specification

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Synthesizer Frequency Range	Programmable, 32 MHz clock	FR	290	-	340	MHz
			424	-	510	MHz
			862	-	1020	MHz
Crystal oscillator frequency		FXOSC	-	32	-	MHz
Crystal oscillator wake-up time		TS_OSC	-	250	500	μs
Frequency synthesizer wake-up time to PllLock signal	From Standby mode	TS_FS	-	80	150	μs
Frequency synthesizer hop time at most 10 kHz away from the target	200 kHz step	TS_HOP	-	20	-	μs
	1 MHz step		-	20	-	μs
	5 MHz step		-	50	-	μs
	7 MHz step		-	50	-	μs
	12 MHz step		-	80	-	μs
	20 MHz step		-	80	-	μs
25 MHz step	-	80	-	μs		
Frequency synthesizer step	$FSTEP = FXOSC/2^{19}$	FSTEP	-	61.0	-	Hz
RC Oscillator frequency	After calibration	FRC	-	62.5	-	kHz
Bit rate, FSK	Programmable	BRF	1.2	-	600	kbps
Bit rate, OOK	Programmable	BRO	1.2	-	32.768	kbps
Frequency deviation, FSK	Programmable FDA + BRF/2 =< 500 kHz	FDA	0.6	-	300	kHz

### 8.3.4 Receiver

All receiver tests are performed with  $RxBw = 10$  kHz (Single Side Bandwidth) as programmed in  $RegRxBw$ , receiving a PN15 sequence with a BER of 0.1% (Bit Synchronizer is enabled), unless otherwise specified. The LNA impedance is set to 200 Ohms, by setting bit  $LnaZin$  in  $RegLna$  to 1. Blocking tests are performed with an unmodulated interferer. The wanted signal power for the Blocking Immunity, ACR, IIP2, IIP3 and AMR tests is set 3 dB above the nominal sensitivity level.

**Table 12. Receiver Specification**

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
FSK sensitivity, highest LNA gain	FDA = 5 kHz, BR = 1.2 kb/s	RFS_F	-	-118	-	dBm
	FDA = 5 kHz, BR = 4.8 kb/s		-	-114	-	dBm
	FDA = 40 kHz, BR = 38.4 kb/s		-	-105	-	dBm
	FDA = 5 kHz, BR = 1.2 kb/s <sup>1</sup>		-	-120	-	dBm
OOK sensitivity, highest LNA gain	BR = 4.8 kb/s	RFS_O	-	-112	-109	dBm
Co-Channel Rejection		CCR	-13	-10	-	dB
Adjacent Channel Rejection	Offset = +/- 25 kHz Offset = +/- 50 kHz	ACR	-	42	-	dB
			37	42	-	dB
Blocking Immunity	Offset = +/- 1 MHz Offset = +/- 2 MHz Offset = +/- 10 MHz	BI	-	-45	-	dBm
			-	-40	-	dBm
			-	-32	-	dBm
Blocking Immunity Wanted signal at sensitivity +16dB	Offset = +/- 1 MHz Offset = +/- 2 MHz Offset = +/- 10 MHz		-	-36	-	dBm
			-	-33	-	dBm
			-	-25	-	dBm
AM Rejection , AM modulated interferer with 100% modulation depth, fm = 1 kHz, square	Offset = +/- 1 MHz Offset = +/- 2 MHz Offset = +/- 10 MHz	AMR	-	-45	-	dBm
			-	-40	-	dBm
			-	-32	-	dBm
2nd order Input Intercept Point Unwanted tones are 20 MHz above the LO	Lowest LNA gain Highest LNA gain	IIP2	-	+75	-	dBm
			-	+35	-	dBm
3rd order Input Intercept point Unwanted tones are 1MHz and 1.995 MHz above the LO	Lowest LNA gain Highest LNA gain	IIP3	- -23	+20 -18	- -	dBm dBm
Single Side channel filter BW	Programmable	BW_SSB	2.6	-	500	kHz
Image rejection in OOK mode	Wanted signal level = -106 dBm	IMR_ OOK	27	30	-	dB
Receiver wake-up time, from PLL locked state to <i>RxReady</i>	$RxBw = 10$ kHz, BR = 4.8 kb/s $RxBw = 200$ kHz, BR = 100 kb/s	TS_RE	-	1.7	-	ms
			-	96	-	$\mu$ s
Receiver wake-up time, from PLL locked state, AGC enabled	$RxBw = 10$ kHz, BR = 4.8 kb/s $RxBw = 200$ kHz, BR = 100 kb/s	TS_RE_ AGC	-	3.0	-	ms
			-	163	-	$\mu$ s
Receiver wake-up time, from PLL lock state, AGC and AFC enabled	$RxBw = 10$ kHz, BR = 4.8 kb/s $RxBw = 200$ kHz, BR = 100 kb/s	TS_RE_ AGC&AFC	-	4.8	-	ms
			-	265	-	$\mu$ s
FEI sampling time	Receiver is ready	TS_FEI	-	$4 \cdot T_{bit}$	-	-
AFC Response Time	Receiver is ready	TS_AFC	-	$4 \cdot T_{bit}$	-	-



**Table 12. Receiver Specification**

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
RSSI Response Time	Receiver is ready	TS_RSSI	-	2.T <sub>bit</sub>	-	-
RSSI Dynamic Range	AGC enabled	DR_RSSI	-	-115	-	dBm
	Min		-	0	-	dBm
	Max		-		-	

<sup>1</sup> Set SensitivityBoost in RegTestLna to 0x2D to reduce the noise floor in the receiver

## 8.3.5 Transmitter

**Table 13. Transmitter Specification**

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
RF output power in 50 ohms On RFIO pin	Programmable with 1dB steps Max Min	RF_OP	-	+13	-	dBm
			-	-18	-	dBm
Max RF output power, on PA_BOOST pin	With external match to 50 ohms	RF_OPH	-	+17	-	dBm
RF output power stability	From VDD=1.8V to 3.6V	ΔRF_OP	-	+/-0.3	-	dB
Transmitter Phase Noise	50 kHz Offset from carrier 868 / 915 MHz bands 434 / 315 MHz bands	PHN	-	-95	-	dBc/Hz
			-	-99	-	
Transmitter adjacent channel power (measured at 25 kHz offset)	BT=0.5 . Measurement conditions as defined by EN 300 220-1 V2.1.1	ACP	-	-	-37	dBm
Transmitter wake up time, to the first rising edge of DCLK	Frequency Synthesizer enabled, PaRamp = 10 μs, BR = 4.8 kb/s.	TS_TR	-	120	-	μs

## 8.4 MCU Electrical Characteristics

The electrical characteristics of the MKW01Z128 MCU are described in the appendix, which pulls information from the document KL15P80M48SF0.

## 9 Typical Applications Circuit

Figure 7 shows a MKW01Z128 typical applications circuit with and without use of an external power amplifier (PA) (driven by the RF power boost feature). Note a number of circuit features:

1. The two metal flags on the package bottom are independent (unconnected), and as a result, both must be connected to ground.
2. The topology of the external RF matching components is consistent across various frequency bandwidths. Only the component values differ as determined by the desired frequency range.
3. Freescale recommends using a single crystal design (as shown) to minimize systems costs - the circuit must connect transceiver signal DIO5/CLKOUT to the MCU EXTAL input to supply the MCU with a crystal accurate clock source. Also, the MCU initialization must enable the DIO5 pin as the ClkOut function.

Freescale also recommends that the transceiver RESET is driven by an MCU GPIO to provide total hardware control of the transceiver. Figure 7 shows GPIO PTC0 (preferred), but any GPIO can be used.

4. The MKW01Z128 provides onboard connection for the DIO1-DIO0 status to the MCU. External connection of DIO4-DIO2 status to MCU GPIO may be useful or required to implement a wireless node communication algorithm.
5. The transceiver reference oscillator uses the specified 32 MHz<sup>1</sup> crystal (pins XTA and XTB).
6. A debug port connector will be provided for programming the MKW01Z128 MCU FLASH and debugging code via the SWD interface.

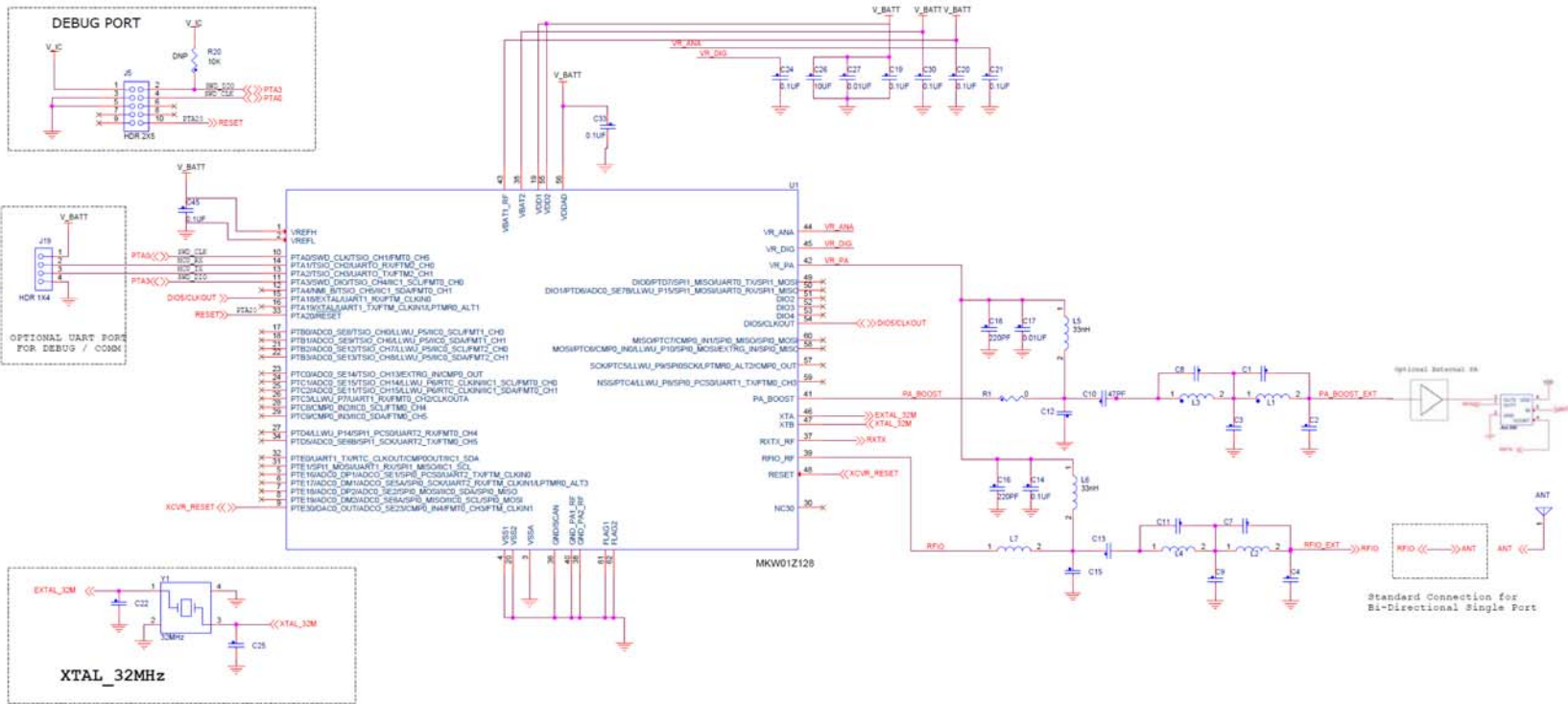
Two common RF wiring options are shown in Figure 7:

1. Bi-directional single port operation - this mode uses the bi-directional RF port pin of the MKW01Z128 designated as RFIO. The device transmits and receives through this single port.
  - Typical +13 dBm TX output power
  - An inductor acts to provide DC power to the onboard transmitter while also acting as an AC signal block.
  - A circuit topology consisting of inductors and capacitors will provide:
    - Impedance matching between the RFIO port and the antenna
    - Low pass filtering for the onboard transmitter - when fully populated can implement an elliptic-function low pass filter.

#### NOTE

- The topology for the RF matching network can be used over the various bands of interest with changes in component values
  - Not all indicated components are used at all frequencies
  - Refer to *MKW01Z128 Sub 1 GHz Low Power Transceiver plus Microcontroller Reference Manual* (MKW01Z128RM.pdf) for additional information
2. Dual port operation with external amplification - this mode uses the RFIO port pin of the MKW01Z128 typically as the RX input and the auxiliary port PA\_BOOST as the TX output. An external PA can optionally be inserted into the transmit path and an external antenna switch is also required.
    - The PA\_BOOST has typical +17 dBm output power - this is +4 dBm higher than the RFIO and helps achieve higher power at the PA output
    - The PA\_BOOST transmit path has a similar filter matching network discussed in the single-port to do low pass filtering and impedance match. The above note about components values also applies.
    - With separate transmit and receive paths, an antenna switch is required - the RXTX signal or another programmed GPIO can be used to switch paths depending on radio operation.
    - The receive side matching network can be simplified as no low pass filtering or harmonic trapping is required as with the transmit and single port networks

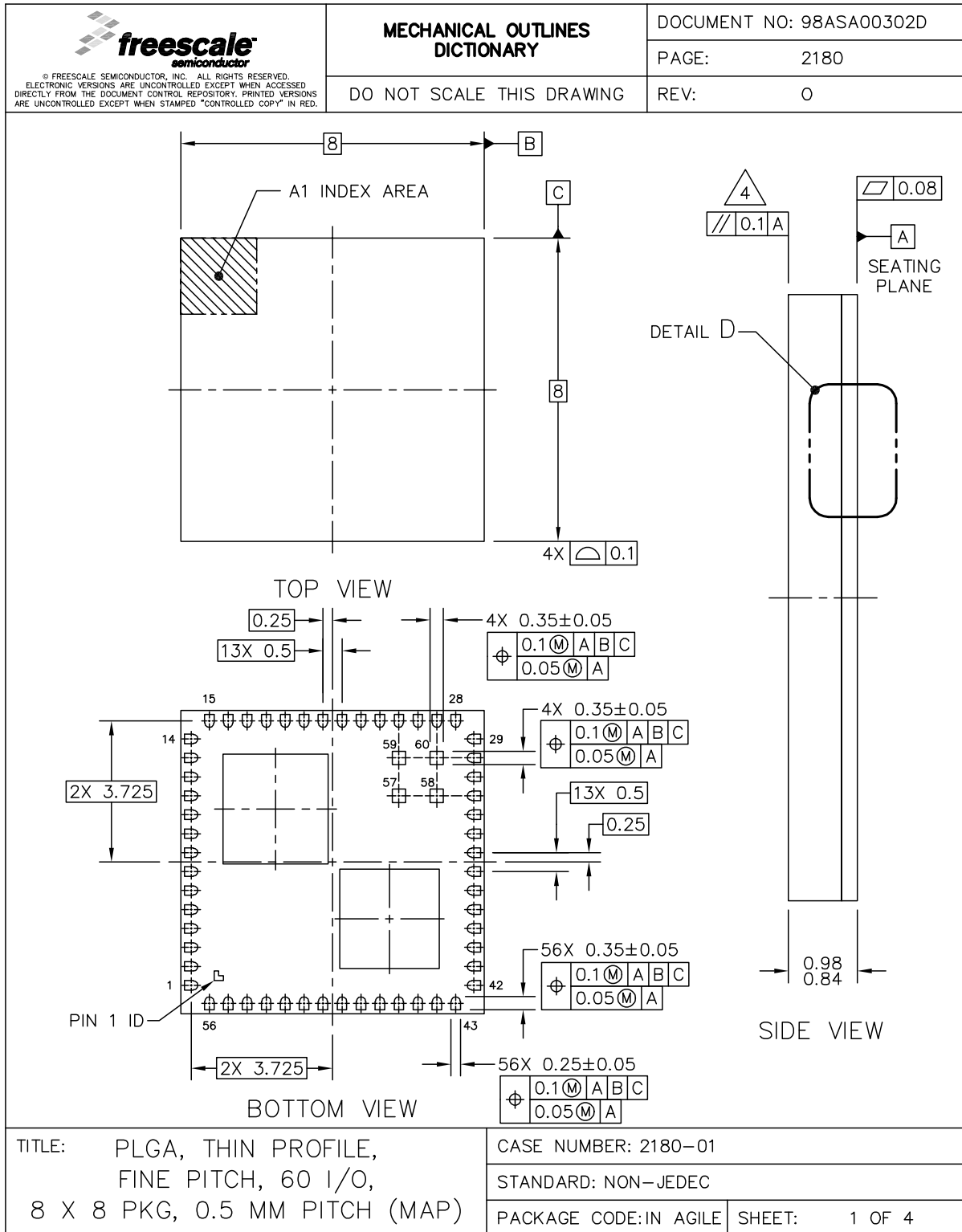
<sup>1</sup>. Or 30 MHz, in some cases.



NOTES: 1) RF components determined by desired frequency range. 2) Recommend that Clkout drive the MCU EXTERNAL input. 3) Recommend that transceiver RESET be driven from MCU GPIO (PTE30 shown) 4) Transceiver status DIO4- DIO2 may be monitored via external connection to MCU GPIO

Figure 7. MKW01Z128 Application Circuit Options

# 10 Mechanical Drawings



**Figure 8. Mechanical Drawing (1 of 2)**



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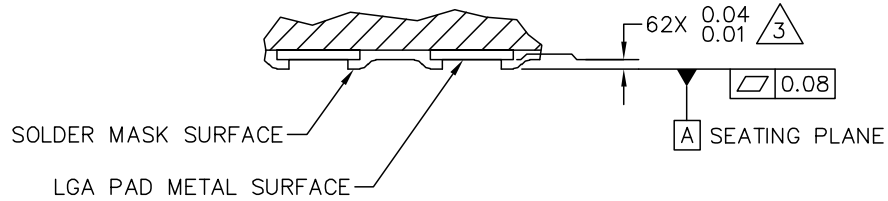
**MECHANICAL OUTLINES  
 DICTIONARY**

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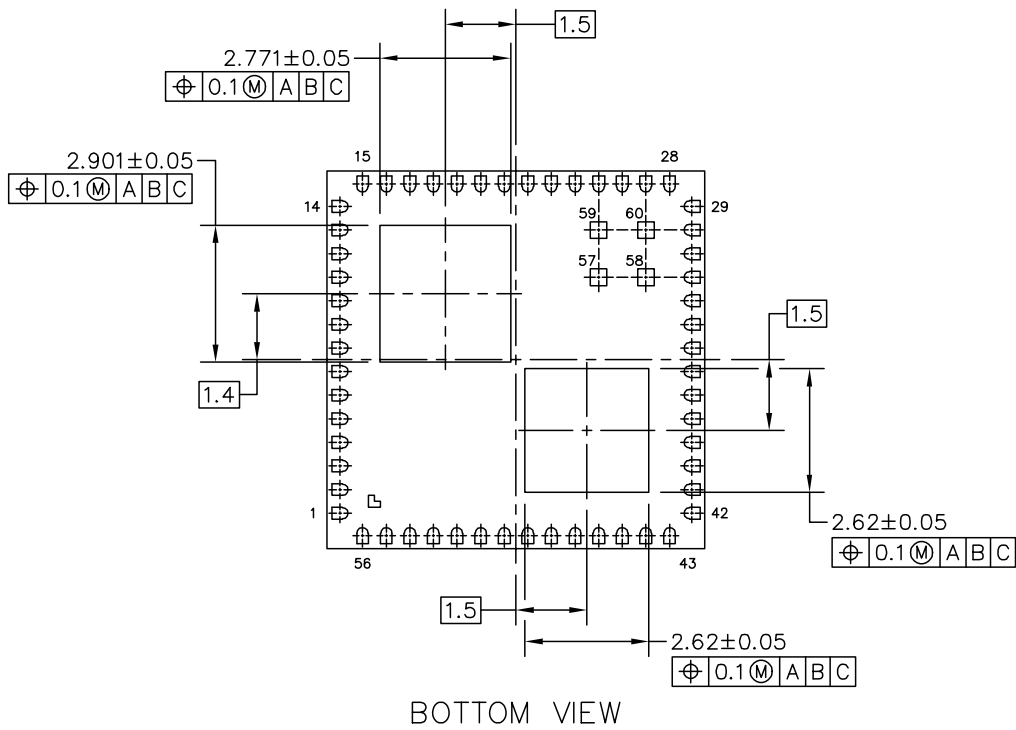
PAGE: 2180

DO NOT SCALE THIS DRAWING

REV: 0



DETAIL D  
 VIEW ROTATED 90° CW



BOTTOM VIEW

TITLE: PLGA, THIN PROFILE,  
 FINE PITCH, 60 I/O,  
 8 X 8 PKG, 0.5 MM PITCH (MAP)

CASE NUMBER: 2180-01

STANDARD: NON-JEDEC

PACKAGE CODE: IN AGILE

SHEET: 2

**Figure 9. Mechanical Drawing (2 of 2)**

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## 11 Appendix — MCU Electrical Characteristics

The following pages are pulled from the KL15P8048MSF0 data sheets. Not all sections apply to the MKW01Z128 device. Where those sections don't apply, we've changed the content to have a gray box hiding the content.

**Table 1. Voltage and current operating requirements (continued)**

Symbol	Description	Min.	Max.	Unit	Notes
$I_{CDIO}$	Digital pin negative DC injection current — single pin <ul style="list-style-type: none"> <li><math>V_{IN} &lt; V_{SS}-0.3V</math></li> </ul>	-5	—	mA	1
$I_{CAIO}$	Analog <sup>2</sup> pin DC injection current — single pin <ul style="list-style-type: none"> <li><math>V_{IN} &lt; V_{SS}-0.3V</math> (Negative current injection)</li> <li><math>V_{IN} &gt; V_{DD}+0.3V</math> (Positive current injection)</li> </ul>	-5 —	— +5	mA	3
$I_{Ccont}$	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins <ul style="list-style-type: none"> <li>Negative current injection</li> <li>Positive current injection</li> </ul>	-25 —	— +25	mA	
$V_{RAM}$	$V_{DD}$ voltage required to retain RAM	1.2	—	V	

- All digital I/O pins are internally clamped to  $V_{SS}$  through a ESD protection diode. There is no diode connection to  $V_{DD}$ . If  $V_{IN}$  greater than  $V_{DIO\_MIN}$  ( $=V_{SS}-0.3V$ ) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as  $R=(V_{DIO\_MIN}-V_{IN})/|I_{ICL}|$ .
- Analog pins are defined as pins that do not have an associated general purpose I/O port function.
- All analog pins are internally clamped to  $V_{SS}$  and  $V_{DD}$  through ESD protection diodes. If  $V_{IN}$  is greater than  $V_{AIO\_MIN}$  ( $=V_{SS}-0.3V$ ) and  $V_{IN}$  is less than  $V_{AIO\_MAX}$  ( $=V_{DD}+0.3V$ ) is observed, then there is no need to provide current limiting resistors at the pads. If these limits cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as  $R=(V_{AIO\_MIN}-V_{IN})/|I_{ICL}|$ . The positive injection current limiting resistor is calculated as  $R=(V_{IN}-V_{AIO\_MAX})/|I_{ICL}|$ . Select the larger of these two calculated resistances.

## 5.2.2 LVD and POR operating requirements

**Table 2.  $V_{DD}$  supply LVD and POR operating requirements**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$V_{POR}$	Falling VDD POR detect voltage	0.8	1.1	1.5	V	
$V_{LVDH}$	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
$V_{LVW1H}$	Low-voltage warning thresholds — high range <ul style="list-style-type: none"> <li>Level 1 falling (LVWV=00)</li> </ul>	2.62	2.70	2.78	V	1
$V_{LVW2H}$	<ul style="list-style-type: none"> <li>Level 2 falling (LVWV=01)</li> </ul>	2.72	2.80	2.88	V	
$V_{LVW3H}$	<ul style="list-style-type: none"> <li>Level 3 falling (LVWV=10)</li> </ul>	2.82	2.90	2.98	V	
$V_{LVW4H}$	<ul style="list-style-type: none"> <li>Level 4 falling (LVWV=11)</li> </ul>	2.92	3.00	3.08	V	
$V_{HYSH}$	Low-voltage inhibit reset/recover hysteresis — high range	—	±60	—	mV	
$V_{LVDL}$	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	

Table continues on the next page...

**Table 2. V<sub>DD</sub> supply LVD and POR operating requirements (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V <sub>LVW1L</sub>	Low-voltage warning thresholds — low range • Level 1 falling (LVWV=00)	1.74	1.80	1.86	V	1
V <sub>LVW2L</sub>	• Level 2 falling (LVWV=01)	1.84	1.90	1.96	V	
V <sub>LVW3L</sub>	• Level 3 falling (LVWV=10)	1.94	2.00	2.06	V	
V <sub>LVW4L</sub>	• Level 4 falling (LVWV=11)	2.04	2.10	2.16	V	
V <sub>HYSL</sub>	Low-voltage inhibit reset/recover hysteresis — low range	—	±40	—	mV	
V <sub>BG</sub>	Bandgap voltage reference	0.97	1.00	1.03	V	
t <sub>LPO</sub>	Internal low power oscillator period — factory trimmed	900	1000	1100	μs	

1. Rising thresholds are falling threshold + hysteresis voltage

### 5.2.3 Voltage and current operating behaviors

**Table 3. Voltage and current operating behaviors**

Symbol	Description	Min.	Max.	Unit	Notes
V <sub>OH</sub>	Output high voltage — Normal drive pad • 2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V, I <sub>OH</sub> = -5 mA • 1.71 V ≤ V <sub>DD</sub> ≤ 2.7 V, I <sub>OH</sub> = -1.5 mA	V <sub>DD</sub> - 0.5 V <sub>DD</sub> - 0.5	— —	V V	1
V <sub>OH</sub>	Output high voltage — High drive pad • 2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V, I <sub>OH</sub> = -18 mA • 1.71 V ≤ V <sub>DD</sub> ≤ 2.7 V, I <sub>OH</sub> = -6 mA	V <sub>DD</sub> - 0.5 V <sub>DD</sub> - 0.5	— —	V V	1
I <sub>OHT</sub>	Output high current total for all ports	—	100	mA	
V <sub>OL</sub>	Output low voltage — Normal drive pad • 2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V, I <sub>OL</sub> = 5 mA • 1.71 V ≤ V <sub>DD</sub> ≤ 2.7 V, I <sub>OL</sub> = 1.5 mA	— —	0.5 0.5	V V	1
V <sub>OL</sub>	Output low voltage — High drive pad • 2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V, I <sub>OL</sub> = 18 mA • 1.71 V ≤ V <sub>DD</sub> ≤ 2.7 V, I <sub>OL</sub> = 6 mA	— —	0.5 0.5	V V	1
I <sub>OLT</sub>	Output low current total for all ports	—	100	mA	
I <sub>IN</sub>	Input leakage current (per pin) for full temperature range	—	1	μA	2
I <sub>IN</sub>	Input leakage current (per pin) at 25 °C	—	0.025	μA	2
I <sub>IN</sub>	Input leakage current (total all pins) for full temperature range	—	65	μA	2
I <sub>OZ</sub>	Hi-Z (off-state) leakage current (per pin)	—	1	μA	

Table continues on the next page...



**Table 3. Voltage and current operating behaviors (continued)**

Symbol	Description	Min.	Max.	Unit	Notes
R <sub>PU</sub>	Internal pullup resistors	20	50	kΩ	3
R <sub>PD</sub>	Internal pulldown resistors	20	50	kΩ	4

1. PTB0, PTB1, PTD6, and PTD7 I/O have both high drive and normal drive capability selected by the associated PTx\_PCRn[DSE] control bit. All other GPIOs are normal drive only.
2. Measured at V<sub>DD</sub> = 3.6 V
3. Measured at V<sub>DD</sub> supply voltage = V<sub>DD</sub> min and V<sub>input</sub> = V<sub>SS</sub>
4. Measured at V<sub>DD</sub> supply voltage = V<sub>DD</sub> min and V<sub>input</sub> = V<sub>DD</sub>

## 5.2.4 Power mode transition operating behaviors

All specifications except t<sub>POR</sub> and VLLSx→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 48 MHz
- Bus and flash clock = 24 MHz
- FEI clock mode

**Table 4. Power mode transition operating behaviors**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t <sub>POR</sub>	After a POR event, amount of time from the point V <sub>DD</sub> reaches 1.8 V to execution of the first instruction across the operating temperature range of the chip.	—	—	300	μs	
	• VLLS0 → RUN	—	95	115	μs	
	• VLLS1 → RUN	—	93	115	μs	
	• VLLS3 → RUN	—	42	53	μs	
	• LLS → RUN	—	4	4.6	μs	
	• VLPS → RUN	—	4	4.4	μs	
	• STOP → RUN	—	4	4.4	μs	

## 5.2.5 Power consumption operating behaviors

**Table 5. Power consumption operating behaviors**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I <sub>DDA</sub>	Analog supply current	—	—	See note	mA	1
I <sub>DD_RUNCO_CM</sub>	Run mode current in compute operation - 48 MHz core / 24 MHz flash/ bus disabled, LPTMR running using 4MHz internal reference clock, CoreMark® benchmark code executing from flash <ul style="list-style-type: none"> <li>at 3.0 V</li> </ul>	—	6.4	—	mA	2
I <sub>DD_RUNCO</sub>	Run mode current in compute operation - 48 MHz core / 24 MHz flash / bus clock disabled, code of while(1) loop executing from flash <ul style="list-style-type: none"> <li>at 3.0 V</li> </ul>	—	4.1	5.2	mA	3
I <sub>DD_RUN</sub>	Run mode current - 48 MHz core / 24 MHz bus and flash, all peripheral clocks disabled, code of while(1) loop executing from flash <ul style="list-style-type: none"> <li>at 3.0 V</li> </ul>	—	5.1	6.3	mA	3
I <sub>DD_RUN</sub>	Run mode current - 48 MHz core / 24 MHz bus and flash, all peripheral clocks enabled, code of while(1) loop executing from flash <ul style="list-style-type: none"> <li>at 3.0 V <ul style="list-style-type: none"> <li>at 25 °C</li> <li>at 125 °C</li> </ul> </li> </ul>	— —	6.4 6.8	7.8 8.3	mA mA	3, 4,
I <sub>DD_WAIT</sub>	Wait mode current - core disabled / 48 MHz system / 24 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled <ul style="list-style-type: none"> <li>at 3.0 V</li> </ul>	—	3.7	5.0	mA	3
I <sub>DD_WAIT</sub>	Wait mode current - core disabled / 24 MHz system / 24 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled <ul style="list-style-type: none"> <li>at 3.0 V</li> </ul>	—	2.9	4.2	mA	3
I <sub>DD_PSTOP2</sub>	Stop mode current with partial stop 2 clocking option - core and system disabled / 10.5 MHz bus <ul style="list-style-type: none"> <li>at 3.0 V</li> </ul>	—	2.5	3.7	mA	3
I <sub>DD_VLPRCO</sub>	Very low power run mode current in compute operation - 4 MHz core / 0.8 MHz flash / bus clock disabled, code of while(1) loop executing from flash <ul style="list-style-type: none"> <li>at 3.0 V</li> </ul>	—	188	570	μA	5
I <sub>DD_VLPR</sub>	Very low power run mode current - 4 MHz core / 0.8 MHz bus and flash, all peripheral clocks disabled, code of while(1) loop executing from flash <ul style="list-style-type: none"> <li>at 3.0 V</li> </ul>	—	224	613	μA	5

Table continues on the next page...

**Table 5. Power consumption operating behaviors (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I <sub>DD_VLPR</sub>	Very low power run mode current - 4 MHz core / 0.8 MHz bus and flash, all peripheral clocks enabled, code of while(1) loop executing from flash • at 3.0 V	—	300	745	μA	5, 4
I <sub>DD_VLPW</sub>	Very low power wait mode current - core disabled / 4 MHz system / 0.8 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled • at 3.0 V	—	135	496	μA	5
I <sub>DD_STOP</sub>	Stop mode current at 3.0 V at 25 °C at 50 °C at 70 °C at 85 °C at 105 °C	— — — — —	345 357 392 438 551	490 827 869 927 1065	μA	
I <sub>DD_VLPS</sub>	Very-low-power stop mode current at 3.0 V at 25 °C at 50 °C at 70 °C at 85 °C at 105 °C	— — — — —	4.4 10 20 37 81	16 35 50 112 201	μA	
I <sub>DD_LLS</sub>	Low leakage stop mode current at 3.0 V at 25 °C at 50 °C at 70 °C at 85 °C at 105 °C	— — — — —	1.9 3.6 6.5 13 30	3.7 39 43 49 69	μA	
I <sub>DD_VLLS3</sub>	Very low-leakage stop mode 3 current at 3.0 V at 25 °C at 50 °C at 70 °C at 85 °C at 105 °C	— — — — —	1.4 2.5 5.1 9.2 21	3.2 19 21 26 38	μA	
I <sub>DD_VLLS1</sub>	Very low-leakage stop mode 1 current at 3.0V at 25°C at 50°C at 70°C at 85°C at 105°C	— — — — —	0.7 1.3 2.3 5.1 13	1.4 13 14 17 25	μA	

Table continues on the next page...

**Table 5. Power consumption operating behaviors (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I <sub>DD_VLLS0</sub>	Very low-leakage stop mode 0 current (SMC_STOPCTRL[PORPO] = 0) at 3.0 V	—	381	943	nA	
	at 25 °C	—	956	11760		
	at 50 °C	—	2370	13260		
	at 70 °C	—	4800	15700		
	at 85 °C	—	12410	23480		
	at 105 °C	—				
I <sub>DD_VLLS0</sub>	Very low-leakage stop mode 0 current (SMC_STOPCTRL[PORPO] = 1) at 3.0 V	—	176	860	nA	6
	at 25 °C	—	760	3577		
	at 50 °C	—	2120	11660		
	at 70 °C	—	4500	18450		
	at 85 °C	—	12130	22441		
	at 105 °C	—				

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. MCG configured for PEE mode. CoreMark benchmark compiled using Keil 4.54 with optimization level 3, optimized for time.
3. MCG configured for FEI mode.
4. Incremental current consumption from peripheral activity is not included.
5. MCG configured for BLPI mode.
6. No brownout

**Table 6. Low power mode peripheral adders — typical value**

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
I <sub>IREFSTEN4MHz</sub>	4 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 4 MHz IRC enabled.	56	56	56	56	56	56	μA
I <sub>IREFSTEN32KHz</sub>	32 kHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 32 kHz IRC enabled.	52	52	52	52	52	52	μA
I <sub>IREFSTEN4MHz</sub>	External 4MHz crystal clock adder. Measured by entering STOP or VLPS mode with the crystal enabled.	206	228	237	245	251	258	uA

Table continues on the next page...

**Table 6. Low power mode peripheral adders — typical value (continued)**

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
I <sub>REFSTEN32KHz</sub>	External 32 kHz crystal clock adder by means of the OSCO_CR[EREFSTEN and EREFSTEN] bits. Measured by entering all modes with the crystal enabled.	440	490	540	560	570	580	nA
		440	490	540	560	570	580	
	VLLS1	490	490	540	560	570	680	
	VLLS3	510	560	560	560	610	680	
	LLS	510	560	560	560	610	680	
	VLPS							
	STOP							
I <sub>CMP</sub>	CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.	22	22	22	22	22	22	μA
I <sub>RTC</sub>	RTC peripheral adder measured by placing the device in VLLS1 mode with external 32 kHz crystal enabled by means of the RTC_CR[OSCE] bit and the RTC ALARM set for 1 minute. Includes ERCLK32K (32 kHz external crystal) power consumption.	432	357	388	475	532	810	nA
I <sub>UART</sub>	UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption.							
	MCGIRCLK (4MHz internal reference clock)	66	66	66	66	66	66	μA
	OSCERCLK (4MHz external crystal)	214	237	246	254	260	268	
I <sub>TPM</sub>	TPM peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source configured for output compare generating 100Hz clock signal. No load is placed on the I/O generating the clock signal. Includes selected clock source and I/O switching currents.							
	MCGIRCLK (4MHz internal reference clock)	86	86	86	86	86	86	μA
	OSCERCLK (4MHz external crystal)	235	256	265	274	280	287	
I <sub>BG</sub>	Bandgap adder when BGEN bit is set and device is placed in VLPx, LLS, or VLLSx mode.	45	45	45	45	45	45	μA

Table continues on the next page...

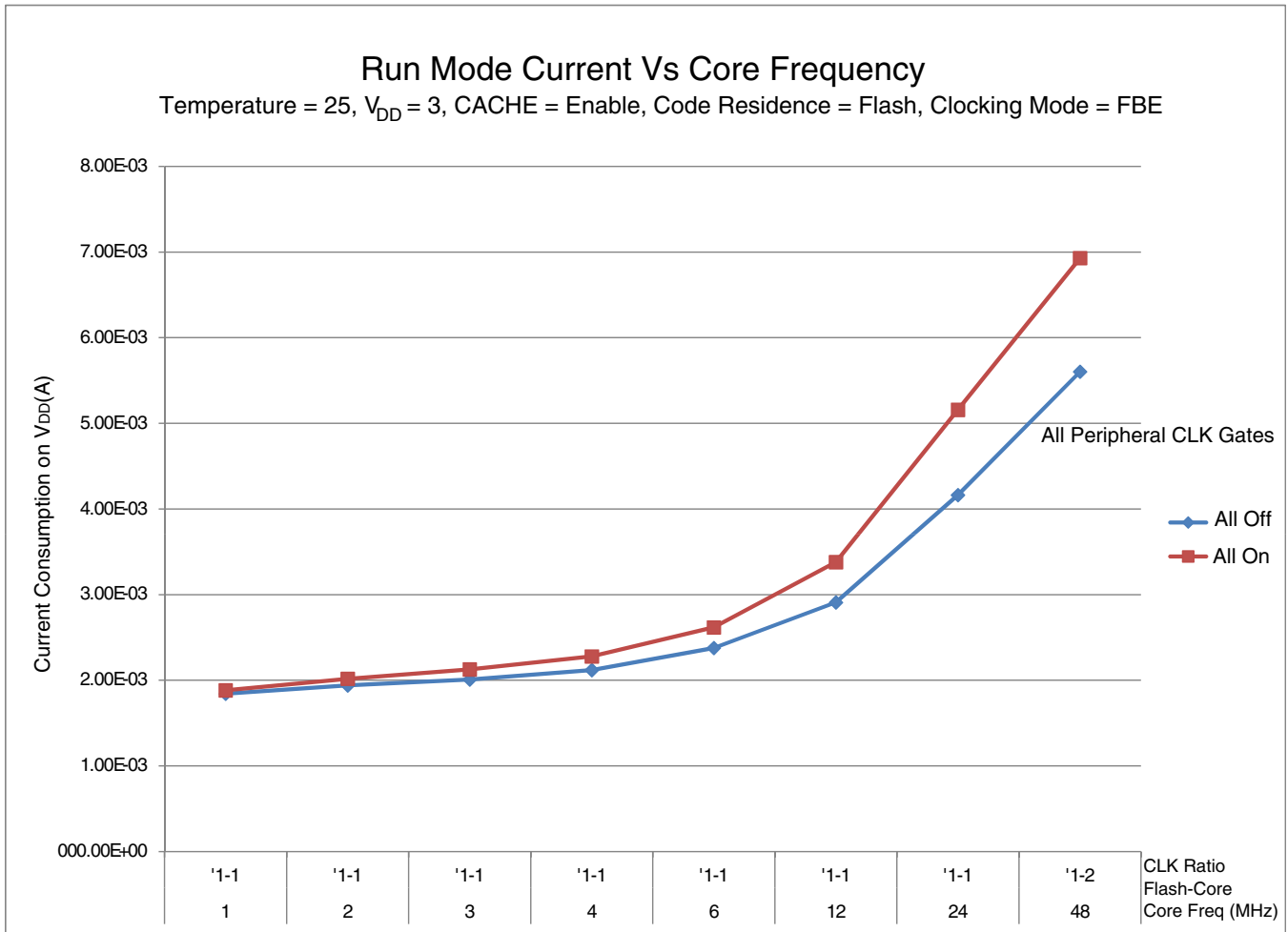
**Table 6. Low power mode peripheral adders — typical value (continued)**

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
I <sub>ADC</sub>	ADC peripheral adder combining the measured values at VDD and VDDA by placing the device in STOP or VLPS mode. ADC is configured for low power mode using the internal clock and continuous conversions.	366	366	366	366	366	366	μA

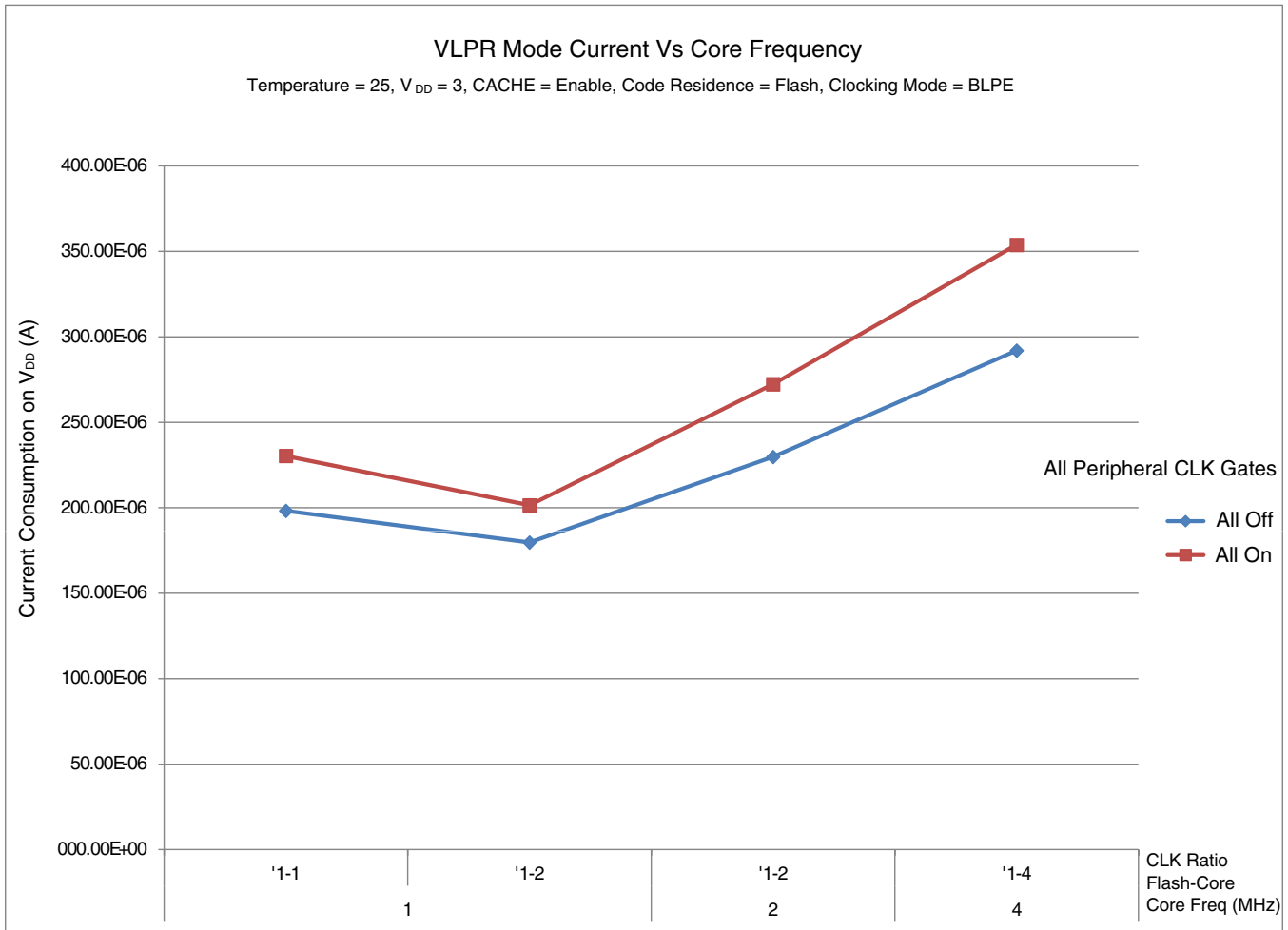
### 5.2.5.1 Diagram: Typical IDD\_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE for run mode, and BLPE for VLPR mode
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA



**Figure 2. Run mode supply current vs. core frequency**



**Figure 3. VLPR mode current vs. core frequency**





## 5.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to [www.freescale.com](http://www.freescale.com).
2. Perform a keyword search for “EMC design.”

## 5.2.8 Capacitance attributes

Table 8. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C <sub>IN_A</sub>	Input capacitance: analog pins	—	7	pF
C <sub>IN_D</sub>	Input capacitance: digital pins	—	7	pF

## 5.3 Switching specifications

### 5.3.1 Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
f <sub>SYS</sub>	System and core clock	—	48	MHz	
f <sub>BUS</sub>	Bus clock	—	24	MHz	
f <sub>FLASH</sub>	Flash clock	—	24	MHz	
f <sub>LPTMR</sub>	LPTMR clock	—	24	MHz	
VLPR mode <sup>1</sup>					
f <sub>SYS</sub>	System and core clock	—	4	MHz	
f <sub>BUS</sub>	Bus clock	—	1	MHz	
f <sub>FLASH</sub>	Flash clock	—	1	MHz	
f <sub>LPTMR</sub>	LPTMR clock	—	24	MHz	
f <sub>ERCLK</sub>	External reference clock	—	16	MHz	
f <sub>LPTMR_pin</sub>	LPTMR clock	—	24	MHz	
f <sub>LPTMR_ERCLK</sub>	LPTMR external reference clock	—	16	MHz	

Table continues on the next page...

## General

Symbol	Description	Min.	Max.	Unit	Notes
$f_{osc\_hi\_2}$	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	—	16	MHz	
$f_{TPM}$	TPM asynchronous clock	—	8	MHz	
$f_{UART0}$	UART0 asynchronous clock	—	8	MHz	

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

### 5.3.2 General Switching Specifications

These general purpose specifications apply to all signals configured for GPIO, UART, and I<sup>2</sup>C signals.

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1
	External RESET and NMI pin interrupt pulse width — Asynchronous path	100	—	ns	2
	GPIO pin interrupt pulse width — Asynchronous path	16	—	ns	2
	Port rise and fall time	—	36	ns	3

1. The greater synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.
3. 75 pF load

## 6 Peripheral operating requirements and behaviors

### 6.1 Core modules

#### 6.1.1 SWD Electricals

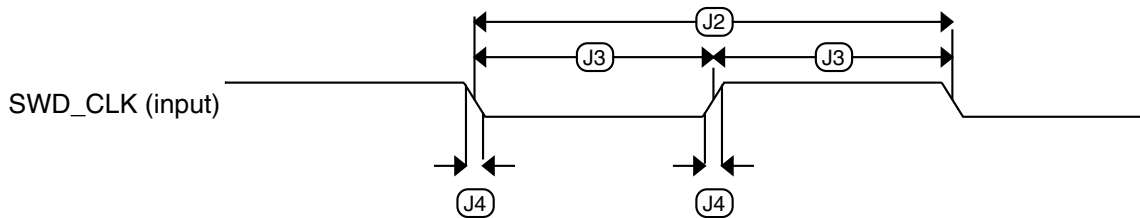
**Table 11. SWD full voltage range electricals**

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V

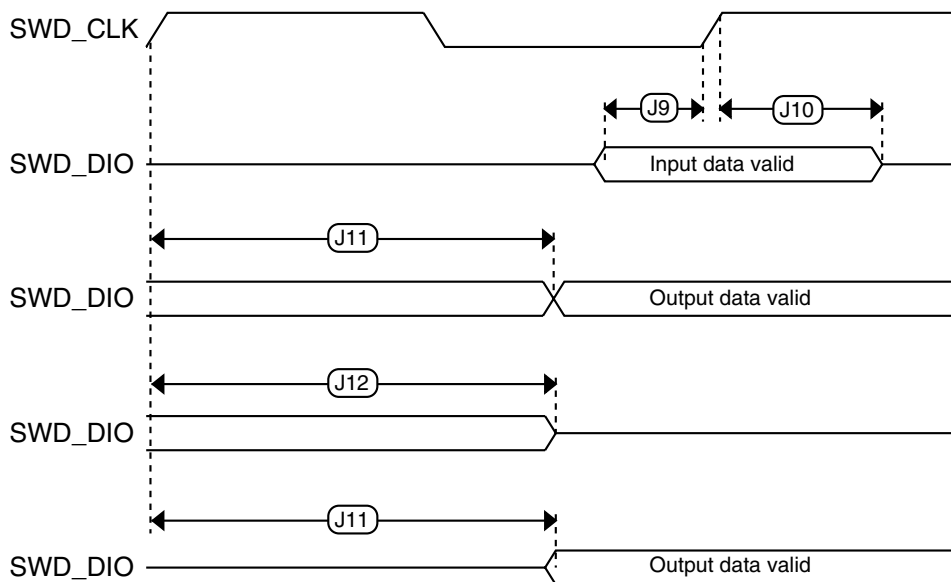
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**Table 11. SWD full voltage range electricals (continued)**

Symbol	Description	Min.	Max.	Unit
J1	SWD_CLK frequency of operation <ul style="list-style-type: none"> <li>Serial wire debug</li> </ul>	0	25	MHz
J2	SWD_CLK cycle period	1/J1	—	ns
J3	SWD_CLK clock pulse width <ul style="list-style-type: none"> <li>Serial wire debug</li> </ul>	20	—	ns
J4	SWD_CLK rise and fall times	—	3	ns
J9	SWD_DIO input data setup time to SWD_CLK rise	10	—	ns
J10	SWD_DIO input data hold time after SWD_CLK rise	0	—	ns
J11	SWD_CLK high to SWD_DIO data valid	—	32	ns
J12	SWD_CLK high to SWD_DIO high-Z	5	—	ns



**Figure 4. Serial wire clock input timing**



**Figure 5. Serial wire data timing**

## 6.2 System modules

There are no specifications necessary for the device's system modules.

## 6.3 Clock modules

### 6.3.1 MCG specifications

Table 12. MCG specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes	
$f_{ints\_ft}$	Internal reference frequency (slow clock) — factory trimmed at nominal $V_{DD}$ and 25 °C	—	32.768	—	kHz		
$f_{ints\_t}$	Internal reference frequency (slow clock) — user trimmed	31.25	—	39.0625	kHz		
$\Delta f_{dco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM	—	$\pm 0.3$	$\pm 0.6$	% $f_{dco}$	1	
$\Delta f_{dco\_t}$	Total deviation of trimmed average DCO output frequency over voltage and temperature	—	+0.5/-0.7	$\pm 3$	% $f_{dco}$	1, 2	
$\Delta f_{dco\_t}$	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0 - 70 °C	—	$\pm 0.4$	$\pm 1.5$	% $f_{dco}$	1, 2	
$f_{intf\_ft}$	Internal reference frequency (fast clock) — factory trimmed at nominal $V_{DD}$ and 25 °C	—	4	—	MHz		
$\Delta f_{intf\_ft}$	Frequency deviation of internal reference clock (fast clock) over temperature and voltage --- factory trimmed at nominal $V_{DD}$ and 25 °C	—	+1/-2	$\pm 3$	% $f_{intf\_ft}$	2	
$f_{intf\_t}$	Internal reference frequency (fast clock) — user trimmed at nominal $V_{DD}$ and 25 °C	3	—	5	MHz		
$f_{loc\_low}$	Loss of external clock minimum frequency — RANGE = 00	$(3/5) \times f_{ints\_t}$	—	—	kHz		
$f_{loc\_high}$	Loss of external clock minimum frequency — RANGE = 01, 10, or 11	$(16/5) \times f_{ints\_t}$	—	—	kHz		
FLL							
$f_{fill\_ref}$	FLL reference frequency range	31.25	—	39.0625	kHz		
$f_{dco}$	DCO output frequency range	Low range (DRS = 00)	20	20.97	25	MHz	3, 4
		Mid range (DRS = 01)	40	41.94	48	MHz	
		$1280 \times f_{fill\_ref}$					

Table continues on the next page...

**Table 12. MCG specifications (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes	
$f_{\text{dco\_t\_DMX32}}$	DCO output frequency	Low range (DRS = 00) $732 \times f_{\text{fil\_ref}}$	—	23.99	—	MHz	5, 6
		Mid range (DRS = 01) $1464 \times f_{\text{fil\_ref}}$	—	47.97	—	MHz	
$J_{\text{cyc\_fll}}$	FLL period jitter • $f_{\text{VCO}} = 48$ MHz	—	180	—	ps	7	
$t_{\text{fll\_acquire}}$	FLL target frequency acquisition time	—	—	1	ms	8	
PLL							
$f_{\text{vco}}$	VCO operating frequency	48.0	—	100	MHz		
$I_{\text{pll}}$	PLL operating current • PLL at 96 MHz ( $f_{\text{osc\_hi\_1}} = 8$ MHz, $f_{\text{pll\_ref}} = 2$ MHz, VDIV multiplier = 48)	—	1060	—	$\mu\text{A}$	9	
$I_{\text{pll}}$	PLL operating current • PLL at 48 MHz ( $f_{\text{osc\_hi\_1}} = 8$ MHz, $f_{\text{pll\_ref}} = 2$ MHz, VDIV multiplier = 24)	—	600	—	$\mu\text{A}$	9	
$f_{\text{pll\_ref}}$	PLL reference frequency range	2.0	—	4.0	MHz		
$J_{\text{cyc\_pll}}$	PLL period jitter (RMS) • $f_{\text{vco}} = 48$ MHz • $f_{\text{vco}} = 100$ MHz	—	120	—	ps	10	
		—	50	—	ps		
$J_{\text{acc\_pll}}$	PLL accumulated jitter over 1 $\mu\text{s}$ (RMS) • $f_{\text{vco}} = 48$ MHz • $f_{\text{vco}} = 100$ MHz	—	1350	—	ps	10	
		—	600	—	ps		
$D_{\text{lock}}$	Lock entry frequency tolerance	$\pm 1.49$	—	$\pm 2.98$	%		
$D_{\text{unl}}$	Lock exit frequency tolerance	$\pm 4.47$	—	$\pm 5.97$	%		
$t_{\text{pll\_lock}}$	Lock detector detection time	—	—	$150 \times 10^{-6} + 1075(1/f_{\text{pll\_ref}})$	s	11	

- This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
- The deviation is relative to the factory trimmed frequency at nominal  $V_{\text{DD}}$  and 25 °C,  $f_{\text{ints\_ft}}$ .
- These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32 = 0.
- The resulting system clock frequencies must not exceed their maximum specified values. The DCO frequency deviation ( $\Delta f_{\text{dco\_t}}$ ) over voltage and temperature must be considered.
- These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32 = 1.
- The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
- This specification is based on standard deviation (RMS) of period or frequency.
- This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
- Excludes any oscillator currents that are also consuming power while PLL is in operation.
- This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
- This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

## 6.3.2 Oscillator electrical specifications

This section provides the electrical characteristics of the module.

### 6.3.2.1 Oscillator DC electrical specifications

Table 13. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$V_{DD}$	Supply voltage	1.71	—	3.6	V	
$I_{DDOSC}$	Supply current — low-power mode (HGO=0) <ul style="list-style-type: none"> <li>• 32 kHz</li> <li>• 4 MHz</li> <li>• 8 MHz (RANGE=01)</li> <li>• 16 MHz</li> <li>• 24 MHz</li> <li>• 32 MHz</li> </ul>	—	500	—	nA	1
		—	200	—	$\mu$ A	
		—	300	—	$\mu$ A	
		—	950	—	$\mu$ A	
		—	1.2	—	mA	
		—	1.5	—	mA	
$I_{DDOSC}$	Supply current — high gain mode (HGO=1) <ul style="list-style-type: none"> <li>• 32 kHz</li> <li>• 4 MHz</li> <li>• 8 MHz (RANGE=01)</li> <li>• 16 MHz</li> <li>• 24 MHz</li> <li>• 32 MHz</li> </ul>	—	25	—	$\mu$ A	1
		—	400	—	$\mu$ A	
		—	500	—	$\mu$ A	
		—	2.5	—	mA	
		—	3	—	mA	
		—	4	—	mA	
$C_x$	EXTAL load capacitance	—	—	—		2, 3
$C_y$	XTAL load capacitance	—	—	—		2, 3
$R_F$	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	M $\Omega$	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	M $\Omega$	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	—	M $\Omega$	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	—	M $\Omega$	

Table continues on the next page...

**Table 13. Oscillator DC electrical specifications (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
R <sub>S</sub>	Series resistor — low-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)	—	0	—	kΩ	
V <sub>pp</sub> <sup>5</sup>	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	—	V <sub>DD</sub>	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	V <sub>DD</sub>	—	V	

1. V<sub>DD</sub>=3.3 V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3. C<sub>x</sub>,C<sub>y</sub> can be provided by using the integrated capacitors when the low frequency oscillator (RANGE = 00) is used. For all other cases external capacitors must be used..
4. When low power mode is selected, R<sub>F</sub> is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

### 6.3.2.2 Oscillator frequency specifications

**Table 14. Oscillator frequency specifications**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f <sub>osc_lo</sub>	Oscillator crystal or resonator frequency — low frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
f <sub>osc_hi_1</sub>	Oscillator crystal or resonator frequency — high frequency mode (low range) (MCG_C2[RANGE]=01)	3	—	8	MHz	
f <sub>osc_hi_2</sub>	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	8	—	32	MHz	
f <sub>ec_extal</sub>	Input clock frequency (external clock mode)	—	—	48	MHz	1, 2
t <sub>dc_extal</sub>	Input clock duty cycle (external clock mode)	40	50	60	%	

Table continues on the next page...



**Table 14. Oscillator frequency specifications (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{cst}$	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—	750	—	ms	3, 4
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—	250	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	—	0.6	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	—	1	—	ms	

1. Other frequency limits may apply when external clock is being used as a reference for the FLL or PLL.
2. When transitioning from FBE to FEI mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
3. Proper PC board layout procedures must be followed to achieve specifications.
4. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG\_S register being set.

## 6.4 Memories and memory interfaces

### 6.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

#### 6.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

**Table 15. NVM program/erase timing specifications**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{hvpgm4}$	Longword Program high-voltage time	—	7.5	18	$\mu$ s	
$t_{hversscr}$	Sector Erase high-voltage time	—	13	113	ms	1
$t_{hversall}$	Erase All high-voltage time	—	52	452	ms	1

1. Maximum time based on expectations at cycling end-of-life.

**6.4.1.2 Flash timing specifications — commands****Table 16. Flash command timing specifications**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1sec1k}$	Read 1s Section execution time (flash sector)	—	—	60	$\mu$ s	1
$t_{pgmchk}$	Program Check execution time	—	—	45	$\mu$ s	1
$t_{rdsrc}$	Read Resource execution time	—	—	30	$\mu$ s	1
$t_{pgm4}$	Program Longword execution time	—	65	145	$\mu$ s	
$t_{ersscr}$	Erase Flash Sector execution time	—	14	114	ms	2
$t_{rd1all}$	Read 1s All Blocks execution time	—	—	1.8	ms	
$t_{rdonce}$	Read Once execution time	—	—	25	$\mu$ s	1
$t_{pgmonce}$	Program Once execution time	—	65	—	$\mu$ s	
$t_{ersall}$	Erase All Blocks execution time	—	62	500	ms	2
$t_{vfykey}$	Verify Backdoor Access Key execution time	—	—	30	$\mu$ s	1

1. Assumes 25MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

**6.4.1.3 Flash high voltage current behaviors****Table 17. Flash high voltage current behaviors**

Symbol	Description	Min.	Typ.	Max.	Unit
$I_{DD\_PGM}$	Average current adder during high voltage flash programming operation	—	2.5	6.0	mA
$I_{DD\_ERS}$	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

**6.4.1.4 Reliability specifications****Table 18. NVM reliability specifications**

Symbol	Description	Min.	Typ. <sup>1</sup>	Max.	Unit	Notes
Program Flash						
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at  $-40^{\circ}\text{C} \leq T_j \leq 125^{\circ}\text{C}$ .

## 6.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

## 6.6 Analog

### 6.6.1 ADC electrical specifications

The 16-bit accuracy specifications listed in [Table 19](#) and [Table 20](#) are achievable on the differential pins ADCx\_DP0, ADCx\_DM0.

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

#### 6.6.1.1 16-bit ADC operating conditions

**Table 19. 16-bit ADC operating conditions**

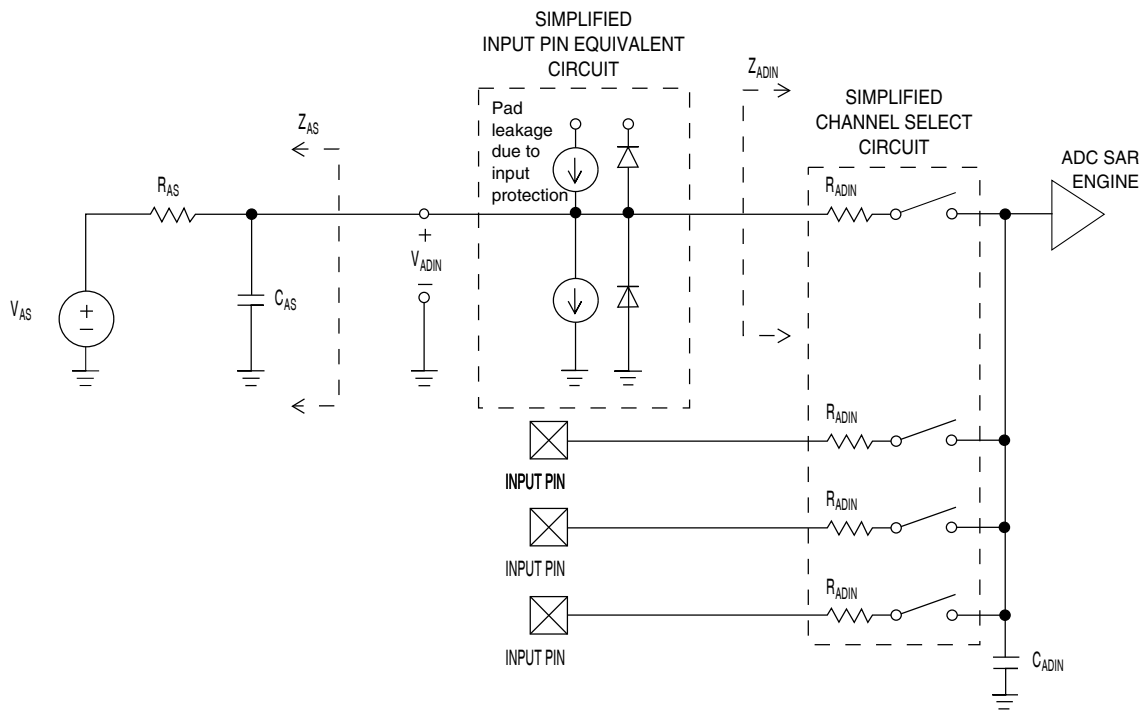
Symbol	Description	Conditions	Min.	Typ. <sup>1</sup>	Max.	Unit	Notes
V <sub>DDA</sub>	Supply voltage	Absolute	1.71	—	3.6	V	
ΔV <sub>DDA</sub>	Supply voltage	Delta to V <sub>DD</sub> (V <sub>DD</sub> -V <sub>DDA</sub> )	-100	0	+100	mV	2
ΔV <sub>SSA</sub>	Ground voltage	Delta to V <sub>SS</sub> (V <sub>SS</sub> - V <sub>SSA</sub> )	-100	0	+100	mV	2
V <sub>REFH</sub>	ADC reference voltage high		1.13	V <sub>DDA</sub>	V <sub>DDA</sub>	V	3
V <sub>REFL</sub>	ADC reference voltage low		V <sub>SSA</sub>	V <sub>SSA</sub>	V <sub>SSA</sub>	V	3
V <sub>ADIN</sub>	Input voltage		V <sub>REFL</sub>	—	V <sub>REFH</sub>	V	
C <sub>ADIN</sub>	Input capacitance	<ul style="list-style-type: none"> <li>16-bit mode</li> <li>8-/10-/12-bit modes</li> </ul>	—	8	10	pF	
R <sub>ADIN</sub>	Input resistance		—	2	5	kΩ	
R <sub>AS</sub>	Analog source resistance	13-/12-bit modes f <sub>ADCK</sub> < 4 MHz	—	—	5	kΩ	4
f <sub>ADCK</sub>	ADC conversion clock frequency	≤ 13/12-bit mode	1.0	—	18.0	MHz	5
f <sub>ADCK</sub>	ADC conversion clock frequency	16-bit mode	2.0	—	12.0	MHz	5
C <sub>rate</sub>	ADC conversion rate	≤ 13/12 bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20.000	—	818.330	Ksps	6

Table continues on the next page...

**Table 19. 16-bit ADC operating conditions (continued)**

Symbol	Description	Conditions	Min.	Typ. <sup>1</sup>	Max.	Unit	Notes
$C_{rate}$	ADC conversion rate	16-bit mode No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	37.037	—	461.467	Ksps	6

1. Typical values assume  $V_{DDA} = 3.0\text{ V}$ ,  $Temp = 25\text{ }^{\circ}\text{C}$ ,  $f_{ADCK} = 1.0\text{ MHz}$  unless otherwise stated. Typical values are for reference only and are not tested in production.
2. DC potential difference.
3. For packages without dedicated VREFH and VREFL pins,  $V_{REFH}$  is internally tied to  $V_{DDA}$ , and  $V_{REFL}$  is internally tied to  $V_{SSA}$ .
4. This resistance is external to MCU. The analog source resistance must be kept as low as possible to achieve the best results. The results in this data sheet were derived from a system which has  $< 8\ \Omega$  analog source resistance. The  $R_{AS}/C_{AS}$  time constant should be kept to  $< 1\text{ ns}$ .
5. To use the maximum ADC conversion clock frequency, the ADHSC bit must be set and the ADLPC bit must be clear.
6. For guidelines and examples of conversion rate calculation, download the [ADC calculator tool](#)



**Figure 6. ADC input impedance equivalency diagram**

### 6.6.1.2 16-bit ADC electrical characteristics

**Table 20. 16-bit ADC characteristics ( $V_{REFH} = V_{DDA}$ ,  $V_{REFL} = V_{SSA}$ )**

Symbol	Description	Conditions <sup>1</sup>	Min.	Typ. <sup>2</sup>	Max.	Unit	Notes
$I_{DDA\_ADC}$	Supply current		0.215	—	1.7	mA	3

Table continues on the next page...

**Table 20. 16-bit ADC characteristics ( $V_{REFH} = V_{DDA}$ ,  $V_{REFL} = V_{SSA}$ ) (continued)**

Symbol	Description	Conditions <sup>1</sup>	Min.	Typ. <sup>2</sup>	Max.	Unit	Notes
$f_{ADACK}$	ADC asynchronous clock source	• ADLPC = 1, ADHSC = 0	1.2	2.4	3.9	MHz	$t_{ADACK} = 1/f_{ADACK}$
		• ADLPC = 1, ADHSC = 1	2.4	4.0	6.1	MHz	
		• ADLPC = 0, ADHSC = 0	3.0	5.2	7.3	MHz	
		• ADLPC = 0, ADHSC = 1	4.4	6.2	9.5	MHz	
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	• 12-bit modes • <12-bit modes	— —	$\pm 4$ $\pm 1.4$	$\pm 6.8$ $\pm 2.1$	LSB <sup>4</sup>	5
DNL	Differential non-linearity	• 12-bit modes  • <12-bit modes	— —	$\pm 0.7$ $\pm 0.2$	-1.1 to +1.9 -0.3 to 0.5	LSB <sup>4</sup>	5
INL	Integral non-linearity	• 12-bit modes  • <12-bit modes	— —	$\pm 1.0$ $\pm 0.5$	-2.7 to +1.9 -0.7 to +0.5	LSB <sup>4</sup>	5
$E_{FS}$	Full-scale error	• 12-bit modes • <12-bit modes	— —	-4 -1.4	-5.4 -1.8	LSB <sup>4</sup>	$V_{ADIN} = V_{DDA}$ 5
$E_Q$	Quantization error	• 16-bit modes • $\leq 1312$ -bit modes	— —	-1 to 0 —	— $\pm 0.5$	LSB <sup>4</sup>	
ENOB	Effective number of bits	16-bit differential mode • Avg = 32 • Avg = 4  16-bit single-ended mode • Avg = 32 • Avg = 4	12.8 11.9  12.2 11.4	14.5 13.8  13.9 13.1	— —  — —	bits bits  bits bits	6
SINAD	Signal-to-noise plus distortion	See ENOB	$6.02 \times \text{ENOB} + 1.76$			dB	
THD	Total harmonic distortion	16-bit differential mode • Avg = 32	—	-94	—	dB	7
		16-bit single-ended mode • Avg = 32	—	-85	—	dB	
SFDR	Spurious free dynamic range	16-bit differential mode • Avg = 32	82	95	—	dB	7
		16-bit single-ended mode • Avg = 32	78	90	—	dB	

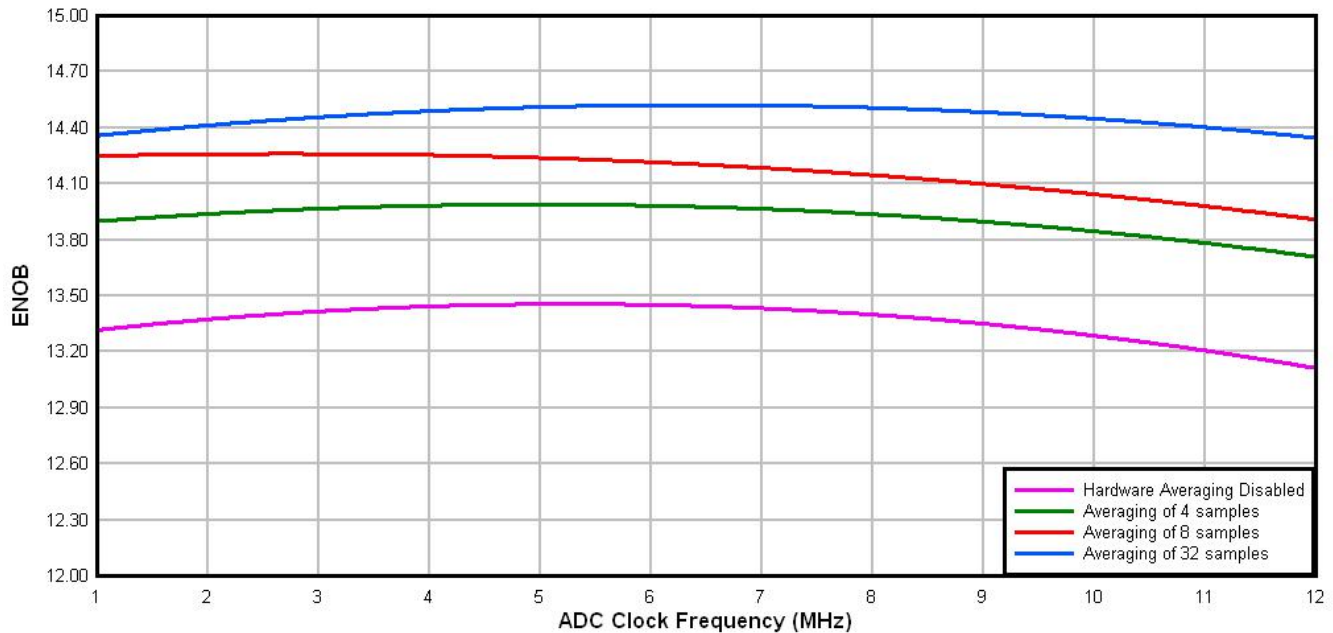
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**Table 20. 16-bit ADC characteristics ( $V_{REFH} = V_{DDA}$ ,  $V_{REFL} = V_{SSA}$ ) (continued)**

Symbol	Description	Conditions <sup>1</sup>	Min.	Typ. <sup>2</sup>	Max.	Unit	Notes
$E_{IL}$	Input leakage error			$I_{in} \times R_{AS}$		mV	$I_{in}$ = leakage current  (refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	Across the full temperature range of the device	—	1.715	—	mV/°C	
$V_{TEMP25}$	Temp sensor voltage	25 °C	—	719	—	mV	

1. All accuracy numbers assume the ADC is calibrated with  $V_{REFH} = V_{DDA}$
2. Typical values assume  $V_{DDA} = 3.0$  V, Temp = 25°C,  $f_{ADCK} = 2.0$  MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and the ADLPC bit (low power). For lowest power operation the ADLPC bit must be set, the HSC bit must be clear with 1 MHz ADC conversion clock speed.
4.  $1 \text{ LSB} = (V_{REFH} - V_{REFL})/2^N$
5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
6. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
7. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.

**Typical ADC 16-bit Differential ENOB vs ADC Clock  
100Hz, 90% FS Sine Input**



**Figure 7. Typical ENOB vs. ADC\_CLK for 16-bit differential mode**

Typical ADC 16-bit Single-Ended ENOB vs ADC Clock  
100Hz, 90% FS Sine Input

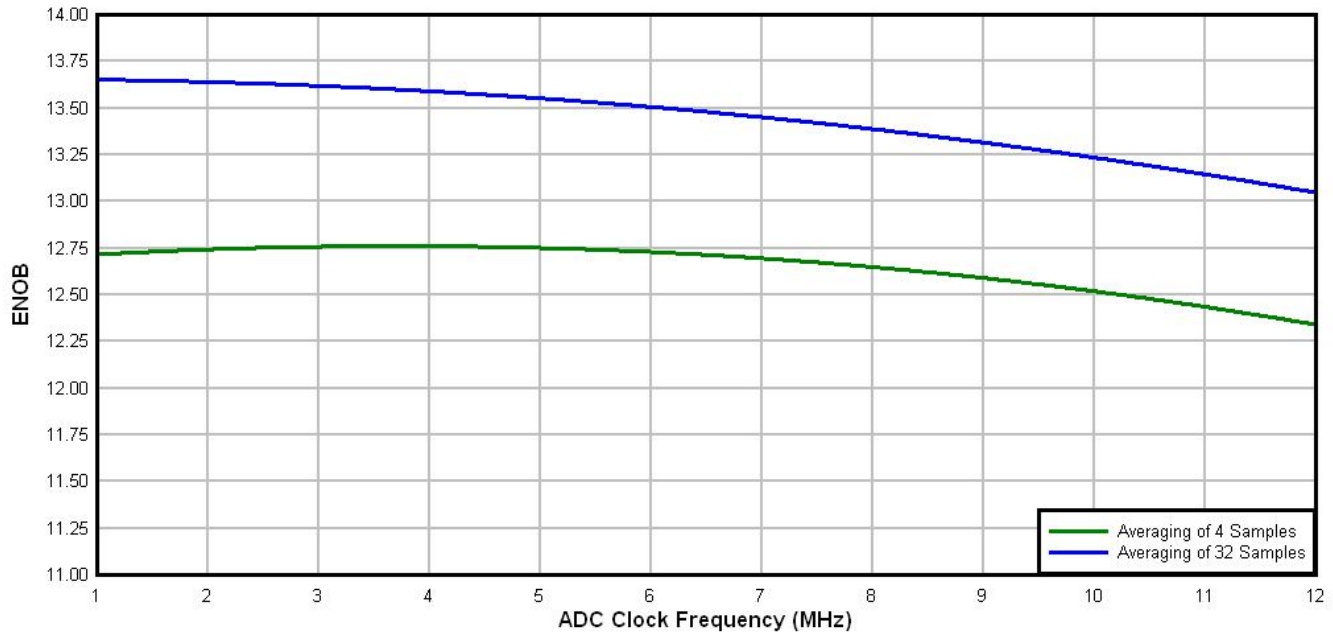


Figure 8. Typical ENOB vs. ADC\_CLK for 16-bit single-ended mode

## 6.6.2 CMP and 6-bit DAC electrical specifications

Table 21. Comparator and 6-bit DAC electrical specifications

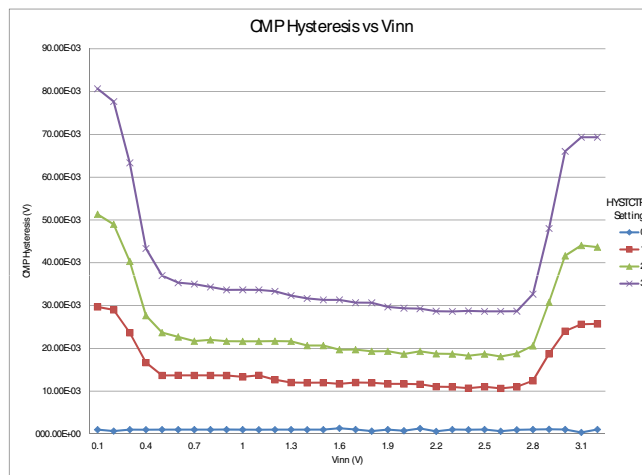
Symbol	Description	Min.	Typ.	Max.	Unit
$V_{DD}$	Supply voltage	1.71	—	3.6	V
$I_{DDHS}$	Supply current, high-speed mode (EN = 1, PMODE = 1)	—	—	200	$\mu$ A
$I_{DDL S}$	Supply current, low-speed mode (EN = 1, PMODE = 0)	—	—	20	$\mu$ A
$V_{AIN}$	Analog input voltage	$V_{SS}$	—	$V_{DD}$	V
$V_{AIO}$	Analog input offset voltage	—	—	20	mV
$V_H$	Analog comparator hysteresis <sup>1</sup> <ul style="list-style-type: none"> <li>• CR0[HYSTCTR] = 00</li> <li>• CR0[HYSTCTR] = 01</li> <li>• CR0[HYSTCTR] = 10</li> <li>• CR0[HYSTCTR] = 11</li> </ul>	—	5 10 20 30	—	mV
$V_{CMPOH}$	Output high	$V_{DD} - 0.5$	—	—	V
$V_{CMPOI}$	Output low	—	—	0.5	V
$t_{DHS}$	Propagation delay, high-speed mode (EN = 1, PMODE = 1)	20	50	200	ns
$t_{DLS}$	Propagation delay, low-speed mode (EN = 1, PMODE = 0)	80	250	600	ns

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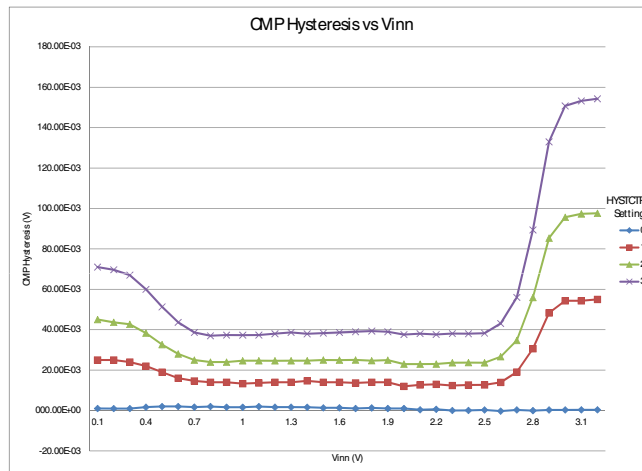
**Table 21. Comparator and 6-bit DAC electrical specifications (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit
	Analog comparator initialization delay <sup>2</sup>	—	—	40	μs
I <sub>DAC6b</sub>	6-bit DAC current adder (enabled)	—	7	—	μA
INL	6-bit DAC integral non-linearity	-0.5	—	0.5	LSB <sup>3</sup>
DNL	6-bit DAC differential non-linearity	-0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.7 to V<sub>DD</sub> - 0.7 V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
3. 1 LSB = V<sub>reference</sub>/64



**Figure 9. Typical hysteresis vs. Vin level (V<sub>DD</sub> = 3.3 V, PMODE = 0)**



**Figure 10. Typical hysteresis vs. Vin level (V<sub>DD</sub> = 3.3 V, PMODE = 1)**

### 6.6.3 12-bit DAC electrical characteristics



### 6.6.3.1 12-bit DAC operating requirements

Table 22. 12-bit DAC operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
$V_{DDA}$	Supply voltage	1.71	3.6	V	
$V_{DACR}$	Reference voltage	1.13	3.6	V	1
$T_A$	Temperature	Operating temperature range of the device		°C	
$C_L$	Output load capacitance	—	100	pF	2
$I_L$	Output load current	—	1	mA	

1. The DAC reference can be selected to be  $V_{DDA}$  or the voltage output of the VREF module (VREF\_OUT)
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC

### 6.6.3.2 12-bit DAC operating behaviors

Table 23. 12-bit DAC operating behaviors

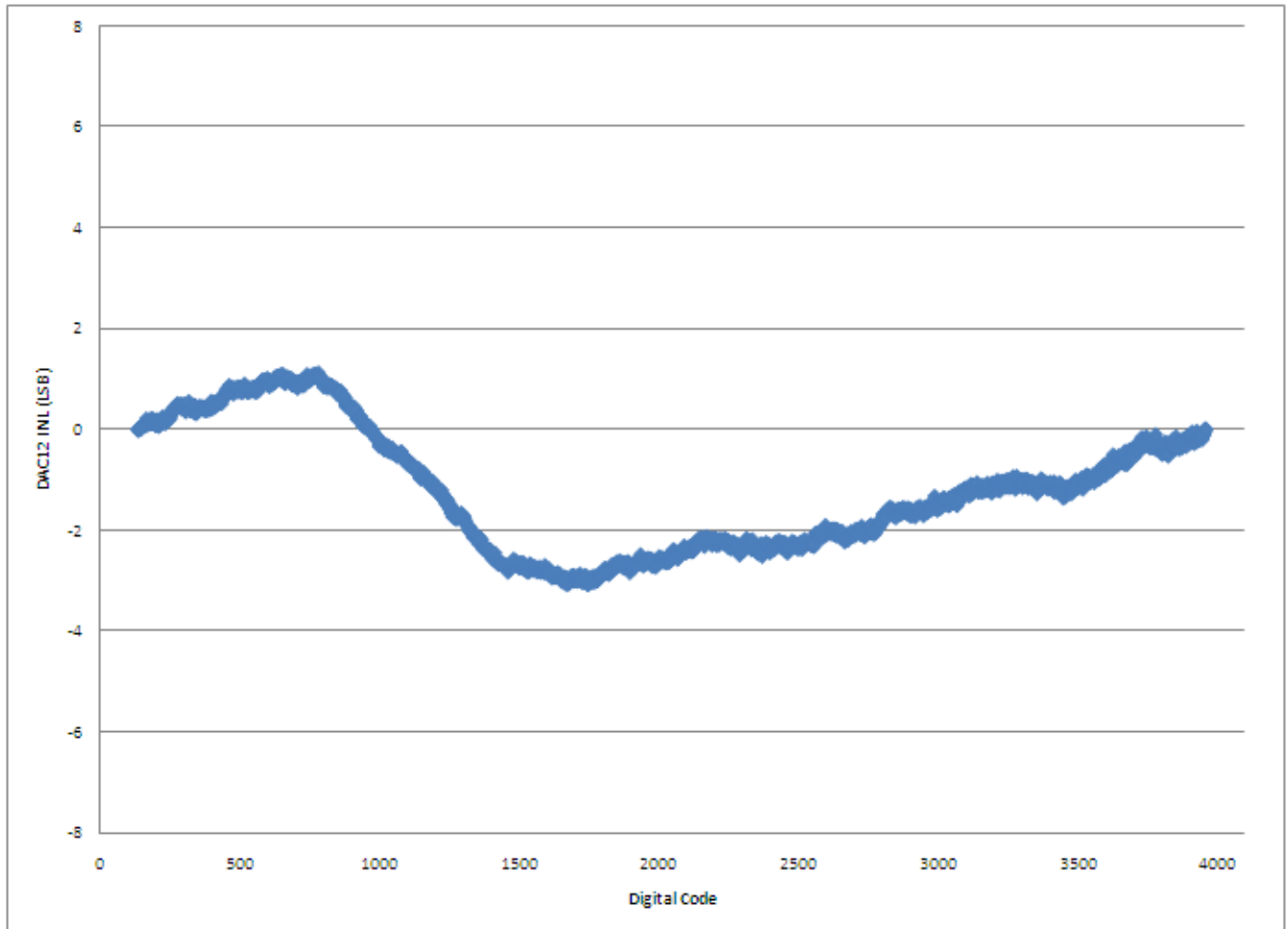
Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$I_{DDA\_DACLP}$	Supply current — low-power mode	—	—	250	μA	
$I_{DDA\_DACHP}$	Supply current — high-speed mode	—	—	900	μA	
$t_{DACLP}$	Full-scale settling time (0x080 to 0xF7F) — low-power mode	—	100	200	μs	1
$t_{DACHP}$	Full-scale settling time (0x080 to 0xF7F) — high-power mode	—	15	30	μs	1
$t_{CCDACLP}$	Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode	—	0.7	1	μs	1
$V_{dacoutl}$	DAC output voltage range low — high-speed mode, no load, DAC set to 0x000	—	—	100	mV	
$V_{dacouth}$	DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFF	$V_{DACR} - 100$	—	$V_{DACR}$	mV	
INL	Integral non-linearity error — high speed mode	—	—	±8	LSB	2
DNL	Differential non-linearity error — $V_{DACR} > 2$ V	—	—	±1	LSB	3
DNL	Differential non-linearity error — $V_{DACR} =$ VREF_OUT	—	—	±1	LSB	4
$V_{OFFSET}$	Offset error	—	±0.4	±0.8	%FSR	5
$E_G$	Gain error	—	±0.1	±0.6	%FSR	5
PSRR	Power supply rejection ratio, $V_{DDA} \geq 2.4$ V	60	—	90	dB	
$T_{CO}$	Temperature coefficient offset voltage	—	3.7	—	μV/C	6
$T_{GE}$	Temperature coefficient gain error	—	0.000421	—	%FSR/C	
Rop	Output resistance load = 3 kΩ	—	—	250	Ω	

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**Table 23. 12-bit DAC operating behaviors (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
SR	Slew rate -80h→ F7Fh→ 80h <ul style="list-style-type: none"> <li>• High power (SP<sub>HP</sub>)</li> <li>• Low power (SP<sub>LP</sub>)</li> </ul>	1.2 0.05	1.7 0.12	— —	V/μs	
BW	3dB bandwidth <ul style="list-style-type: none"> <li>• High power (SP<sub>HP</sub>)</li> <li>• Low power (SP<sub>LP</sub>)</li> </ul>	550 40	— —	— —	kHz	

1. Settling within ±1 LSB
2. The INL is measured for 0 + 100 mV to V<sub>DACR</sub> -100 mV
3. The DNL is measured for 0 + 100 mV to V<sub>DACR</sub> -100 mV
4. The DNL is measured for 0 + 100 mV to V<sub>DACR</sub> -100 mV with V<sub>DDA</sub> > 2.4 V
5. Calculated by a best fit curve from V<sub>SS</sub> + 100 mV to V<sub>DACR</sub> - 100 mV
6. V<sub>DDA</sub> = 3.0 V, reference select set for V<sub>DDA</sub> (DACx\_CO:DACRFS = 1), high power mode (DACx\_C0:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device



**Figure 11. Typical INL error vs. digital code**

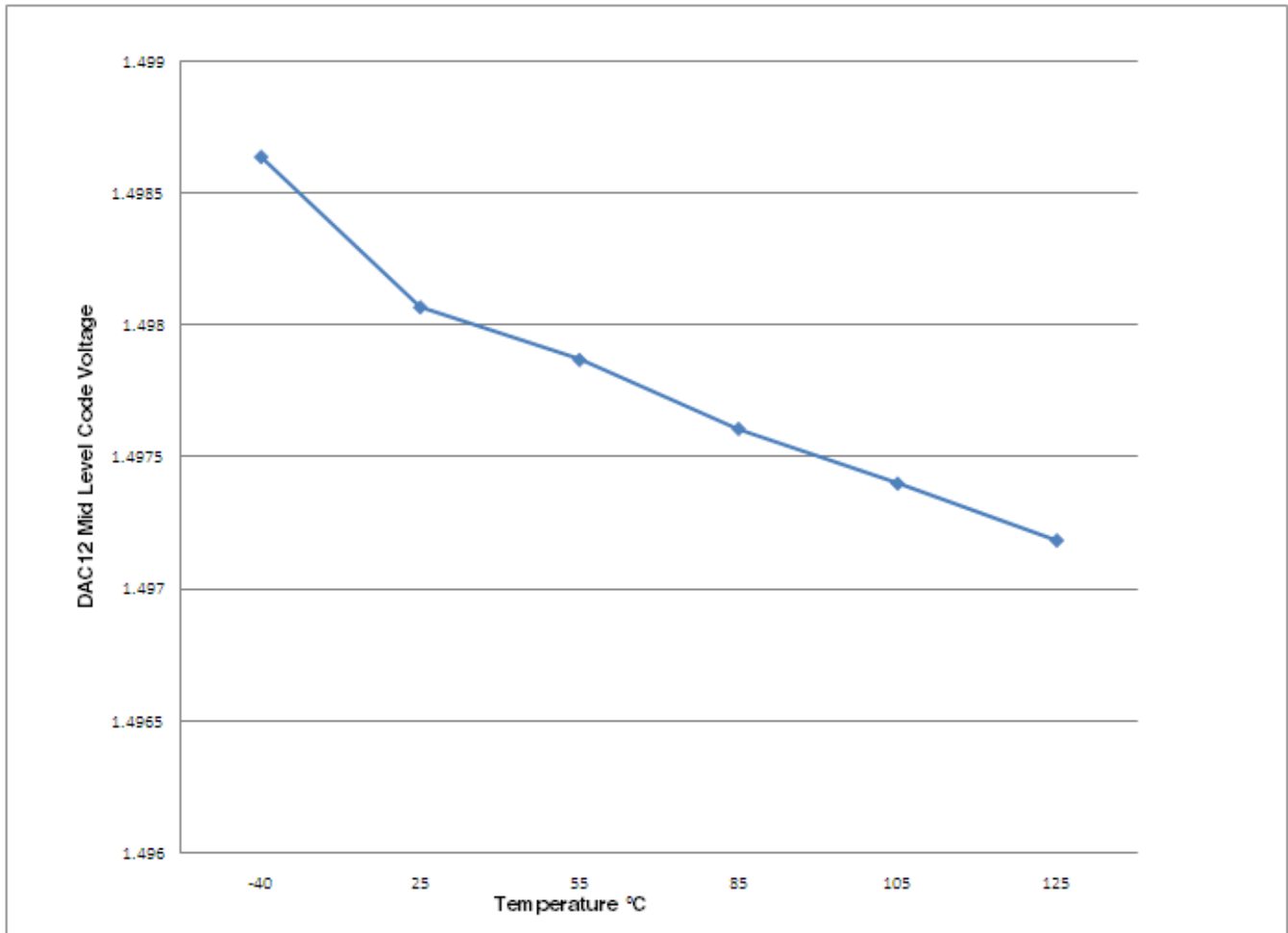


Figure 12. Offset at half scale vs. temperature

## 6.7 Timers

See General switching specifications.

## 6.8 Communication interfaces

### 6.8.1 SPI switching specifications

The Serial Peripheral Interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. See the SPI chapter of the chip's Reference Manual for information about the modified transfer formats used for communicating with slower peripheral devices.

## Peripheral operating requirements and behaviors

All timing is shown with respect to 20%  $V_{DD}$  and 80%  $V_{DD}$  thresholds, unless noted, as well as input signal transitions of 3 ns and a 30 pF maximum load on all SPI pins.

**Table 24. SPI master mode timing on slew rate disabled pads**

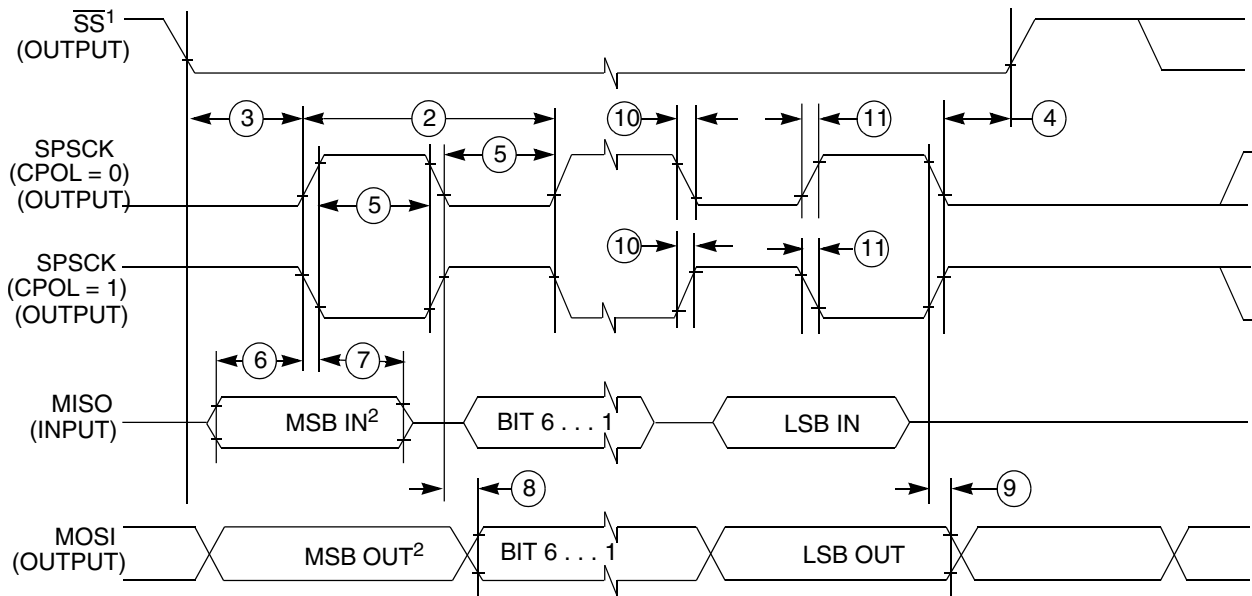
Num.	Symbol	Description	Min.	Max.	Unit	Note
1	$f_{op}$	Frequency of operation	$f_{periph}/2048$	$f_{periph}/2$	Hz	1
2	$t_{SPSCK}$	SPSCK period	$2 \times t_{periph}$	$2048 \times t_{periph}$	ns	2
3	$t_{Lead}$	Enable lead time	1/2	—	$t_{SPSCK}$	—
4	$t_{Lag}$	Enable lag time	1/2	—	$t_{SPSCK}$	—
5	$t_{WSPSCK}$	Clock (SPSCK) high or low time	$t_{periph} - 30$	$1024 \times t_{periph}$	ns	—
6	$t_{SU}$	Data setup time (inputs)	16	—	ns	—
7	$t_{HI}$	Data hold time (inputs)	0	—	ns	—
8	$t_v$	Data valid (after SPSCK edge)	—	10	ns	—
9	$t_{HO}$	Data hold time (outputs)	0	—	ns	—
10	$t_{RI}$	Rise time input	—	$t_{periph} - 25$	ns	—
	$t_{FI}$	Fall time input				
11	$t_{RO}$	Rise time output	—	25	ns	—
	$t_{FO}$	Fall time output				

1. For SPI0  $f_{periph}$  is the bus clock ( $f_{BUS}$ ). For SPI1  $f_{periph}$  is the system clock ( $f_{SYS}$ ).
2.  $t_{periph} = 1/f_{periph}$

**Table 25. SPI master mode timing on slew rate enabled pads**

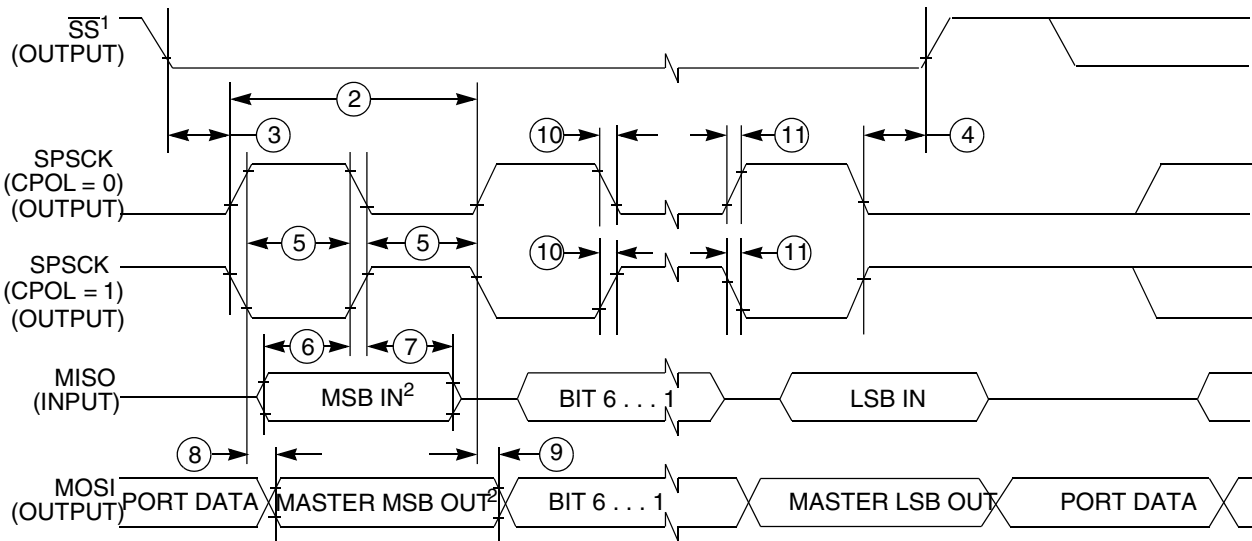
Num.	Symbol	Description	Min.	Max.	Unit	Note
1	$f_{op}$	Frequency of operation	$f_{periph}/2048$	$f_{periph}/2$	Hz	1
2	$t_{SPSCK}$	SPSCK period	$2 \times t_{periph}$	$2048 \times t_{periph}$	ns	2
3	$t_{Lead}$	Enable lead time	1/2	—	$t_{SPSCK}$	—
4	$t_{Lag}$	Enable lag time	1/2	—	$t_{SPSCK}$	—
5	$t_{WSPSCK}$	Clock (SPSCK) high or low time	$t_{periph} - 30$	$1024 \times t_{periph}$	ns	—
6	$t_{SU}$	Data setup time (inputs)	96	—	ns	—
7	$t_{HI}$	Data hold time (inputs)	0	—	ns	—
8	$t_v$	Data valid (after SPSCK edge)	—	52	ns	—
9	$t_{HO}$	Data hold time (outputs)	0	—	ns	—
10	$t_{RI}$	Rise time input	—	$t_{periph} - 25$	ns	—
	$t_{FI}$	Fall time input				
11	$t_{RO}$	Rise time output	—	36	ns	—
	$t_{FO}$	Fall time output				

1. For SPI0  $f_{periph}$  is the bus clock ( $f_{BUS}$ ). For SPI1  $f_{periph}$  is the system clock ( $f_{SYS}$ ).
2.  $t_{periph} = 1/f_{periph}$



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

**Figure 13. SPI master mode timing (CPHA = 0)**



1. If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

**Figure 14. SPI master mode timing (CPHA = 1)**

**Table 26. SPI slave mode timing on slew rate disabled pads**

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	$f_{op}$	Frequency of operation	0	$f_{periph}/4$	Hz	1
2	$t_{SPSCCK}$	SPSCCK period	$4 \times t_{periph}$	—	ns	2
3	$t_{Lead}$	Enable lead time	1	—	$t_{periph}$	—
4	$t_{Lag}$	Enable lag time	1	—	$t_{periph}$	—
5	$t_{WSPSCCK}$	Clock (SPSCCK) high or low time	$t_{periph} - 30$	—	ns	—

Table continues on the next page...

**Table 26. SPI slave mode timing on slew rate disabled pads (continued)**

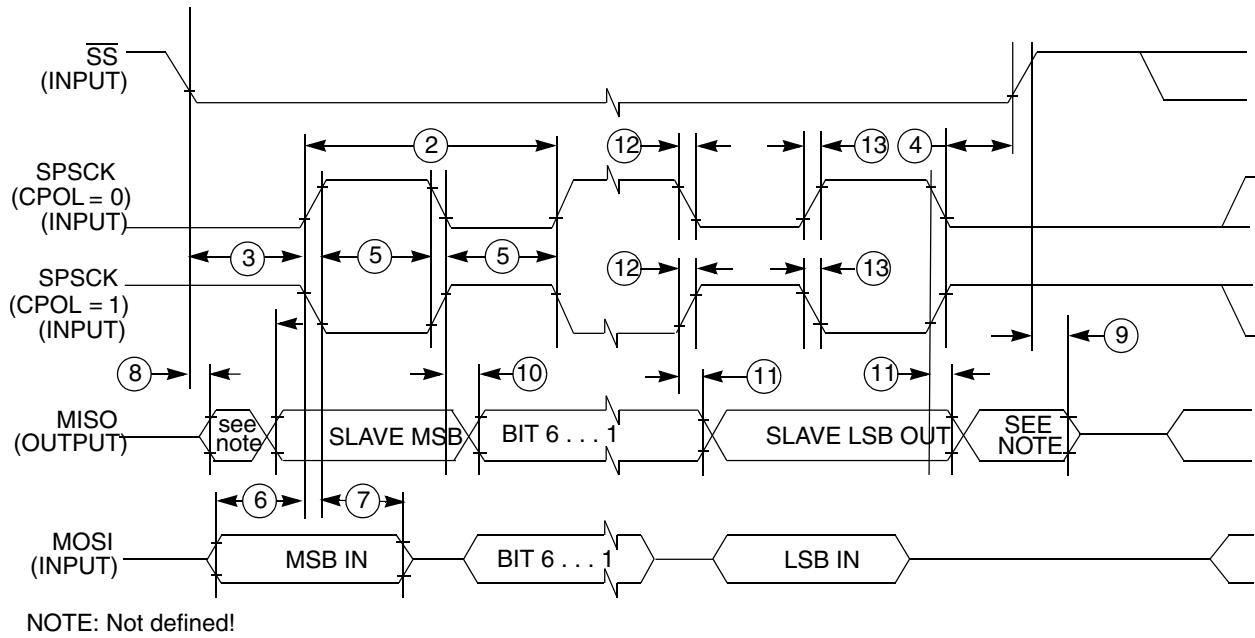
Num.	Symbol	Description	Min.	Max.	Unit	Note
6	$t_{SU}$	Data setup time (inputs)	2	—	ns	—
7	$t_{HI}$	Data hold time (inputs)	7	—	ns	—
8	$t_a$	Slave access time	—	$t_{periph}$	ns	3
9	$t_{dis}$	Slave MISO disable time	—	$t_{periph}$	ns	4
10	$t_v$	Data valid (after SPSCCK edge)	—	22	ns	—
11	$t_{HO}$	Data hold time (outputs)	0	—	ns	—
12	$t_{RI}$	Rise time input	—	$t_{periph} - 25$	ns	—
	$t_{FI}$	Fall time input				
13	$t_{RO}$	Rise time output	—	25	ns	—
	$t_{FO}$	Fall time output				

1. For SPI0  $f_{periph}$  is the bus clock ( $f_{BUS}$ ). For SPI1  $f_{periph}$  is the system clock ( $f_{SYS}$ ).
2.  $t_{periph} = 1/f_{periph}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state

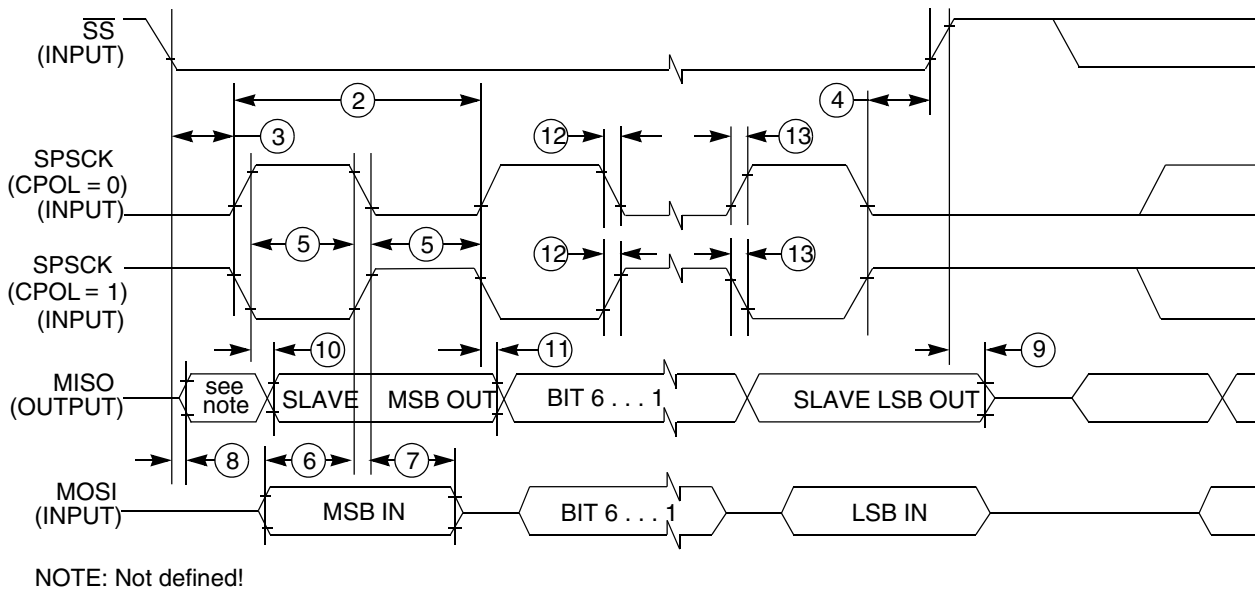
**Table 27. SPI slave mode timing on slew rate enabled pads**

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	$f_{op}$	Frequency of operation	0	$f_{periph}/4$	Hz	1
2	$t_{SPSCCK}$	SPSCCK period	$4 \times t_{periph}$	—	ns	2
3	$t_{Lead}$	Enable lead time	1	—	$t_{periph}$	—
4	$t_{Lag}$	Enable lag time	1	—	$t_{periph}$	—
5	$t_{WSPSCCK}$	Clock (SPSCCK) high or low time	$t_{periph} - 30$	—	ns	—
6	$t_{SU}$	Data setup time (inputs)	2	—	ns	—
7	$t_{HI}$	Data hold time (inputs)	7	—	ns	—
8	$t_a$	Slave access time	—	$t_{periph}$	ns	3
9	$t_{dis}$	Slave MISO disable time	—	$t_{periph}$	ns	4
10	$t_v$	Data valid (after SPSCCK edge)	—	122	ns	—
11	$t_{HO}$	Data hold time (outputs)	0	—	ns	—
12	$t_{RI}$	Rise time input	—	$t_{periph} - 25$	ns	—
	$t_{FI}$	Fall time input				
13	$t_{RO}$	Rise time output	—	36	ns	—
	$t_{FO}$	Fall time output				

1. For SPI0  $f_{periph}$  is the bus clock ( $f_{BUS}$ ). For SPI1  $f_{periph}$  is the system clock ( $f_{SYS}$ ).
2.  $t_{periph} = 1/f_{periph}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state



**Figure 15. SPI slave mode timing (CPHA = 0)**



**Figure 16. SPI slave mode timing (CPHA = 1)**

## 6.8.2 I<sup>2</sup>C

See General switching specifications.

## 6.8.3 UART

See General switching specifications.

## 6.9 Human-machine interfaces (HMI)

### 6.9.1 TSI electrical specifications

**Table 28. TSI electrical specifications**

Symbol	Description	Min.	Type	Max	Unit
TSI_RUNF	Fixed power consumption in run mode	—	100	—	μA
TSI_RUNV	Variable power consumption in run mode (depends on oscillator's current selection)	1.0	—	128	μA
TSI_EN	Power consumption in enable mode	—	100	—	μA
TSI_DIS	Power consumption in disable mode	—	1.2	—	μA
TSI_TEN	TSI analog enable time	—	66	—	μs
TSI_CREF	TSI reference capacitor	—	1.0	—	pF
TSI_DVOLT	Voltage variation of VP & VM around nominal values	0.19	—	1.03	V



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