



PSMN075-100MSE

N-channel 100 V 71 mΩ standard level MOSFET in LFPAK33 designed specifically for PoE applications

26 March 2013

Product data sheet

1. General description

New standards and proprietary approaches are enabling the next generation of Power-over-Ethernet (PoE) systems capable of delivering up to 100W to each powered device (PD). Large screen LCD displays, 3G / 4G / Wi-Fi hot-spots and pan-tilt-zoom CCTV cameras, for example, are placing increased demands on the power sourcing equipment (PSE) in terms of “soft-start” procedures, resilience to short-circuits, thermal management and power density. Part of NXP’s “NextPower Live” MOSFET portfolio, the PSMN075-100MSE has been designed specifically to compliment the latest PoE controllers, offering both superior linear mode operation and very low $R_{DS(on)}$ in a cost-effective, industry compatible, LFPAK33 package.

2. Features and benefits

- Enhanced forward biased safe operating area for superior linear mode operation
- Low $R_{DS(on)}$ for low conduction losses
- Ultra reliable LFPAK33 package – no glue, no wires, 175°C
- Very low I_{DSS}

3. Applications

- IEEE802.3at and proprietary solutions - (type 2)
- Suitable for PoE applications upto 30W
- Use PSMN040-100MSE for higher power requirements

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	-	100	V
I_D	drain current	$T_j = 25\text{ °C}; V_{GS} = 10\text{ V}; \text{Fig. 1}$	-	-	18	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}; \text{Fig. 2}$	-	-	65	W
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 5\text{ A}; T_j = 25\text{ °C}; \text{Fig. 12}$	-	57	71	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 10\text{ V}; I_D = 5\text{ A}; V_{DS} = 50\text{ V}; T_j = 25\text{ °C}; \text{Fig. 14}; \text{Fig. 15}$	-	5.3	-	nC

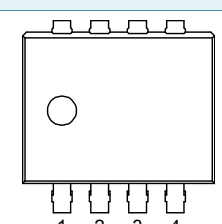
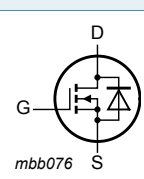


N-channel 100 V 71 mΩ standard level MOSFET in LFAK33 designed specifically for PoE applications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$Q_{G(tot)}$	total gate charge	$V_{GS} = 10\text{ V}$; $I_D = 5\text{ A}$; $V_{DS} = 50\text{ V}$; $T_j = 25\text{ °C}$; Fig. 14 ; Fig. 15	-	16.4	-	nC
Avalanche Ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; $I_D = 18\text{ A}$; $V_{sup} \leq 100\text{ V}$; $R_{GS} = 50\text{ }\Omega$; unclamped; Fig. 3	-	-	25	mJ

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>LFAK33 (SOT1210)</p>	
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN075-100MSE	LFAK33	Plastic single ended surface mounted package (LFAK33); 4 leads	SOT1210

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN075-100MSE	M75E10

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	100	V
V_{DGR}	drain-gate voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	100	V

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Symbol	Parameter	Conditions	Min	Max	Unit
V _{GS}	gate-source voltage		-20	20	V
I _D	drain current	V _{GS} = 10 V; T _j = 25 °C; Fig. 1	-	18	A
		V _{GS} = 10 V; T _{mb} = 100 °C; Fig. 1	-	13	A
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; Fig. 4	-	74	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 2	-	65	W
T _{stg}	storage temperature		-55	175	°C
T _j	junction temperature		-55	175	°C
T _{slid(M)}	peak soldering temperature		-	260	°C
Source-drain diode					
I _S	source current	T _{mb} = 25 °C	-	54	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C	-	74	A
Avalanche Ruggedness					
E _{D(S(AL)S)}	non-repetitive drain-source avalanche energy	V _{GS} = 10 V; T _{j(init)} = 25 °C; I _D = 18 A; V _{sup} ≤ 100 V; R _{GS} = 50 Ω; unclamped; Fig. 3	-	25	mJ

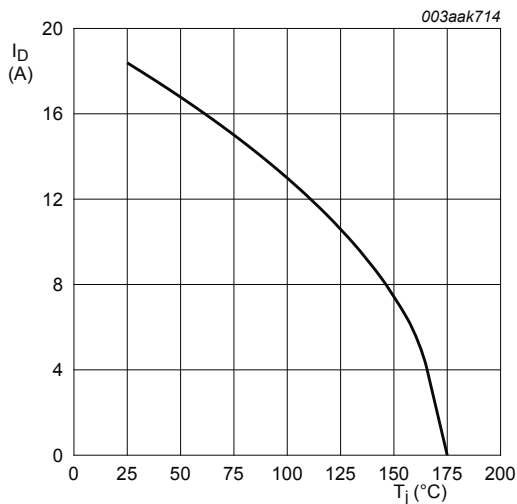


Fig. 1. Continuous drain current as a function of mounting base temperature

$$V_{GS} \geq 10V$$

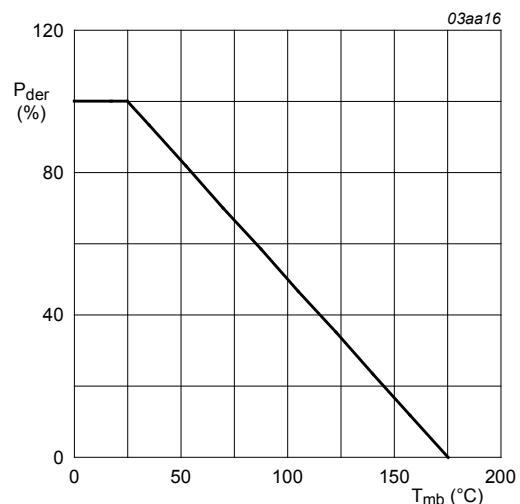


Fig. 2. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

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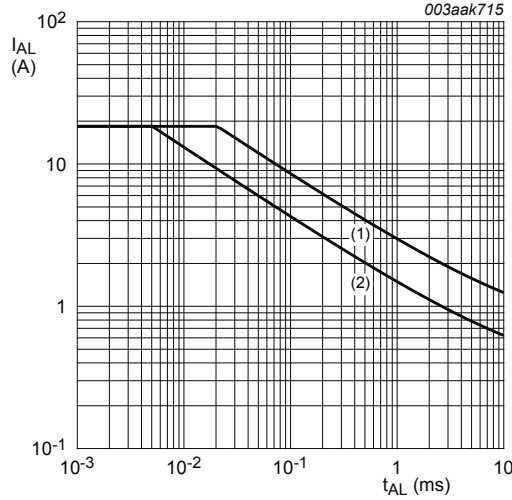


Fig. 3. Single pulse avalanche rating; avalanche current as a function of avalanche time

(1) $T_{j (init)} = 25^{\circ}C$; (2) $T_{j (init)} = 100^{\circ}C$

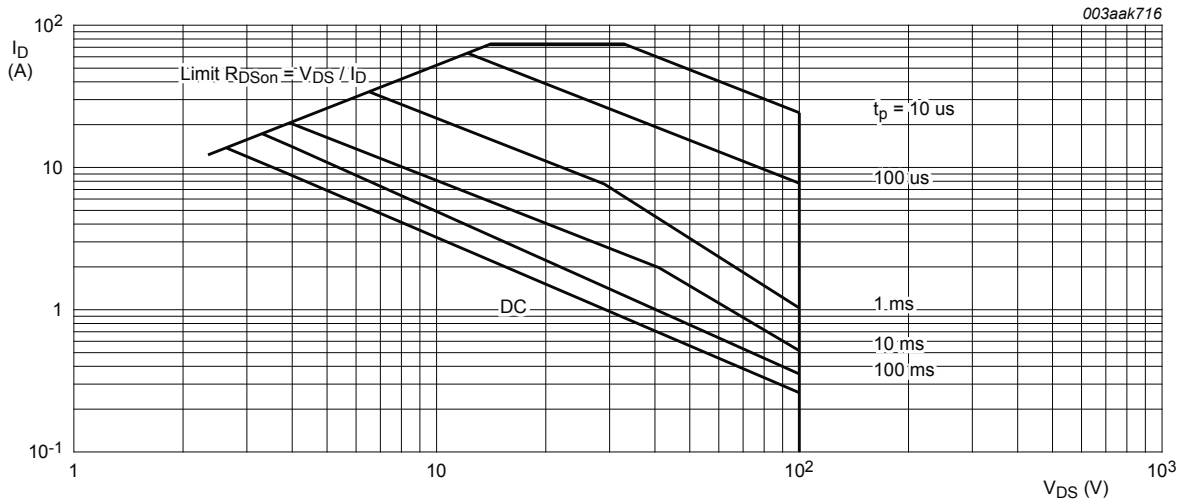


Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25^{\circ}C$; I_{DM} is a single pulse

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	2.09	2.32	K/W

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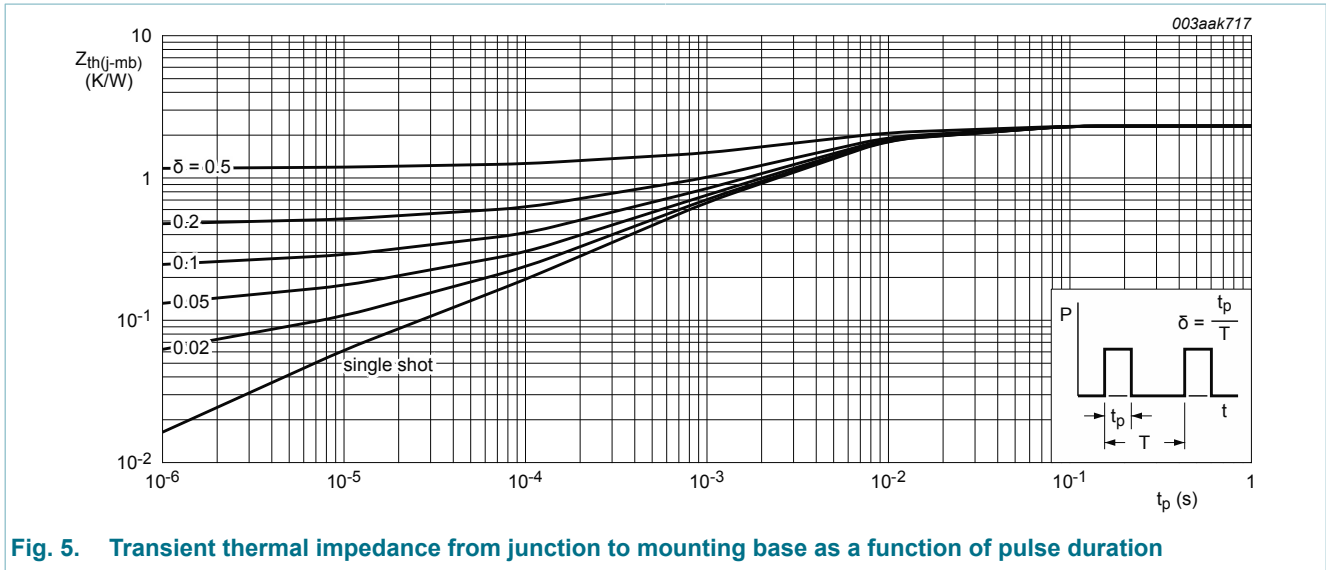


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	100	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	90	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C;$ Fig. 10; Fig. 11	2.3	3.3	4	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C;$ Fig. 10	1	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C;$ Fig. 10	-	-	4.6	V
I_{DSS}	drain leakage current	$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.01	1	μA
		$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ C$	-	-	500	μA
I_{GSS}	gate leakage current	$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	10	100	nA
		$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	10	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ }^\circ C;$ Fig. 12	-	57	71	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 5 \text{ A}; T_j = 100 \text{ }^\circ C;$ Fig. 13; Fig. 12	-	-	128	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 5 \text{ A}; T_j = 175 \text{ }^\circ C;$ Fig. 13; Fig. 12	-	-	192	mΩ
R_G	gate resistance	$f = 10 \text{ MHz}$	-	1.55	-	Ω

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 5 A; V _{DS} = 50 V; V _{GS} = 10 V; T _J = 25 °C; Fig. 14 ; Fig. 15	-	16.4	-	nC
		I _D = 0 A; V _{DS} = 0 V; V _{GS} = 10 V; T _J = 25 °C	-	12.9	-	nC
Q _{GS}	gate-source charge	I _D = 5 A; V _{DS} = 50 V; V _{GS} = 10 V; T _J = 25 °C; Fig. 14 ; Fig. 15	-	3.1	-	nC
Q _{GS(th)}	pre-threshold gate-source charge		-	2.1	-	nC
Q _{GS(th-pl)}	post-threshold gate-source charge		-	1	-	nC
Q _{GD}	gate-drain charge	I _D = 5 A; V _{DS} = 50 V; V _{GS} = 10 V; T _J = 25 °C; Fig. 14 ; Fig. 15	-	5.3	-	nC
V _{GS(pl)}	gate-source plateau voltage	I _D = 5 A; V _{DS} = 50 V; T _J = 25 °C; Fig. 14 ; Fig. 15	-	4.3	-	V
C _{iss}	input capacitance	V _{DS} = 50 V; V _{GS} = 0 V; f = 1 MHz; T _J = 25 °C; Fig. 16	-	773	-	pF
C _{oss}	output capacitance		-	66	-	pF
C _{rss}	reverse transfer capacitance		-	48	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = 50 V; R _L = 10 Ω; V _{GS} = 10 V; R _{G(ext)} = 5 Ω; T _J = 25 °C	-	5.5	-	ns
t _r	rise time		-	5.8	-	ns
t _{d(off)}	turn-off delay time		-	12.4	-	ns
t _f	fall time		-	6.2	-	ns
Source-drain diode						
V _{SD}	source-drain voltage	I _S = 15 A; V _{GS} = 0 V; T _J = 25 °C; Fig. 17	-	0.89	1.2	V
t _{rr}	reverse recovery time	I _S = 5 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V;	-	35.8	-	ns
Q _r	recovered charge	V _{DS} = 50 V; T _J = 25 °C	-	50.7	-	nC

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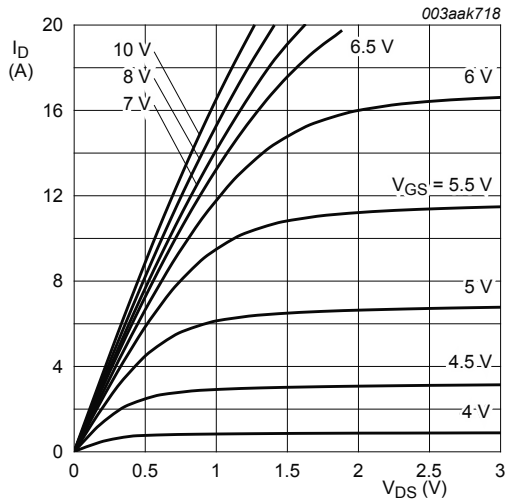


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

$T_j = 25^\circ C$

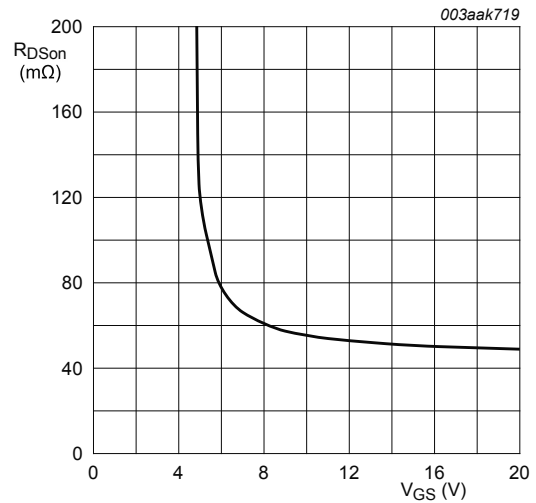


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25^\circ C; I_D = 5 A$

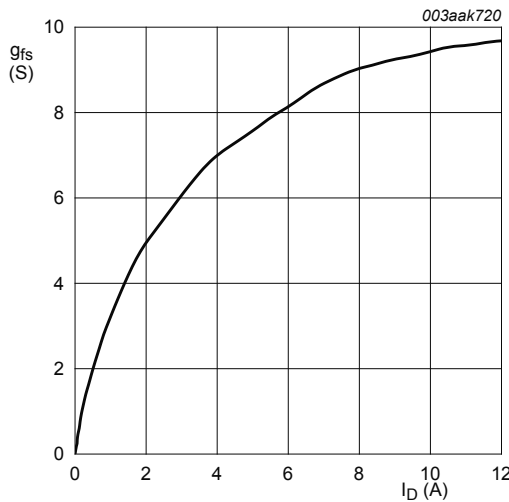


Fig. 8. Forward transconductance as a function of drain current; typical values

$T_j = 25^\circ C; V_{DS} = 10 V$

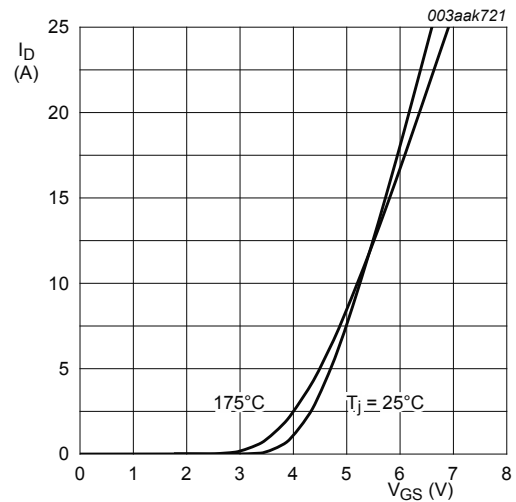


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

$V_{DS} = 10 V$

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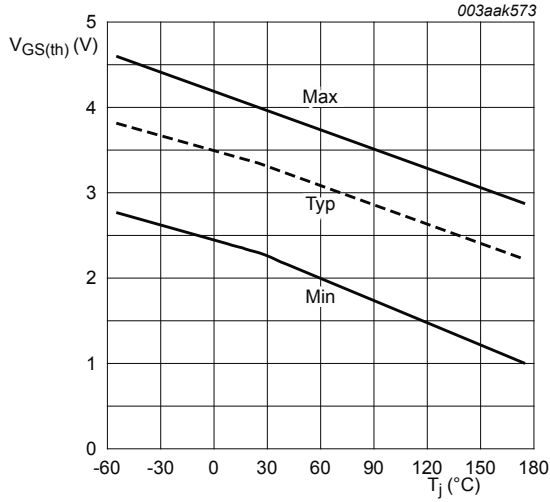


Fig. 10. Gate-source threshold voltage as a function of junction temperature

$$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$$

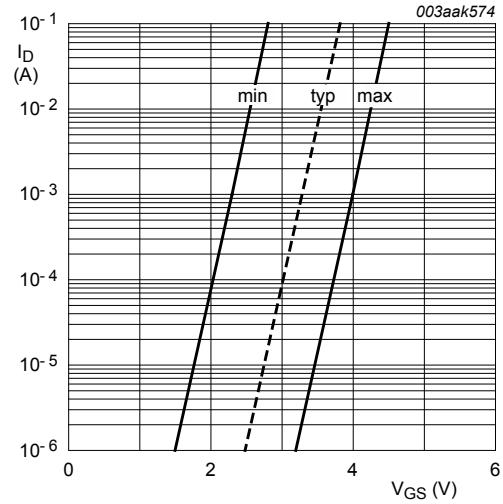


Fig. 11. Sub-threshold drain current as a function of gate-source voltage

$$T_j = 25^\circ\text{C}; V_{DS} = 5 \text{ V}$$

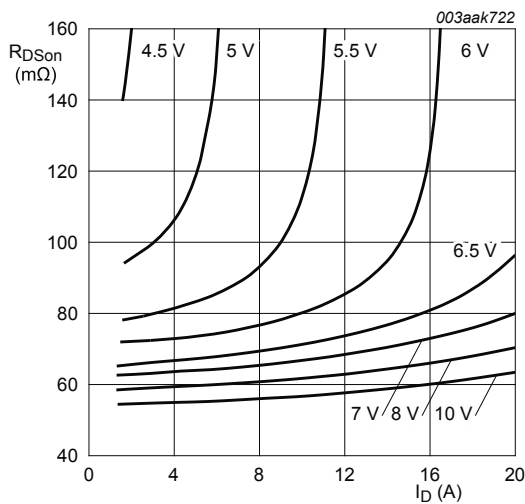


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

$$T_j = 25^\circ\text{C}$$

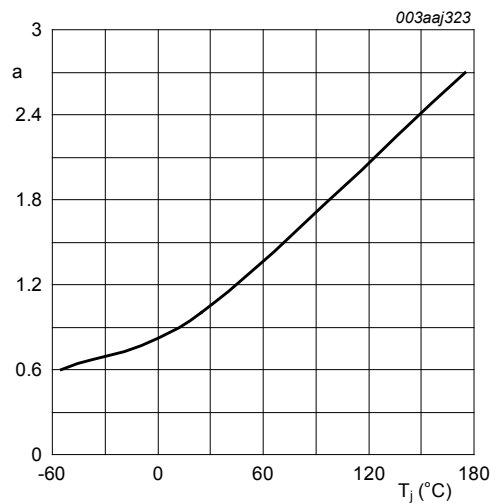


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

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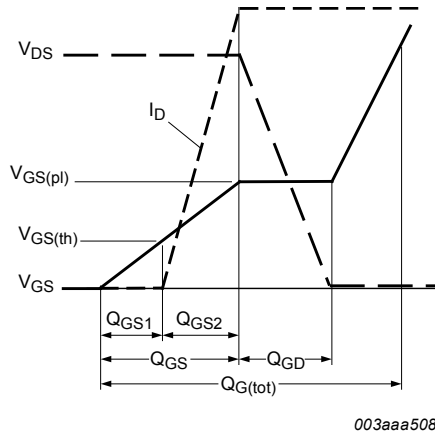


Fig. 14. Gate charge waveform definitions

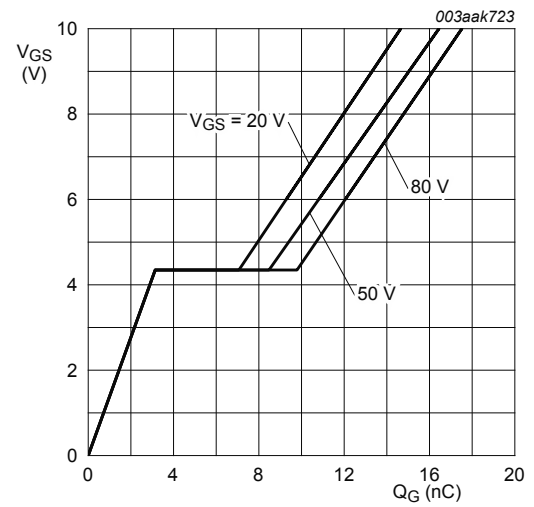


Fig. 15. Gate-source voltage as a function of gate charge; typical values

$T_j = 25^\circ C; I_D = 5A$

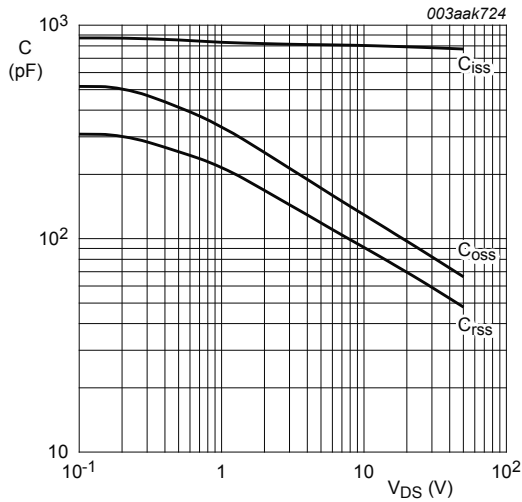


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0V; f = 1MHz$

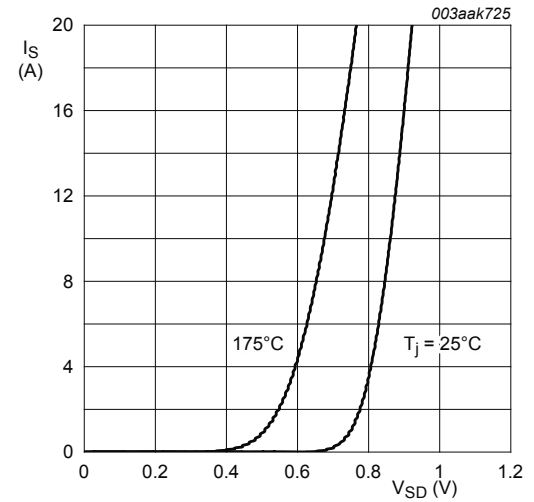


Fig. 17. Source current as a function of source-drain voltage; typical values

$V_{GS} = 0V$

11. Package outline

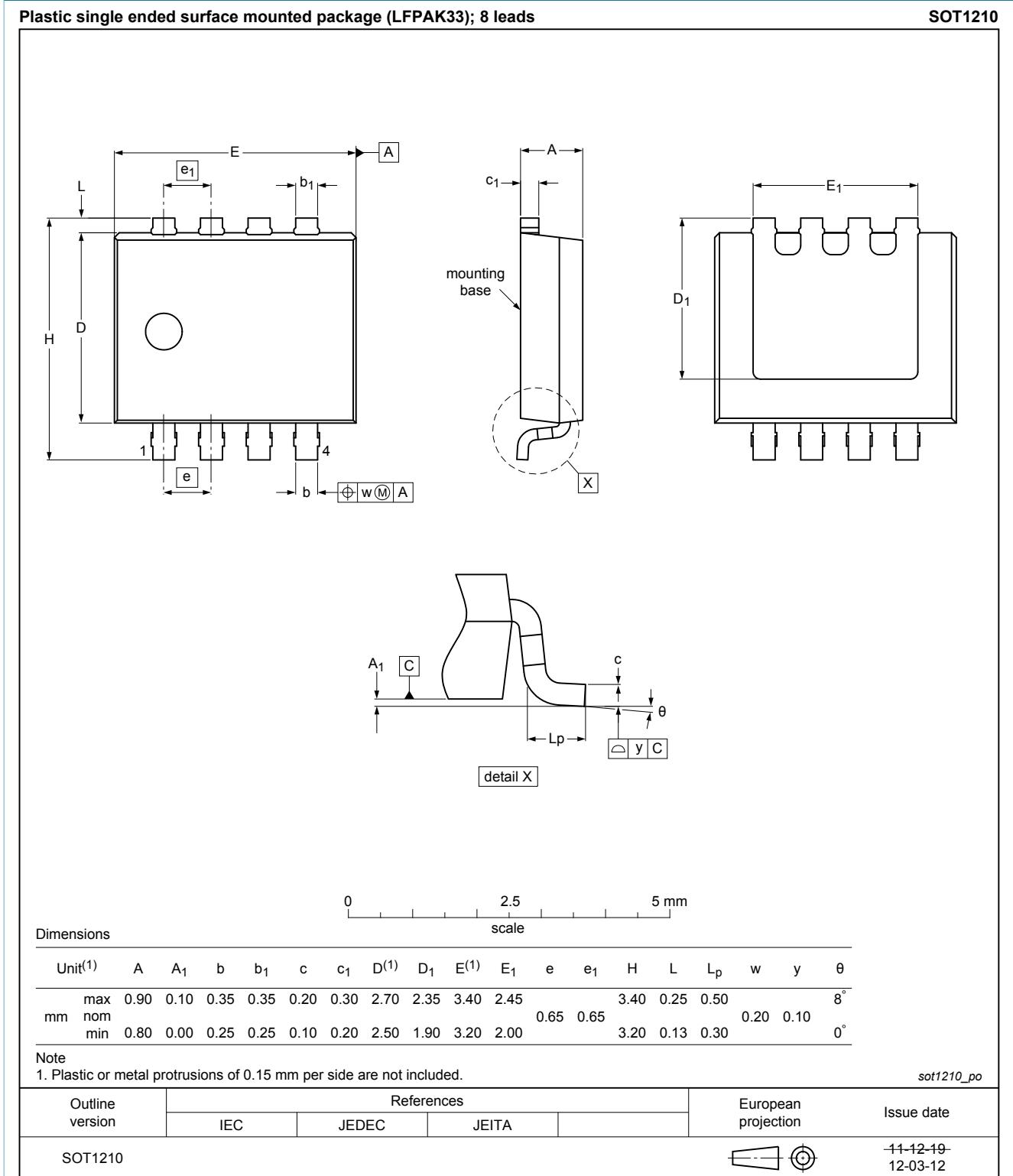


Fig. 18. Package outline LFAK33 (SOT1210)

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12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
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