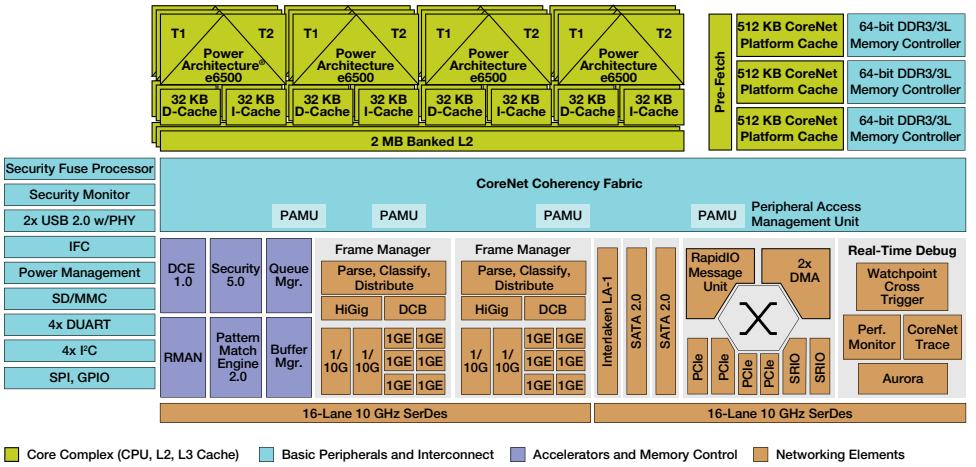
QorIQ Communications Platforms

QorIQ T Series T4240/T4160 Processors

Overview

The first products in the QorIQ T series are the T4240 (12 physical cores and 24 virtual cores) and the T4160 (eight physical, 16 virtual cores). With frequencies scaling up to 1.8 GHz, large caches, hardware acceleration and modern system peripherals, these products target applications that benefit from consolidation of control and data plane processing in a single SoC.

QorIQ T4240 Communications Processor



Target Markets and Applications

The T4240 is ideal for combined control and data plane processing. A wide variety of applications can benefit from the processing, I/O integration and power management offered by T4240. Like other QorIQ devices, the T4240's high level of integration offers significant space, weight and power benefits compared to multiple discrete devices.

- Service provider networking: RNC, metro networking, gateway, core/edge router
- Enterprise equipment: Router, switch services, UTM
- Data centers: ADC, WOC, UTM, proxy, server appliance
- Storage controllers: FCoE bridging, iSCSI controller, SAN controller
- Aerospace, defense and government: Radar imaging, ruggedized network appliance
- Industrial computing: Single board computers

T4240 vs. T4160 Comparison Chart

	T4240	T4160
Cores	12	8
Core clusters	3	2
DDR memory controllers	3	2
SerDes lanes	32	24
10 GbE MAC	4	2

e6500 Core

The T4240 is based on the new Power Architecture® e6500 core. The e6500 uses a seven-stage pipeline for low latency response to unpredictable code execution paths, boosting single threaded performance. The e6500 also offers higher aggregate instructions per clock at lower power with an innovative "fused core" approach to threading. The e6500's fully resourced dual threads provide 1.7 times the performance of a single thread.

The e6500 cores are clustered in banks of four cores sharing a 2 MB L2 cache, allowing efficient sharing of code and data within a multicore cluster. Each e6500 core implements the Freescale AltiVec technology SIMD engine, dramatically boosting the performance of media and networking algorithms, offering native inline programming and using less power than a separate DSP. Features include:

- Up to 1.8 GHz dual threaded operation
- 6.0 DMIPS/MHz per core
- Advanced power saving modes including state retention power gating

Virtualization

The T4240 includes support for hardware-assisted virtualization. The e6500 offers an extra core privilege level (hypervisor) and hardware offload of logical to real address translation. In addition, the T4240 includes platform-level enhancements supporting I/O virtualization with DMA memory protection through IOMMUs and configurable "storage profiles," which provide isolation of I/O buffers between guest environments. Virtualization software for the T4 family includes kernel virtualization model (KVM), Linux® containers, Freescale hypervisor and commercial virtualization software from Enea, Greenhills Software, Mentor Graphics, QNX and Wind River.

DPAA Hardware Accelerators

Frame manager (FMAN)	24 Gb/s classify, parse and distribute
Buffer manager (BMAN)	64 buffer pools
Queue manager (QMAN)	Up to 2^{24} queues
RapidIO manager (RMAN)	Seamless mapping to DPAA
Security (SEC)	40 Gb/s: 3 DES, AES, SHA; 25K/s 1024-bit RSA
Pattern matching engine (PME)	10 Gb/s aggregate
Data compression engine (DCE)	20 Gb/s aggregate

Data Path Acceleration Architecture (DPAA)

The T4240 enhances the QorIQ DPAA, an innovative multicore infrastructure for scheduling work to cores (physical and virtual), hardware accelerators and network interfaces. The FMAN, a primary element of the DPAA, parses headers from incoming packets and classifies and selects data buffers with optional policing and congestion management. The FMAN passes its work to the QMAN, which assigns it to cores or accelerators with a multi-level scheduling hierarchy. The T4240's implementation of the DPAA offers accelerators for cryptography, enhanced regular expression pattern matching and compression/decompression.

System Peripherals and Networking

For networking, there are dual FMANs with an aggregate of 16 any-speed MAC controllers that connect to PHY, switches and backplanes over RGMII, SGIMII, XAUI, XFI and KR. The FMAN also supports new quality of service features through egress traffic shaping and priority flow control for data center bridging in converged data center networking applications. High-speed system expansion is supported through four PCI Express® controllers that support varieties of lane lengths for PCIe specification 3.0, including endpoint SR-IOV. Other peripheral include SRIO, Interlaken-LA, SATA, SD/MMC, I²C, UART, SPI, a NOR/NAND controller, GPIO and a 2.13 GHz DDR3/L controller.

T4240 Features List

Twelve dual-threaded e6500 cores built on Power Architecture technology	• Arranged as clusters of four e6500s sharing a 2 MB L2 cache • Up to 1.8 GHz at 1 V with 64-bit ISA support (Power Architecture® v2.06-compliant) • User, supervisor and hypervisor instruction levels
CoreNet platform cache	• 1.5 MB configured as triple 512 KB blocks
Hierarchical interconnect fabric	• CoreNet fabric supporting coherent and non-coherent transactions with prioritization and bandwidth allocation amongst CoreNet endpoints • 1.6 Tb/s coherent read bandwidth • QMAN fabric supporting packet-level queue management and quality of service scheduling
Three 64-bit DDR3/3L SDRAM memory controllers with ECC and interleaving support	• Up to 2.1 GHz • Memory pre-fetch engine
DPAA incorporates acceleration for the following functions	• Packet parsing, classification and distribution (FMAN 1.1) • Queue management for scheduling, packet sequencing and congestion management (QMAN 1.1) • Hardware buffer management for buffer allocation and de-allocation (BMAN 1.1) • Cryptography acceleration (SEC 5.0) at up to 40 Gb/s • RegEx pattern matching acceleration (PME 2.0) at up to 10 Gb/s • Decompression/compression acceleration (DCE 1.0) at up to 20 Gb/s • DPAA chip-to-chip interconnect via RapidIO message manager (RMAN 1.0)
SerDes	• 32 lanes total at up to 10 GHz • Supports SGMII, QSGMII, XAUI, XFI, KR, PCIe rev 1.1/2.0/3.0, Interlaken-LA, sRIO
Ethernet interfaces	• Up to four 10 Gb/s Ethernet MACs • Up to 16 1 Gb/s Ethernet MACs • Maximum configuration of 4 x 10 GE + 8 x 1 GE
High-speed peripheral interfaces	• Four PCI Express 2.0/3.0 controllers • Endpoint SR-IOV • Two serial RapidIO 2.0 controllers/ports running at up to 5 GHz with Type 11 messaging and Type 9 data streaming support • Interlaken look-aside interface for serial TCAM connection
Additional peripheral interfaces	• Two serial ATA (SATA 2.0) controllers • Two High-Speed USB 2.0 controllers with integrated PHY • Enhanced secure digital host controller (SD/MMC/eMMC) • Enhanced serial peripheral interface • Four I²C controllers • Four UARTs • Integrated flash controller supporting NAND and NOR flash
DMA	• Dual eight channel
Support for hardware virtualization and partitioning enforcement	• Extra privilege level for hypervisor support • Logical to real address translation • Virtual core aware MMU/TLB • vMPIC (virtualized interrupt controller)/virtual core capable PPC cores • vDMA (user-level DMA engine) • PAMUv2 (I/O MMU supporting paging) • DPAA (Ethernet MAC virtualization, accelerator virtualization)
QorIQ trust architecture 2.0	• Secure boot, secure debug, tamper detection, volatile key storage, alternate image and key revocation

Software and Tool Support

- Enea®: Real-time operating system support and virtualization software
- Green Hills®: Comprehensive portfolio of software and hardware development tools, trace tools, RTOS and virtualization software
- Mentor Graphics®: Commercial-grade Linux® solution and Vista simulation model which allows for a TLM2 simulation environment, software development and power estimation
- Wind River: Development tools, RTOS, Linux and virtualization software
- QNX: RTOS and development tool support

For more information, please visit freescale.com/QorIQ

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