Power Logic 8-BIT SHIFT REGISTER LED DRIVER

Check for Samples: TLC6C598-Q1

FEATURES

- **Qualified for Automotive Applications**
- **AEC-Q100 Qualified With the Following Results:**
  - **Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range**
  - **Device HBM ESD Classification Level H2**
  - **Device CDM ESD Classification Level C3B**
- **Wide Vcc From 3 V to 5.5 V**
- **Output Maximum Rating of.40 V**
- **Eight Power DMOS Transistor Outputs of 50-mA Continuous Current With Vcc = 5 V**
- **Thermal Shutdown Protection**
- **Enhanced Cascading for Multiple Stages**
- **All Registers Cleared With Single Input**
- **Low Power Consumption**
- **Slow Switching Time (t_r and t_f), Which Helps Significantly With Reducing EMI**
- **16-Pin TSSOP-PW Package**
- **16-Pin SOIC-D Package**

APPLICATIONS

- **Instrumentation Cluster**
- **Tell-Tale Lamps**
- **LED Illumination and Control**

DESCRIPTION

The TLC6C598-Q1 is a monolithic, medium-voltage, low-current power 8-bit shift register designed for use in systems that require relatively moderate load power, such as LEDs.

This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Data transfers through both the shift and storage registers on the rising edge of the shift-register clock (SRCK) and the register clock (RCK), respectively. The storage register transfers data to the output buffer when shift register clear ($\overline{CLR}$) is high. A low on $\overline{CLR}$ clears all registers in the device. Holding the output enable ($\overline{G}$) high, holds all data in the output buffers low, and all drain outputs are off. Holding $\overline{G}$ low makes data from the storage register transparent to the output buffers. When data in the output buffers is low, the DMOS transistor outputs are off. When data is high, the DMOS transistor outputs have sink-current capability. The serial output (SER OUT) clocks out of the device on the falling edge of SRCK to provide additional hold time for cascaded applications. This provides improved performance for applications where clock signals may be skewed, devices are not located near one another, or the system must tolerate electromagnetic interference. The device contains built-in thermal shutdown protection.

Outputs are low-side, open-drain DMOS transistors with output ratings of 40 V and 50 mA continuous sink-current capabilities when Vcc = 5 V. The current limit decreases as the junction temperature increases for additional device protection. The device also provides up to 2000 V of ESD protection when tested using the human-body model and 200 V when using the machine model.

The TLC6C598-Q1 characterization is for for operation over the operating ambient temperature range of −40°C to 125°C.

APPLICATION SCHEMATIC

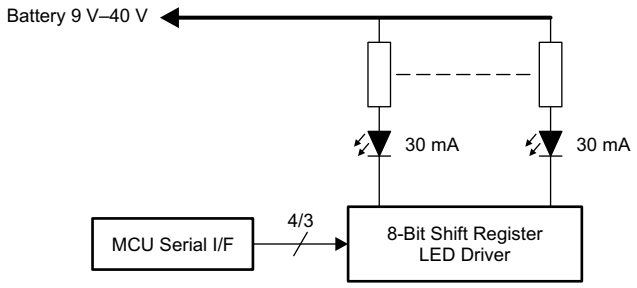


Figure 1. Typical Application Schematic

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

For the most-current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

Logic Diagram (Positive Logic)

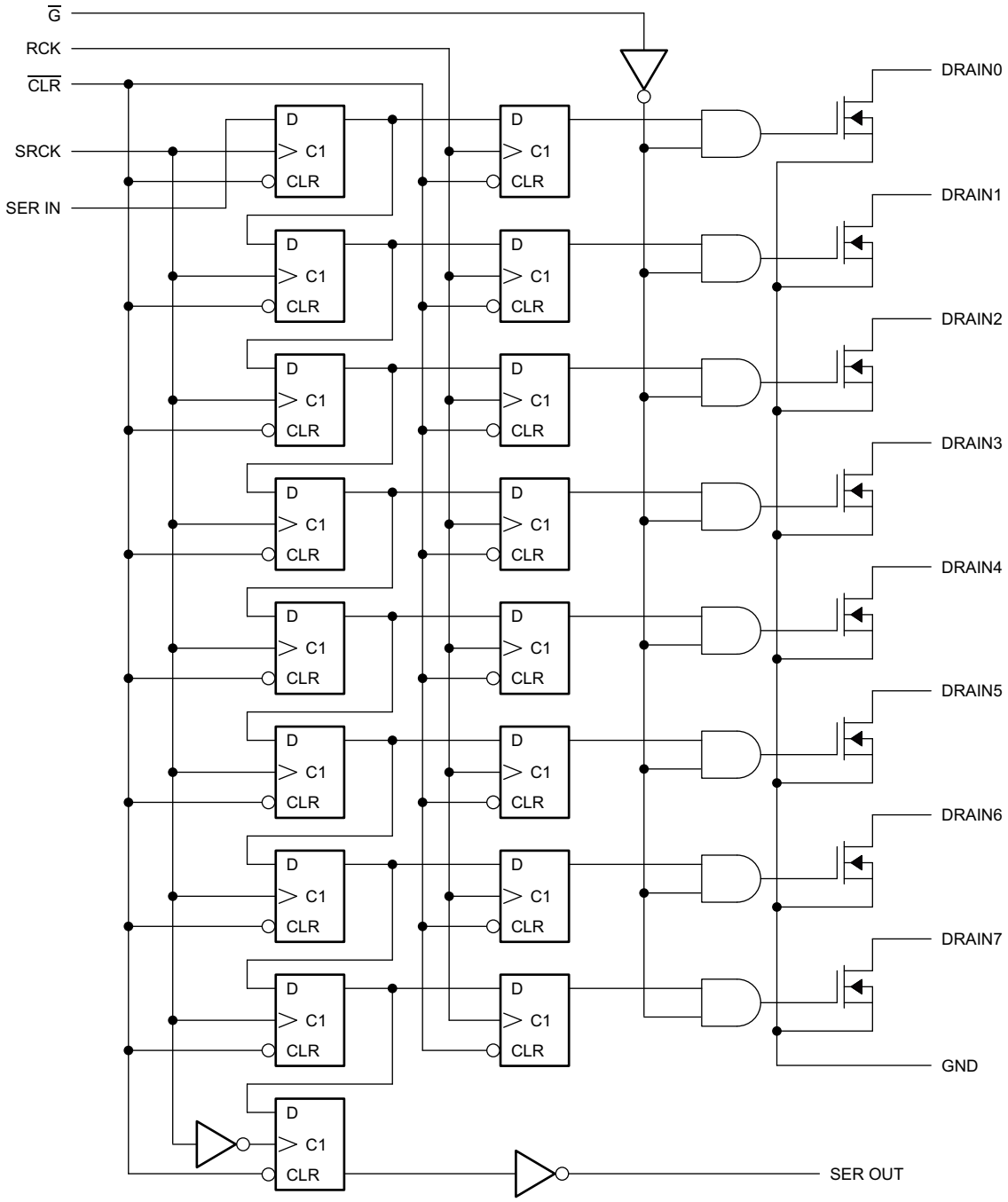


Figure 2. Logic Diagram of TLC6C598-Q1

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE		
		MIN	MAX	UNIT
V_{CC}	Logic supply voltage	–0.3	8	V
V_I	Logic input-voltage range	–0.3	8	V
V_{DS}	Power DMOS drain-to-source voltage	–0.3	42	V
	Continuous total dissipation	See Thermal Information table		
ESD(2)	Electrostatic discharge HBM		2	kV
T_A	Operating ambient temperature	–40	125	°C
T_{stg}	Storage temperature range	–55	165	°C
T_J	Operating junction temperature range	–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The human-body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin.

THERMAL INFORMATION

THERMAL METRIC(1)		TLC6C598-Q1		UNIT
		PW (16 PINS)	D (16 PINS)	
θ_{JA}	Junction-to-ambient thermal resistance	129.4	100	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	55.4	45	°C/W
θ_{JB}	Junction-to-board thermal resistance	65.8	40	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9.9	10	°C/W
ψ_{JB}	Junction-to-board characterization parameter	65.2	40	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	NA	NA	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V_{CC}	Supply voltage	3	5.5	V
V_{IH}	High-level input voltage	2.4		V
V_{IL}	Low-level input voltage		0.7	V
t_{su}	Setup time, SER IN high before SRCK↑	15		ns
t_h	Hold time, SER IN high after SRCK↑	15		ns
t_w	Pulse duration	40		ns
T_A	Operating ambient temperature	–40	125	°C

ELECTRICAL CHARACTERISTICS

V_{CC} = 5 V, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	DRAIN0 to DRAIN7. Drain-to-source voltage					40	V
V_{OH}	High-level output voltage, SER OUT	I_{OH} = –20 µA	V_{CC} = 5 V	4.9	4.99		V
		I_{OH} = −4 mA		4.5	4.69		V
V_{OL}	Low-level output voltage, SER OUT	I_{OH} = 20 µA	V_{CC} = 5 V		0.001	0.01	V
		I_{OH} = 4 mA			0.25	0.4	V
I_{IH}	High-level input current	V_{CC} = 5 V, V_I = V_{CC}			0.2		µA
I_{IL}	Low-level input current	V_{CC} = 5 V, V_I = 0			–0.2		µA
I_{CC}	Logic supply current	V_{CC} = 5 V, no clock signal	All outputs off		0.1	1	µA
			All outputs on		88	160	
$I_{CC(FRQ)}$	Logic supply current at frequency	f_{SRCK} = 5 MHz, C_L = 30 pF	All outputs on		200		µA
I_{DSX}	Off-state drain current	V_{DS} = 30 V	V_{CC} = 5 V			0.1	
		V_{DS} = 30 V, T_C = 125°C	V_{CC} = 5 V		0.15	0.3	µA
$r_{DS(on)}$	Static drain-source on-state resistance	I_D = 20 mA, V_{CC} = 5 V, T_A = 25°C, Single channel ON		6	7.41	8.6	Ω
		I_D = 20 mA, V_{CC} = 5 V, T_A = 25°C, All channels ON		6.7	8.3	9.6	
		I_D = 20 mA, V_{CC} = 3.3 V, T_A = 25°C, Single channel ON		7.9	9.34	11.2	
		I_D = 20 mA, V_{CC} = 3.3 V, T_A = 25°C, All channels ON		8.7	10.25	12.3	
		I_D = 20 mA, V_{CC} = 5 V, T_A = 125°C, Single channel ON		9.1	11.13	12.9	
		I_D = 20 mA, V_{CC} = 5 V, T_A = 125°C, All channels ON		10.3	12.28	14.5	
		I_D = 20 mA, V_{CC} = 3.3 V, T_A = 125°C, Single channel ON		11.6	13.69	16.4	
		I_D = 20 mA, V_{CC} = 3.3 V, T_A = 125°C, All channels ON		12.8	14.89	18.2	
$T_{SHUTDOWN}$	Thermal shutdown trip point			150	175	200	ºC
T_{hys}	Hysteresis				15		ºC

SWITCHING CHARACTERISTICS

V_{CC} = 5 V, T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from $\overline{G}$	C_L = 30 pF, I_D = 48 mA; see		220		ns
t_{PHL}	Propagation delay time, high-to-low-level output from $\overline{G}$			75		ns
t_r	Rise time, drain output			210		ns
t_f	Fall time, drain output			128		ns
t_{pd}	Propagation delay time, SRCK↓ to SEROUT	C_L = 30 pF, I_D = 48 mA		49.4		ns
t_{or}	SEROUT rise time (10% to 90%)	C_L = 30 pF		20		ns
t_{of}	SEROUT fall time (90% to 10%)	C_L = 30 pF		20		ns
$f_{(SRCK)}$	Serial clock frequency	C_L = 30 pF, I_D = 20 mA			10	MHz
t_{SRCK_WH}	SRCK pulse duration, high		30			ns
t_{SRCK_WL}	SRCK pulse duration, low		30			ns

DEVICE INFORMATION

PIN CONFIGURATIONS

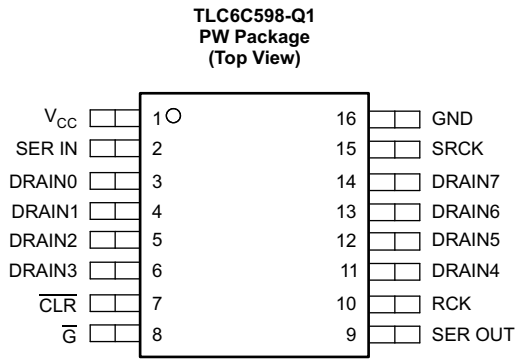


Figure 3. PW-Package Pin Configuration of TLC6C598-Q1

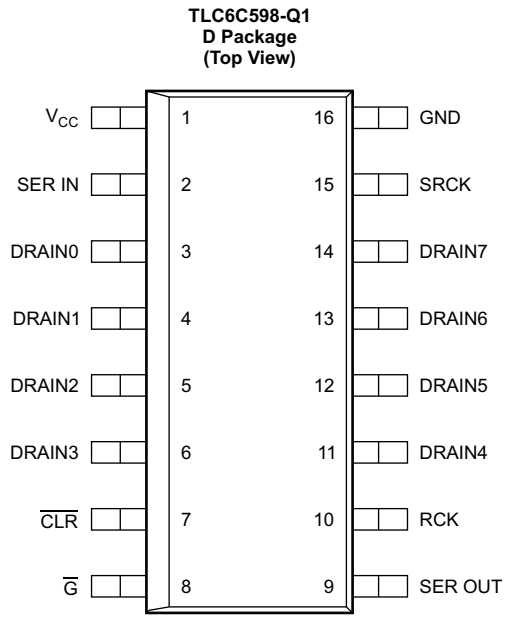


Figure 4. D-Package Pin Configuration of TLC6C598-Q1

PIN FUNCTIONS

NAME	NO.	I/O	DESCRIPTION
$\overline{CLR}$	7	I	Shift register clear, active-low
DRAIN0	3	O	Open-drain output
DRAIN1	4	O	Open-drain output
DRAIN2	5	O	Open-drain output
DRAIN3	6	O	Open-drain output
DRAIN4	11	O	Open-drain output
DRAIN5	12	O	Open-drain output
DRAIN6	13	O	Open-drain output
DRAIN7	14	O	Open-drain output
$\overline{G}$	8	I	Output enable, active-low
GND	16	—	Power ground
RCK	10	I	Register clock
SER IN	2	I	Serial data input
SER OUT	9	O	Serial data output
SRCK	15	I	Shift register clock
V_{CC}	1	I	Power supply

PIN DESCRIPTIONS

$\overline{CLR}$ is the signal used to clear all the registers. The storage register transfers data to the output buffer when shift register clear ($\overline{CLR}$) is high. Driving $\overline{CLR}$ low clears all the registers in the device.

DRAIN0–DRAIN7 are the LED current-sink channels. These pins connect to LED cathodes, and can survive up to 40-V LED supply voltage. This is quite helpful during automotive load-dump conditions.

$\overline{G}$ is the LED-channel enable and disable input pin. Having $\overline{G}$ low enables all drain channels according to the output-latch register content. When high, all channels are off.

GND is the ground reference pin for the device. This pin must connect to the ground plane on the PCB.

RCK is the storage-register clock. The data in each shift register stage transfers to the storage register at the rising edge of RCK. Data in the storage register appears at the output whenever the output enable ($\overline{G}$) input signal is high.

SER IN is the serial data input. Data on SER IN loads into the internal register on each rising edge of SRCK.

SER OUT is the serial data output of the 8-bit serial shift register. The purpose of this pin is to cascade several devices on the serial bus. By connecting the SER OUT pin to the SER IN input of the next device on the serial bus to cascade, the data transfers to the next device on the falling edge of SRCK. This can improve the cascade application reliability, as it can avoid the issue that the second device receives SRCK and data input at the same rising edge of SRCK.

SRCK is the serial clock input. On each rising SRCK edge, data transfers from SER IN to the internal serial shift registers.

V_{CC} is the power-supply pin voltage for the device. TI recommends adding a 0.1-μF ceramic capacitor close to the pin.

THERMAL SHUTDOWN

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 175°C (typical). The thermal shutdown forces the device to have an open state when the junction temperature exceeds the thermal trip threshold. Once the junction temperature decreases below 160°C (typical), the device begins to operate again.

APPLICATION INFORMATION

Figure 5 shows a typical cascade application circuit with two TLC6C598-Q1 chips configured to cascade topology. The MCU generates all the input signals.

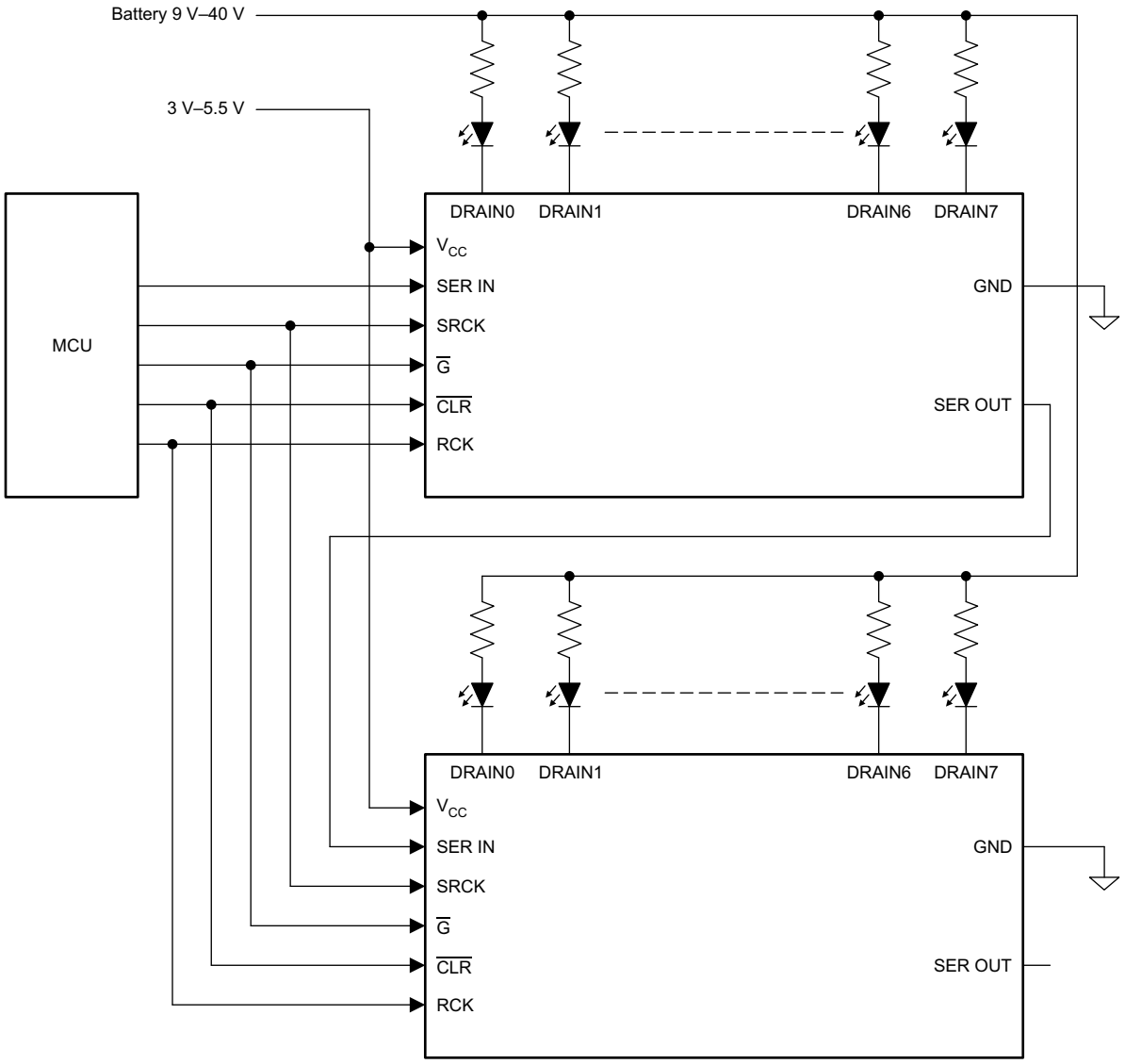
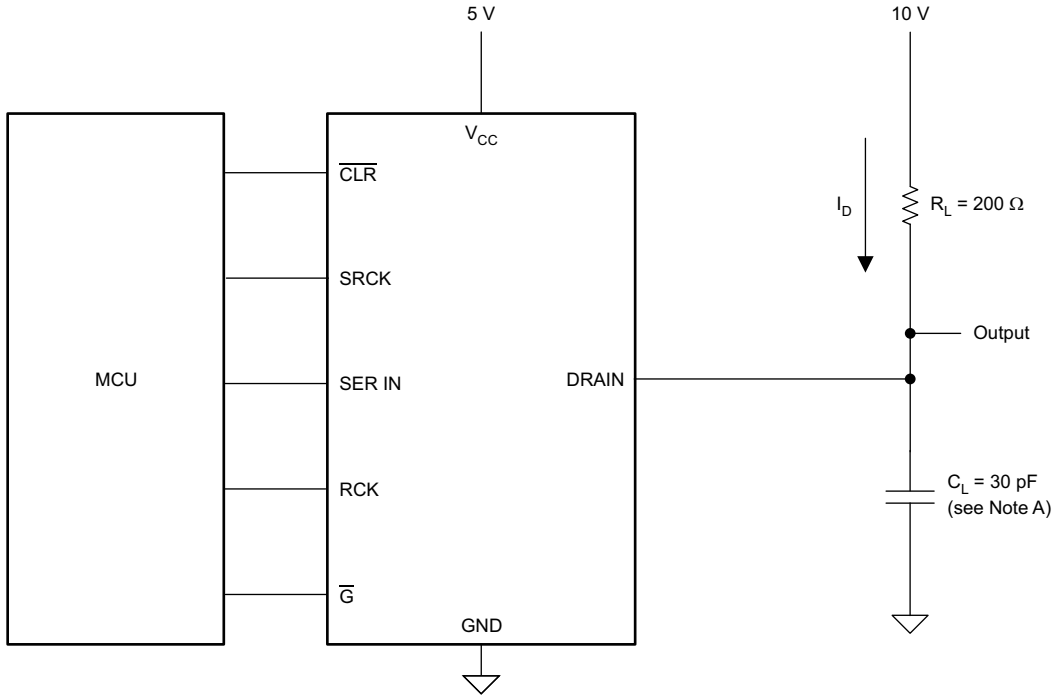


Figure 5. Typical Application Circuit

PARAMETER MEASUREMENT INFORMATION

Figure 6 and Figure 7 show the resistive-load test circuit and voltage waveforms. One can see from Figure 7 that with G held low and CLR held high, the status of each drain changes on the rising edge of the register clock, indicating the transfer of data to the output buffers at that time.

PARAMETER MEASUREMENT INFORMATION (continued)



A. C_L includes probe and jig capacitance.

Figure 6. Resistive-Load Test Circuit

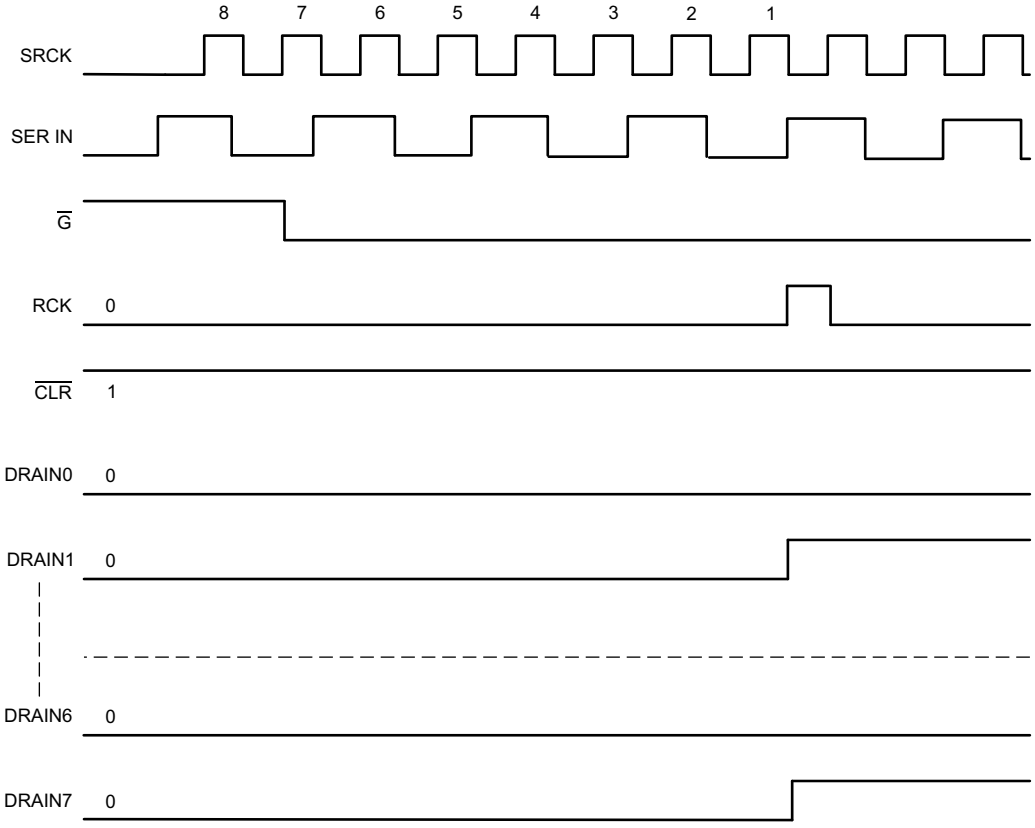


Figure 7. Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

Timing Waveform

Figure 8 shows the SER IN to SER OUT waveform. The output signal appears on the falling edge of the shift register clock (SRCK) because there is a phase inverter at SER OUT (see Figure 2). As a result, it takes seven and a half periods of SRCK for data to transfer from SER IN to SER OUT.

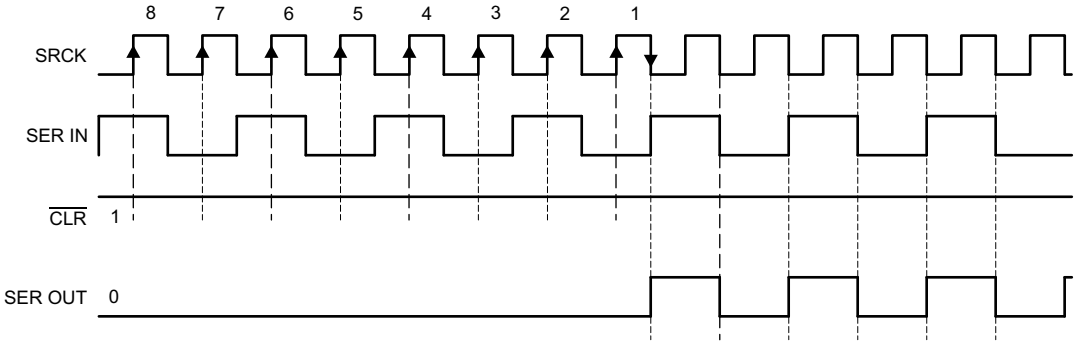


Figure 8. SER IN to SER OUT Waveform

Figure 9 shows the switching times and voltage waveforms. Tests for all these parameters took place using the test circuit shown in Figure 6.

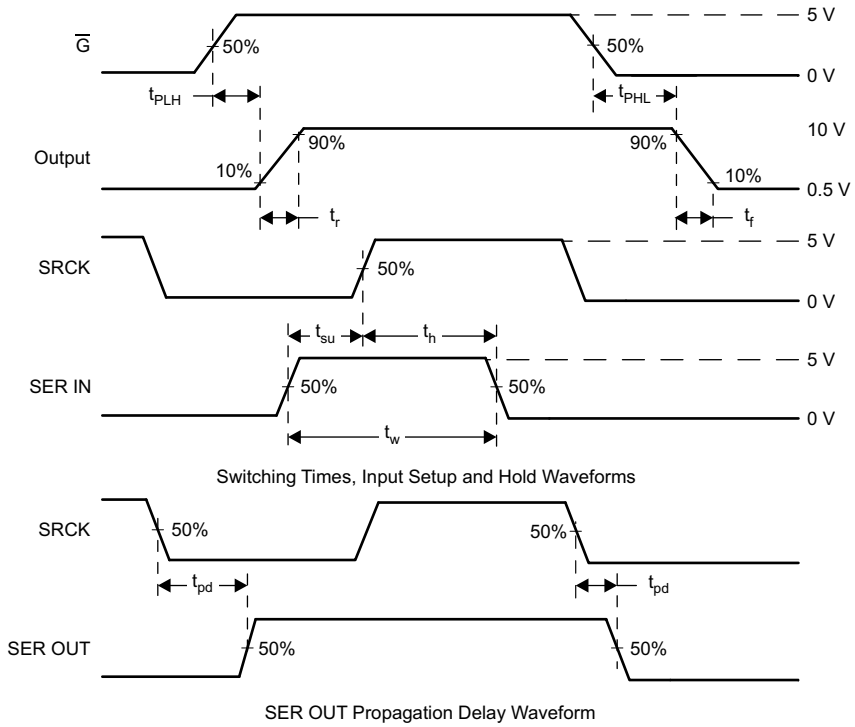


Figure 9. Switching Times and Voltage Waveforms

TYPICAL CHARACTERISTICS

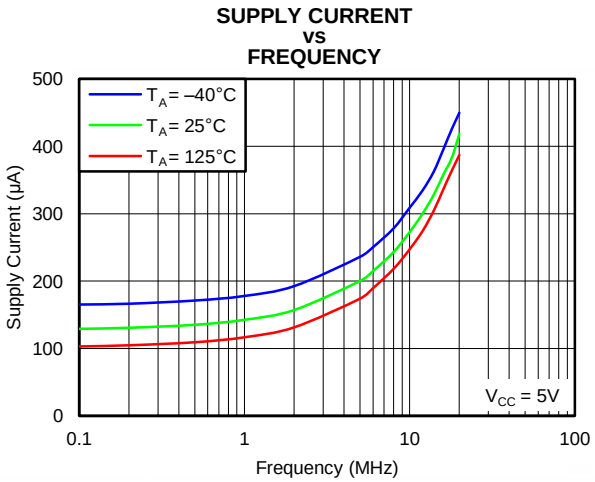


Figure 10.

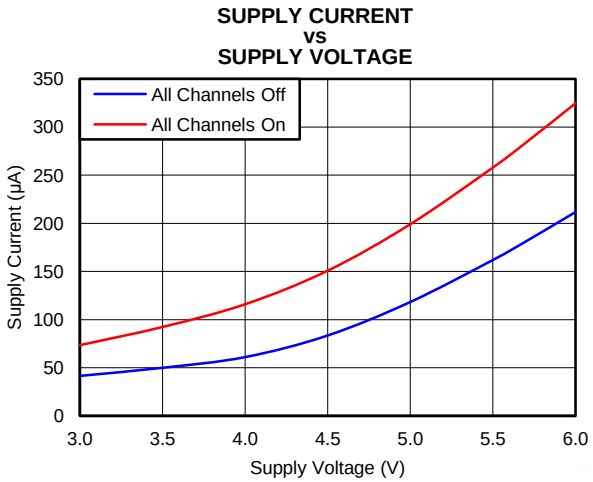


Figure 11.

Conditions for Figure 12 and Figure 13: Single channel on

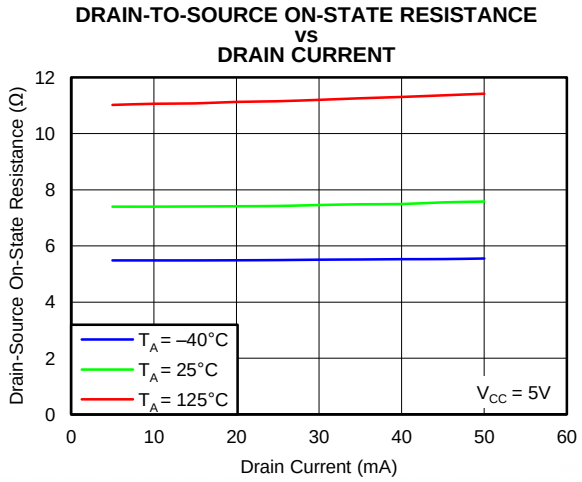


Figure 12.

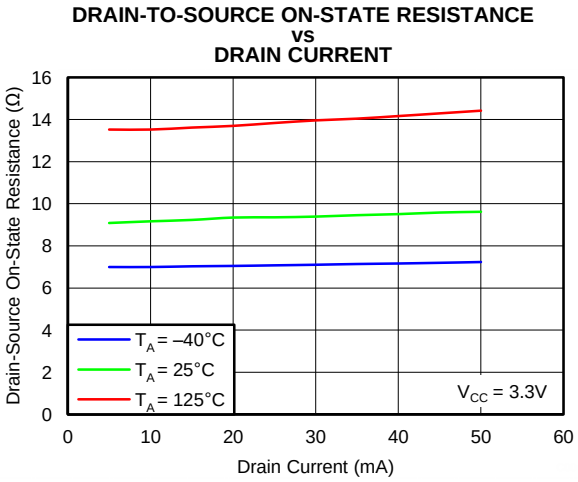


Figure 13.

TYPICAL CHARACTERISTICS

Conditions for Figure 14, Figure 15 and Figure 16: All channels on

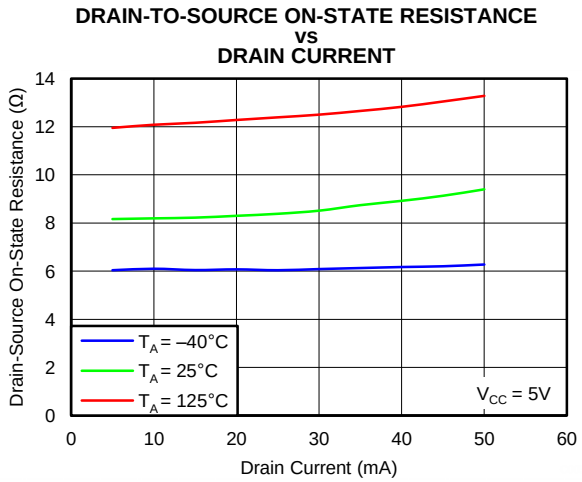


Figure 14.

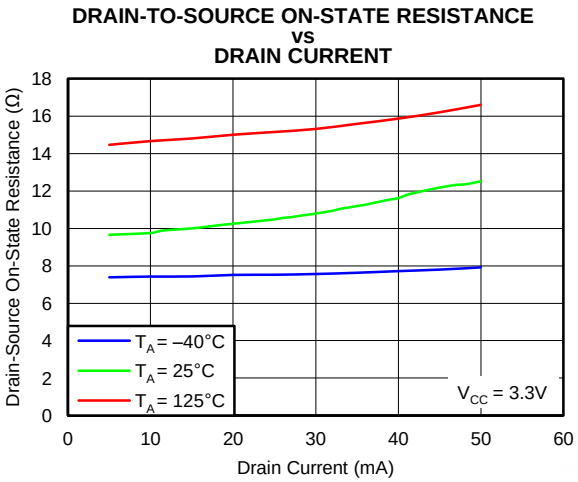


Figure 15.

TYPICAL CHARACTERISTICS (continued)

Conditions for Figure 14, Figure 15 and Figure 16: All channels on

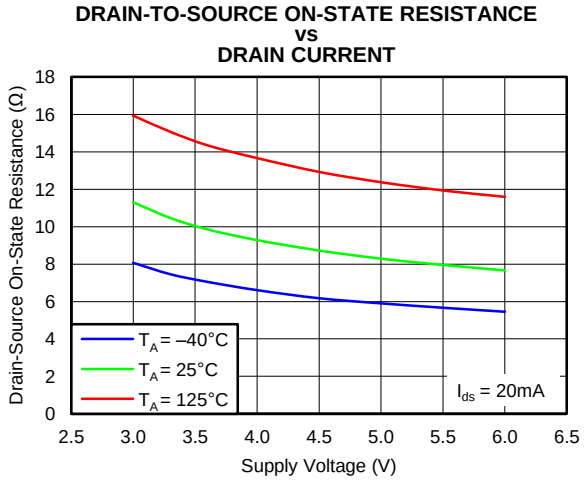


Figure 16.

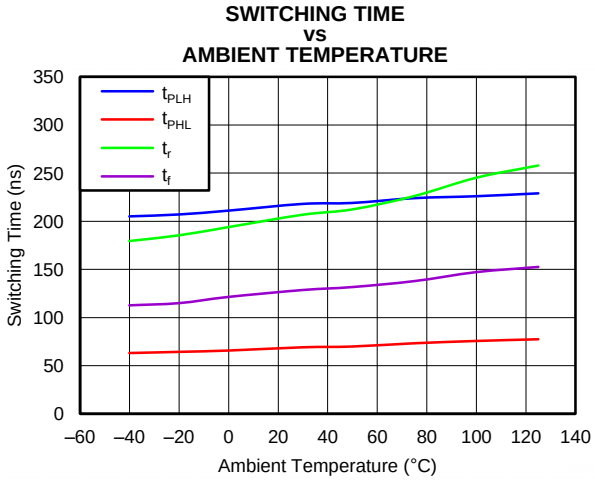


Figure 17.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC6C598QDRQ1	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	TLC6C598	Samples
TLC6C598QPWRQ1	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	6C598	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

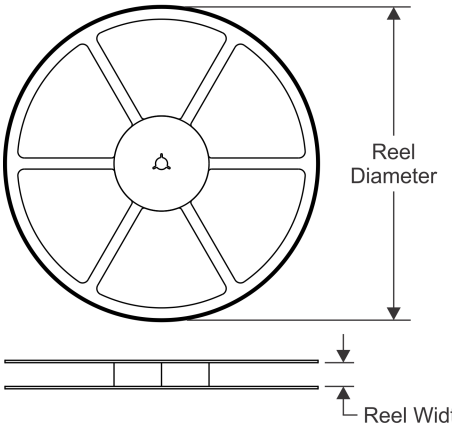
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

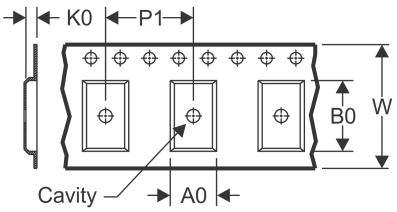
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

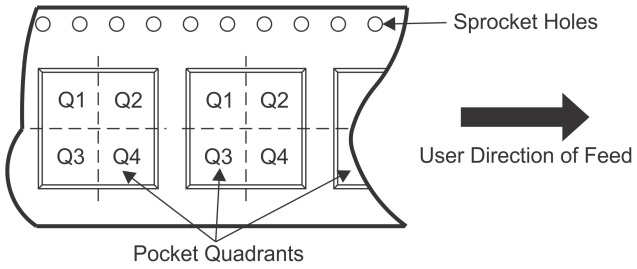


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

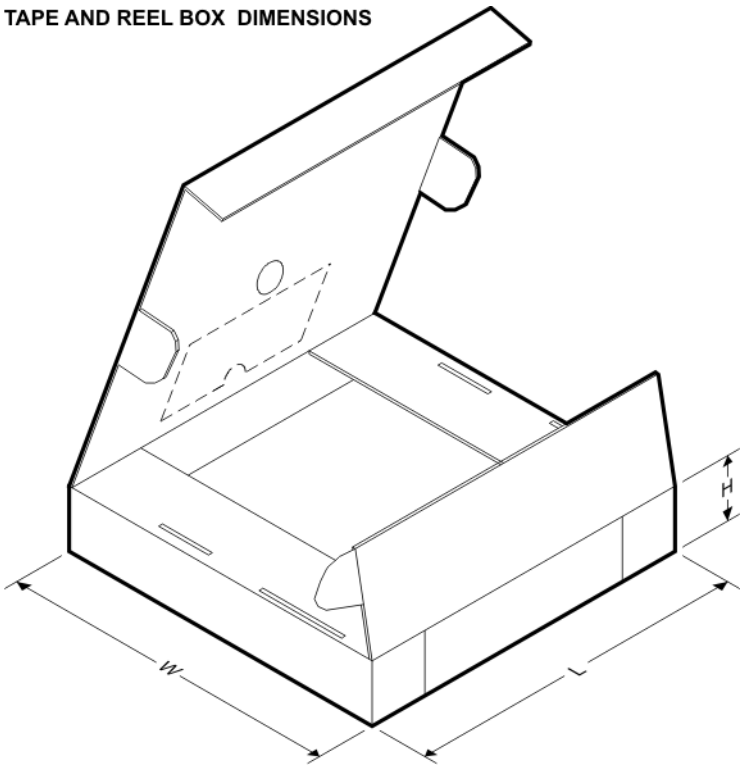
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC6C598QDRQ1	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TLC6C598QPWRQ1	TSSOP	PW	16	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

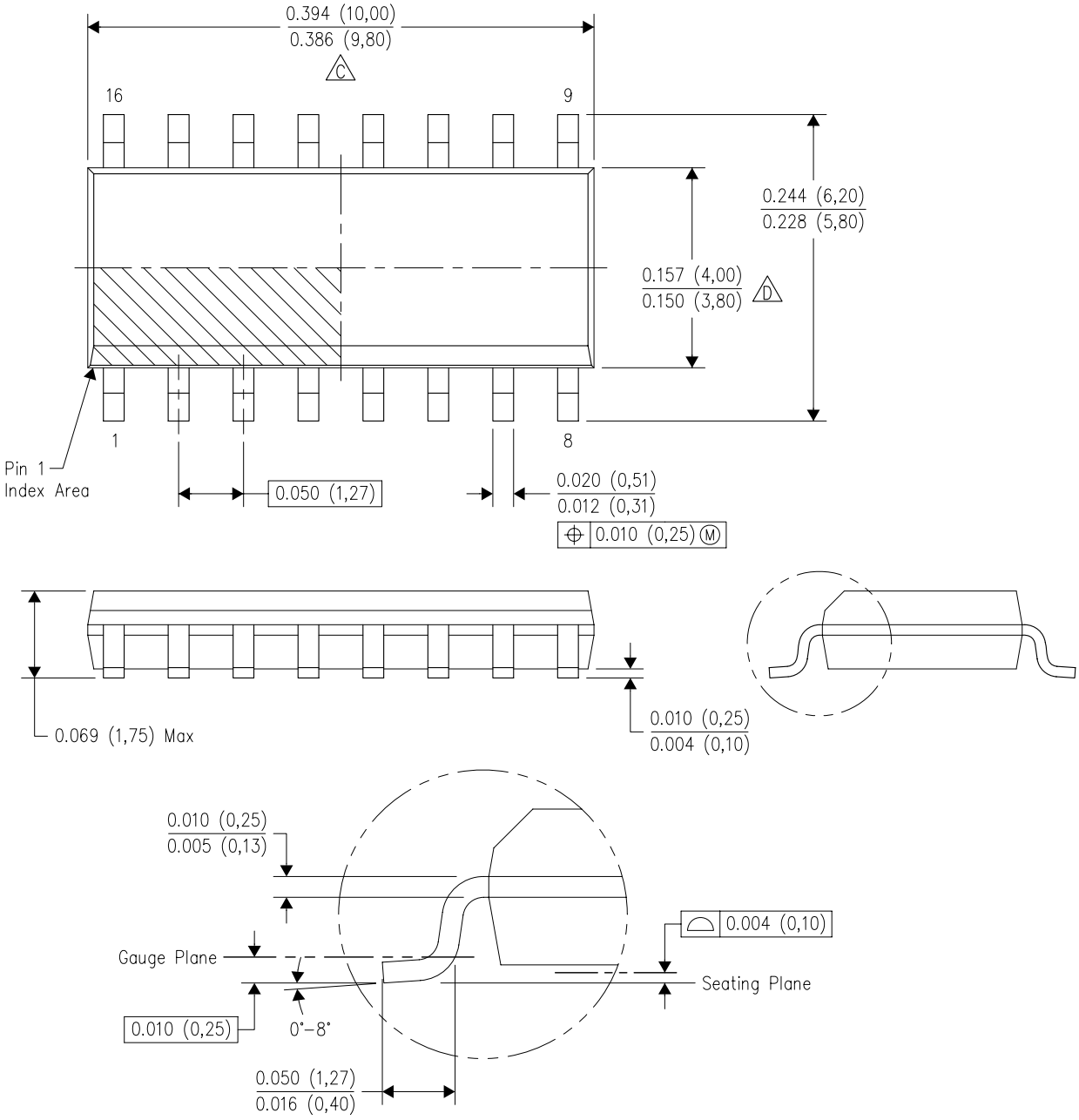
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

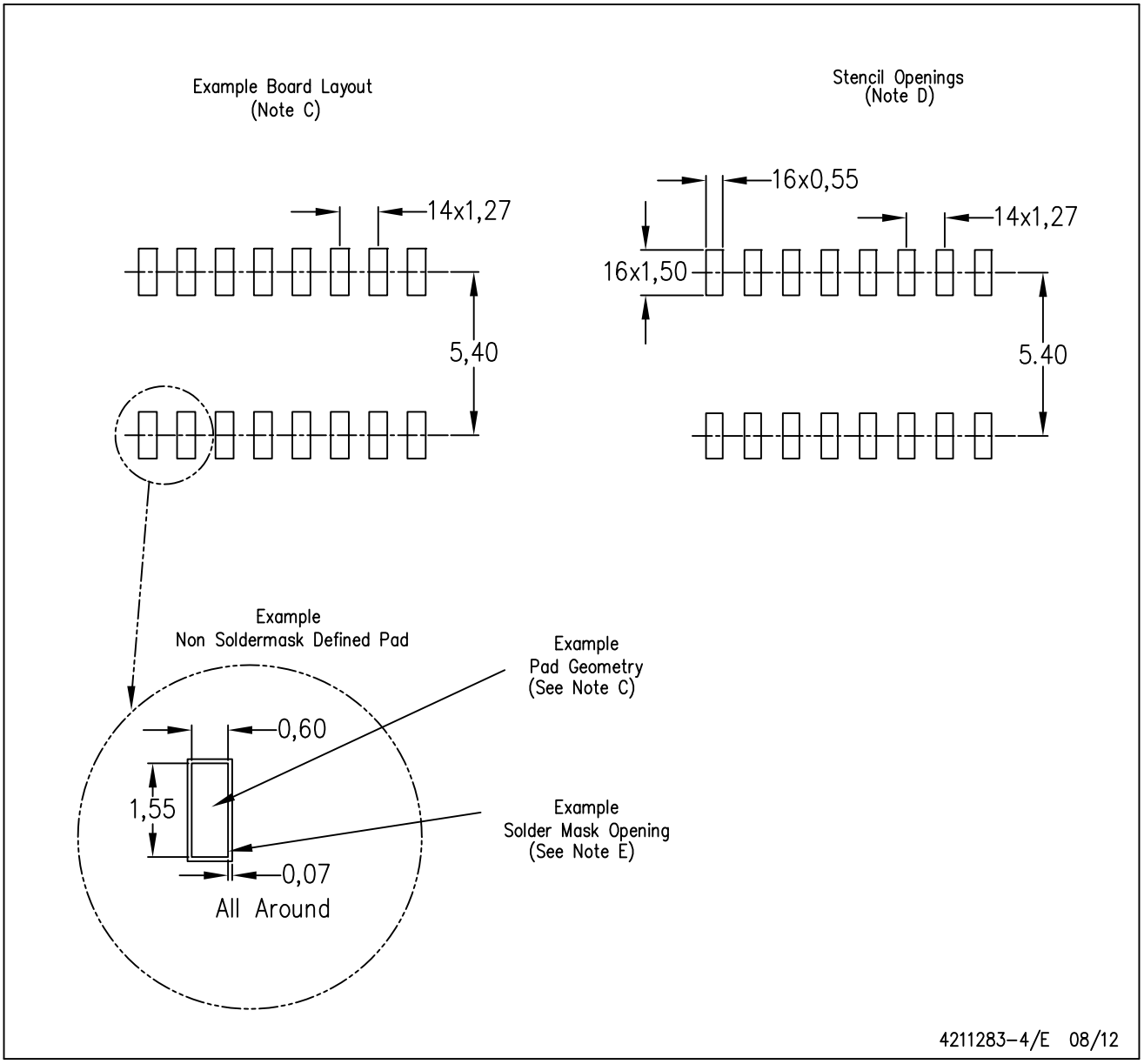
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC6C598QDRQ1	SOIC	D	16	2500	367.0	367.0	38.0
TLC6C598QPWRQ1	TSSOP	PW	16	2000	367.0	367.0	38.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



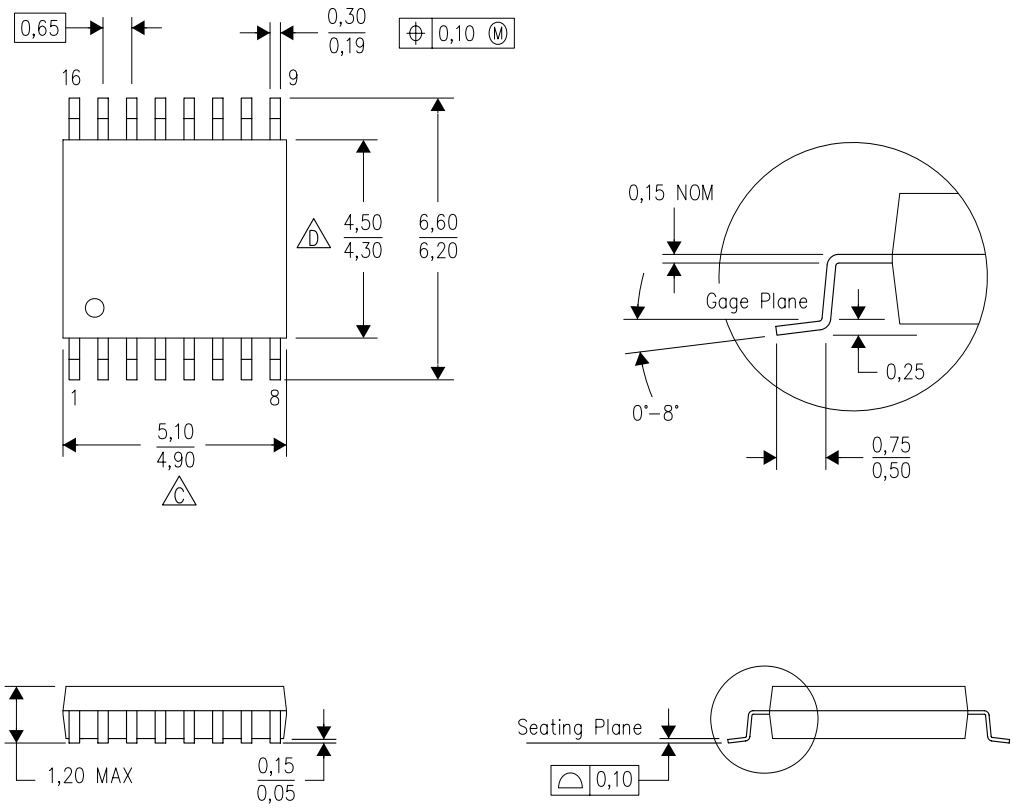
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

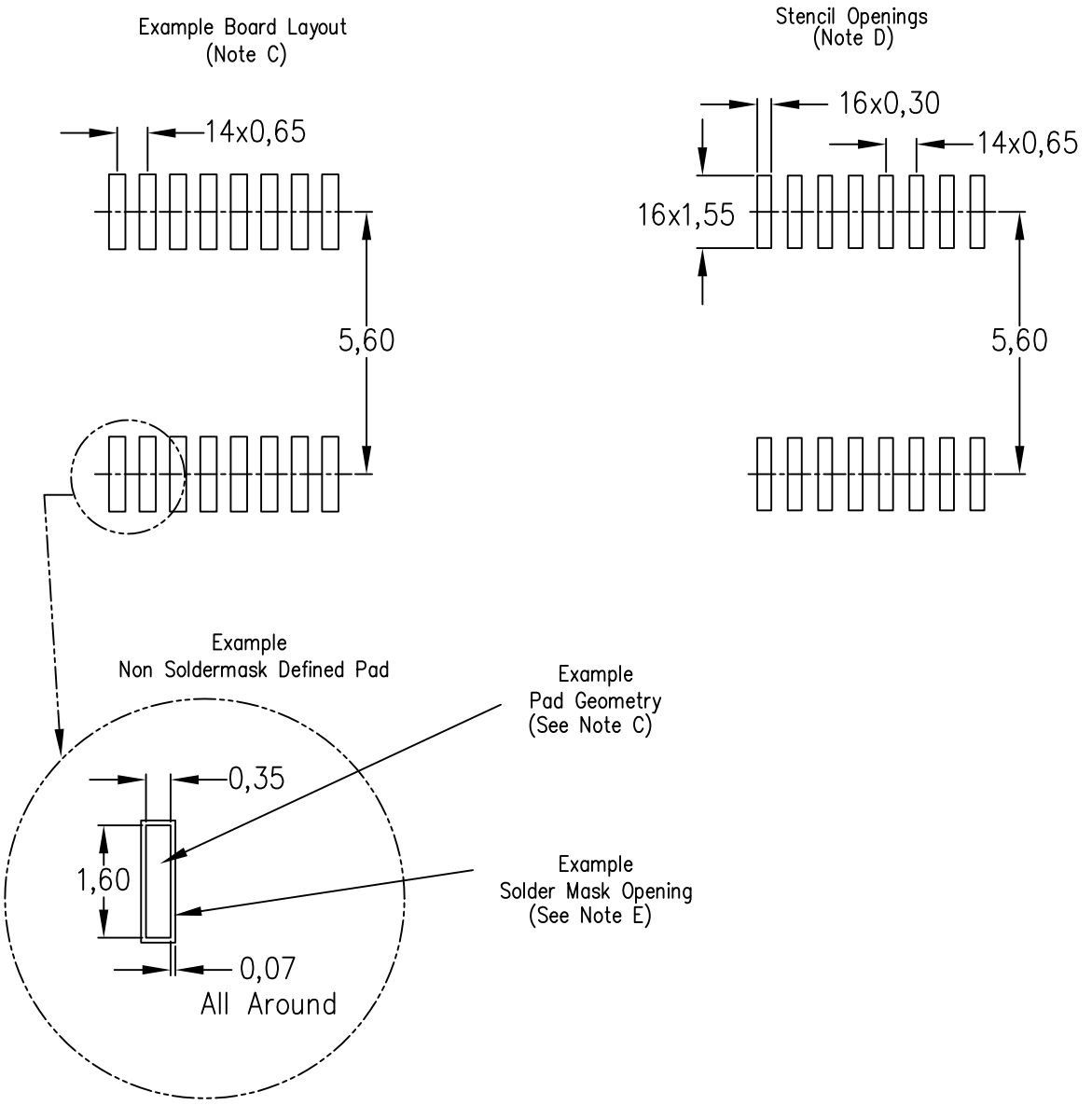
PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



4040064–4/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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