OptiMOS™3 Power-MOSFET

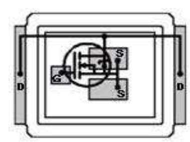
Features

- Optimized for high switching frequency DC/DC converter
- Very low on-resistance $R_{DS(on)}$
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Low parasitic inductance
- Low profile (<0.7 mm)
- 100% avalanche tested
- 100% Rg Tested
- Double-sided cooling
- Pb-free plating; RoHS compliant
- Compatible with DirectFET® package MX footprint and outline [1)]
- Qualified according to JEDEC[2)] for target applications

Product Summary

V_{DS}	30	V
$R_{DS(on),max}$	1.2	mΩ
I_D	180	A

MG-WDSON-2



Type	Package	Outline	Marking
BSB012N03LX3 G	MG-WDSON-2	MX	0103

Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	V_{GS}=10 V, T_C=25 °C	180	A
		V_{GS}=10 V, T_C=100 °C	139	
		V_{GS}=10 V, T_A=25 °C, R_{thJA}=45 K/W	39	
Pulsed drain current[3)]	$I_{D,pulse}$	T_C=25 °C	400	
Avalanche current, single pulse[4)]	I_{AS}	T_C=25 °C	40	
Avalanche energy, single pulse	E_{AS}	I_D=40 A, R_{GS}=25 Ω	290	mJ
Gate source voltage	V_{GS}		±20	V

[1)] CanPAK™ uses DirectFET ® technology licensed from International Rectifier Corporation. DirectFET® is a registered trademark of International Rectifier Corporation.

[2)] J-STD20 and JESD22

[3)] See figure 3 for more detailed information

[4)] See figure 13 for more detailed information

Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Power dissipation	P_{tot}	T_C=25 °C	89	W
		T_A=25 °C, R_{thJA}=45 K/W	2.8	
Operating and storage temperature	T_j, T_{stg}		-40….150	°C
IEC climatic category; DIN IEC 68-1			55/150/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics						
Thermal resistance, junction - case	R_{thJC}	bottom	-	1.0		K/W
		top	-	-	1.4	
Device on PCB	R_{thJA}	6 cm^2 cooling area[5]	-	-	45	
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=1 mA	30	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250 µA	1	-	2.2	
Zero gate voltage drain current	I_{DSS}	V_{DS}=30 V, V_{GS}=0 V, T_j=25 °C	-	0.1	10	µA
		V_{DS}=30 V, V_{GS}=0 V, T_j=125 °C	-	10	100	
Gate-source leakage current	I_{GSS}	V_{GS}=20 V, V_{DS}=0 V	-	10	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=4.5 V, I_D=25 A	-	1.4	1.8	mΩ
		V_{GS}=10 V, I_D=30 A	-	1.0	1.2	
Gate resistance	R_G		0.2	0.5	1.0	Ω
Transconductance	g_{fs}	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=30 A	70	140	-	S

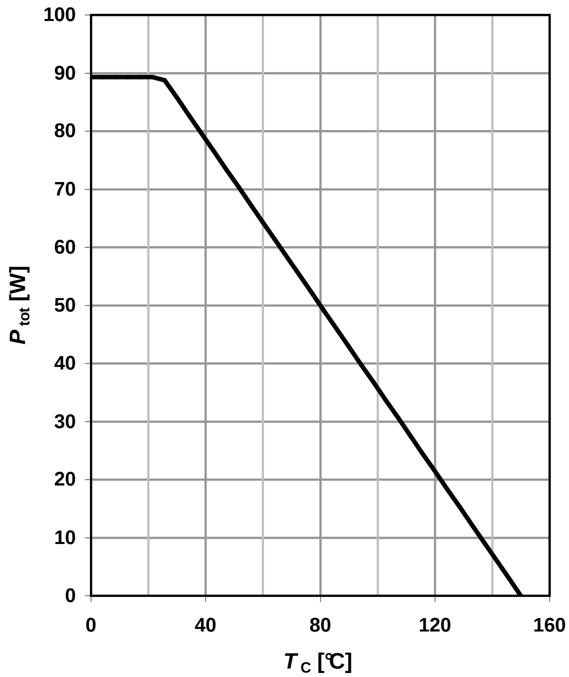
[5] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=15 V, f=1 MHz	-	12700	16900	pF
Output capacitance	C_{oss}		-	3300	4400	
Reverse transfer capacitance	C_{rss}		-	200	-	
Turn-on delay time	$t_{d(on)}$	V_{DD}=15 V, V_{GS}=10 V, I_D=30 A, R_G=1.6 Ω	-	7.9	-	ns
Rise time	t_r		-	8.6	-	
Turn-off delay time	$t_{d(off)}$		-	47	-	
Fall time	t_f		-	8.4	-	
Gate Charge Characteristics[6]						
Gate to source charge	Q_{gs}	V_{DD}=15 V, I_D=30 A, V_{GS}=0 to 4.5 V	-	26	-	nC
Gate charge at threshold	$Q_{g(th)}$		-	16	-	
Gate to drain charge	Q_{gd}		-	13	-	
Switching charge	Q_{sw}		-	24	-	
Gate charge total	Q_g		-	61	81	
Gate plateau voltage	$V_{plateau}$		-	2.7	-	V
Gate charge total	Q_g	V_{DD}=15 V, I_D=30 A, V_{GS}=0 to 10 V	-	127	169	
Gate charge total, sync. FET	$Q_{g(sync)}$	V_{DS}=0.1 V, V_{GS}=0 to 4.5 V	-	53	-	nC
Output charge	Q_{oss}	V_{DD}=15 V, V_{GS}=0 V	-	85	-	
Reverse Diode						
Diode continuous forward current	I_S	T_C=25 °C	-	-	81	A
Diode pulse current	$I_{S,pulse}$		-	-	400	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=30 A, T_j=25 °C	-	0.77	1.1	V
Reverse recovery charge	Q_{rr}	V_R=15 V, I_F=I_S, di_F/dt=400 A/µs	-	-	50	nC

[6] See figure 16 for gate charge parameter definition

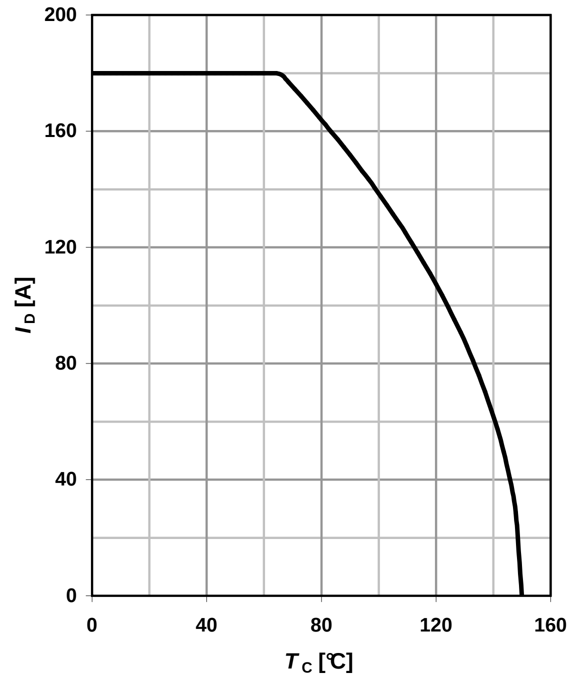
1 Power dissipation

P_{tot}=f(T_C)



2 Drain current

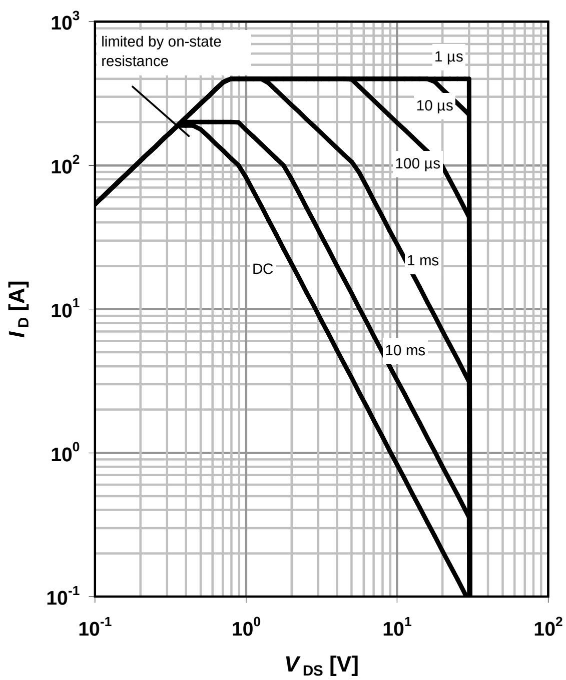
I_D=f(T_C); V_{GS}≥10 V



3 Safe operating area

I_D=f(V_{DS}); T_C=25 °C; D=0

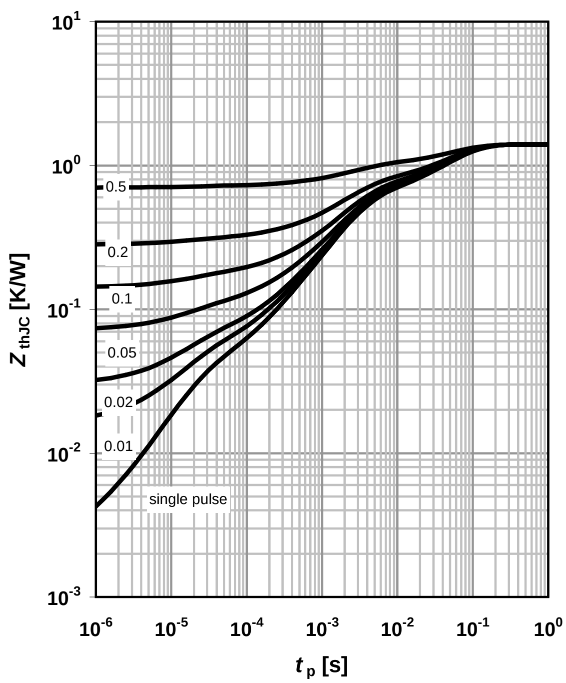
parameter: t_p



4 Max. transient thermal impedance

Z_{thJC}=f(t_p)

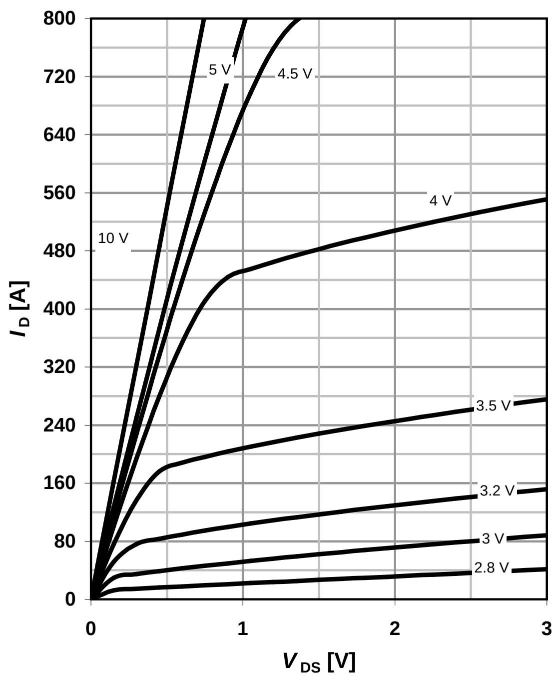
parameter: D=t_p/T



5 Typ. output characteristics

$I_D = f(V_{DS})$; $T_j = 25$ °C

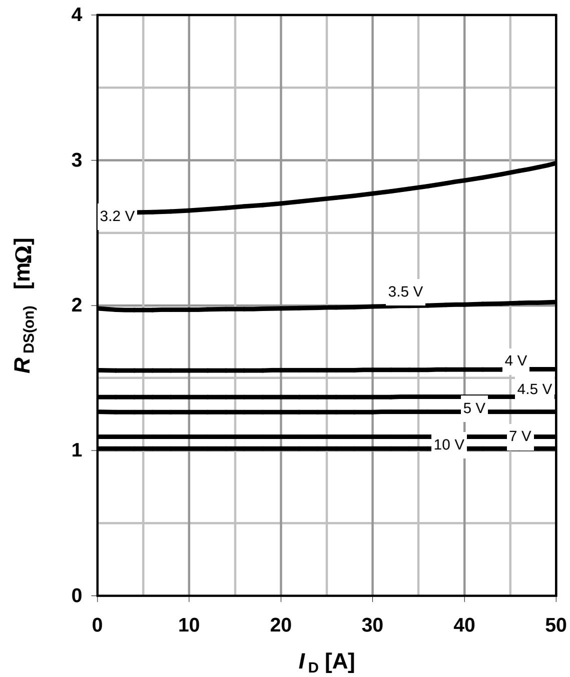
parameter: V_{GS}



6 Typ. drain-source on resistance

$R_{DS(on)} = f(I_D)$; $T_j = 25$ °C

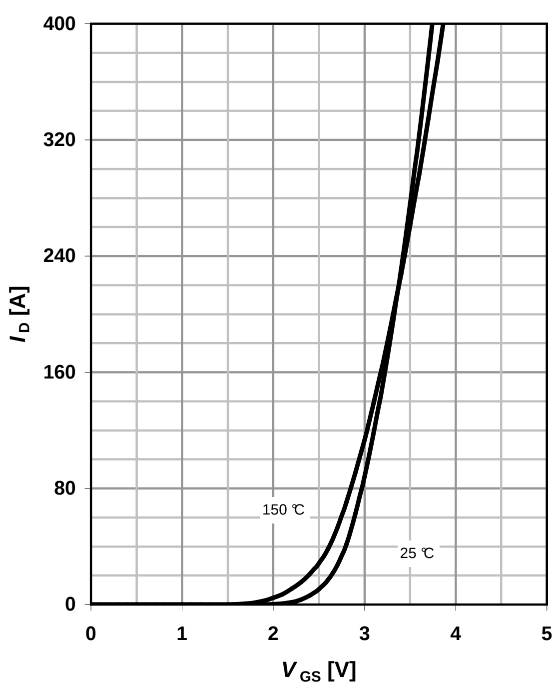
parameter: V_{GS}



7 Typ. transfer characteristics

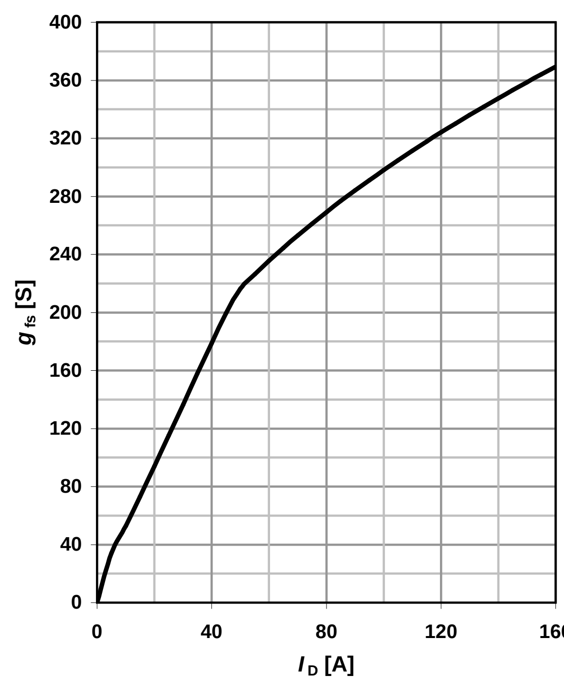
$I_D = f(V_{GS})$; $|V_{DS}| > 2|I_D|R_{DS(on)max}$

parameter: T_j



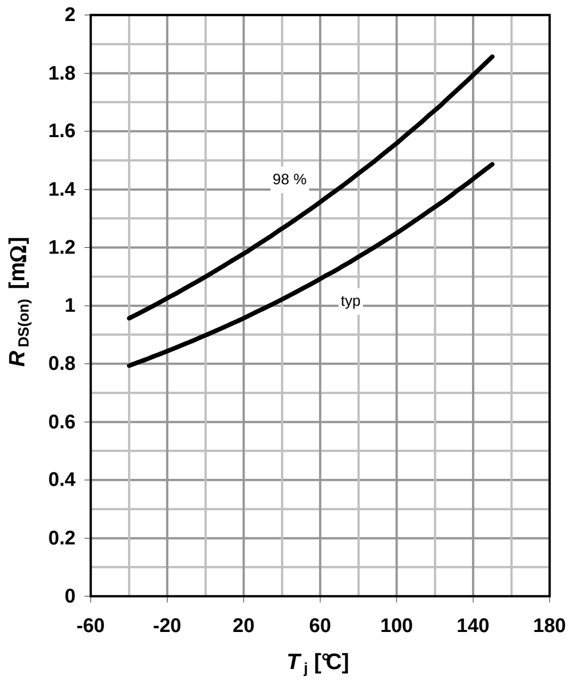
8 Typ. forward transconductance

$g_{fs} = f(I_D)$; $T_j = 25$ °C



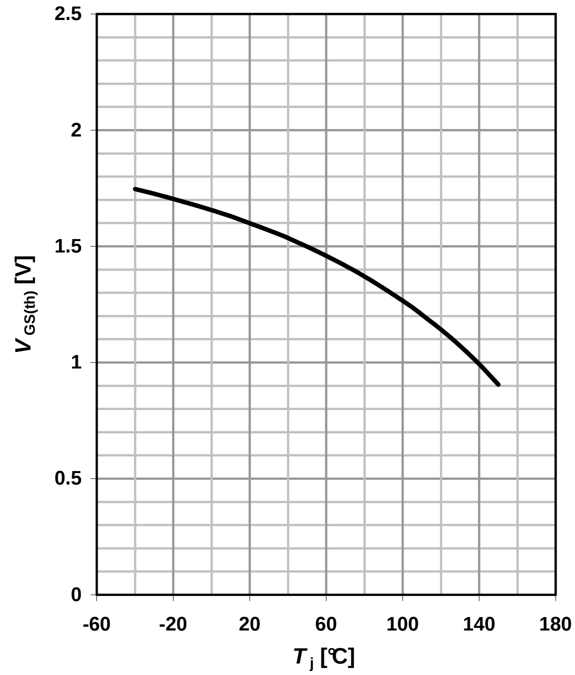
9 Drain-source on-state resistance

$R_{DS(on)}$=f(T_j); I_D=30 A; V_{GS}=10 V



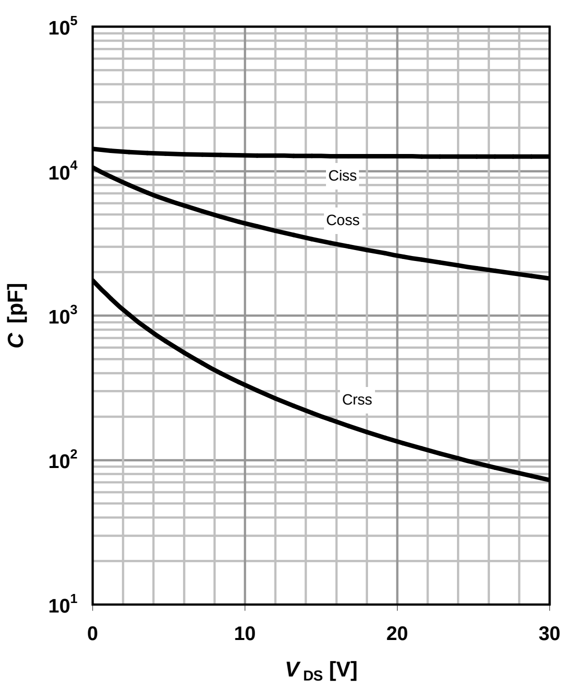
10 Typ. gate threshold voltage

$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}; I_D=250 µA



11 Typ. capacitances

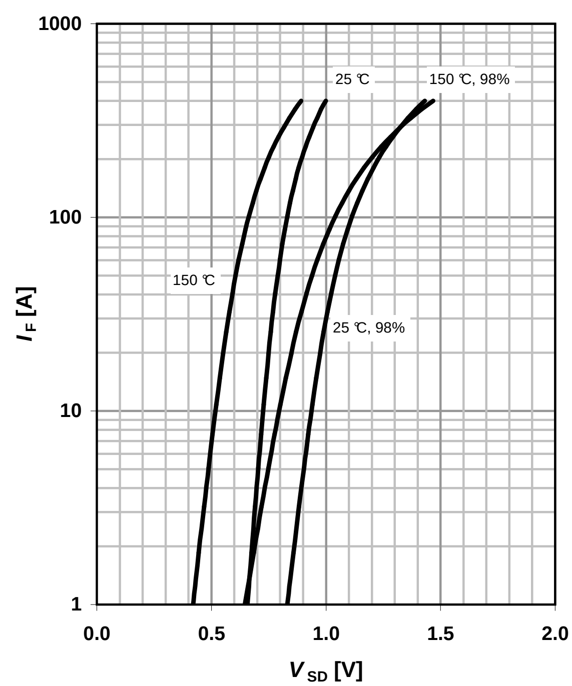
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz



12 Forward characteristics of reverse diode

I_F=f(V_{SD})

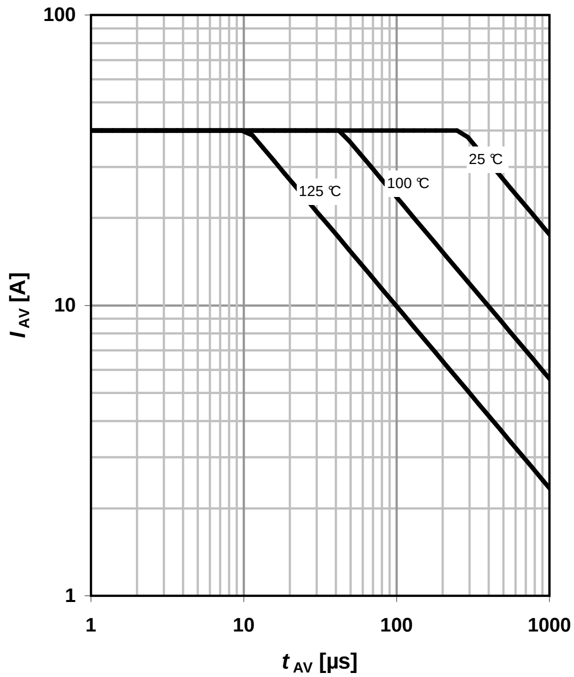
parameter: T_j



13 Avalanche characteristics

I_{AS}=f(t_{AV}); R_{GS}=25 Ω

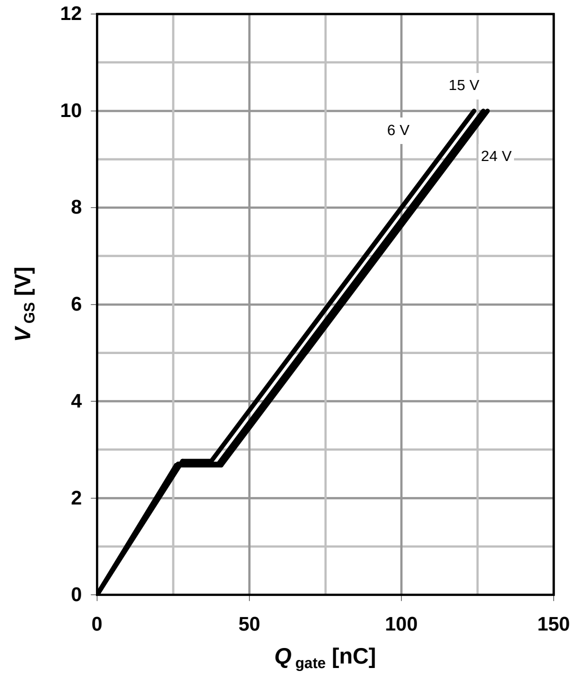
parameter: $T_{j(start)}$



14 Typ. gate charge

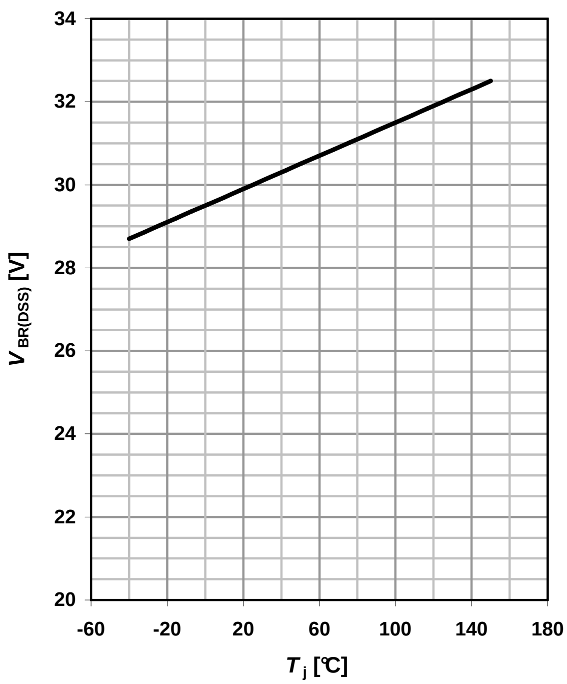
V_{GS}=f(Q_{gate}); I_D=30 A pulsed

parameter: V_{DD}

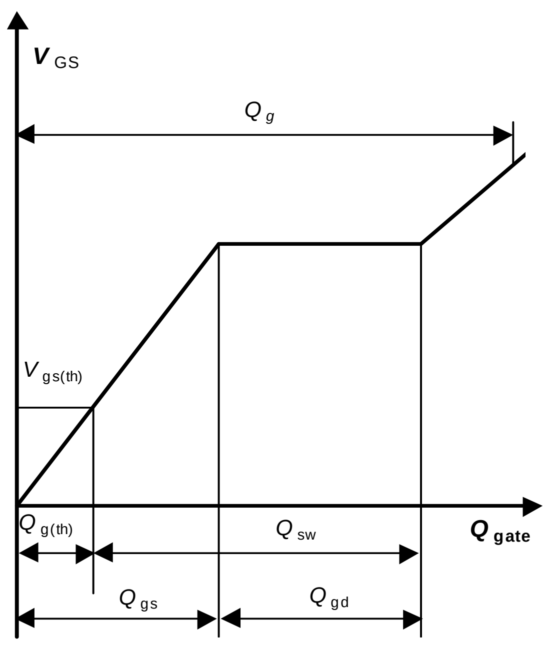


15 Drain-source breakdown voltage

$V_{BR(DSS)}$=f(T_j); I_D=1 mA

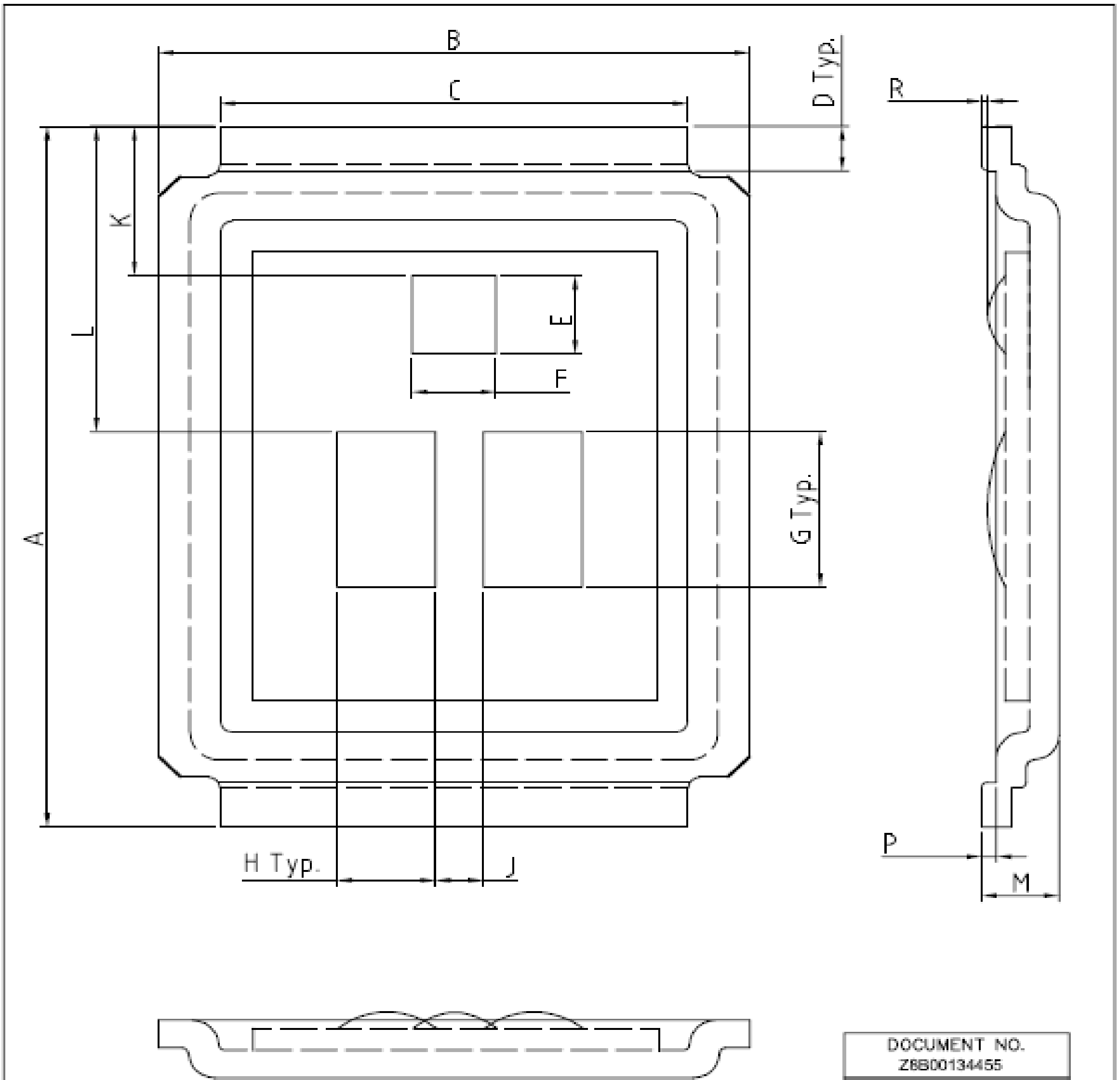


16 Gate charge waveforms



Package Outline

MG-WDSON-2



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.25	6.35	0.246	0.250
B	4.80	5.05	0.189	0.199
C	3.85	3.95	0.152	0.156
D	0.35	0.45	0.014	0.018
E	0.68	0.72	0.027	0.028
F	0.68	0.72	0.027	0.028
G	1.38	1.42	0.054	0.056
H	0.80	0.84	0.031	0.033
J	0.38	0.42	0.015	0.017
K	1.25	1.45	0.049	0.057
L	2.65	2.85	0.104	0.112
M	0.60	0.70	0.024	0.028
R	0.00	0.10	0.000	0.004
P	0.08	0.17	0.003	0.007

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Z8B00134455

SCALE 0 5 7.5mm

EUROPEAN PROJECTION

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03

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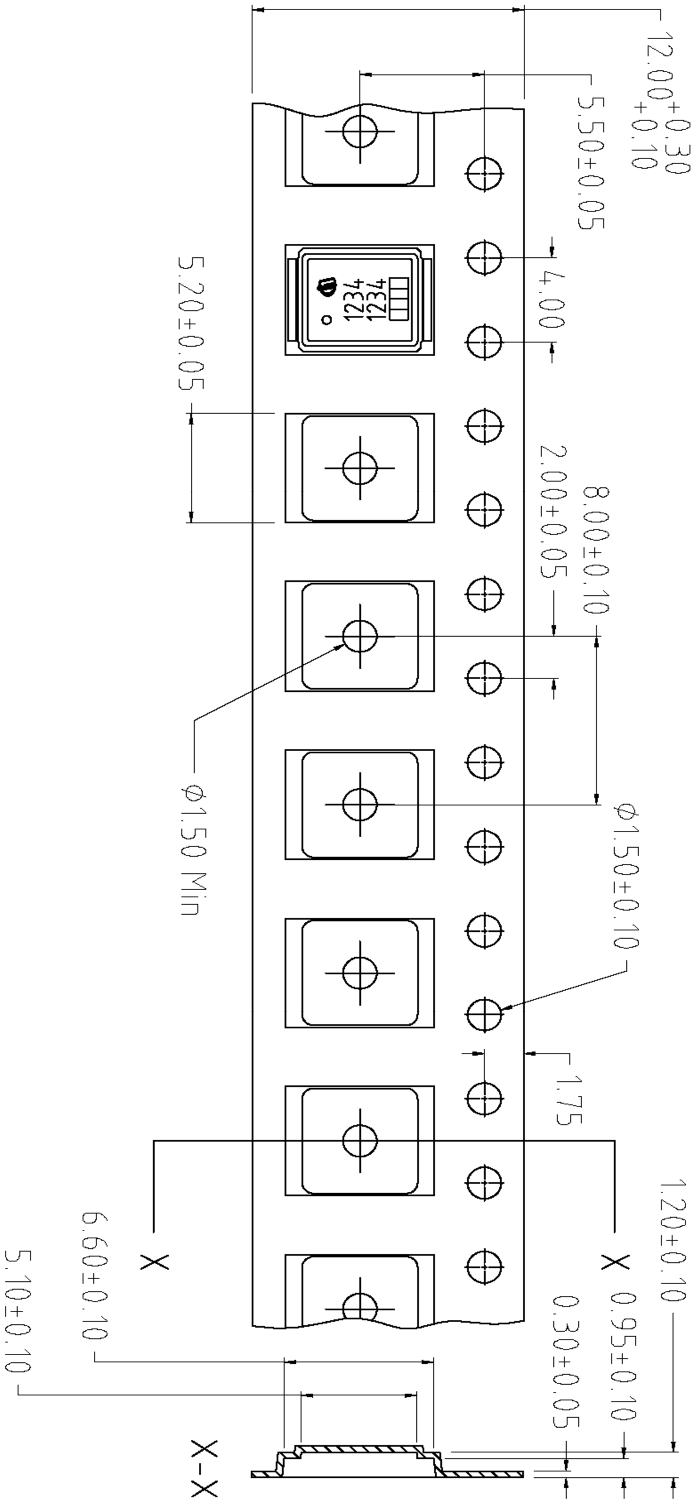
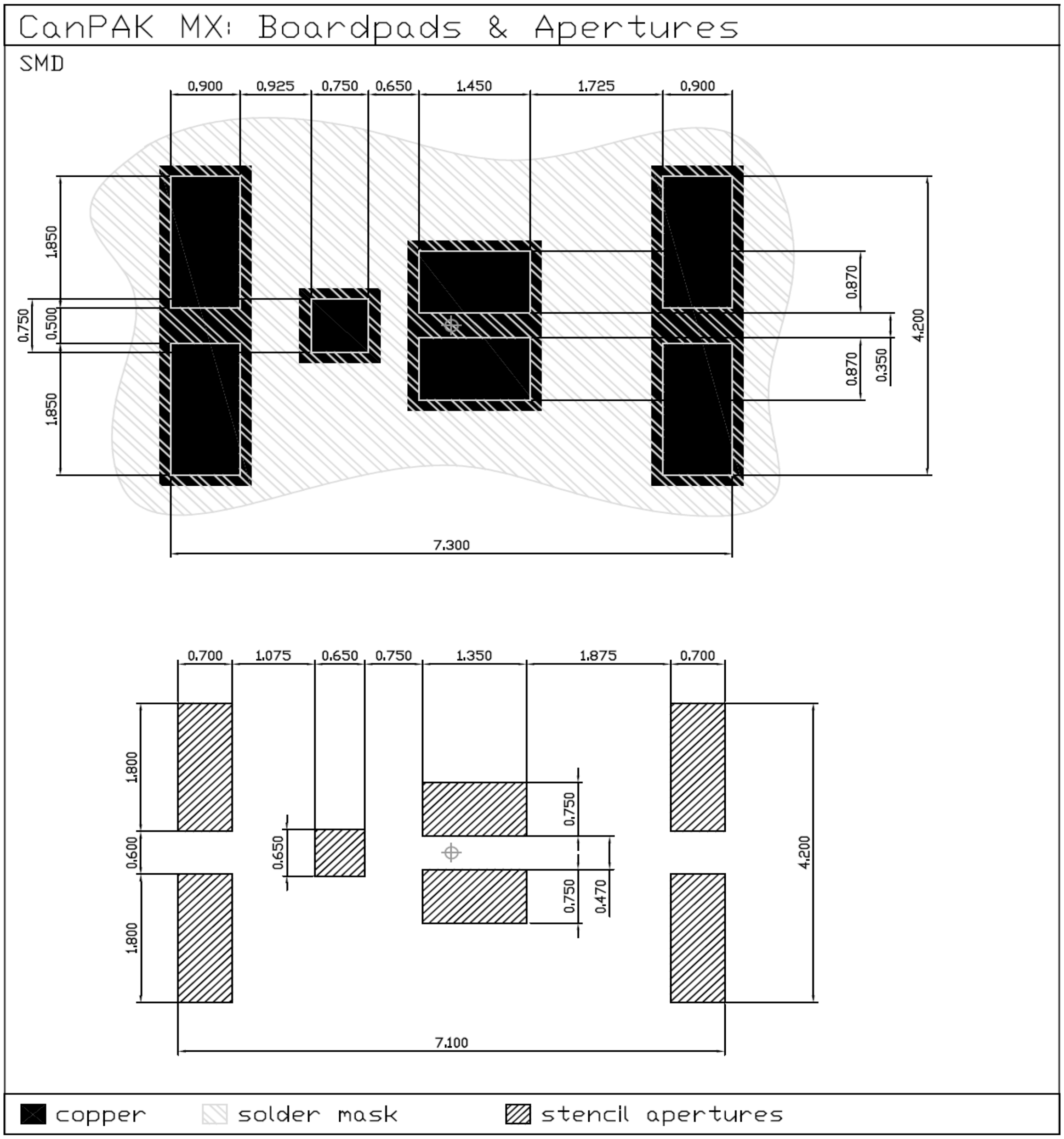


Dimensions in mm



Dimensions in mm

Recommended stencil thickness 150 µm

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