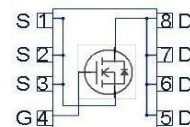
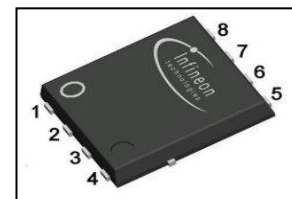


OptiMOS™ Power-MOSFET
Features

- Optimized for high performance SMPS, e.g. sync. rec.
- Very low on-resistance $R_{DS(on)}$ @ $V_{GS}=4.5\text{ V}$
- 100% avalanche tested
- Superior thermal resistance
- N-channel
- Qualified according to JEDEC¹⁾ for target applications
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21


Product Summary

V_{DS}	40	V
$R_{DS(on),max}$	2.2	mΩ
I_D	100	A
Q_{OSS}	33	nC
$Q_G(0V..10V)$	37	nC

PG-TDSON-8


Type	Package	Marking
BSC022N04LS	PG-TDSON-8	022N04LS

Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$V_{GS}=10\text{ V}, T_C=25\text{ °C}$	100	A
		$V_{GS}=10\text{ V}, T_C=100\text{ °C}$	85	
		$V_{GS}=4.5\text{ V}, T_C=25\text{ °C}$	100	
		$V_{GS}=4.5\text{ V}, T_C=100\text{ °C}$	70	
		$V_{GS}=10\text{ V}, T_A=25\text{ °C}, R_{thJA}=50\text{ K/W}^2)$	25	
Pulsed drain current ³⁾	$I_{D,pulse}$	$T_C=25\text{ °C}$	400	
Avalanche current, single pulse	I_{AS}	$T_C=25\text{ °C}$	50	
Avalanche energy, single pulse ⁴⁾	E_{AS}	$I_D=50\text{ A}, R_{GS}=25\text{ Ω}$	70	mJ
Gate source voltage	V_{GS}		±20	V

¹⁾ J-STD20 and JESD22

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

³⁾ See figure 3 for more detailed information

⁴⁾ See figure 13 for more detailed information

Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	69	W
		$T_A=25\text{ °C}$, $R_{\text{thJA}}=50\text{ K/W}^2)$	2.5	
Operating and storage temperature	T_j, T_{stg}		-55 ... 150	°C
IEC climatic category; DIN IEC 68-1			55/150/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics

Thermal resistance, junction - case	R_{thJC}		-	-	1.8	K/W
		top	-	-	20	
Device on PCB	R_{thJA}	6 cm ² cooling area ²⁾	-	-	50	

Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified

Static characteristics

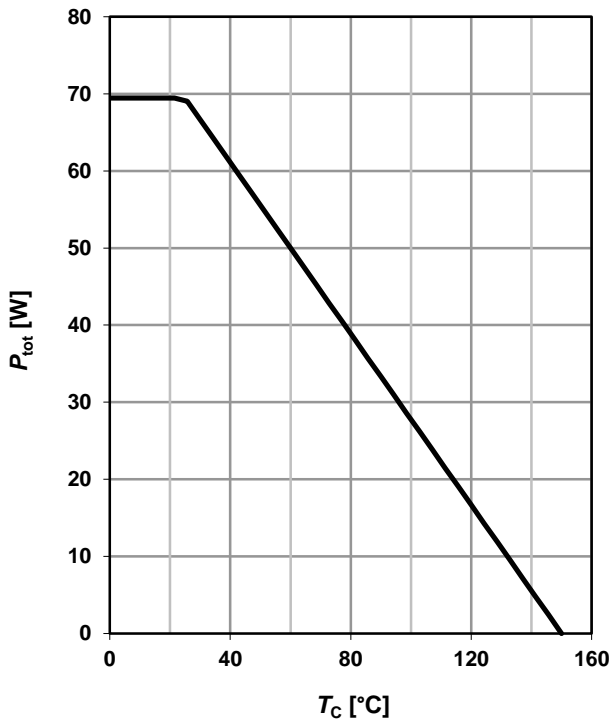
Drain-source breakdown voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}}=0\text{ V}$, $I_{\text{D}}=1\text{ mA}$	40	-	-	V
Gate threshold voltage	$V_{\text{GS(th)}}$	$V_{\text{DS}}=V_{\text{GS}}$, $I_{\text{D}}=250\text{ }\mu\text{A}$	1.2	-	2	
Zero gate voltage drain current	I_{DSS}	$V_{\text{DS}}=40\text{ V}$, $V_{\text{GS}}=0\text{ V}$, $T_j=25\text{ °C}$	-	0.1	1	μA
		$V_{\text{DS}}=40\text{ V}$, $V_{\text{GS}}=0\text{ V}$, $T_j=125\text{ °C}$	-	10	100	
Gate-source leakage current	I_{GSS}	$V_{\text{GS}}=20\text{ V}$, $V_{\text{DS}}=0\text{ V}$	-	10	100	nA
Drain-source on-state resistance	$R_{\text{DS(on)}}$	$V_{\text{GS}}=4.5\text{ V}$, $I_{\text{D}}=50\text{ A}$	-	2.3	3.2	m Ω
		$V_{\text{GS}}=10\text{ V}$, $I_{\text{D}}=50\text{ A}$	-	1.8	2.2	
Gate resistance	R_{G}		-	1.1	-	Ω
Transconductance	g_{fs}	$ V_{\text{DS}} >2 I_{\text{D}} R_{\text{DS(on)max}}$, $I_{\text{D}}=50\text{ A}$	90	180	-	S

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics						
Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=20\text{ V}, f=1\text{ MHz}$	-	2600	-	pF
Output capacitance	C_{oss}		-	750	-	
Reverse transfer capacitance	C_{rss}		-	60	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=20\text{ V}, V_{GS}=10\text{ V}, I_D=50\text{ A}, R_{G,ext}=1.6\ \Omega$	-	6.1	-	ns
Rise time	t_r		-	6.8	-	
Turn-off delay time	$t_{d(off)}$		-	26	-	
Fall time	t_f		-	5.0	-	
Gate Charge Characteristics⁵⁾						
Gate to source charge	Q_{gs}	$V_{DD}=20\text{ V}, I_D=50\text{ A}, V_{GS}=0\text{ to }10\text{ V}$	-	6.8	-	nC
Gate charge at threshold	$Q_{g(th)}$		-	4.2	-	
Gate to drain charge	Q_{gd}		-	6.0	-	
Switching charge	Q_{sw}		-	8.7	-	
Gate charge total	Q_g		-	37	-	
Gate plateau voltage	$V_{plateau}$		-	2.6	-	V
Gate charge total	Q_g	$V_{DD}=20\text{ V}, I_D=50\text{ A}, V_{GS}=0\text{ to }4.5\text{ V}$	-	19	-	nC
Gate charge total, sync. FET	$Q_{g(sync)}$	$V_{DS}=0.1\text{ V}, V_{GS}=0\text{ to }4.5\text{ V}$	-	15	-	
Output charge	Q_{oss}	$V_{DD}=20\text{ V}, V_{GS}=0\text{ V}$	-	33	-	
Reverse Diode						
Diode continuous forward current	I_S	$T_C=25\text{ }^\circ\text{C}$	-	-	69	A
Diode pulse current	$I_{S,pulse}$		-	-	400	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=50\text{ A}, T_j=25\text{ }^\circ\text{C}$	-	0.85	1	V
Reverse recovery time	t_{rr}	$V_R=20\text{ V}, I_F=50\text{ A}, di_F/dt=400\text{ A}/\mu\text{s}$	-	20	-	ns
Reverse recovery charge	Q_{rr}		-	36	-	nC

⁵⁾ See figure 16 for gate charge parameter definition

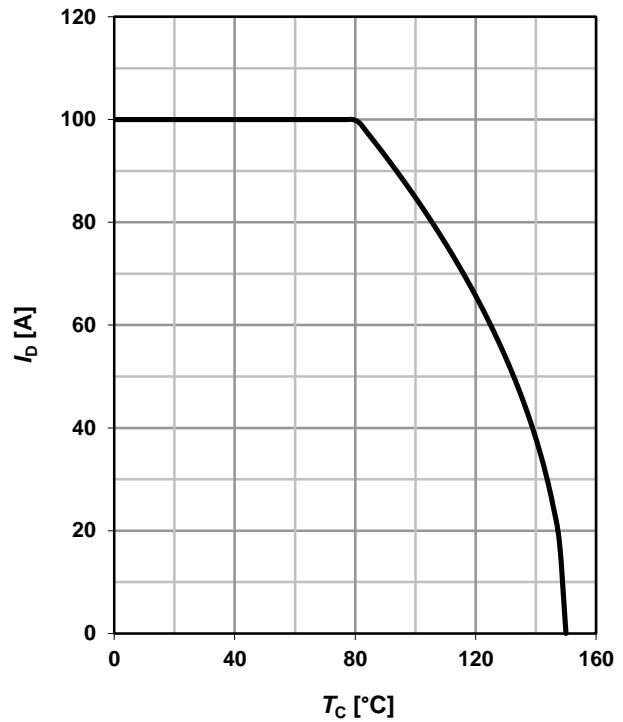
1 Power dissipation

$P_{tot}=f(T_C)$



2 Drain current

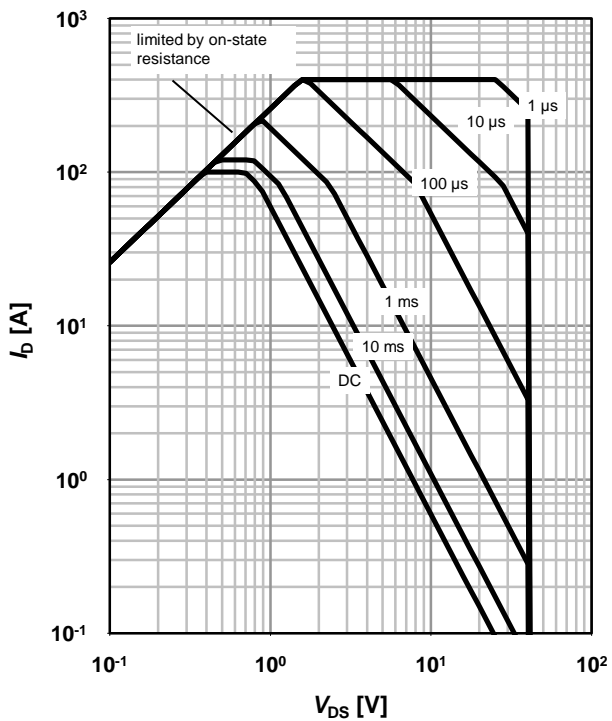
$I_D=f(T_C); V_{GS} \geq 10\text{ V}$



3 Safe operating area

$I_D=f(V_{DS}); T_C=25\text{ °C}; D=0$

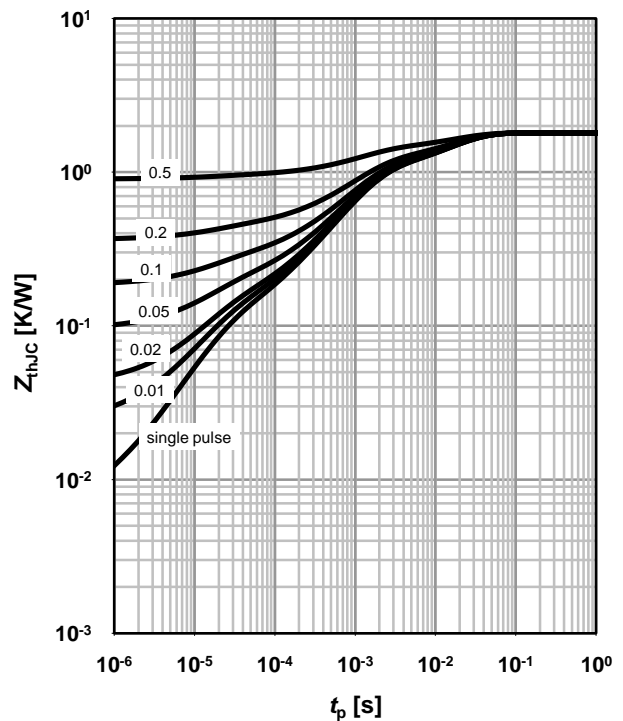
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC}=f(t_p)$

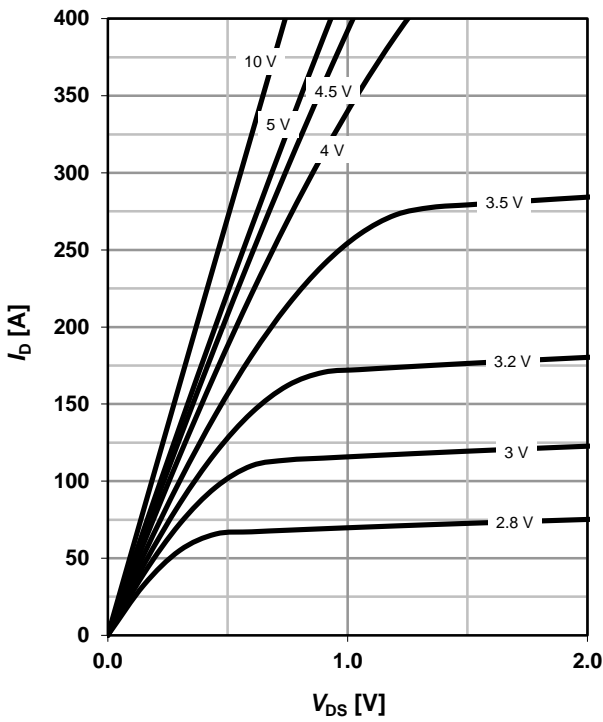
parameter: $D=t_p/T$



5 Typ. output characteristics

$I_D = f(V_{DS}); T_j = 25\text{ °C}$

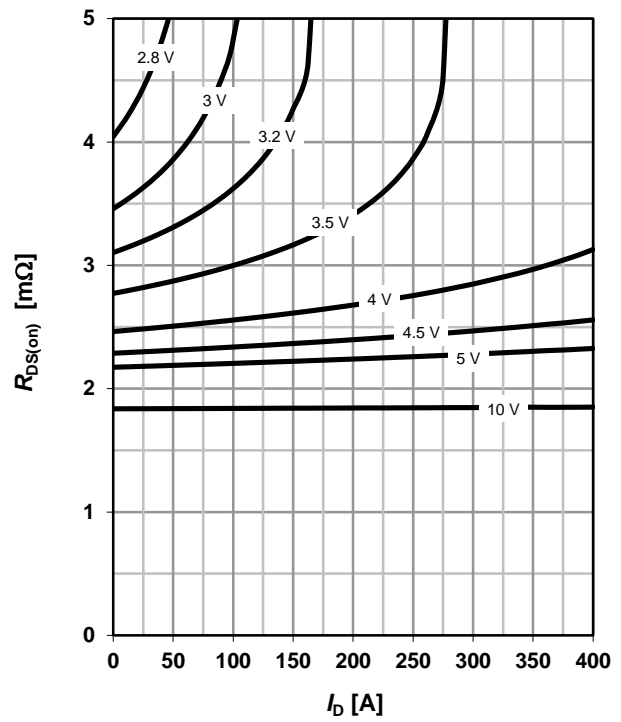
parameter: V_{GS}



6 Typ. drain-source on resistance

$R_{DS(on)} = f(I_D); T_j = 25\text{ °C}$

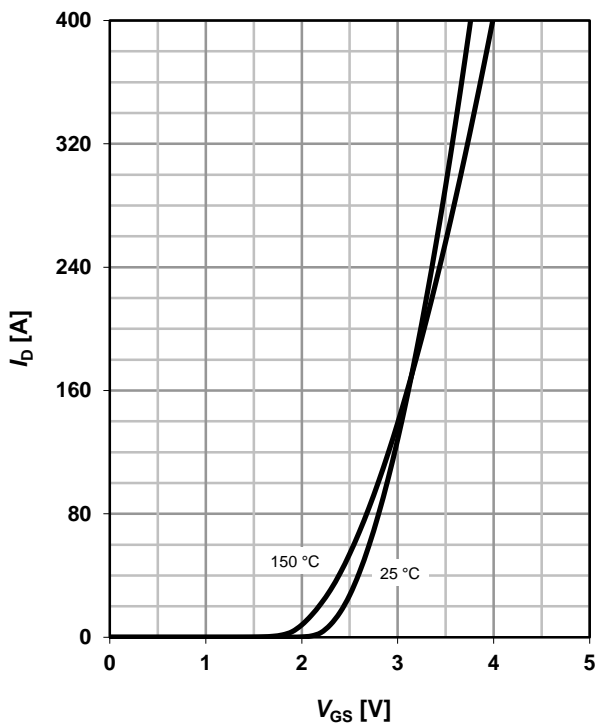
parameter: V_{GS}



7 Typ. transfer characteristics

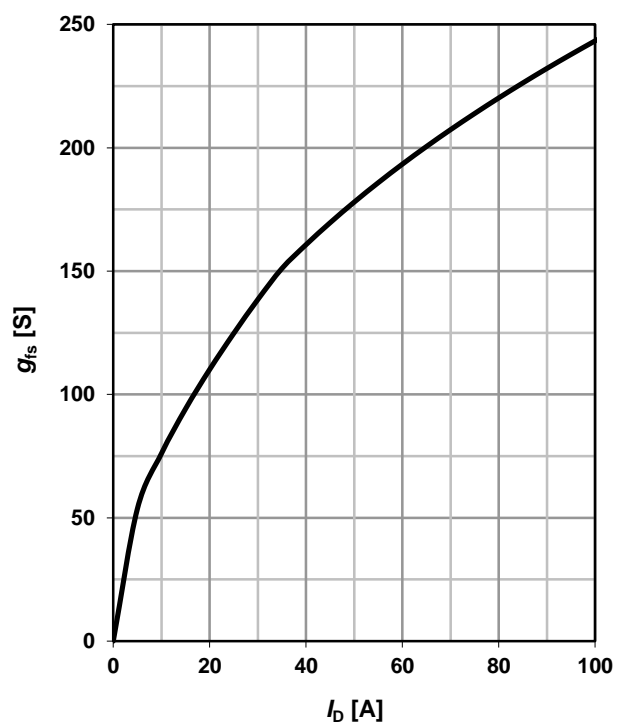
$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}$

parameter: T_j



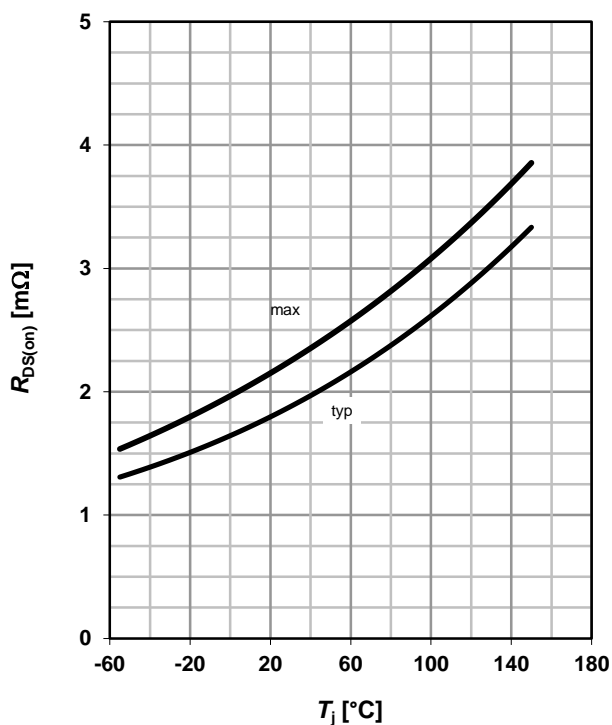
8 Typ. forward transconductance

$g_{fs} = f(I_D); T_j = 25\text{ °C}$



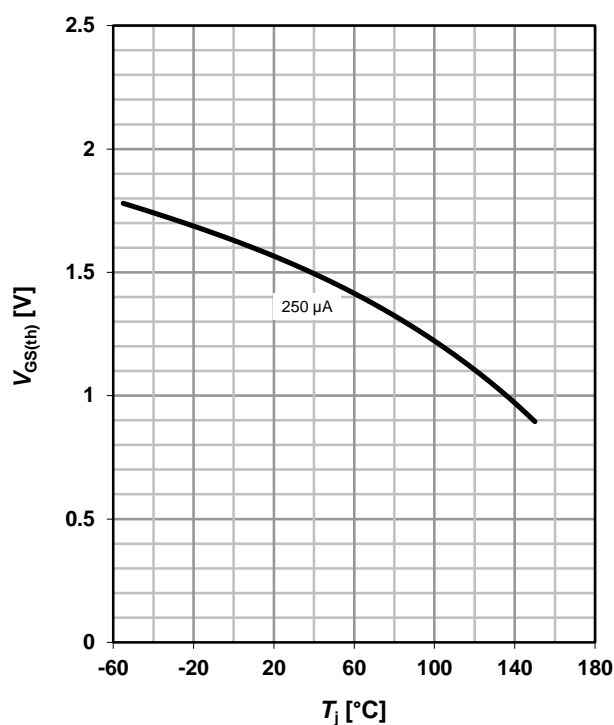
9 Drain-source on-state resistance

$R_{DS(on)}=f(T_j); I_D=50\text{ A}; V_{GS}=10\text{ V}$



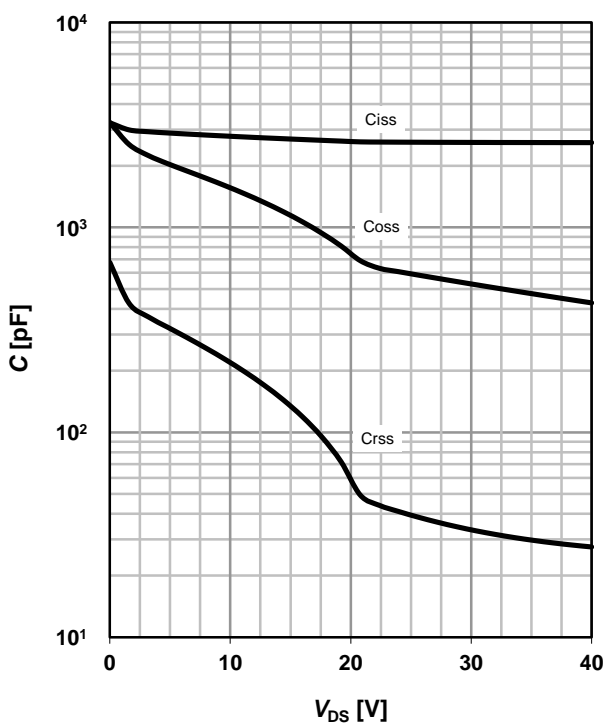
10 Typ. gate threshold voltage

$V_{GS(th)}=f(T_j); V_{GS}=V_{DS}; I_D=250\text{ }\mu\text{A}$



11 Typ. capacitances

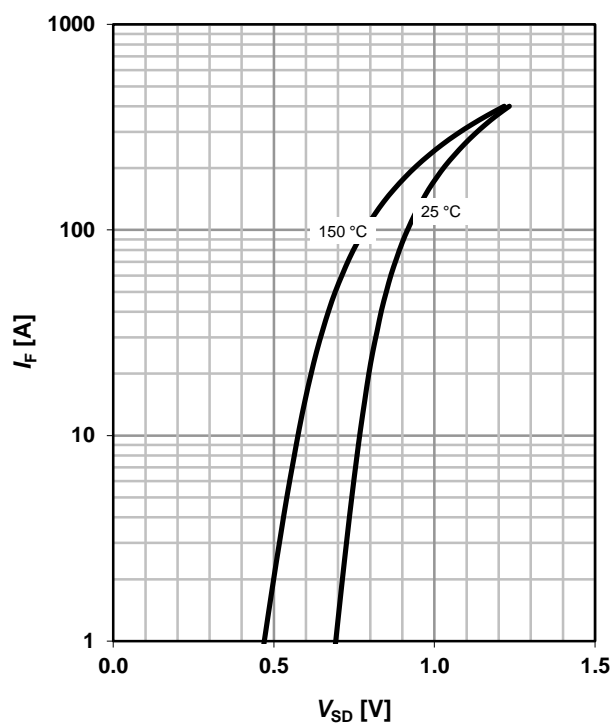
$C=f(V_{DS}); V_{GS}=0\text{ V}; f=1\text{ MHz}$



12 Forward characteristics of reverse diode

$I_F=f(V_{SD})$

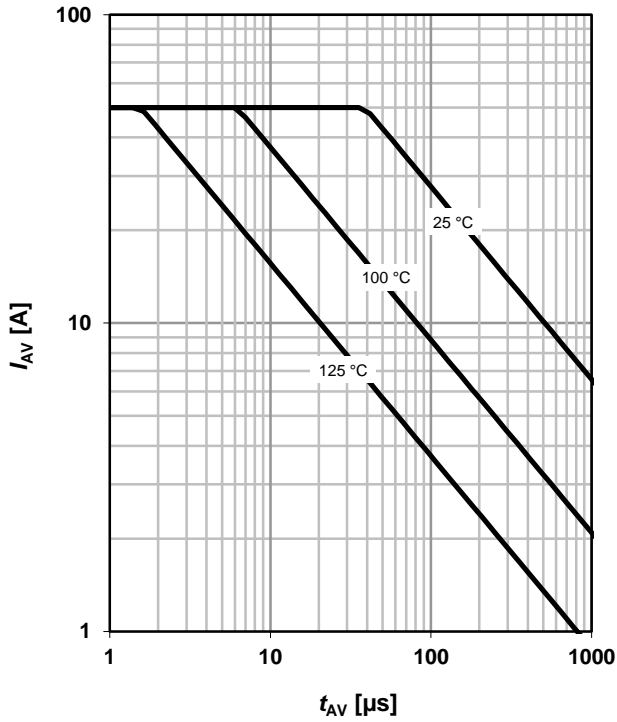
parameter: T_j



13 Avalanche characteristics

$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$

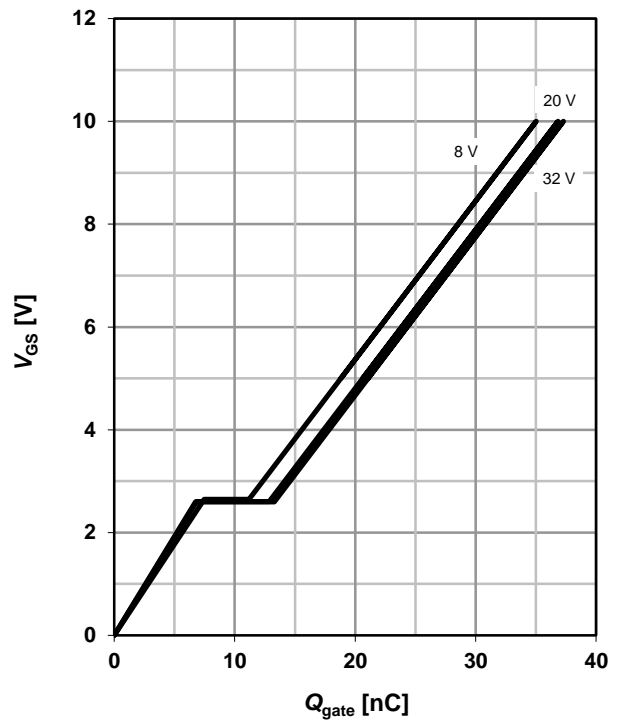
parameter: $T_{j(start)}$



14 Typ. gate charge

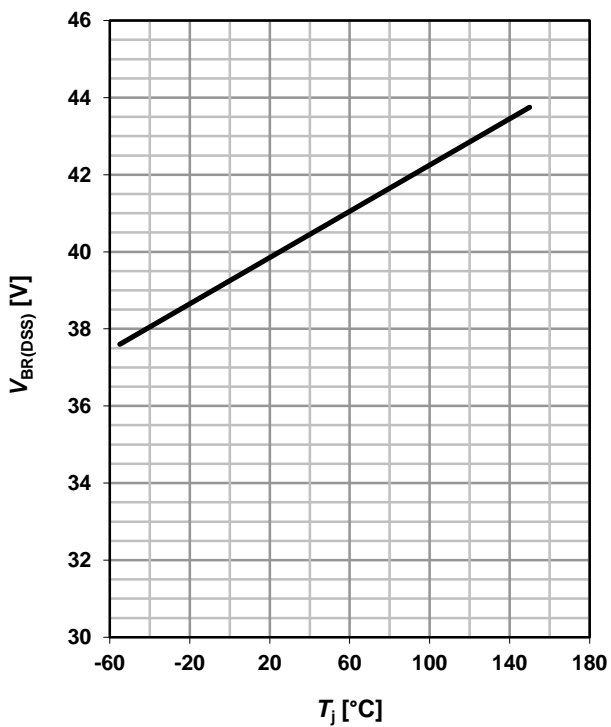
$V_{GS}=f(Q_{gate}); I_D=50 \text{ A pulsed}$

parameter: V_{DD}

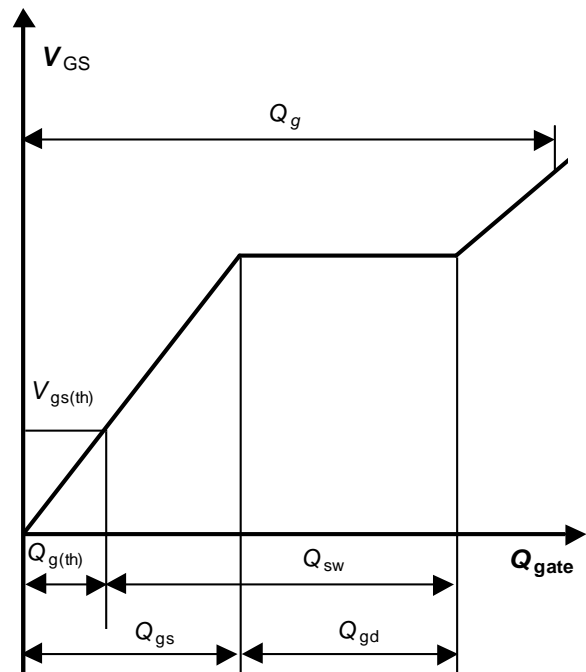


15 Drain-source breakdown voltage

$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$



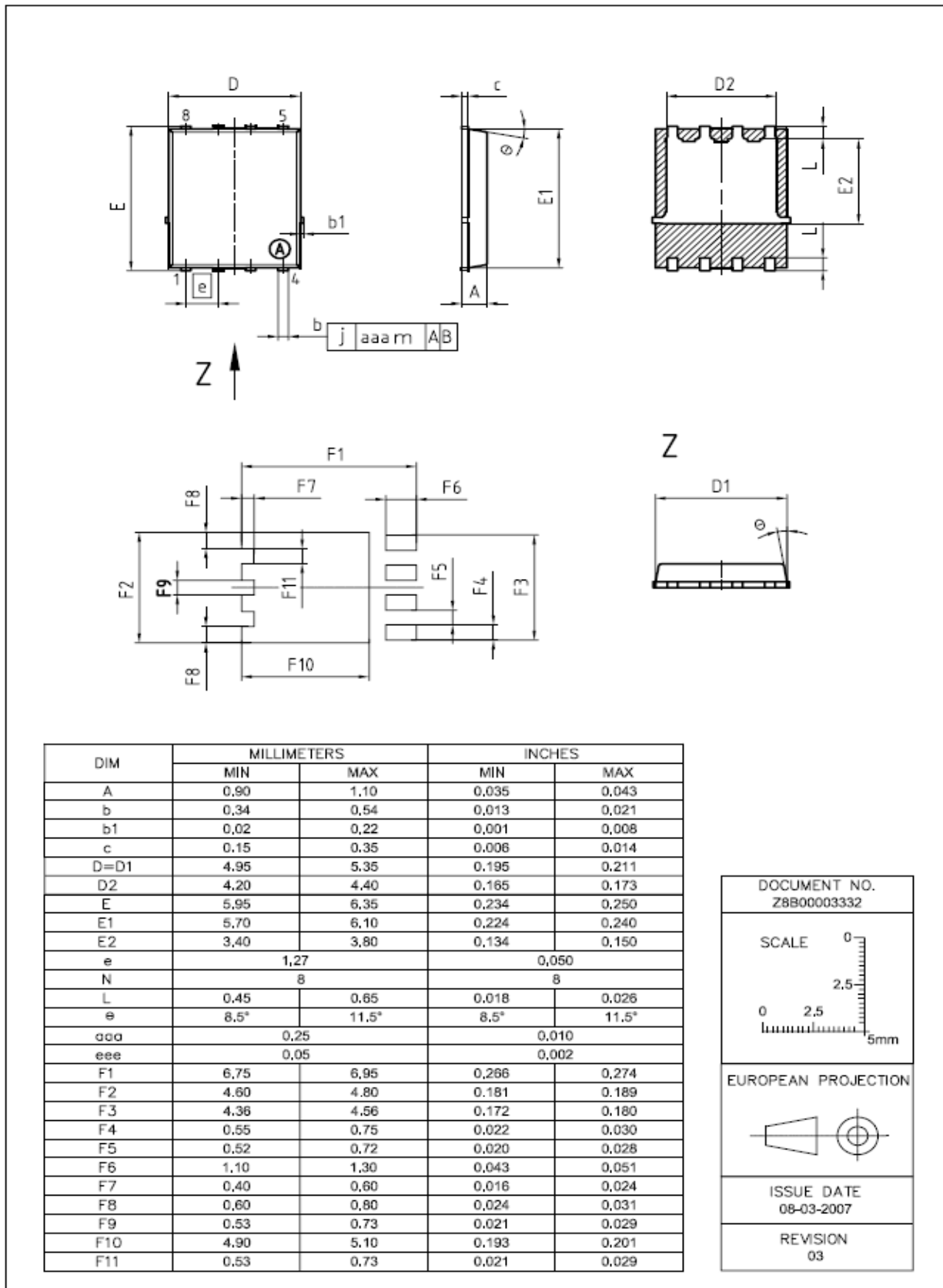
16 Gate charge waveforms



Package Outline

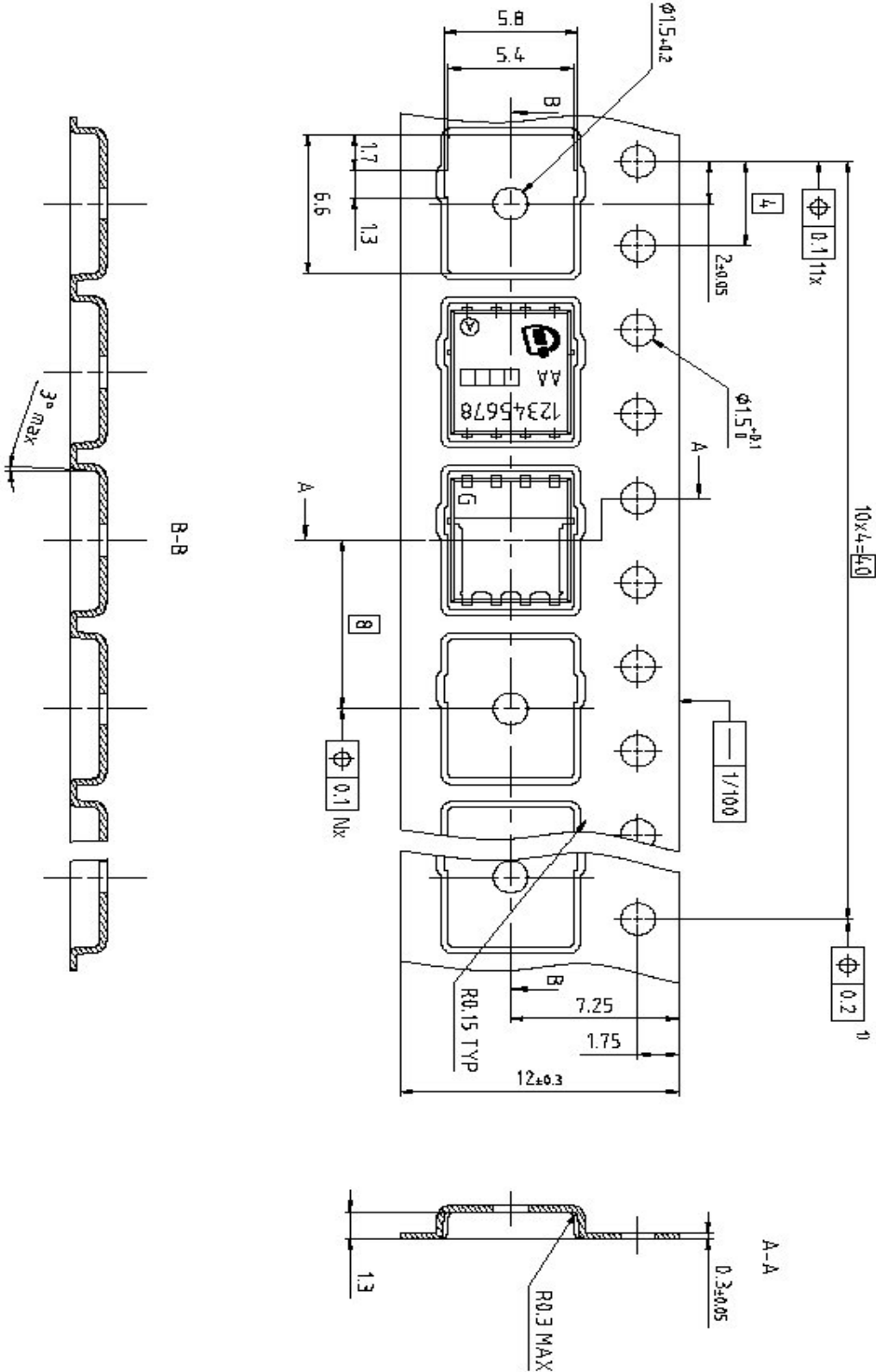
PG-TDSON-8

PG-TDSON-8: Outline



Package Outline

PG-TDSON-8: Tape



Dimensions in mm

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