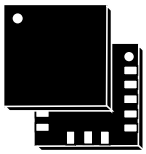
LIS331EB

iNEMO-A advanced MEMS: 3D high-performance accelerometer and signal processor

Datasheet - production data



LGA-16 (3x3x1 mm)

Features

- Motion sensor:
  - Ultra-low-power mode consumption down to 10 µA
  - ±2*g*/±4*g*/±6*g*/±8*g*/±16*g* selectable full scale
  - Data rate: 3.125 Hz to 1.6 kHz
  - 16-bit data output
  - 2 embedded state machines
  - Embedded self-test
  - 10000 *g* high shock survivability
  - ECOPACK® RoHS and “Green” compliant
- Signal processor:
  - Brain: ARM-based, 32-bit Cortex-M0 CPU core
  - 64 Kbyte Flash memory
  - 128 Kbyte SRAM including 64 Kbyte with error code correction (ECC)
  - I^2C master port
  - I^2C slave port
  - SPI master/slave
  - 4-wire UART
  - 11 programmable GPIOs
  - Low-power features
  - 8 x 32-bit dual timers, watchdog timer (WDG), Cortex-M0 system tick (SysTick) timer
  - Standard 4-wire JTAG and 2-wire SWD
  - 80 MHz / 32 kHz RC / up to 80 MHz from single-ended external clock

Applications

- Sensor hubs
- Sensor fusion
- Gaming and virtual reality input devices
- LBS and augmented reality
- Enhanced navigation and motion tracking
- Vibration monitoring and compensation
- Pedometers

Description

The LIS331EB is an advanced low-power high-performance smart sensor system which includes a three-axis linear accelerometer and Cortex-M0 core with 64 KB Flash, 128 KB SRAM, 8 dual timers, 2 I^2C (master/slave), 1 SPI (master/slave) and 1 UART (transmitter/receiver) in a 3x3x1 mm LGA package. The device features ultra-low-power operational modes that allow advanced power saving and smart sleep-to-wakeup functions. The LIS331EB has user-selectable full scales and is capable of measuring accelerations with selectable output data rates up to 1.6 kHz. An embedded self-test capability allows the user to check the functioning of the sensor in the final application. One possible use of the LIS331EB is as a sensor hub. For example, the device can collect inputs from the accelerometer (embedded), gyroscopes, compasses, pressure and other sensors through the master I^2C and elaborates/fuses together 9 or 10 axes (iNemo Engine software) to provide quaternions to the main application processor. The LIS331EB is ECOPACK®, RoHS and “Green” compliant.

Table 1. Device summary

Order codes	Temperature range [°C]	Package	Packaging
LIS331EB	-40 to +85	LGA-16	Tray
LIS331EBTR	-40 to +85	LGA-16	Tape and reel

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1 Block diagram and pin description

1.1 Block diagram

Figure 1. LIS331EB application block diagram

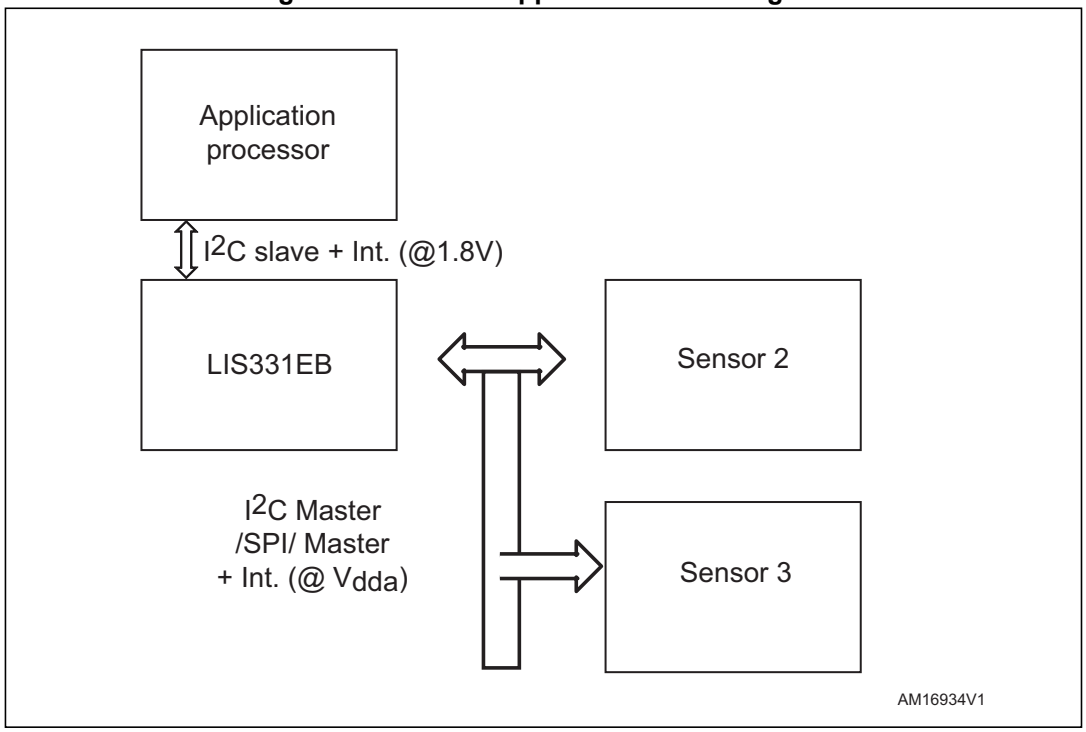


Figure 2. LIS331EB smart sensor block diagram

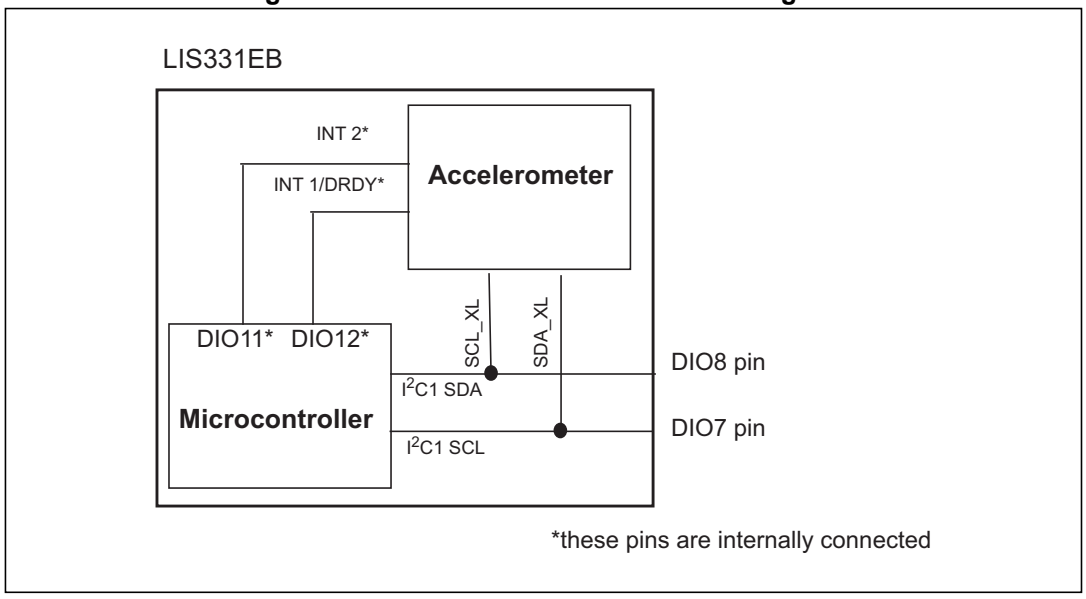


Figure 3. Accelerometer block diagram

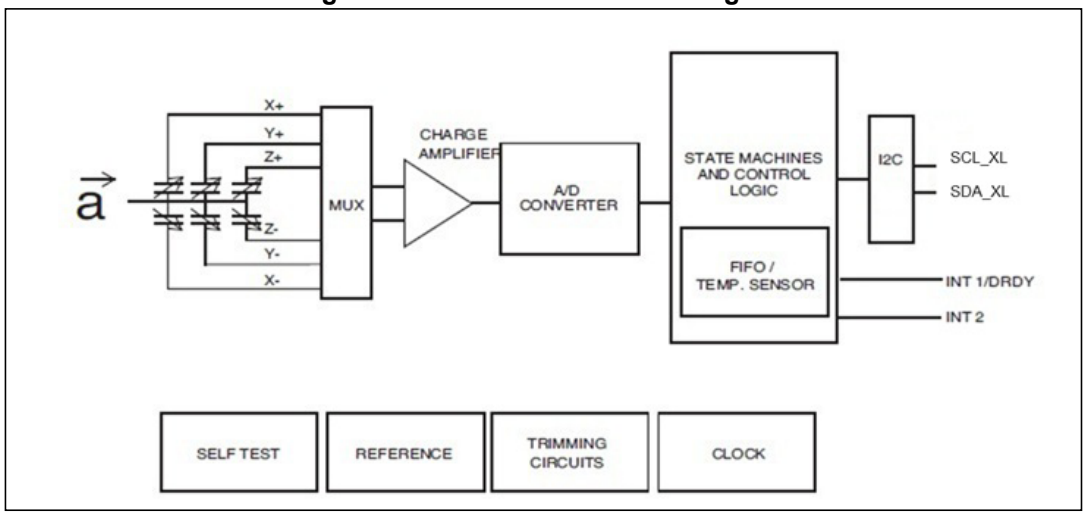
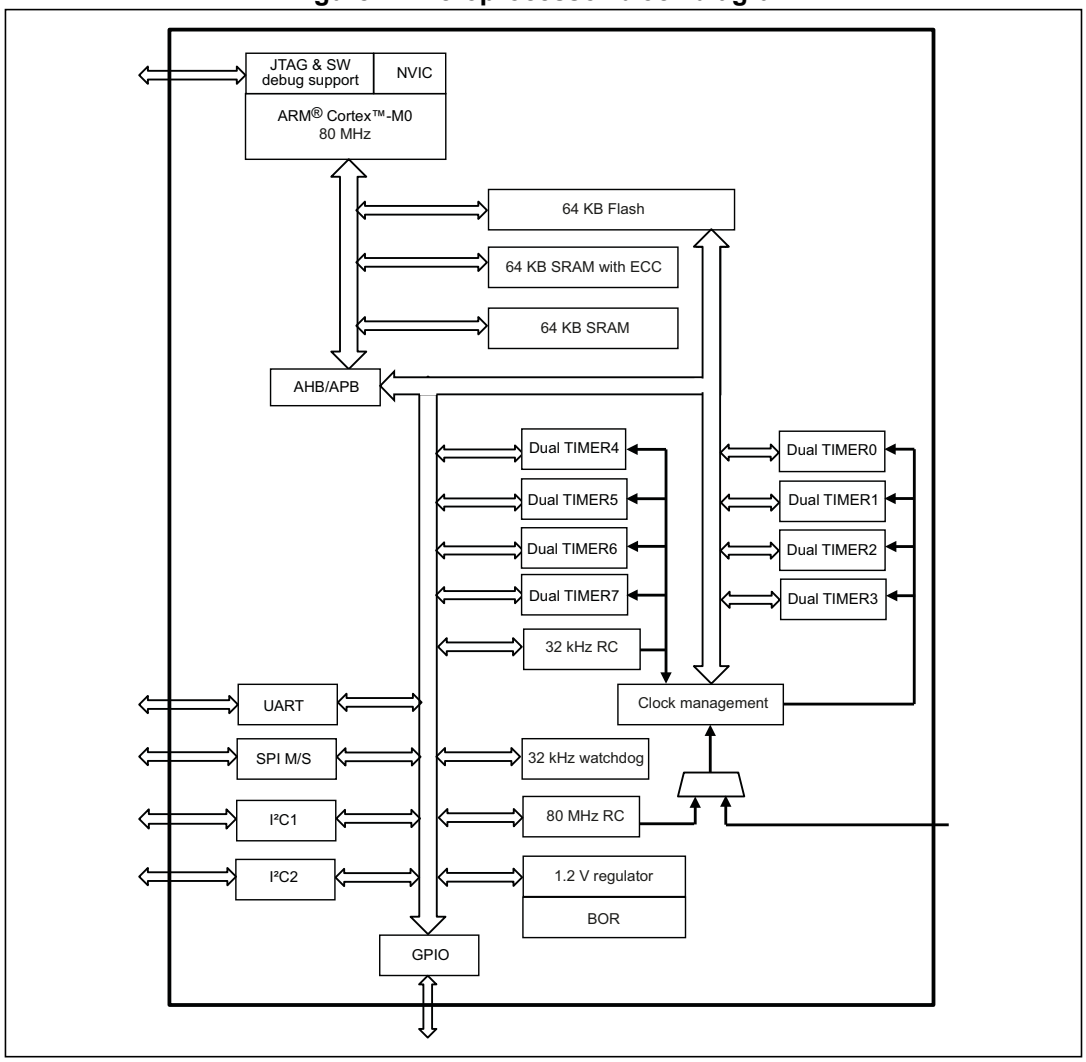


Figure 4. Microprocessor block diagram



Legend: NVIC = nested vectored interrupt controller, GPIO = general-purpose input/output

1.2 Pin description

Figure 5. Pin connections

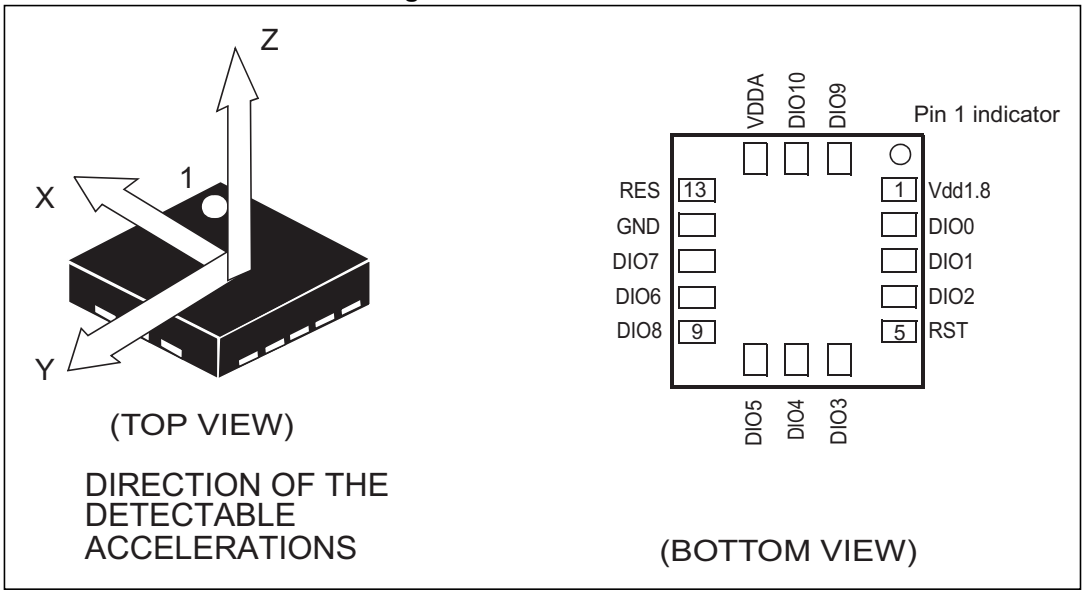


Table 2. Pin description

Pin#	Name	Function	I/O level
1	Vdd1.8	Power supply for I/O pins	
2	DIO0	GPIO0 / SW_TDIO / JTAG TMS / UART_CTS	Vdd1.8
3	DIO1	GPIO1 / SW_TCK / JTAG TCK / UART_RTS	Vdd1.8
4	DIO2	GPIO2 / I^2C2_SCL (slave) / UART_TXD	Vdd1.8
5	RST	Microcontroller reset	Vdd1.8
6	DIO3	GPIO3 / I^2C2_SDA (slave) / UART_RXD	Vdd1.8
7	DIO4	GPIO4 / JTAG TDO	Vdd1.8
8	DIO5	GPIO5 / JTAG TDI / Clock input	Vdd1.8
9	DIO8	GPIO8 / I^2C1_SDA (master) / SPI_OUT	VDDA
10	DIO6	GPIO6 / 16 MHz clock output / Clock 32 kHz	VDDA
11	DIO7	GPIO7 / I^2C1_SCL (master) / SPI_Clock	VDDA
12	GND	0 V supply	
13	RES	Connect to decoupling capacitor for 1.2 V digital regulator to GND	
14	VDDA	Power supply for I/O pins 1.8 - 3.3 V	
15	DIO10	GPIO10 / SPI_Input	VDDA
16	DIO9	GPIO9 / SPI_CS	VDDA

Note: DIO11, DIO12 are internally connected to INT2 and INT1/DRDY accelerometer pins.

2 LIS331EB application hints

Figure 6. Application circuit with I²C sensors

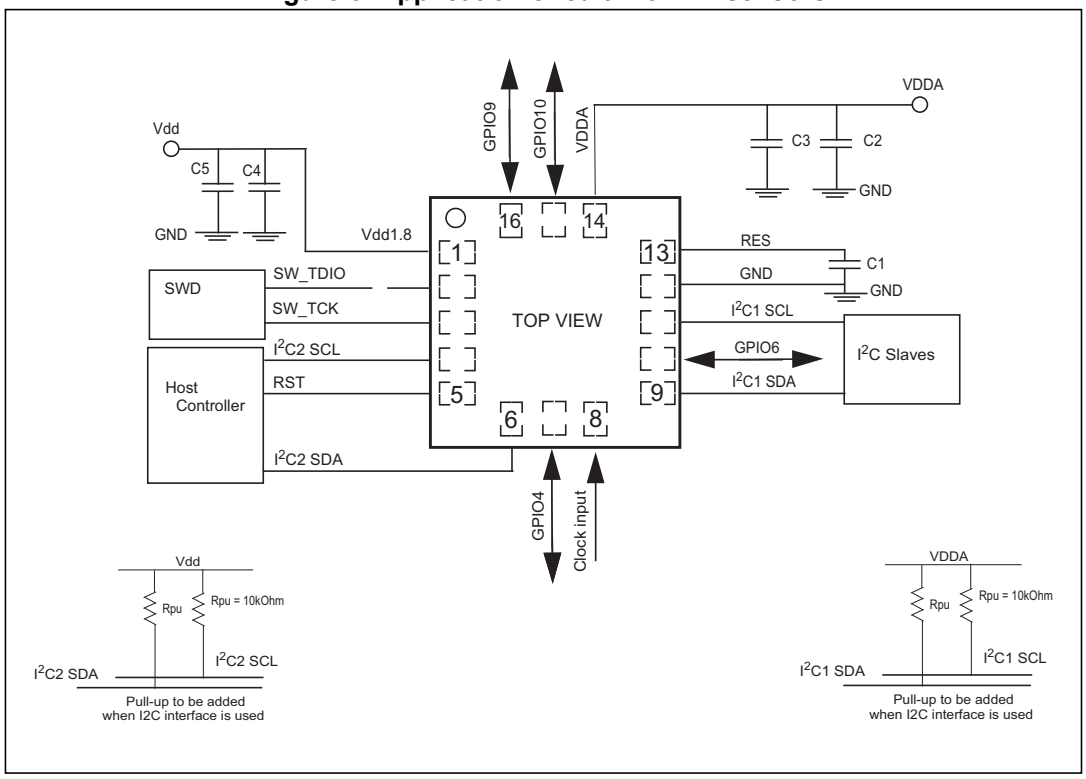
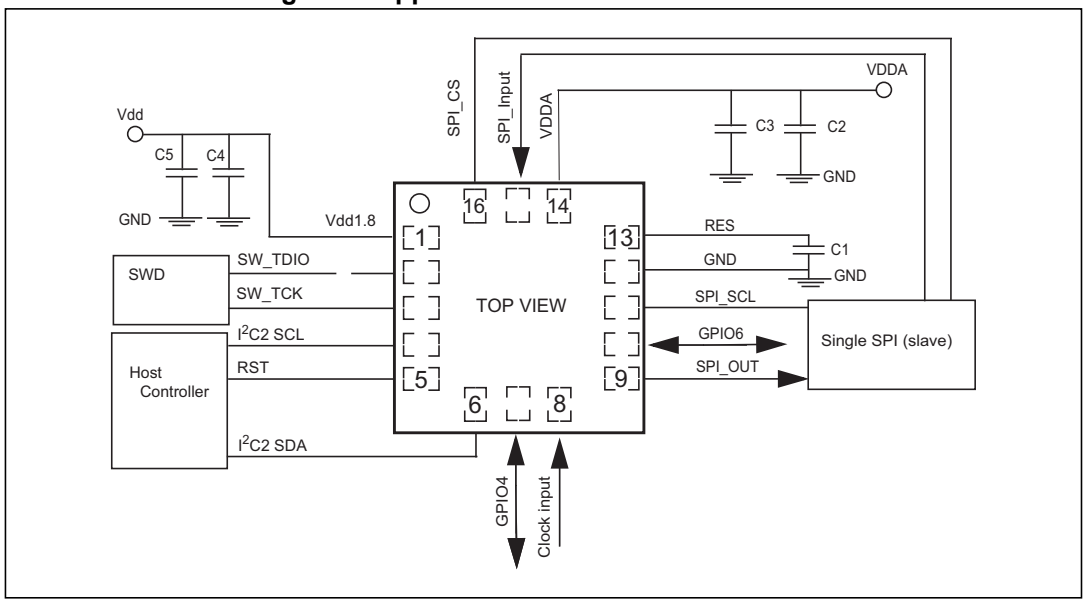


Table 3. External components

Component	Description	Value
C1	Decoupling capacitor for 1.2 V digital regulator	220 nF
C2	Decoupling capacitor for 1.8 V - 3.6 V digital regulator (HF)	100 nF
C3	Decoupling capacitor for 1.8 V - 3.6 V digital regulator (LF)	10 µF
C4	Decoupling capacitor for 1.8 V digital regulator (LF)	10 µF
C5	Decoupling capacitor for 1.8 V digital regulator (HF)	100 nF

Figure 7. Application circuit with SPI sensors



For external components refer to *Table 3.*

3 Accelerometer mechanical and electrical specifications

3.1 Mechanical characteristics

@ VDDA = 2.5 V, T = 25 °C unless otherwise noted[a].

Table 4. Mechanical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.[1]	Max.	Unit
FS	Measurement range[2]	FS bit set to 000		±2.0		*g*
		FS bit set to 001		±4.0		*g*
		FS bit set to 010		±6.0		*g*
		FS bit set to 011		±8.0		*g*
		FS bit set to 100		±16.0		*g*
So	Sensitivity	FS bit set to 000		0.061		mg/digit
		FS bit set to 001		0.122		mg/digit
		FS bit set to 010		0.183		mg/digit
		FS bit set to 011		0.244		mg/digit
		FS bit set to 100		0.732		mg/digit
TCSo	Sensitivity change vs. temperature	FS bit set to 00		0.01		%/°C
TyOff	Typical zero-*g* level offset accuracy[3]	FS bit set to 00		±40		m*g*
TCOff	Zero-*g* level change vs. temperature	Max. delta from 25 °C		±0.5		m*g*/°C
An	Acceleration noise density	FS bit set to 00, normal mode, ODR = 100 Hz		150		µ*g*/ sqrt(Hz)
ST	Self test positive difference[4]	± 2 *g* range, X,Y-axis ST2,ST1 = [01]		140		m*g*
		± 2 *g* range, Z-axis ST2,ST1 = [01]		590		
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. Verified by wafer level test and measurement of initial offset and sensitivity.
3. Typical zero-*g* level offset value after MSL3 preconditioning.
4. “Self-test output change” is defined as: OUTPUT[mg]$_{(}$ *CTRL_REG5 (24h)* $_{\text{ST2, ST1 bits=01)}}$ - OUTPUT[mg]$_{(}$*CTRL_REG5 (24h)* $_{\text{ST2, ST1 bits=00)}}$

a. The product is factory calibrated at 2.5 V. The operational power supply range is from 1.71 V to 3.6 V.

3.2 Electrical characteristics

@ VDDA = 2.5 V, T = 25 °C unless otherwise noted[b].

Table 5. Electrical characteristics (1)

Symbol	Parameter	Test conditions	Min.	Typ.(2)	Max.	Unit
VDDA	Core and I/O pins supply voltage		1.71	1.8 - 3.3	3.6	V
IddA	Current consumption in active mode	1.6 kHz ODR		225		µA
		3.125 Hz ODR		11		µA
IddPdn	Current consumption in power-down/standby mode			2		µA
VIH	Digital high-level input voltage		0.8*VDDA			V
VIL	Digital low-level input voltage				0.2*VDDA	V
VOH	High-level output voltage		0.9*VDDA			V
VOL	Low-level output voltage				0.1*VDDA	V
Top	Operating temperature range		-40		+85	°C

1. The product is factory calibrated at 2.5 V. The operational power supply range is from 1.71 V to 3.6 V.
2. Typical specifications are not guaranteed.

b. The product is factory calibrated at 2.5 V. The operational power supply range is from 1.71 V to 3.6 V.

3.3 Communication interface characteristics

3.3.1 I²C - inter IC control interface

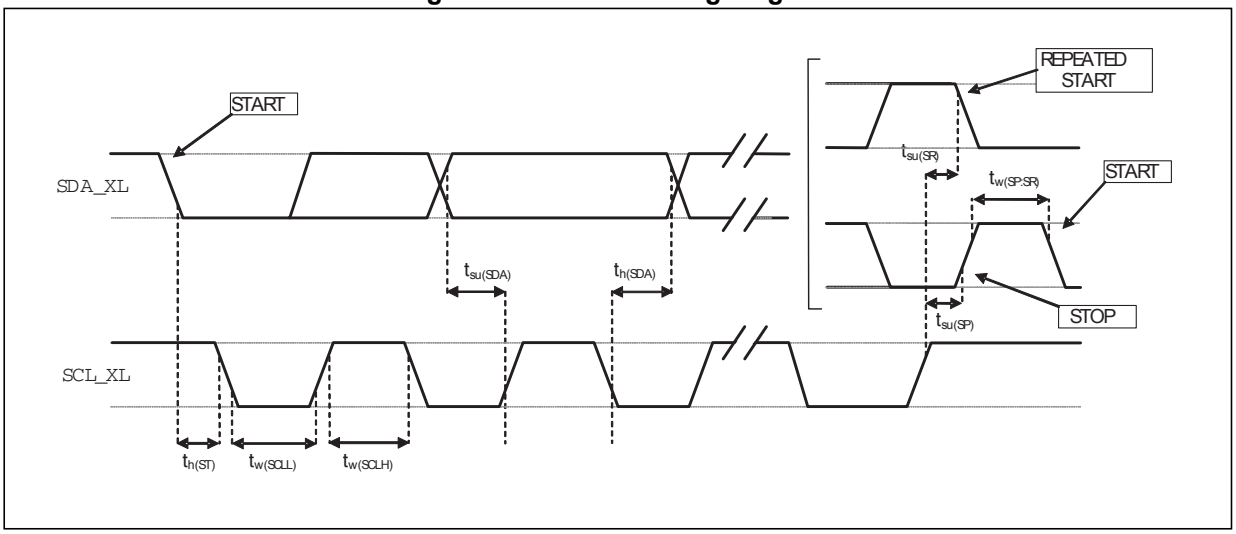
Subject to general operating conditions for VDDA and Top.

Table 6. I²C slave timing values

Symbol	Parameter	I²C standard mode (1)		I²C fast mode (1)		Unit
		Min.	Max.	Min.	Max.	
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	kHz
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0.01	3.45	0.01	0.9	µs
$t_{h(ST)}$	START condition hold time	4		0.6		µs
$t_{su(SR)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(SP)}$	STOP condition setup time	4		0.6		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	4.7		1.3		

1. Data based on standard I²C protocol requirement, not tested in production.

Figure 8. I²C slave timing diagram



Note: Measurement points are done at 0.2·VDDA and 0.8·VDDA, for both ports.

3.4 Terminology

3.4.1 Sensitivity

Sensitivity describes the gain of the sensor and can be determined by applying 1 *g* acceleration to it. As the sensor can measure DC accelerations this can be done easily by pointing the axis of interest towards the center of the Earth, noting the output value, rotating the sensor by 180 degrees (pointing to the sky) and noting the output value again. By doing so, ±1 *g* acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and time. The sensitivity tolerance describes the range of sensitivities of a large population of sensors.

3.4.2 Zero-*g* level

Zero-*g* level offset (TyOff) describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady-state on a horizontal surface measures 0 *g* on the X-axis and 0 *g* on the Y-axis, whereas the Z-axis measures 1 *g*. The output is ideally in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as two's complement number). A deviation from the ideal value in this case is called Zero-*g* offset. Offset is to some extent a result of stress to the MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature, see "Zero-*g* level change vs. temperature" in *Table 4*. The Zero-*g* level tolerance (TyOff) describes the standard deviation of the range of Zero-*g* levels of a population of sensors.

3.5 Functionality

3.5.1 Self-test

The self-test allows checking the sensor functionality without moving it. The self-test function is off when the self-test bit (ST) is programmed to '0'. When the self-test bit is programmed to '1', an actuation force is applied to the sensor, simulating a definite input acceleration. In this case the sensor outputs exhibit a change in their DC levels which are related to the selected full scale through the device sensitivity. When the self-test is activated, the device output level is given by the algebraic sum of the signals produced by the acceleration acting on the sensor and by the electrostatic test force. If the output signals change within the amplitude specified in *Table 4*, then the sensor is working properly and the parameters of the interface chip are within the defined specifications.

3.6 Sensing element

A proprietary process is used to create a surface micromachined accelerometer. The technology allows processing suspended silicon structures which are attached to the substrate in a few points called anchors and are free to move in the direction of the sensed acceleration. To be compatible with traditional packaging techniques, a cap is placed on top of the sensing element to avoid blocking the moving parts during the molding phase of the plastic encapsulation.

When an acceleration is applied to the sensor, the proof mass displaces from its nominal position, causing an imbalance in the capacitive half bridge. This imbalance is measured using charge integration in response to a voltage pulse applied to the capacitor.

At steady-state the nominal value of the capacitors are a few pF and when an acceleration is applied, the maximum variation of the capacitive load is in the fF range.

3.7 IC interface

The complete measurement chain is made up of a low-noise capacitive amplifier which converts the capacitive unbalancing of the MEMS sensor into an analog voltage made available to the user through an analog-to-digital converter.

The acceleration data may be accessed through an I^2C interface, therefore making the device particularly suitable for direct interfacing with a microcontroller.

The LIS331EB features a Data-Ready signal (DRDY) which indicates when a new set of measured acceleration data is available, therefore simplifying data synchronization in the digital system that uses the device.

3.8 Factory calibration

The IC interface is factory calibrated for sensitivity (So) and Zero-*g* level (TyOff).

The trim values are stored inside the device in nonvolatile memory. Any time the device is turned on, the trim parameters are downloaded into the registers to be used during active operation. This allows using the device without further calibration.

4 Accelerometer digital main blocks

4.1 State machine

The LIS331EB embeds two state machines capable of running a user-defined program.

The program is made up of a set of instructions that define the transition to successive states. Conditional branches are possible.

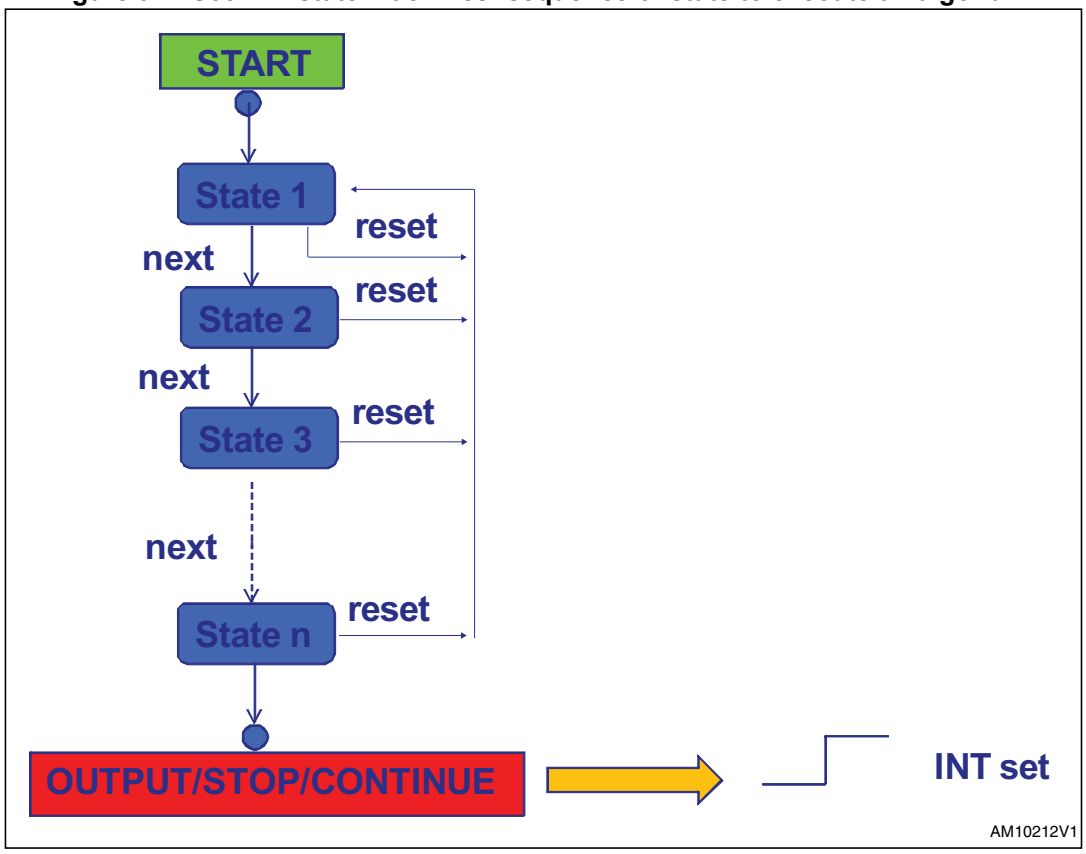
From each state (n) it is possible to transition to the next state (n+1) or to a reset state. The transition to a reset point occurs when the “RESET condition” is true; the transition to the next step happens when “NEXT condition” is true.

An interrupt is triggered when an output/stop/continue state is reached.

Each state machine allows implementing gesture recognition in a flexible way. Free-fall, wake-up, 4D/6D orientation, pulse counter and step recognition, click/double-click, shake/double-shake, face-up/face-down, and turn/double-turn features are managed as follows:

- Code and parameters are loaded by the host into dedicated memory areas for the state program
- State program with timing based on ODR or decimated time
- Possibility of conditional branches

Figure 9. LIS331EB state machines: sequence of state to execute an algorithm



4.2 FIFO

The LIS331EB embeds FIFO acceleration data for each of the three output channels, X, Y, and Z. This allows consistent power saving for the system, since the host processor does not need to continuously poll data from the sensor, but it can wake up only when needed and burst the significant data out from the FIFO. This buffer can work according to four different modes: Bypass mode, FIFO mode, Stream mode and Stream-to-FIFO mode. Each mode is selected by the FIFO_MODE bits. Programmable Watermark level, FIFO_empty or FIFO_Full events can be enabled to generate dedicated interrupts on the INT1/2 pins internally connected to the microcontroller (DIO11 and DIO12).

4.2.1 Bypass mode

In Bypass mode, the FIFO is not operational and for this reason it remains empty. For each channel only the first address is used. The remaining FIFO slots are empty.

4.2.2 FIFO mode

In FIFO mode, data from X, Y, and Z channels are stored in the FIFO. A watermark interrupt can be enabled in order to be raised when the FIFO is filled to the level specified by the internal register. The FIFO continues filling until it is full. When full, the FIFO stops collecting data from the input channels.

4.2.3 Stream mode

In Stream mode, data from the X, Y, and Z measurements are stored in the FIFO. A watermark interrupt can be enabled and set as in FIFO mode. The FIFO continues filling until it's full. When full, the FIFO discards the older data as the new arrive.

4.2.4 Stream-to-FIFO mode

In Stream-to-FIFO mode, data from the X, Y, and Z measurements are stored in the FIFO. A watermark interrupt can be enabled in order to be raised when the FIFO is filled to the level specified by the internal register. The FIFO continues filling until it's full. When full, the FIFO discards the older data as the new arrive. Once a trigger event occurs, the FIFO starts operating in FIFO mode.

4.2.5 Retrieving data from FIFO

FIFO data is read from the *OUT_X (28h - 29h)*, *OUT_Y (2Ah - 2Bh)* and *OUT_Z (2Ch - 2Dh)* registers. When the FIFO is in Stream, Stream-to-FIFO or FIFO mode, a read operation to the *OUT_X (28h - 29h)*, *OUT_Y (2Ah - 2Bh)* or *OUT_Z (2Ch - 2Dh)* registers provides the data stored in the FIFO. Each time data is read from the FIFO, the oldest X, Y, and Z data are placed in the *OUT_X (28h - 29h)*, *OUT_Y (2Ah - 2Bh)* and *OUT_Z (2Ch - 2Dh)* registers and both single read and read_burst operations can be used.

5 Accelerometer digital interfaces

The accelerometer registers embedded inside the LIS331EB can be accessed through the I^2C serial interface. The serial interfaces are mapped to the same pins.

Table 7. Serial interface pin description

Pin name	Pin description
Master SCL (I^2C2 _SCL)	I^2C serial clock (SCL_XL)
Master SDA (I^2C2 _SDA)	I^2C serial data (SDA_XL)

5.1 I^2C serial interface

The LIS331EB I^2C is a bus slave. The I^2C is employed to write data into registers whose content can also be read back.

The relevant I^2C terminology is given in the table below.

Table 8. Serial interface pin description

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I^2C bus: the serial clock line (SCL_XL) and the serial data line (SDA_XL). The latter is a bi-directional line used for sending and receiving the data to/from the interface. Both lines must be connected to VDDA through an external pull-up resistor. When the bus is free, both lines are high.

The I^2C interface is compliant with fast mode (400 kHz) I^2C standards as well as with normal mode.

5.1.1 I²C operation

The transaction on the bus is started through a start (ST) signal. A start condition is defined as a high-to-low transition on the data line while the SCL_XL line is held high. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

The slave address (SAD) associated to the LIS331EB accelerometer is 0011101b.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA_XL line during the acknowledge pulse. The receiver must then pull the data line low so that it remains stable low during the high period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded inside the LIS331EB accelerometer behaves as a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, an 8-bit sub-address (SUB) is transmitted: the 7 LSb represents the actual register address while the ADD_INC bit (*CTRL_REG6 (25h)*) defines the address increment.

The slave address is completed with a read/write bit. If the bit is '1' (Read), a repeated start (SR) condition must be issued after the two sub-address bytes; if the bit is '0' (Write), the master transmits to the slave with direction unchanged. *Table 9* explains how the SAD+Read/Write bit pattern is composed, listing all the possible configurations.

Table 9. SAD+Read/Write patterns

Command	SAD[7:1]	R/W	SAD+R/W
Read	0011101	1	00111011 (3Bh)
Write	0011101	0	00111010(3Ah)

Table 10. Transfer when master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Table 11. Transfer when master is writing multiple bytes to slave

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Table 12. Transfer when master is receiving (reading) one byte of data from slave

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Table 13. Transfer when master is receiving (reading) multiple bytes of data from slave

Master	ST	SAD+W		SUB		SR	SAD+R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DATA		DATA		

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the Most Significant bit (MSb) first. If a receiver can't receive another complete byte of data until it has performed some other function, it can hold the clock line, SCL low, to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver doesn't acknowledge the slave address (i.e. it is not able to receive because it is performing some real-time function) the data line must be left high by the slave. The master can then abort the transfer. A low-to-high transition on the SDA_XL line while the SCL_XL line is high is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

In the presented communication format, MAK is Master acknowledge and NMAK is No Master Acknowledge.

6 Accelerometer register mapping

Table 14 provides a list of the 8/16-bit registers embedded in the device and the corresponding addresses.

Table 14. Register address map

Name	Type	Register address		Default	Comment
		Hex	Binary		
Reserved	r	0D-0F		Reserved	Reserved
CTRL_REG4	r/w	20	00100000	-	Control registers
CTRL_REG3	r/w	23	00100011	-	
CTRL_REG5	r/w	24	00100100	-	
CTRL_REG6	r/w	25	00100101	-	
STATUS	r	27	00100111	-	Status data register
OUT_T	r	0C	00001100	-	Temperature output
OFF_X	r/w	10	00010000	0000 0000	X-axis offset correction
OFF_Y	r/w	11	00010001	0000 0000	Y-axis offset correction
OFF_Z	r/w	12	00010010	0000 0000	Z-axis offset correction
CS_X	r/w	13	00010011	0000 0000	Constant shift X
CS_Y	r/w	14	00010100	0000 0000	Constant shift Y
CS_Z	r/w	15	00010101	0000 0000	Constant shift Z
LC_L	r/w	16	00010110	0000 0001	Long counter registers
LC_H	r/w	17	00010111	0000 0000	
STAT	r	18	00011000	-	Interrupt synchronization
VFC_1	r/w	1B	00011011	-	Vector filter coefficient 1
VFC_2	r/w	1C	00011100	-	Vector filter coefficient 2
VFC_3	r/w	1D	00011101	-	Vector filter coefficient 3
VFC_4	r/w	1E	00011110	-	Vector filter coefficient 4
THRS3	r/w	1F	00011111	-	Threshold value 3

Table 14. Register address map (continued)

Name	Type	Register address		Default	Comment
		Hex	Binary		
OUT_X_L	r	28	00101000	0000 0000	Output registers
OUT_X_H	r	29	00101001		
OUT_Y_L	r	2A	00101010		
OUT_Y_H	r	2B	00101011		
OUT_Z_L	r	2C	00101100		
OUT_Z_H	r	2D	00101101		
FIFO_CTRL	r/w	2E	00101110	0000 0000	FIFO registers
FIFO_SRC	r	2F	00101111	-	
CTRL_REG1	r/w	21	00100001	0000 0000	SM1 control register
STx_1	w	40-4F	01000000 01001111		SM1 code register (X =1-16)
TIM4_1	w	50	01010000	0000 0000	SM1 general timer
TIM3_1	w	51	01010001	-	
TIM2_1	w	52-53	01010010 01010011	-	
TIM1_1	w	54-55	01010100 01010101	-	
THRS2_1	w	56	01010110	-	SM1 threshold value 1
THRS1_1	w	57	01010111	-	SM1 threshold value 2
MASK1_B	w	59	01011001	-	SM1 axis and sign mask
MASK1_A	w	5A	01011010	-	SM1 axis and sign mask
SETT1	w	5B	01011011	-	SM1 detection settings
PR1	r	5C	01011100	-	Program-reset pointer
TC1	r	5D-5E	01011101 01011110	-	Timer counter
OUTS1	r	5F	01011111	-	Main set flag
PEAK1	r	19	00011001	-	Peak value
CTRL_REG2	r/w	22	00100010	-	SM2 control register

Table 14. Register address map (continued)

Name	Type	Register address		Default	Comment
		Hex	Binary		
STx_2	w	60-6F	01100000 01101111		SM2 code register (X =1-16)
TIM4_2	w	70	01110000	0000 0000	SM2 general timer
TIM3_2	w	71	01110001	-	
TIM2_2	w	72-73	01110010 01110011	-	
TIM1_2	w	74-75	01110100 01110101	-	
THRS2_2	w	76	01110110	-	SM2 threshold value 1
THRS1_2	w	77	01110111	-	SM2 threshold value 2
MASK2_B	w	79	01111001	-	SM2 axis and sign mask
MASK2_A	w	7A	01111010		SM2 axis and sign mask
SETT2	w	7B	01111011	-	SM2 detection settings
PR2	r	7C	01111100	-	Program-reset pointer
TC2	r	7D-7E	01111101 01111110	-	Timer counter
OUTS2	r	7F	01111111		Main set flag
PEAK2	r	1A	00011010	-	Peak value
DES2	w	78	01111000	-	Decimation factor

7 Accelerometer register description

7.1 CTRL_REG4 (20h)

Control register 4.

Table 15. CTRL_REG4 register

ODR3	ODR2	ODR1	ODR0	BDU	ZEN	YEN	XEN

Table 16. CTRL_REG4 register description

ODR [3:0]	Output data rate and power mode selection. Default value: 0000 (see *Table 17*)
BDU	Block data update. Default value: 0 0: continuous update; 1: output registers not updated until MSB and LSB read)
Zen	Z-axis enable. Default value: 1 (0: Z-axis disabled; 1: Z-axis enabled)
Yen	Y-axis enable. Default value: 1 (0: Y-axis disabled; 1: Y-axis enabled)
Xen	X-axis enable. Default value: 1 0: X-axis disabled; 1: X-axis enabled

ODR[3:0] is used to set power mode and ODR selection. *Table 17* lists all available frequencies.

Table 17. CTRL_REG4 ODR configuration

ODR3	ODR2	ODR1	ODR0	ODR selection
0	0	0	0	Power down
0	0	0	1	3.125 Hz
0	0	1	0	6.25 Hz
0	0	1	1	12.5 Hz
0	1	0	0	25 Hz
0	1	0	1	50 Hz
0	1	1	0	100 Hz
0	1	1	1	400 Hz
1	0	0	0	800 Hz
1	0	0	1	1600 Hz

The **BDU** bit is used to inhibit the output registers update until both upper and lower register parts are read. In default mode (BDU='0') the output register values are updated continuously. If for any reason it is not sure whether to read faster than the output data rate,

it is recommended to set the BDU bit to ‘1’. In this way the content of output registers is not updated until both MSb and LSb are read, avoiding to read values related to a different sample times.

7.2 CTRL_REG3 (23h)

Control register 3.

Table 18. CTRL_REG3 register

DR_EN	IEA	IEL	INT2_EN	INT1_EN	VFILT	-	STRT

Table 19. CTRL_REG3 register description

DR_EN	DRDY signal enable to INT1. Default value: 0 0: data ready signal not connected; 1: data ready signal connected to INT1
IEA	Interrupt signal polarity. Default value: 0 0: interrupt signals active low; 1: interrupt signals active high
IEL	Interrupt signal latching. Default value: 0 0: interrupt signals latched; 1: interrupt signal pulsed
INT2_EN	Interrupt 2 enable/disable. Default value: 0 0: INT2 signal disabled; 1: INT2 signal enabled
INT1_EN	Interrupt 1 enable/disable. Default value: 0 0: INT1/DRDY signal disabled; 1: INT1/DRDY signal enabled
VFILT	Vector filter enable/disable. Default value: 0 0: vector filter disabled; 1: vector filter enabled
STRT	Soft reset bit 0: no soft reset; 1: soft reset (POR function)

7.3 CTRL_REG5 (24h)

Control register 5.

Table 20. CTRL_REG5 register

BW2	BW1	FSCALE2	FSCALE1	FSCALE0	ST2	ST1	0(1)

1. This bit must be set to ‘0’ for proper operation of the device.

Table 21. CTRL_REG5 register description

BW [2:1]	Anti-aliasing filter bandwidth. Default value: 00 00=800 Hz; 01=200 Hz; 10=400 Hz; 11=50 Hz
FSCALE[2:0]	Full-scale selection. Default value: 000 000 = ±2 *g*; 001 = ±4 *g*; 010 = ±6 *g*; 011 = ±8 *g*; 100 = ±16 *g*
ST[2:1]	Self-test enable. Default value: 00 00: self-test disabled; refer to *Table 22*.

Table 22. Self-test mode selection

ST2	ST1	Self-test mode
0	0	Normal mode
0	1	Positive sign self-test
1	0	Negative sign self-test
1	1	Not allowed

7.4 CTRL_REG6 (25h)

Control register 6.

Table 23. CTRL_REG6 register

BOOT	FIFO_EN	WTM_EN	ADD_ INC	P1_ EMPTY	P1_WTM	P1_OVER RUN	P2_ BOOT

Table 24. CTRL_REG6 register description

BOOT	Force reboot, cleared as soon as the reboot is finished. Active high.
FIFO_EN	FIFO enable. Default value: 0 0: disable; 1: enable
WTM_EN	Enable FIFO watermark level use. Default value: 0 0: disable; 1: enable
ADD_INC	Register address automatically incremented during a multiple byte access with a serial interface (I^2C). 0: disable; 1: enable
P1_EMPTY	Enable FIFO empty indication on INT 1. Default value: 0 0: disable; 1: enable
P1_WTM	FIFO watermark interrupt on INT 1. Default value: 0 0: disable; 1: enable
P1_OVERRUN	FIFO overrun interrupt on INT 1. Default value: 0 0: disable; 1: enable
P2_BOOT	BOOT interrupt on INT 2. Default value: 0 0: disable; 1: enable

7.5 STATUS (27h)

Status register.

Table 25. STATUS register

ZYXOR	ZOR	YOR	XOR	ZYXDA	ZDA	YDA	XDA

Table 26. STATUS register description

ZYXOR	X-, Y-, and Z-axis data overrun. Default value: 0 0: no overrun has occurred; 1: a new set of data has overwritten the previous set
ZOR	Z-axis data overrun. Default value: 0 0: no overrun has occurred; 1: new data for the Z-axis has overwritten the previous data
YOR	Y-axis data overrun. Default value: 0 0: no overrun has occurred; 1: new data for the Y-axis has overwritten the previous data
XOR	X-axis data overrun. Default value: 0 0: no overrun has occurred; 1: new data for the X-axis has overwritten the previous data
ZYXDA	X-, Y-, and Z-axis new data available. Default value: 0 0: a new set of data is not yet available; 1: a new set of data is available
ZDA	Z-axis new data available. Default value: 0 0: new data for the Z-axis is not yet available; 1: new data for the Z-axis is available
YDA	Y-axis new data available. Default value: 0 0: new data for the Y-axis is not yet available; 1: new data for the Y-axis is available
XDA	X-axis new data available. Default value: 0 0: new data for the X-axis is not yet available; 1: new data for the X-axis is available

7.6 OUT_T (0Ch)

Temperature output register. Temperature data (1LSB/deg - 8-bit resolution). The value is expressed as two's complement.

Table 27. OUT_T register

Temp7	Temp6	Temp5	Temp4	Temp3	Temp2	Temp1	Temp0

Table 28. OUT_T register description

Temp [7:0]	Temperature data

7.7 OFF_X (10h)

Offset correction X-axis register, signed value.

Table 29. OFF_X default values

0	0	0	0	0	0	0	0

7.8 OFF_Y (11h)

Offset correction Y-axis register, signed value.

Table 30. OFF_Y default values

0	0	0	0	0	0	0	0

7.9 OFF_Z (12h)

Offset correction Z-axis register, signed value.

Table 31. OFF_Z default values

0	0	0	0	0	0	0	0

7.10 CS_X (13h)

Constant shift signed value X-axis register - state machine only.

Table 32. CS_X default values

0	0	0	0	0	0	0	0

7.11 CS_Y (14h)

Constant shift signed value Y-axis register - state machine only.

Table 33. CS_Y default values

0	0	0	0	0	0	0	0

7.12 CS_Z (15h)

Constant shift signed value Z-axis register - state machine only.

Table 34. CS_Z default values

0	0	0	0	0	0	0	0

7.13 LC (16h - 17h)

16-bit long-counter register for interrupt state machine programs timing.

Table 35. LC_L default values

0	0	0	0	0	0	0	1

Table 36. LC_H default values

0	0	0	0	0	0	0	0

01h=counting stopped, 00h=counter full: interrupt available and counter is set to default. Values higher than 00h: counting

7.14 STAT (18h)

Interrupt status - interrupt synchronization register.

Table 37. STAT register

LONG	SYNCW	SYNC1	SYNC2	INT_SM1	INT_SM2	DOR	DRDY

Table 38. STAT register description

LONG	0: no interrupt; 1: long counter (LC) interrupt flag common for both SM
SYNCW	Synchronization for external Host Controller interrupt based on output data 0: no action waiting from host; 1: action from host based on output data
SYNC1	0: SM1 running normally; 1: SM1 stopped and await restart request from SM2
SYNC2	0: SM2 running normally; 1: SM2 stopped and await restart request from SM1
INT_SM1	SM1 - Interrupt Selection - 1: SM1 interrupt enabled; 0: SM1 interrupt disabled
INT_SM2	SM2 - Interrupt Selection - 1: SM2 interrupt enabled; 0: SM2 interrupt disabled
DOR	Data overrun indicates unread data from output register when the measurement of the next data samples starts; 0: no overrun; 1: data overrun bit is reset when next sample is ready
DRDY	Data ready from output register 0: data not ready; 1: data ready

7.15 VFC_1 (1Bh)

Vector coefficient register 1 for DIff filter.

Table 39. VFC_1 default values

0	0	0	0	0	0	0	0

7.16 VFC_2 (1Ch)

Vector coefficient register 2 for DIff filter.

Table 40. VFC_2 default values

0	0	0	0	0	0	0	0

7.17 VFC_3 (1Dh)

Vector coefficient register 3 for FSM2 filter.

Table 41. VFC_3 default values

0	0	0	0	0	0	0	0

7.18 VFC_4 (1Eh)

Vector coefficient register 4 for DIff filter.

Table 42. VFC_4 default values

0	0	0	0	0	0	0	0

7.19 THRS3 (1Fh)

Threshold value 3 register.

Table 43. THRS3 default values

0	0	0	0	0	0	0	0

7.20 OUT_X (28h - 29h)

X-axis output register.

Table 44. OUT_X_L register default values

0	0	0	0	0	0	0	0

Table 45. OUT_X_H register default values

0	0	0	0	0	0	0	0

7.21 OUT_Y (2Ah - 2Bh)

Y-axis output register.

Table 46. OUT_Y_L register default values

0	0	0	0	0	0	0	0

Table 47. OUT_Y_H register default values

0	0	0	0	0	0	0	0

7.22 OUT_Z (2Ch - 2Dh)

Z-axis output register.

Table 48. OUT_Z_L register default values

0	0	0	0	0	0	0	0

Table 49. OUT_Z_H register default values

0	0	0	0	0	0	0	0

7.23 FIFO_CTRL (2Eh)

FIFO control register.

Table 50. FIFO_CTRL register

FMODE2	FMODE1	FMODE0	WTMP4	WTMP3	WTMP2	WTMP1	WTMP4

Table 51. FIFO_CTRL register description

FMODE [2:0]	FIFO mode selection. Default value 000 (see *Table 52*)
WTMP [4:0]	FIFO threshold. Watermark level setting. FIFO depth if the watermark is enabled.

Table 52. FIFO mode selection

FMODE2	FMODE1	FMODE0	Mode
0	0	0	Bypass mode. FIFO turned off
0	0	1	FIFO mode. Stops collecting data when FIFO is full.
0	1	0	Stream mode. If the FIFO is full, the new sample overwrites the older one.
0	1	1	Stream mode until trigger is de-asserted, then FIFO mode.
1	0	0	Bypass mode until trigger is de-asserted, then Stream mode.
1	0	1	Not used
1	1	0	Not used
1	1	1	Bypass mode until trigger is de-asserted, then FIFO mode.

The FIFO trigger is INT2.

7.24 FIFO_SRC (2Fh)

FIFO SRC control register.

Table 53. FIFO_SRC register

WTM	OVRN_ FIFO	EMPTY	FSS4	FSS3	FSS2	FSS1	FSS0

Table 54. FIFO_SRC register description

WTM	Watermark status. 0: FIFO filling is lower than WTM level; 1: FIFO filling is equal to or higher than WTM level
OVRN_FIFO	Overrun bit status. 0: FIFO is not completely filled; 1:FIFO is completely filled
EMPTY	FIFO empty bit. 0: FIFO not empty; 1: FIFO empty
FSS[4:0]	FIFO stored data level

7.25 CTRL_REG1 (21h)

SM1 control register.

Table 55. CTRL_REG1 register

HYST2_1	HYST1_1	HYST0_1	-	SM1_PIN	-	-	SM1_EN

Table 56. CTRL_REG1 register description

HYST2_1 HYST1_1 HYST0_1	Hysteresis unsigned value to be added to or subtracted from threshold value in SM1 Default value: 000
SM1_PIN	0: SM1 interrupt routed to INT 1; 1: SM1 interrupt routed to the INT2 pin Default value: 0
SM1_EN	0: SM1 disabled; 1: SM1 enabled Default value: 0

7.26 STx_1 (40h-4Fh)

State machine 1 code register STx_1 (x = 1-16).

State machine 1 system register is made up of 16, 8-bit registers to implement 16-step op-code.

7.27 TIM4_1 (50h)

8-bit general timer (unsigned value) for SM1 operation timing.

Table 57. TIM4_1 default values

0	0	0	0	0	0	0	0

7.28 TIM3_1 (51h)

8-bit general timer (unsigned value) for SM1 operation timing.

Table 58. TIM3_1 default values

0	0	0	0	0	0	0	0

7.29 TIM2_1 (52h - 53h)

16-bit general timer (unsigned value) for SM1 operation timing.

Table 59. TIM2_1_L default values

0	0	0	0	0	0	0	0

Table 60. TIM2_1_H default values

0	0	0	0	0	0	0	0

7.30 TIM1_1 (54h - 55h)

16-bit general timer (unsigned value) for SM1 operation timing.

Table 61. TIM1_1_L default values

0	0	0	0	0	0	0	0

Table 62. TIM1_1_H default values

0	0	0	0	0	0	0	0

7.31 THRS2_1 (56h)

Threshold value for SM1 operation.

Table 63. THRS2_1 default values

0	0	0	0	0	0	0	0

7.32 THRS1_1 (57h)

Threshold value for SM1 operation.

Table 64. THRS1_1 default values

0	0	0	0	0	0	0	0

7.33 MASK1_B (59h)

Axis and sign mask (swap) for SM1 motion detection operation.

Table 65. MASK1_B axis and sign mask register

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V

Table 66. MASK1_B register structure

P_X	0: X + disabled; 1: X + enabled
N_X	0: X - disabled; 1: X – enabled
P_Y	0: Y+ disabled; 1: Y + enabled
N_Y	0: Y- disabled; 1: Y – enabled
P_Z	0: Z + disabled; 1: Z + enabled
N_Z	0: Z - disabled; 1: Z – enabled
P_V	0: V + disabled; 1: V + enabled
N_V	0: V - disabled; 1: V – enabled

7.34 MASK1_A (5Ah)

Axis and sign mask (default) for SM1 motion detection operation.

Table 67. MASK1_A axis and sign mask register

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V

Table 68. MASK1_A register structure

P_X	0: X + disabled; 1: X + enabled
N_X	0: X - disabled; 1: X – enabled
P_Y	0: Y + disabled; 1: Y + enabled
N_Y	0: Y - disabled; 1: Y – enabled
P_Z	0: Z + disabled; 1: Z + enabled
N_Z	0: Z - disabled; 1: Z – enabled
P_V	0: V + disabled; 1: V + enabled
N_V	0: V - disabled; 1: V – enabled

7.35 SETT1 (5Bh)

Setting of threshold, peak detection and flags for SM1 motion detection operation.

Table 69. SETT1 register

P_DET	THR3_SA	ABS	-	-	THR3_MA	R_TAM	SITR

Table 70. SETT1 register description

P_DET	SM1 peak detection. Default value: 0 0: peak detection disabled; 1: peak detection enabled
THR3_SA	Default value: 0 0: no action; 1: threshold 3 limit value for axis and sign mask reset (MASKB_1)
ABS	Default value: 0 0: unsigned thresholds; 1: signed thresholds
THR3_MA	Default value: 0 0: no action; 1: threshold 3 limit value for axis and sign mask reset (MASKA_1)
R_TAM	Next condition validation flag. Default value: 0 0: no valid next condition found; 1: valid next condition found and reset
SITR	Default value: 0 0: no actions; 1: program flow can be modified by STOP and CONT commands

7.36 PR1 (5Ch)

Program and reset pointer for SM1 motion detection operation.

Table 71. PR1 register

PP3	PP2	PP1	PP0	RP3	RP2	RP1	RP0

Table 72. PR1 register description

PP[3:0]	SM1 program pointer address
RP[3:0]	SM1 reset pointer address

7.37 TC1 (5Dh-5Eh)

16-bit general timer (unsigned output value) for SM1 operation timing.

Table 73. TC1_L default values

0	0	0	0	0	0	0	0

Table 74. TC1_H default values

0	0	0	0	0	0	0	0

7.38 OUTS1 (5Fh)

Output flags on axis for interrupt SM1 management.

Table 75. OUTS1 register

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V

Read action of this register, depending on the flag affects SM1 interrupt functions.

Table 76. OUTS1 register description

P_X	0: X + not shown; 1: X+ shown
N_X	0: X - not shown; 1: X – shown
P_Y	0: Y + not shown; 1: Y + shown
N_Y	0: Y - not shown; 1: Y – shown
P_Z	0: Z + not shown; 1: Z + shown
N_Z	0: Z - not shown; 1: Z – shown
P_V	0: V + not shown; 1: V + shown
N_V	0: V - not shown; 1: V – shown

7.39 PEAK1 (19h)

Peak detection value register for SM1 operation.

Table 77. PEAK1 default values

0	0	0	0	0	0	0	0

Peak detected value for next condition SM1.

7.40 CTRL_REG2 (22h)

State program 2 interrupt MNG - SM2 control register.

Table 78. CTRL_REG2 register

HYST2_2	HYST1_2	HYST0_2	-	SM2_PIN	-	-	SM2_EN

Table 79. CTRL_REG2 register description

HYST2_2 HYST1_2 HYST0_2	Hysteresis unsigned value to be added to or subtracted from threshold value in SM2. Default value: 000
SM2_PIN	0: SM2 interrupt routed to INT1; 1: SM2 interrupt routed to INT1 pin. Default value: 0
SM2_EN	0: SM2 disabled; 1: SM2 enabled. Default value: 0

7.41 STx_2 (60h-6Fh)

State machine 2 code register STx_1 (x = 1-16).

State machine 2 system register is made up of 16 8-bit registers, to implement 16-step op-code.

7.42 TIM4_2 (70h)

8-bit general timer (unsigned value) for SM2 operation timing.

Table 80. TIM4_2 default values

0	0	0	0	0	0	0	0

7.43 TIM3_2 (71h)

8-bit general timer (unsigned value) for SM2 operation timing.

Table 81. TIM3_2 default values

0	0	0	0	0	0	0	0

7.44 TIM2_2 (72h - 73h)

16-bit general timer (unsigned value) for SM2 operation timing.

Table 82. TIM2_2_L default values

0	0	0	0	0	0	0	0

Table 83. TIM2_2_H default values

0	0	0	0	0	0	0	0

7.45 TIM1_2 (74h - 75h)

16-bit general timer (unsigned value) for SM2 operation timing.

Table 84. TIM1_2_L default values

0	0	0	0	0	0	0	0

Table 85. TIM1_2_H default values

0	0	0	0	0	0	0	0

7.46 THRS2_2 (76h)

Threshold signed value for SM2 operation.

Table 86. THRS2_2 default values

0	0	0	0	0	0	0	0

7.47 THRS1_2 (77h)

Threshold signed value for SM2 operation.

Table 87. THRS1_2 default values

0	0	0	0	0	0	0	0

7.48 MASK2_B (79h)

Axis and sign mask (swap) for SM2 motion detection operation.

Table 88. MASK2_B register

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V

Table 89. MASK2_B register description

P_X	0: X + disabled; 1: X + enabled
N_X	0: X - disabled; 1: X – enabled
P_Y	0: Y + disabled; 1: Y + enabled
N_Y	0: Y - disabled; 1: Y – enabled
P_Z	0: Z + disabled; 1: Z + enabled
N_Z	0: Z - disabled; 1: Z – enabled
P_V	0: V + disabled; 1: V + enabled
N_V	0: V - disabled; 1: V – enabled

7.49 MASK2_A (7Ah)

Axis and sign mask (default) for SM2 motion detection operation.

Table 90. MASK2_A axis and sign mask register

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V

Table 91. MASK2_A register description

P_X	0: X + disabled; 1: X + enabled
N_X	0: X - disabled; 1: X – enabled
P_Y	0: Y + disabled; 1: Y + enabled
N_Y	0: Y - disabled; 1: Y – enabled
P_Z	0: Z + disabled; 1: Z + enabled
N_Z	0: Z - disabled; 1: Z – enabled
P_V	0: V + disabled; 1: V + enabled
N_V	0: V - disabled; 1: V – enabled

7.50 SETT2 (7Bh)

Setting of threshold, peak detection and flags for SM2 motion detection operation.

Table 92. SETT2 register

P_DET	THR3_SA	ABS	RADI	D_CS	THR3_MA	R_TAM	SITR

Table 93. SETT2 register description

P_DET	SM2 peak detection. Default value: 0 0: peak detection disabled; 1: peak detection enabled
THR3_SA	Default value: 0 0: no action; 1: threshold 3 limit value for axis and sign mask reset (MASK2_B)
ABS	Default value: 0 0: unsigned thresholds; 1: signed thresholds
RADI	0: raw data; 1: diff data for State Machine 2
D_CS	0: DIFF2 enable (difference between current data and previous data) 1: constant shift enabled (difference between current data and constant values)
THR3_MA	Default value: 0 0: no action; 1: threshold 3 limit value for axis and sign mask reset (MASK2_A)
R_TAM	Next condition validation flag. Default value: 0 0: no valid next condition found; 1: valid next condition found and reset
SITR	Default value: 0 0: no actions; 1: program flow can be modified by STOP and CONT commands

7.51 PR2 (7Ch)

Program and reset pointer for SM2 motion detection operation.

Table 94. PR2 register

PP3	PP2	PP1	PP0	RP3	RP2	RP1	RP0

Table 95. PR2 register description

PP[3:0]	SM2 program pointer address
RP[3:0]	SM2 reset pointer address

7.52 TC2 (7Dh-7Eh)

16-bit general timer (unsigned output value) for SM2 operation timing.

Table 96. TC2_L default values

0	0	0	0	0	0	0	0

Table 97. TC2_H default values

0	0	0	0	0	0	0	0

7.53 OUTS2 (7Fh)

Output flags on axis for interrupt SM2 management.

Table 98. OUTS2 register

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V

Read action of this register, depending on the flag affects SM2 interrupt functions.

Table 99. OUTS2 register description

P_X	0: X + not shown; 1: X + shown
N_X	0: X - not shown; 1: X – shown
P_Y	0: Y + not shown; 1: Y + shown
N_Y	0: Y - not shown; 1: Y – shown
P_Z	0: Z + not shown; 1: Z + shown
N_Z	0: Z - not shown; 1: Z – shown
P_V	0: V + not shown; 1: V + shown
N_V	0: V - not shown; 1: V – shown

7.54 PEAK2 (1Ah)

Peak detection value register for SM2 operation.

Table 100. PEAK2 default values

0	0	0	0	0	0	0	0

Peak detected value for next condition SM2.

7.55 DES2 (78h)

Decimation counter value register for SM2 operation.

Table 101. DES2 default values

0	0	0	0	0	0	0	0

Registers marked as '*Reserved*' must not be changed. Writing to those registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

8 Microprocessor electrical specifications

Characteristics measured in *Table 102* are within recommended operating conditions unless otherwise specified. Typical values are in reference to T_A = 25 °C, $V_{dd1.8}$ = 1.8 V.

Table 102. DC and AC parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
VDDA	Operating supply voltage master serial port (DIO6 to DIO10)		1.71		3.6	V
Vdd1.8	Operating supply voltage (DIO0 to DIO5)		1.75	1.8	1.95	V
Power consumption (Dhrystone without compiler options)						
I_{supply}	Supply current	Reset		50		nA
		Active (CPU, Flash, and RAM)			20	mA
		From RAM 80 MHz (0.79 DMIPS/MHz) 40 MHz (0.79 DMIPS/MHz) 20 MHz (0.79 DMIPS/MHz) 16 MHz (0.79 DMIPS/MHz) 10 MHz (0.79 DMIPS/MHz)		 10.3 5.95 3.85 3.48 2.9		
		From Flash 80 MHz (0.3 DMIPS/MHz) 40 MHz (0.43 DMIPS/MHz) 20 MHz (0.56 DMIPS/MHz) 16 MHz (0.79 DMIPS/MHz) 10 MHz (0.79 DMIPS/MHz)		 7.5 5.5 4.74 4.34 3.7		
Digital input and output (1.8 V supply)						
C_{IN}(1)	Port I/O capacitance		1.3	1.4	1.7	pF
R_{PD}(1)	Pull-down value		117	211	334	kW
T_{RISE}(1)	Rise time	0.1*$V_{dd1.8}$ to 0.9*$V_{dd1.8}$, C_L = 50 pF	10.3		19	ns
T_{FALL}(1)	Fall time	0.9*$V_{dd1.8}$ to 0.1*$V_{dd1.8}$, C_L = 50 pF	11		22	
V_{IH}(1)	Logic high-level input voltage		0.65 $V_{dd1.8}$			V
V_{IL}(1)	Logic low-level input voltage				0.35 $V_{dd1.8}$	
Digital input and output (3.3 V supply)						
C_{IN}(1)	Port I/O capacitance		1.3	1.4	1.7	pF
R_{PD}(1)	Pull-down value		53	84	144	kW
R_{PU}(1)	Pull-up value		57	81	122	

Table 102. DC and AC parameters (continued)

T_{RISE}(1)	Rise time	0.1*$V_{dd1.8}$ to 0.9*$V_{dd1.8}$, C_L = 50 pF	1.4		12	ns
T_{FALL}(1)	Fall time	0.9*$V_{dd1.8}$ to 0.1*$V_{dd1.8}$, C_L = 50 pF	1.5		12.5	
V_{IH}(1)	Logic high-level input voltage		0.65 $V_{dd1.8}$			V
V_{IL}(1)	Logic low-level input voltage				0.35 $V_{dd1.8}$	
T_A	Operating ambient temperature range		-40		85	°C

1. Guaranteed by design

8.1 External clock input pin (GPIO5) characteristics

Table 103. External clock input characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{NOM}	Nominal frequency	-40 °C to 85 °C	-	-	80	MHz
f_{TOL}	Frequency tolerance			±1		%
DuCy	Duty Cycle		48		52	%

8.2 Internal high-speed RC oscillator (HSRCOSC) characteristics

Table 104. High-speed crystal oscillator characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
f_{NOM}	Nominal frequency	-40 °C to 85 °C	-	80		MHz
f_{TOL}	Frequency tolerance			±1	±5	%
I_{NOM}	Nominal power			800		µA

8.3 Internal low-speed RC oscillator (LSRCOSC) characteristics

Table 105 concerns the 32 kHz RC oscillator.

Table 105. Low-speed crystal oscillator characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{NOM}	Nominal frequency	-40 °C to 85 °C	-	32		kHz
f_{TOL}	Frequency tolerance			±1	±5	%
I_{NOM}	Nominal power			35		µA

9 Microprocessor

9.1 ARM Cortex-M0 core

The ARM Cortex-M0 processor is a very low gate count, energy-efficient processor. It has been developed to provide an energy-efficient processor for microcontrollers and embedded applications requiring an area-optimized processor. The ARM Cortex-M0 32-bit RISC processor uses Thumb-2® technology, providing a blend of 16/32-bit instructions delivering a smaller code size to 8-bit and 16-bit architectures.

Owing to its embedded ARM core, the LIS331EB is compatible with all ARM tools and software.

9.1.1 Nested vectored interrupt controller (NVIC)

The ARM Cortex-M0 processor supports up to 32 interrupt requests (IRQ), a non-maskable interrupt (NMI), and various system exceptions. The NVIC and the ARM Cortex-M0 processor core are closely coupled and provide:

- Low-latency interrupt processing
- Four interrupt priority levels
- Efficient processing of late arriving interrupts and higher priority interrupts
- Support for tail-chaining

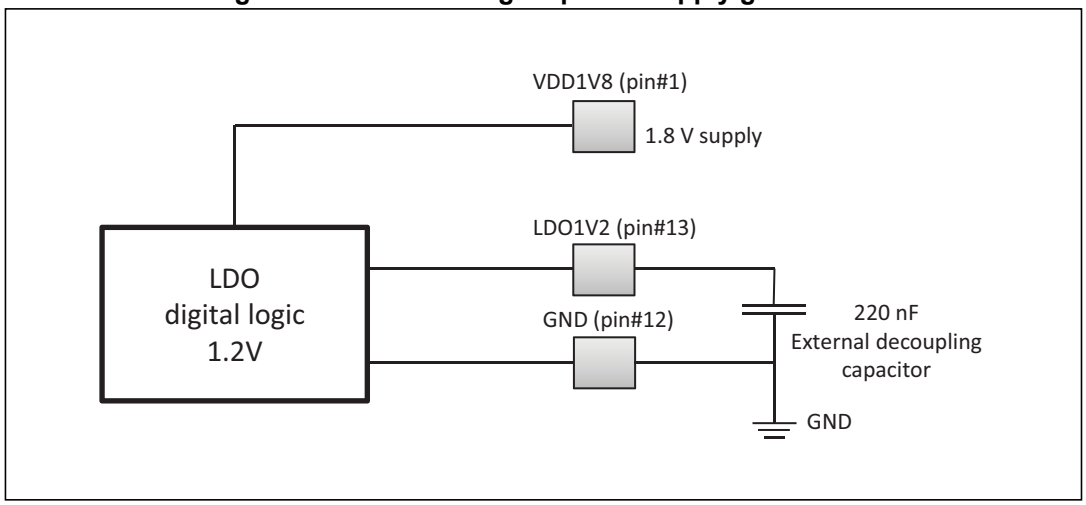
9.2 Power supply scheme

- V_{DDA}[(c)] = 1.8 V to 3.3 V: external power supply for master serial port (GPIO6 to GPIO10). Provided through V_{DDA} pin.
- $V_{dd1.8}$[(c)] = 1.8 V: external power supply for internal regulator. Provided through $V_{dd1.8}$ pin.

The LIS331EB integrates an LDO regulator which is used to generate the power supply for the internal digital circuitry. The LDO supplies 1.2 V for the digital blocks and requires a decoupling capacitor for stable operation.

c. For minimum and maximum operating conditions of V_{DDA} and $V_{dd1.8}$ refer to *Table 102*.

Figure 10. LIS331EB digital power supply generation



9.3 Reset management

The device has an integrated brownout reset (BOR) circuit and an integrated power-on reset (POR).

In the LIS331EB, the BOR threshold is 1.5 V. When $V_{dd1.8}$ is below this threshold, the device is in reset. The BOR is always active in the LIS331EB at power-on.

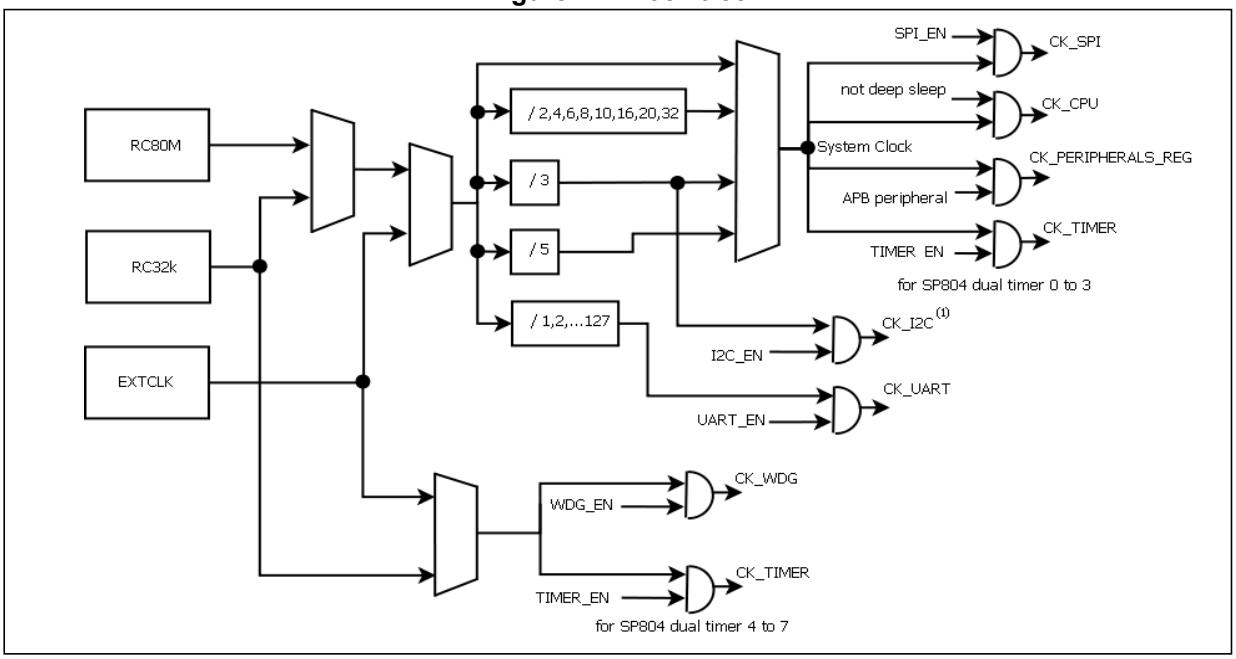
The POR circuit is activated when the LDO has stabilized. The startup time of the LIS331EB at power-on is typically 1 ms with the BOR active.

9.4 Boot modes

At startup, the LIS331EB boots from a reserved section of the Flash memory programmed by ST during production. It is used to adjust accurately the oscillator frequencies and contains manufacturing information. Any interference with this initialization sequence can degrade the performance of the device. At the end of this sequence, the system boots from the main Flash which contains the user's program.

9.5 Clock management

Figure 11. Clock tree



(1) Same clock supply for both I^2C

The clock management block distributes clocks from various clock sources to the CPU and peripherals. The clock management block is comprised of the following circuitry and switches:

- Clock divider: the system contains various clock dividers which allow the frequency of the peripherals and CPU clock sources to be changed.
- Glitch-free clock switching: the clock sources can be changed dynamically and securely in active mode.
- Clock gating: the peripherals can have their clocks gated off to reduce their power consumption.
- Three system clock sources:
- RC80M 80 MHz internal RC oscillator which is trimmed at 1% accuracy with factory settings
- RC32K 32 kHz internal RC oscillator which is trimmed at 1% accuracy with factory settings
- EXTCLK external clock up to 80 MHz
- Watchdog clock sources: the RC32k or EXTCLK.
- I^2C clock source: system clock divided by 3.
- UART clock source: system clock divided by a programmable division factor between 1 and 127.
- SPI clock source: clock synchronous to the processor.
- Dual timers: four timers clocked by 32 kHz clock pulses synchronous to the system clock sources and four timers clocked on a clock synchronous to the processor clock.
- Clock-out capability: either the 32 kHz clock or the output of the divide-by 5 clock can be output on a GPIO for external use.

9.6 General-purpose inputs/outputs (GPIOs)

The LIS331EB contains up to 11 GPIO pins each of which can be configured by software as output, as input (either pull-up or pull-down), or as an alternate function in serial mode 0 or serial mode1 (see *Table 106*). Each of the GPIOs can also be used as an external interrupt source.

Table 106. Alternate function input/output

Pin name	Serial mode 0		Serial mode 1		GPIO mode	
	Direction	Function	Direction	Function	Direction	Function
IO0	Input/Output	JTAG TMS / SW_TDIO	Input	UART CTS	Input/Output	GPIO
IO1	Input	JTAG TCK / SW_TCK	Output	UART RTS		
IO2	Input/Output	I^2C2_SCL		UART TXD		
IO3		I^2C2_SDA	Input	UART RXD		
IO4	Output	JTAG TDO		None		
IO5	Input	JTAG TDI		Clock input		
IO6	Output	16 MHz clock	Output	32 kHz clock		
IO7	Input/Output	I^2C1_SCL	Input/Output	SPI SCLK		
IO8		I^2C1_SDA	Output	SPI output		
IO9	Input	IRQ input	Input	SPI CS		
IO10				SPI input		

9.7 Memories

The LIS331EB has the following memory features:

- 64 Kbyte embedded Flash memory with 0 wait states at 26.66 MHz and 2 wait states at 80 MHz.
- 64 Kbyte embedded SRAM with ECC for data and program access (read/write) referred to as RAM bank0.
- 64 Kbyte SRAM for data and program access (read/write) referred to as RAM bank1
- Memory protection: the Flash and RAM memory banks cannot be read from or written to by the JTAG link if the debug features are connected.

9.8 Timers and watchdogs

The LIS331EB includes eight dual timers, one WDG timer, and a SysTick timer.

9.8.1 Dual timer

The dual timer features are listed below. They consist of two identical programmable free running counters (FRCs) that can be configured for 32-bit or 16-bit operations. The FRCs operate from a common timer clock which must be synchronous to the CPU clock.

- 16/32-bit down counter
- Interrupt generation when the counter reaches zero
- Free-running mode: the counter operates continuously and wraps around to its maximum value each time it reaches zero.
- Periodic mode: the counter operates continuously by reloading the programmed value each time it reaches zero.
- One-shot mode: the counter decrements to zero and then halts until it is reprogrammed
- The timer clock prescaler factors are 1, 16, or 256

9.8.2 Watchdog (WDG) timer

The WDG timer is a 32-bit down counter which operates on either the RC32k clock or the EXTCLK clock. It can generate an interrupt and/or a reset when the counter reaches zero. For more details, refer to ARM Dual-timer module (SP804) in the Technical Reference Manual.

9.8.3 System tick (SysTick) timer

The SysTick timer provides a 24-bit clear on write, decrementing counter which wraps around when it reaches zero. It operates on the CPU clock.

9.9 Communication interfaces

9.9.1 I²C bus

The LIS331EB provides two I²C interfaces which can operate in master and slave modes. They can support standard mode and fast mode.

9.9.2 Universal asynchronous receiver transmitter (UART)

The UART interface (IO0, IO1, IO2, IO3 pins) of the LIS331EB supports the following maximum baud rates:

- 921600 bps in UART mode
- 460800 bps in Infrared data association (IrDA) mode
- 115200 bps in Low-power IrDA mode

The interface supports the IrDA serial infrared (SIR) ENDEC and also provides flow control capabilities through the hardware management of the clear to send (CTS) and request to send (RTS) signals.

For more details, refer to the ARM document “DDIO83G_uart_pl011_trm.pdf”.

9.9.3 Serial peripheral interface (SPI)

The SPI interface operates as a master or slave interface. This supports 6 MHz bit rate max in slave mode and 16 MHz bit rate max in master mode due to the limitation of the IOs. A programmable clock prescaler inside the SPI allows the input clock to be divided by a factor of 2 to 254 in steps of two to provide the serial output clock. The SPI interface provides data frames between 4 and 16 bits long.

For more details, refer to the ARM document “DDIO94C_ssp_PL022_trm.pdf”.

9.10 JTAG and SW debug support

The ARM JTAG debug port is embedded which enables debugging using a standard JTAG connection. The ARM SWD (serial wire debug) port is also embedded which enables the serial wire debug to be connected to the CPU. The JTAG TMS and TCK pins are shared with the SW_TDIO and SW_TCK respectively.

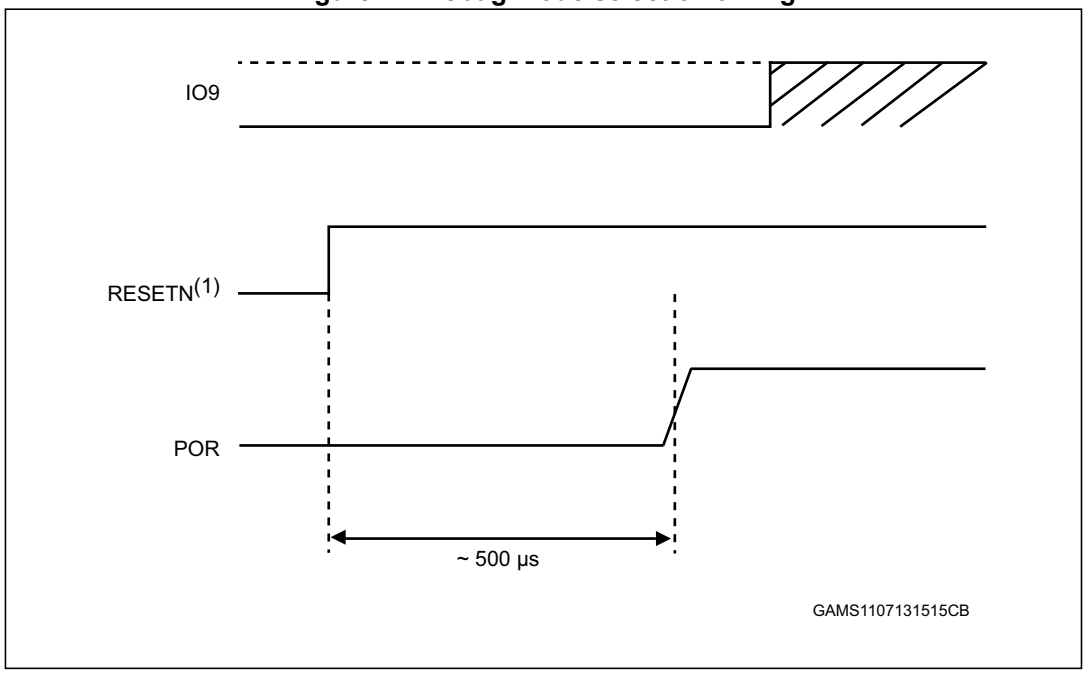
These two debug mode mechanisms can be selected by driving the IO9 pin during reset: JTAG debug mode is selected by setting the IO9 pin to zero, while SWD mode is selected by setting the IO9 pin to 1.

Table 107. Debug mode selection

POR	IO9	Debug mode
0	0	JTAG: SOC(1) + CPU TAP(2) selected
0	1	SW: CPU TAP(2) selected
1	X(3)	JTAG or SW available

1. SOC = chip and processor
2. TAP = test access port
3. X = don't care

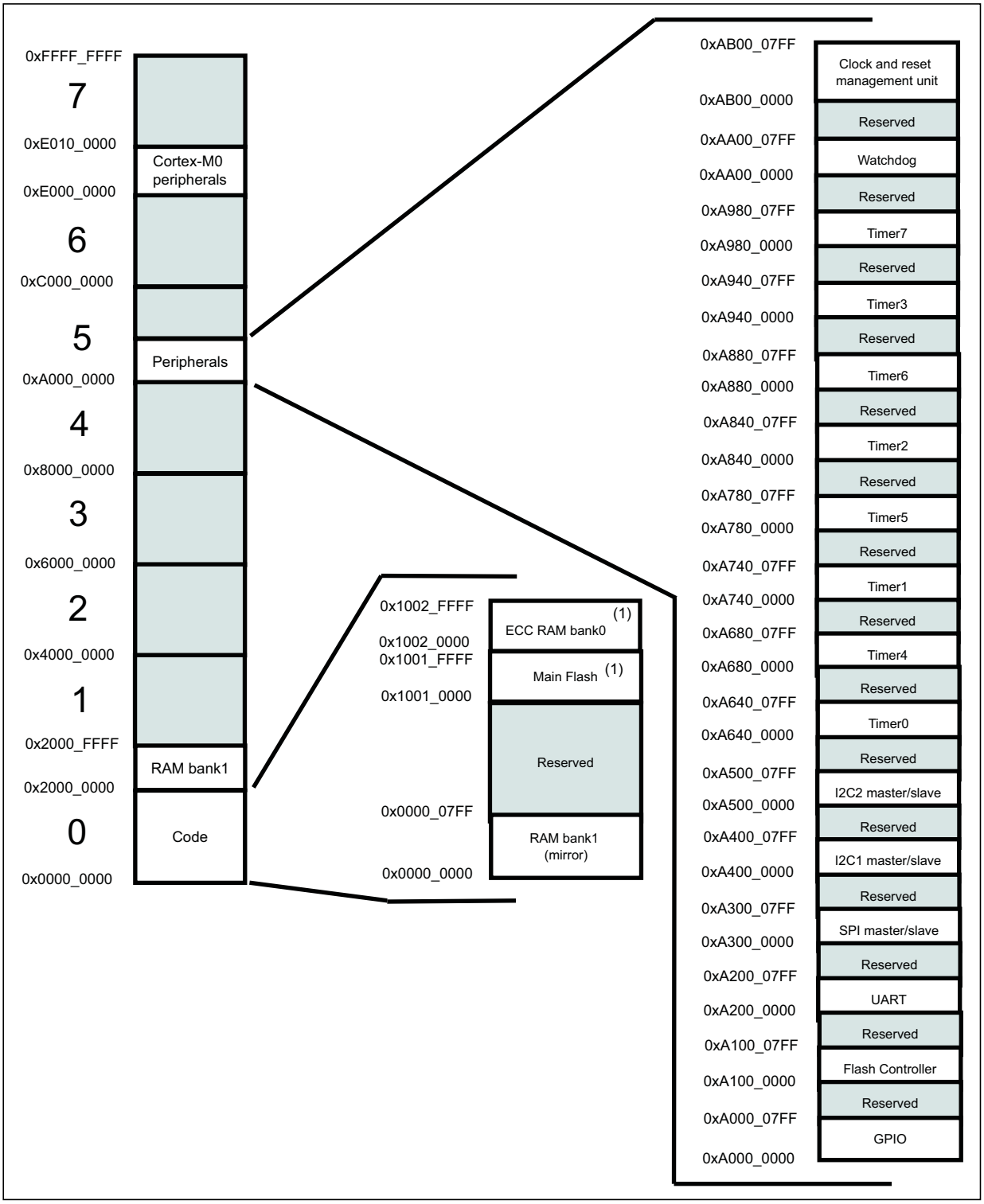
Figure 12. Debug mode selection timing



1. RESETN needs an external pull-up if not driven

10 Memory map

Figure 13. Memory map



1. Default option depending on software configuration

10.1 Microprocessor operating modes

Several operating modes are defined for the LIS331EB:

- Reset mode
- Two low-power modes: low-power wait-for-interrupt (WFI) mode and high-power wait-for-interrupt (WFI) mode
- Active mode

In reset mode the LIS331EB is in ultra-low power consumption: all voltage regulator, clocks are not powered. The LIS331EB enters reset mode by asserting the external reset signal.

While in low-power WFI mode, the LIS331EB CPU is stopped and the high-frequency 80 MHz RC oscillator is powered down. All peripherals, apart from one timer, are disabled. The power consumption is about 800 µA with a 1 kHz clock.

In high-power WFI mode, the CPU is stopped and the high-frequency 80 MHz RC oscillator is powered up. This mode allows a faster response time for an interrupt to wake up the CPU. All peripherals are enabled and can wake up the CPU with an interrupt. The power consumption in this mode is around 2 mA with an 80 MHz clock.

In active mode the LIS331EB is fully operational: all interfaces, including SPI, I^2C, JTAG and UART, are active as well as all internal power supplies together with the high speed frequency oscillator. The MCU core is also running.

Table 108 summarizes the modes of operation and transition times.

Table 108. LIS331EB operating modes

IP	Active mode	High-power WFI mode	Low-power WFI mode
CPU	Yes	Yes	Yes
Flash			
SRAM			
BOR			Yes
POR			
High-speed internal osc.			No
Low-speed internal osc.			Yes
Timer			Yes
SPI			No
I²C			
UART			
WDG			Yes
GPIOs			Yes
Wakeup time to active mode	0 µs	50 ns	300 µs
Consumption (typ)	10 mA	3 mA	800 µA

11 Absolute maximum ratings

11.1 Accelerometer

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 109. Absolute maximum ratings for accelerometer

Symbol	Ratings	Maximum value	Unit
VDDA	Core and I/O pins supply voltage	-0.3 to 4.8	V
Vin	Input voltage on any control pin (SCL_XL, SDA_XL)	-0.3 to VDDA +0.3	V
A_{POW}	Acceleration (any axis, powered, VDDA = 2.5 V)	3000 for 0.5 ms	g
		10000 for 0.1 ms	g
A_{UNP}	Acceleration (any axis, unpowered)	3000 for 0.5 ms	g
		10000 for 0.1 ms	g
T_{OP}	Operating temperature range	-40 to +85	°C
T_{STG}	Storage temperature range	-40 to +125	°C
ESD	Electrostatic discharge protection	2 (HBM)	kV

Note: Supply voltage on any pin should never exceed 4.8 V

This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.

This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

11.2 Microprocessor

Absolute maximum ratings are those values above which damage to the device may occur. Functional operation under these conditions is not implied. All voltages are in reference to GND.

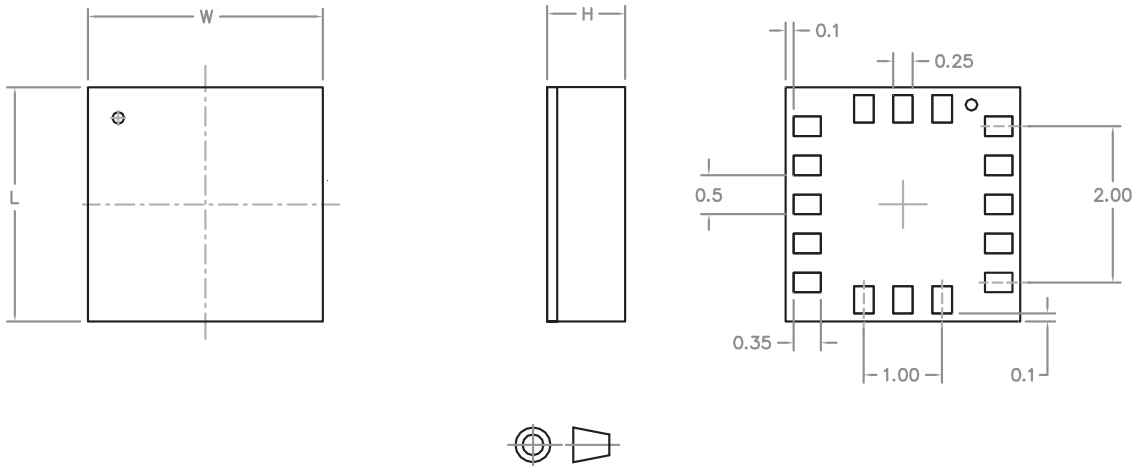
Table 110. Absolute maximum ratings for microprocessor

Pin	Parameter	Value (min to max)	Unit
9, 10, 11, 15, 16	DC voltage on digital output pins	-0.3 to +3.6	V
2, 3, 4, 6, 7, 8		-0.3 to +1.95	
5	DC voltage on analog pins	-0.3 to +1.95	
T_{STG}	Storage temperature range	-40 to +125	°C
$V_{ESD-HBM}$	Electrostatic discharge voltage	±2.0	kV

12 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 14. LGA-16: mechanical data and package dimensions



Dimensions are in millimeter unless otherwise specified
General Tolerance is +/-0.1mm unless otherwise specified

OUTER DIMENSIONS

ITEM	DIMENSION [mm]	TOLERANCE [mm]
Length [L]	3.00	±0.1
Width [W]	3.00	±0.1
Height [H]	1.00	MAX

8526629_A

13 Revision history

Table 111. Document revision history

Date	Revision	Changes
18-Dec-2012	1	Initial release.
13-Feb-2014	2	Updated *Table 2*, *Figure 2*, *Figure 4*, *Figure 6*, *Figure 7*, *Section 3.1: Mechanical characteristics*, *Section 3.2: Electrical characteristics*, *Table 14*, *Table 102*, *Section 9.10: JTAG and SW debug support*, *Figure 13*, *Figure 14*; general revision and minor textual updates.

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