LMK00334 4-Output PCIe/Gen1/Gen2/Gen3 Clock Buffer/Level Translator

Check for Samples: LMK00334

FEATURES

- **3:1 Input Multiplexer**
  - **Two Universal Inputs Operate up to 400 MHz and Accept LVPECL, LVDS, CML, SSTL, HSTL, HCSL, or Single-Ended Clocks**
  - **One Crystal Input Accepts a 10 to 40 MHz Crystal or Single-Ended Clock**
- **Two Banks with 2 Differential Outputs Each**
  - **HCSL, or Hi-Z (Selectable)**
  - **Additive RMS Phase Jitter for PCIe Gen3 at 100MHz:**
    - **30 fs RMS (typical)**
- **High PSRR: -72 dBc at 156.25 MHz**
- **LVCMOS Output with Synchronous Enable Input**
- **Pin-Controlled Configuration**
- **V_{CC} Core Supply: 3.3 V ± 5%**
- **3 Independent V_{CCO} Output Supplies: 3.3 V/2.5 V ± 5%**
- **Industrial Temperature Range: -40°C to +85°C**
- **32-lead WQFN (5 mm x 5 mm)**

APPLICATIONS

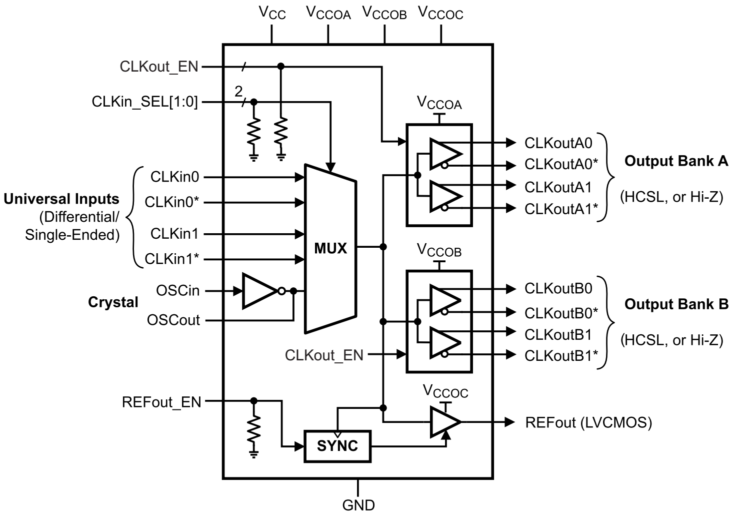
- **Clock Distribution and Level Translation for ADCs, DACs, Multi-Gigabit Ethernet, XAUI, Fibre Channel, SATA/SAS, SONET/SDH, CPRI, High-Frequency Backplanes**
- **Switches, Routers, Line Cards, Timing Cards**
- **Servers, Computing, PCI Express (PCIe 3.0)**
- **Remote Radio Units and Baseband Units**

DESCRIPTION

The LMK00334 is a 4-output HCSL fanout buffer intended for high-frequency, low-jitter clock/data distribution and level translation. The input clock can be selected from two universal inputs or one crystal input. The selected input clock is distributed to two banks of 2 HCSL outputs and one LVCMOS output. The LVCMOS output has a synchronous enable input for runt-pulse-free operation when enabled or disabled. The LMK00334 operates from a 3.3 V core supply and 3 independent 3.3 V/2.5 V output supplies.

The LMK00334 provides high performance, versatility, and power efficiency, making it ideal for replacing fixed-output buffer devices while increasing timing margin in the system.

FUNCTIONAL BLOCK DIAGRAM



Connection Diagram

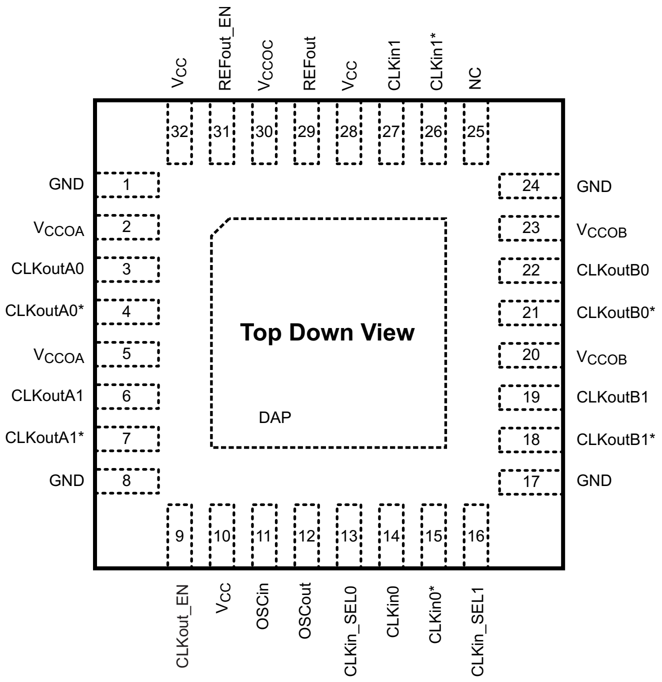


Figure 1. 32-Pin Package RTV0032A Package

Application Diagram

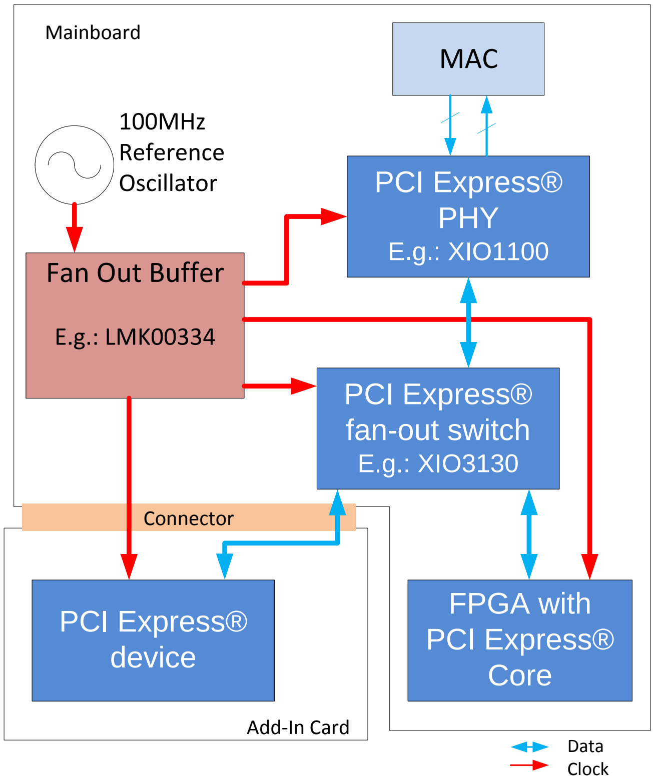


Figure 2. Example PCI Express Application

Pin Descriptions(1)

Pin #	Pin Name(s)	Type	Description
DAP	DAP	GND	Die Attach Pad. Connect to the PCB ground plane for heat dissipation.
1, 8 17, 24	GND	GND	Ground
2, 5	V_{CCOA}	PWR	Power supply for Bank A Output buffers. V_{CCOA} operates from 3.3 V or 2.5 V. The V_{CCOA} pins are internally tied together. Bypass with a 0.1 uF low-ESR capacitor placed very close to each Vcco pin. (2)
3, 4	CLKoutA0, CLKoutA0*	O	Differential clock output A0.
6, 7	CLKoutA1, CLKoutA1*	O	Differential clock output A1.
9	CLKout_EN	I	Bank A and Bank B low active output buffer enable. (3)
10	Vcc	PWR	Power supply for Core and Input Buffer blocks. The Vcc supply operates from 3.3 V. Bypass with a 0.1 uF low-ESR capacitor placed very close to each Vcc pin.
11	OSCin	I	Input for crystal. Can also be driven by a XO, TCXO, or other external single-ended clock.
12	OSCout	O	Output for crystal. Leave OSCout floating if OSCin is driven by a single-ended clock.
13, 16	CLKin_SEL0, CLKin_SEL1	I	Clock input selection pins (3)
14, 15	CLKin0, CLKin0*	I	Universal clock input 0 (differential/single-ended)
18, 19	CLKoutB1*, CLKoutB1	O	Differential clock output B1.
20, 23	V_{CCOB}	PWR	Power supply for Bank B Output buffers. V_{CCOB} operates from 3.3 V or 2.5 V. The V_{CCOB} pins are internally tied together. Bypass with a 0.1 uF low-ESR capacitor placed very close to each Vcco pin. (2)
21, 22	CLKoutB0*, CLKoutB0	O	Differential clock output B0.
25	NC	—	Not connected internally. Pin may be floated, grounded, or otherwise tied to any potential within the Supply Voltage range stated in the Absolute Maximum Ratings.
26, 27	CLKin1*, CLKin1	I	Universal clock input 1 (differential/single-ended)
29	REFout	O	LVCMOS reference output. Enable output by pulling REFout_EN pin high.
30	V_{CCOC}	PWR	Power supply for REFout buffer. V_{CCOC} operates from 3.3 V or 2.5 V. Bypass with a 0.1 uF low-ESR capacitor placed very close to each Vcco pin. (2)
31	REFout_EN	I	REFout enable input. Enable signal is internally synchronized to selected clock input. (3)

(1) Any unused output pins should be left floating with minimum copper length (see note in Clock Outputs), or properly terminated if connected to a transmission line, or disabled/Hi-Z if possible. See Clock Outputs for output configuration and Termination and Use of Clock Drivers for output interface and termination techniques.
(2) The output supply voltages or pins (V_{CCOA}, V_{CCOB}, and V_{CCOC}) will be called V_{CCO} in general when no distinction is needed, or when the output supply can be inferred from the output bank/type.
(3) CMOS control input with internal pull-down resistor.

Functional Description

The LMK00334 is a 4-output HCSL clock fanout buffer with low additive jitter that can operate up to 400 MHz. It features a 3:1 input multiplexer with an optional crystal oscillator input, two banks of 2 HCSL outputs, one LVCMOS output, and 3 independent output buffer supplies. The input selection and output buffer modes are controlled via pin strapping. The device is offered in a 32-pin WQFN package and leverages much of the high-speed, low-noise circuit design employed in the LMK04800 family of clock conditioners.

V_{CC} and V_{CCO} Power Supplies

The LMK00334 has separate 3.3 V core supply (V_{CC}) and 3 independent 3.3 V/2.5 V output power supplies (V_{CCOA}, V_{CCOB}, V_{CCOC}). Output supply operation at 2.5 V enables lower power consumption and output-level compatibility with 2.5 V receiver devices. The output levels for HCSL are relatively constant over the specified Vcco range. Refer to Power Supply and Thermal Considerations for additional supply related considerations, such as power dissipation, power supply bypassing, and power supply ripple rejection (PSRR).

NOTE

Care should be taken to ensure the Vcco voltages do not exceed the Vcc voltage to prevent turning-on the internal ESD protection circuitry.

Clock Inputs

The input clock can be selected from CLKin0/CLKin0*, CLKin1/CLKin1*, or OSCin. Clock input selection is controlled using the CLKin_SEL[1:0] inputs as shown in Table 1. Refer to Driving the Clock Inputs for clock input requirements. When CLKin0 or CLKin1 is selected, the crystal circuit is powered down. When OSCin is selected, the crystal oscillator circuit will start-up and its clock will be distributed to all outputs. Refer to Crystal Interface for more information. Alternatively, OSCin may be driven by a single-ended clock (up to 250 MHz) instead of a crystal.

Table 1. Input Selection

CLKin_SEL1	CLKin_SEL0	Selected Input
0	0	CLKin0, CLKin0*
0	1	CLKin1, CLKin1*
1	X	OSCin

Table 2 shows the output logic state vs. input state when either CLKin0/CLKin0* or CLKin1/CLKin1* is selected. When OSCin is selected, the output state will be an inverted copy of the OSCin input state.

Table 2. CLKin Input vs. Output States

State of Selected CLKin	State of Enabled Outputs
CLKinX and CLKinX* inputs floating	Logic low
CLKinX and CLKinX* inputs shorted together	Logic low
CLKin logic low	Logic low
CLKin logic high	Logic high

Clock Outputs

The HCSL output buffer for both Bank A and B outputs are can be disabled to Hi-Z using the CLKout_EN [1:0] as shown in Table 3. For applications where all differential outputs are not needed, any unused output pin should be left floating with a minimum copper length (see note below) to minimize capacitance and potential coupling and reduce power consumption. If all differential outputs are not used, it is recommended to disable (Hi-Z) the banks to reduce power. Refer to Termination and Use of Clock Drivers for more information on output interface and termination techniques.

NOTE

For best soldering practices, the minimum trace length for any unused pin should extend to include the pin solder mask. This way during reflow, the solder has the same copper area as connected pins. This allows for good, uniform fillet solder joints helping to keep the IC level during reflow.

Table 3. Differential Output Buffer Type Selection

CLKout_EN	CLKoutX Buffer Type (Bank A and B)
0	HCSL
1	Disabled (Hi-Z)

Reference Output

The reference output (REFout) provides a LVCMOS copy of the selected input clock. The LVCMOS output high level is referenced to the Vcco voltage. REFout can be enabled or disabled using the enable input pin, REFout_EN, as shown in Table 4.

Table 4. Reference Output Enable

REFout_EN	REFout State
0	Disabled (Hi-Z)
1	Enabled

The REFout_EN input is internally synchronized with the selected input clock by the SYNC block. This synchronizing function prevents glitches and runt pulses from occurring on the REFout clock when enabled or disabled. REFout will be enabled within 3 cycles (t_{EN}) of the input clock after REFout_EN is toggled high. REFout will be disabled within 3 cycles (t_{DIS}) of the input clock after REFout_EN is toggled low.

When REFout is disabled, the use of a resistive loading can be used to set the output to a predetermined level. For example, if REFout is configured with a 1 kΩ load to ground, then the output will be pulled to low when disabled.

ABSOLUTE MAXIMUM RATINGS(1)(2)(3)

Parameter	Symbol	Ratings	Units
Supply Voltages	V_{CC}, V_{CCO}	-0.3 to 3.6	V
Input Voltage	V_{IN}	-0.3 to (V_{CC} + 0.3)	V
Storage Temperature Range	T_{STG}	-65 to +150	°C
Lead Temperature (solder 4 s)	T_L	+260	°C
Junction Temperature	T_J	+150	°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see ELECTRICAL CHARACTERISTICS. The ensured specifications apply only to the test conditions listed.

(2) This device is a high-performance integrated circuit with an ESD rating up to 2 kV Human Body Model, up to 150 V Machine Model, and up to 750 V Charged Device Model and is ESD sensitive. Handling and assembly of this device should only be done at ESD-free workstations.

(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
Ambient Temperature Range	T_A	-40	25	85	°C
Junction Temperature	T_J			125	°C
Core Supply Voltage Range	V_{CC}	3.15	3.3	3.45	V
Output Supply Voltage Range (1) (2)	V_{CCO}	3.3 – 5% 2.5 – 5%	3.3 2.5	3.3 + 5% 2.5 + 5%	V

(1) The output supply voltages or pins (V_{CCOA}, V_{CCOB}, and V_{CCOC}) will be called V_{CCO} in general when no distinction is needed, or when the output supply can be inferred from the output bank/type.

(2) Vcco for any output bank should be less than or equal to Vcc (Vcco ≤ Vcc).

PACKAGE THERMAL RESISTANCE

Package	θ_{JA}	$\theta_{JC\ (DAP)}$
32-Lead WQFN (1)	38.1 °C/W	7.2 °C/W

(1) Specification assumes 5 thermal vias connect the die attach pad (DAP) to the embedded copper plane on the 4-layer JEDEC board. These vias play a key role in improving the thermal performance of the package. It is recommended that the maximum number of vias be used in the board layout.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified: Vcc = 3.3 V ± 5%, Vcco = 3.3 V ± 5%, 2.5 V ± 5%, -40 °C ≤ T_A ≤ 85 °C, CLKin driven differentially, input slew rate ≥ 3 V/ns. Typical values represent most likely parametric norms at Vcc = 3.3 V, Vcco = 3.3 V, T_A = 25 °C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured. (1)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
Current Consumption(2)							
ICC_CORE	Core Supply Current, All Outputs Disabled	CLKinX selected			8.5	10.5	mA
		OSCin selected			10	13.5	mA
ICC_HCSL					50	58.5	mA
ICC_CMOS					3.5	5.5	mA
ICCO_HCSL	Additive Output Supply Current, HCSL Banks Enabled	Includes Output Bank Bias and Load Currents for both banks, RT = 50 Ω on all outputs			65	81.5	mA
ICCO_CMOS	Additive Output Supply Current, LVCMOS Output Enabled	200 MHz, C_L = 5 pF	Vcco = 3.3 V ±5%		9	10	mA
			Vcco = 2.5V ± 5%		7	8	mA
Power Supply Ripple Rejection (PSRR)							
$PSRR_{HCSL}$	Ripple-Induced Phase Spur Level(3) Differential HCSL Output		156.25 MHz		-72		dBc
			312.5 MHz		-63		
CMOS Control Inputs (CLKin_SELn, CLKout_TYPEn, REFout_EN)							
V_{IH}	High-Level Input Voltage			1.6		Vcc	V
V_{IL}	Low-Level Input Voltage			GND		0.4	V
I_{IH}	High-Level Input Current	V_{IH} = V_{cc}, Internal pull-down resistor				50	µA
I_{IL}	Low-Level Input Current	V_{IL} = 0 V, Internal pull-down resistor		-5	0.1		µA
Clock Inputs (CLKin0/CLKin0*, CLKin1/CLKin1*)							
f_{CLKin}	Input Frequency Range(4)	Functional up to 400 MHz Output frequency range and timing specified per output type (refer to LVCMOS output specifications)		DC		400	MHz
V_{IHD}	Differential Input High Voltage	CLKin driven differentially				Vcc	V
V_{ILD}	Differential Input Low Voltage			GND			V
V_{ID}	Differential Input Voltage Swing(5)			0.15		1.3	V
V_{CMD}	Differential Input CMD Common Mode Voltage	V_{ID} = 150 mV		0.25		Vcc - 1.2	V
		V_{ID} = 350 mV		0.25		Vcc - 1.1	
		V_{ID} = 800 mV		0.25		Vcc - 0.9	
V_{IH}	Single-Ended Input IH High Voltage	CLKinX driven single-ended (AC or DC coupled), CLKinX* AC coupled to GND or externally biased within V_{CM} range				VCC	V
V_{IL}	Single-Ended Input IL Low Voltage			GND			V
V_{I_SE}	Single-Ended Input Voltage Swing(4)			0.3		2	Vpp
V_{CM}	Single-Ended Input CM Common Mode Voltage			0.25		VCC - 1.2	V

(1) The output supply voltages or pins (V_{CCOA}, V_{CCOB}, and V_{CCOC}) will be called V_{CCO} in general when no distinction is needed, or when the output supply can be inferred from the output bank/type.

(2) See Power Supply and Thermal Considerations for more information on current consumption and power dissipation calculations.

(3) Power supply ripple rejection, or PSRR, is defined as the single-sideband phase spur level (in dBc) modulated onto the clock output when a single-tone sinusoidal signal (ripple) is injected onto the Vcco supply. Assuming no amplitude modulation effects and small index modulation, the peak-to-peak deterministic jitter (DJ) can be calculated using the measured single-sideband phase spur level (PSRR) as follows: DJ (ps pk-pk) = [(2 * 10(^{PSRR} / 20)) / (π * f_{CLK})] * 1E12

(4) Specification is ensured by characterization and is not tested in production.

(5) See Differential Voltage Measurement Terminology for definition of V_{ID} and V_{OD} voltages.

ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise specified: Vcc = 3.3 V ± 5%, Vcco = 3.3 V ± 5%, 2.5 V ± 5%, -40 °C ≤ T_A ≤ 85 °C, CLKin driven differentially, input slew rate ≥ 3 V/ns. Typical values represent most likely parametric norms at Vcc = 3.3 V, Vcco = 3.3 V, T_A = 25 °C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured. (1)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
ISO_{MUX}	Mux Isolation, CLKin0 to CLKin1	f_{OFFSET} > 50 kHz, P_{CLKinX} = 0 dBm	f_{CLKin0} = 100 MHz		-84		dBc
			f_{CLKin0} = 200 MHz		-82		
			f_{CLKin0} = 500 MHz		-71		
			f_{CLKin0} = 1000 MHz		-65		
Crystal Interface (OSCin, OSCout)							
F_{CLK}	External Clock Frequency Range (6)	OSCin driven single-ended, OSCout floating				250	MHz
F_{XTAL}	Crystal Frequency Range	Fundamental mode crystal ESR ≤ 200 Ω (10 to 30 MHz) ESR ≤ 125 Ω (30 to 40 MHz) (7)		10		40	MHz
C_{IN}	OSCin Input Capacitance				1		pF
HCSL Outputs (CLKoutAn/CLKoutAn*, CLKoutBn/CLKoutBn*)							
f_{CLKout}	Output Frequency Range (6)	R_L = 50 Ω to GND, C_L ≤ 5 pF		DC		400	MHz
$Jitter_{ADD\_PCIe}$	Additive RMS Phase Jitter for PCIe 3.0 (6)	PCIe Gen 3, PLL BW = 2–5 MHz, CDR = 10 MHz	CLKin: 100 MHz, Slew rate ≥ 0.6 V/ns		0.03	0.15	ps
$Jitter_{ADD}$	Additive RMS Jitter Integration Bandwidth 1 MHz to 20 MHz (8)	Vcco = 3.3 V, RT = 50 Ω to GND	CLKin: 100 MHz, Slew rate ≥ 3 V/ns		77		fs
			CLKin: 156.25 MHz, Slew rate ≥ 2.7 V/ns		86		
Noise Floor	Noise Floor f_{OFFSET} ≥ 10 MHz (9) (10)	Vcco = 3.3 V, RT = 50 Ω to GND	CLKin: 100 MHz, Slew rate ≥ 3 V/ns		-161.3		dBc/Hz
			CLKin: 156.25 MHz, Slew rate ≥ 2.7 V/ns		-156.3		
DUTY	Duty Cycle (6)	50% input clock duty cycle		45		55	%
V_{OH}	Output High Voltage	T_A = 25 °C, DC Measurement, R_T = 50 Ω to GND		520	810	920	mV
V_{OL}	Output Low Voltage			-150	0.5	150	mV
V_{CROSS}	Absolute Crossing Voltage (6) (11)	R_L = 50 Ω to GND, C_L ≤ 5 pF		250	350	460	mV
ΔV_{CROSS}	Total Variation of V_{CROSS} (6) (11)					140	mV
t_R	Output Rise Time 20% to 80% (11) (12)	250 MHz, Uniform transmission line up to 10 in. with 50-Ω characteristic impedance, RL = 50 Ω to GND, C_L ≤ 5 pF			300	500	ps
t_F	Output Fall Time 80% to 20% (11) (12)				300	500	ps

(6) Specification is ensured by characterization and is not tested in production.

(7) The ESR requirements stated must be met to ensure that the oscillator circuitry has no startup issues. However, lower ESR values for the crystal may be necessary to stay below the maximum power dissipation (drive level) specification of the crystal. Refer to Crystal Interface for crystal drive level considerations.

(8) For the 100 MHz and 156.25 MHz clock input conditions, Additive RMS Jitter (J_{ADD}) is calculated using Method #1: $J_{ADD} = SQRT(J_{OUT}^2 - J_{SOURCE}^2)$, where J_{OUT} is the total RMS jitter measured at the output driver and J_{SOURCE} is the RMS jitter of the clock source applied to CLKin. For the 625 MHz clock input condition, Additive RMS Jitter is approximated using Method #2: $J_{ADD} = SQRT(2*10^{dBc/10}) / (2*\pi*f_{CLK})$, where dBc is the phase noise power of the Output Noise Floor integrated from 1 to 20 MHz bandwidth. The phase noise power can be calculated as: dBc = Noise Floor + $10*\log_{10}$(20 MHz - 1 MHz). The additive RMS jitter was approximated for 625 MHz using Method #2 because the RMS jitter of the clock source was not sufficiently low enough to allow practical use of Method #1. Refer to the “Noise Floor vs. CLKin Slew Rate” and “RMS Jitter vs. CLKin Slew Rate” plots in TYPICAL CHARACTERISTICS.

(9) The noise floor of the output buffer is measured as the far-out phase noise of the buffer. Typically this offset is ≥ 10 MHz, but for lower frequencies this measurement offset can be as low as 5 MHz due to measurement equipment limitations.

(10) Phase noise floor will degrade as the clock input slew rate is reduced. Compared to a single-ended clock, a differential clock input (LVPECL, LVDS) will be less susceptible to degradation in noise floor at lower slew rates due to its common mode noise rejection. However, it is recommended to use the highest possible input slew rate for differential clocks to achieve optimal noise floor performance at the device outputs.

(11) AC timing parameters for HCSL or CMOS are dependent on output capacitive loading.

(12) Parameter is specified by design, not tested in production.

ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise specified: Vcc = 3.3 V ± 5%, Vcco = 3.3 V ± 5%, 2.5 V ± 5%, -40 °C ≤ T_A ≤ 85 °C, CLKin driven differentially, input slew rate ≥ 3 V/ns. Typical values represent most likely parametric norms at Vcc = 3.3 V, Vcco = 3.3 V, T_A = 25 °C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured. (1)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
LVCMOS Output (REFout)							
f_{CLKout}	Output Frequency Range (13)	CL ≤ 5 pF		DC		250	MHz
$Jitter_{ADD}$	Additive RMS Jitter Integration Bandwidth 1 MHz to 20 MHz (14)	Vcco = 3.3 V, CL ≤ 5 pF	100 MHz, Input Slew rate ≥ 3 V/ns		95		fs
Noise Floor	Noise Floor f_{OFFSET} ≥ 10 MHz (15) (16)	Vcco = 3.3 V, CL ≤ 5 pF	100 MHz, Input Slew rate ≥ 3 V/ns		-159.3		dBc/Hz
DUTY	Duty Cycle (13)	50% input clock duty cycle		45		55	%
V_{OH}	Output High Voltage	1 mA load		Vcco - 0.1			V
V_{OL}	Output Low Voltage					0.1	V
I_{OH}	Output High Current (Source)	Vo = Vcco / 2	Vcco = 3.3 V		28		mA
			Vcco = 2.5 V		20		
			Vcco = 3.3 V		28		mA
I_{OL}	Output Low Current (Sink)		Vcco = 2.5 V		20		
t_R	Output Rise Time 20% to 80% (17) (18)	250 MHz, Uniform transmission line up to 10 in. with 50-Ω characteristic impedance, RL = 50 Ω to GND, CL ≤ 5 pF			225	400	ps
t_F	Output Fall Time 80% to 20% (19) (18)				225	400	ps
t_{EN}	Output Enable Time (19)	C_L ≤ 5 pF				3	cycles
t_{DIS}	Output Disable Time (19)					3	cycles
Propagation Delay and Output Skew							
t_{PD_HCSL}	Propagation Delay CLKin-to-HCSL (17) (18)	R_T = 50 Ω to GND, C_L ≤ 5 pF		295	590	885	ps
t_{PD_CMOS}	Propagation Delay CLKin-to-LVCMOS (17) (18)	CL ≤ 5 pF	Vcco = 3.3 V	900	1475	2300	ps
			Vcco = 2.5 V	1000	1550	2700	
$t_{SK(O)}$	Output Skew (20) (17) (13)	Skew specified between any two CLKouts. Load conditions are the same as propagation delay specifications.			30	50	ps
$t_{SK(PP)}$	Part-to-Part Output Skew (17) (18) (20)				80	120	ps

(13) Specification is ensured by characterization and is not tested in production.
(14) For the 100 MHz and 156.25 MHz clock input conditions, Additive RMS Jitter (J_{ADD}) is calculated using Method #1: J_{ADD} = SQRT(J_{OUT}^2 - J_{SOURCE}^2), where J_{OUT} is the total RMS jitter measured at the output driver and J_{SOURCE} is the RMS jitter of the clock source applied to CLKin. For the 625 MHz clock input condition, Additive RMS Jitter is approximated using Method #2: J_{ADD} = SQRT(2*$10^{dBc/10}$) / (2*π*f_{CLK}), where dBc is the phase noise power of the Output Noise Floor integrated from 1 to 20 MHz bandwidth. The phase noise power can be calculated as: dBc = Noise Floor + 10*$\log_{10}$(20 MHz - 1 MHz). The additive RMS jitter was approximated for 625 MHz using Method #2 because the RMS jitter of the clock source was not sufficiently low enough to allow practical use of Method #1. Refer to the "Noise Floor vs. CLKin Slew Rate" and "RMS Jitter vs. CLKin Slew Rate" plots in TYPICAL CHARACTERISTICS.
(15) The noise floor of the output buffer is measured as the far-out phase noise of the buffer. Typically this offset is ≥ 10 MHz, but for lower frequencies this measurement offset can be as low as 5 MHz due to measurement equipment limitations.
(16) Phase noise floor will degrade as the clock input slew rate is reduced. Compared to a single-ended clock, a differential clock input (LVPECL, LVDS) will be less susceptible to degradation in noise floor at lower slew rates due to its common mode noise rejection. However, it is recommended to use the highest possible input slew rate for differential clocks to achieve optimal noise floor performance at the device outputs.
(17) AC timing parameters for HCSL or CMOS are dependent on output capacitive loading.
(18) Parameter is specified by design, not tested in production.
(19) Output Enable Time is the number of input clock cycles it takes for the output to be enabled after REFout_EN is pulled high. Similarly, Output Disable Time is the number of input clock cycles it takes for the output to be disabled after REFout_EN is pulled low. The REFout_EN signal should have an edge transition much faster than that of the input clock period for accurate measurement.
(20) Output skew is the propagation delay difference between any two outputs with identical output buffer type and equal loading while operating at the same supply voltage and temperature conditions.

MEASUREMENT DEFINITIONS

Differential Voltage Measurement Terminology

The differential voltage of a differential signal can be described by two different definitions causing confusion when reading datasheets or communicating with other engineers. This section will address the measurement and description of a differential signal so that the reader will be able to understand and discern between the two different definitions when used.

The first definition used to describe a differential signal is the absolute value of the voltage potential between the inverting and non-inverting signal. The symbol for this first measurement is typically V_{ID} or V_{OD} depending on if an input or output voltage is being described.

The second definition used to describe a differential signal is to measure the potential of the non-inverting signal with respect to the inverting signal. The symbol for this second measurement is V_{SS} and is a calculated parameter. Nowhere in the IC does this signal exist with respect to ground, it only exists in reference to its differential pair. V_{SS} can be measured directly by oscilloscopes with floating references, otherwise this value can be calculated as twice the value of V_{OD} as described in the first description.

Figure 3 illustrates the two different definitions side-by-side for inputs and Figure 4 illustrates the two different definitions side-by-side for outputs. The V_{ID} (or V_{OD}) definition show the DC levels, V_{IH} and V_{OL} (or V_{OH} and V_{OL}), that the non-inverting and inverting signals toggle between with respect to ground. V_{SS} input and output definitions show that if the inverting signal is considered the voltage potential reference, the non-inverting signal voltage potential is now increasing and decreasing above and below the non-inverting reference. Thus the peak-to-peak voltage of the differential signal can be measured.

V_{ID} and V_{OD} are often defined as volts (V) and V_{SS} is often defined as volts peak-to-peak (V_{PP}).

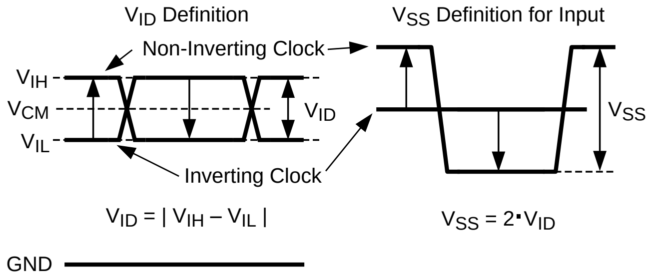


Figure 3. Two Different Definitions for Differential Input Signals

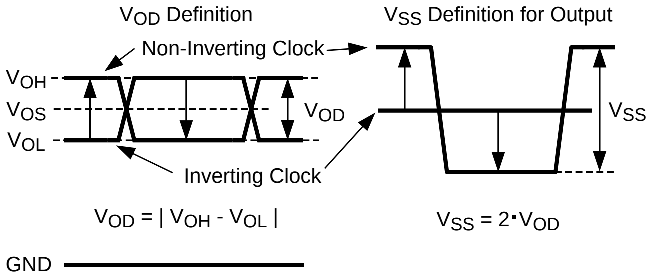


Figure 4. Two Different Definitions for Differential Output Signals

Refer to Application Note AN-912 (literature number SNLA036), *Common Data Transmission Parameters and their Definitions*, for more information.

TYPICAL CHARACTERISTICS

Unless otherwise specified: Vcc = 3.3 V, Vcco = 3.3 V, T_A = 25 °C, CLKin driven differentially, input slew rate ≥ 3 V/ns.

HCSL Output Swing @ 250 MHz

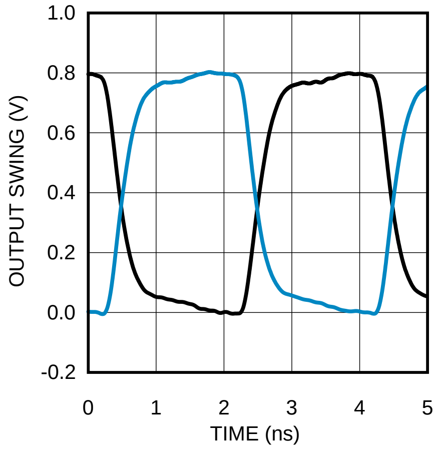


Figure 5.

LVCMOS Output Swing @ 250 MHz

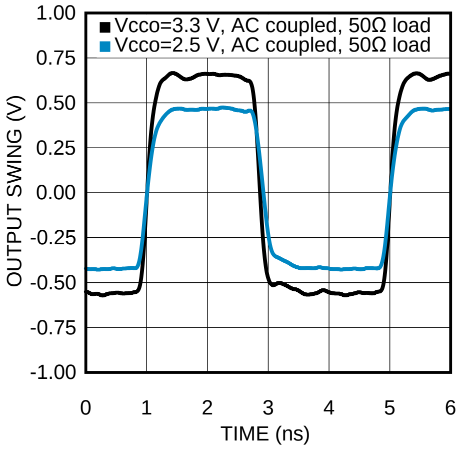


Figure 6.

Noise Floor vs. CLKin Slew Rate @ 100 MHz

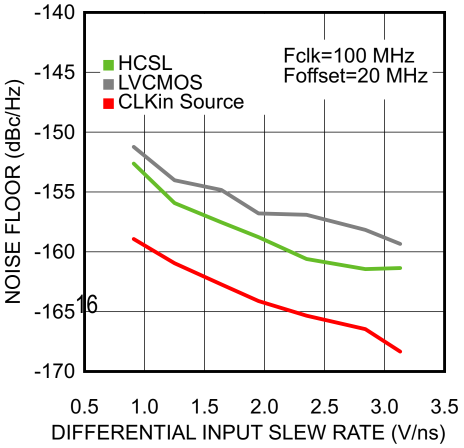


Figure 7.

Noise Floor vs. CLKin Slew Rate @ 156.25 MHz

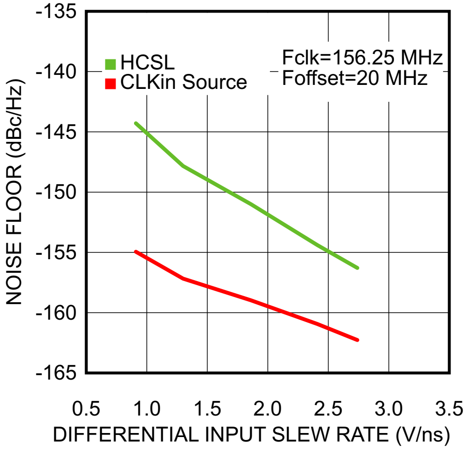


Figure 8.

RMS Jitter vs. CLKin Slew Rate @ 100 MHz

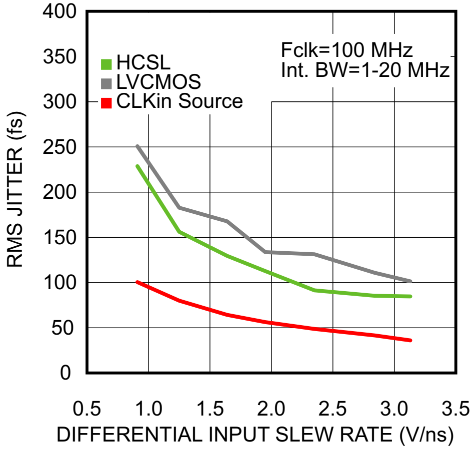


Figure 9.

RMS Jitter vs. CLKin Slew Rate @ 156.25 MHz

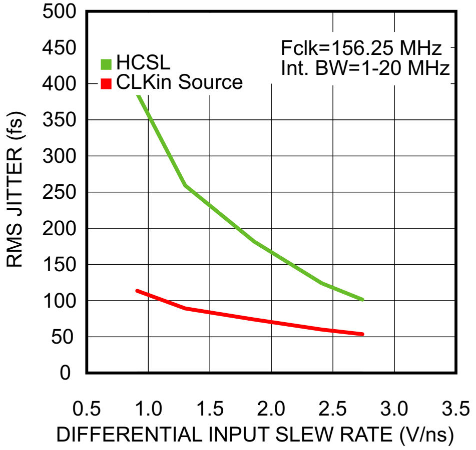


Figure 10.

TYPICAL CHARACTERISTICS (continued)

Unless otherwise specified: Vcc = 3.3 V, Vcco = 3.3 V, T_A = 25 °C, CLKin driven differentially, input slew rate ≥ 3 V/ns.

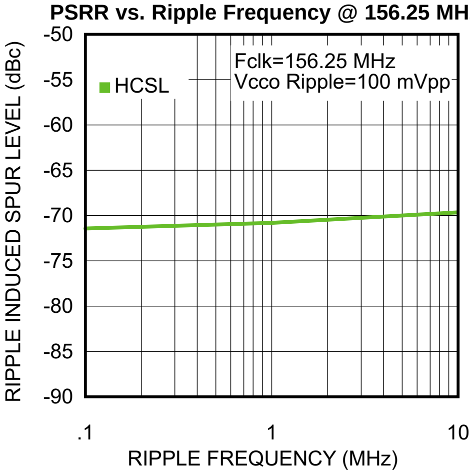


Figure 11.

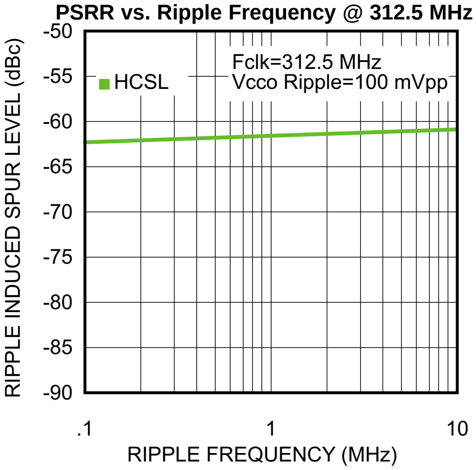


Figure 12.

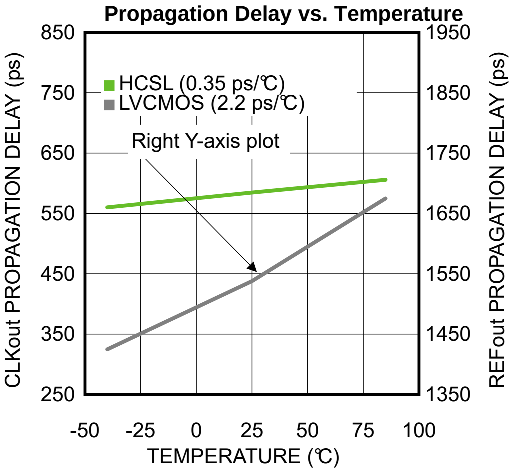
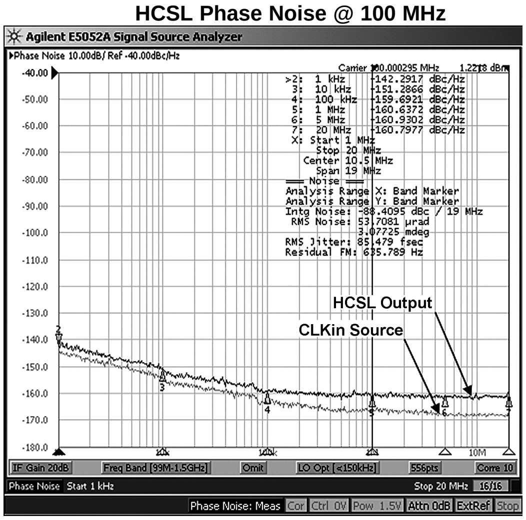


Figure 13.



```
Phase Noise 10.00dB/ Ref -40.00dBc/Hz
                              Carrier 100.000295 MHz      1.2218 dBm
>2:  1 kHz     -142.2917 dBc/Hz
 3:  10 kHz    -151.2866 dBc/Hz
 4:  100 kHz   -159.6921 dBc/Hz
 5:  1 MHz     -160.6372 dBc/Hz
 6:  5 MHz     -160.9302 dBc/Hz
 7:  20 MHz    -160.7977 dBc/Hz
 X: Start 1 MHz
      Stop 20 MHz
    Center 10.5 MHz
      Span 19 MHz
═══ Noise ═══
Analysis Range X: Band Marker
Analysis Range Y: Band Marker
Intg Noise: -88.4095 dBc / 19 MHz
 RMS Noise: 53.7081 µrad
            3.07725 mdeg
RMS Jitter: 85.479 fsec
Residual FM: 635.789 Hz
Phase Noise  Start 1 kHz                         Stop 20 MHz
Phase Noise: Meas
```

Figure 14.

(1) The typical RMS jitter values in the plots show the total output RMS jitter (J_{OUT}) for each output buffer type and the source clock RMS jitter (J_{SOURCE}). From these values, the Additive RMS Jitter can be calculated as: J_{ADD} = SQRT(J_{OUT}^2 - J_{SOURCE}^2).

(2) 20 MHz crystal characteristics: Abracon ABL series, AT cut, C_L = 18 pF , C_0 = 4.4 pF measured (7 pF max), ESR = 8.5 Ω measured (40 Ω max), and Drive Level = 1 mW max (100 µW typical).

(3) 40 MHz crystal characteristics: Abracon ABLS2 series, AT cut, C_L = 18 pF , C_0 = 5 pF measured (7 pF max), ESR = 5 Ω measured (40 Ω max), and Drive Level = 1 mW max (100 µW typical).

TYPICAL CHARACTERISTICS (continued)

Unless otherwise specified: Vcc = 3.3 V, Vcco = 3.3 V, T_A = 25 °C, CLKin driven differentially, input slew rate ≥ 3 V/ns.

Crystal Power Dissipation vs. R_{LIM}

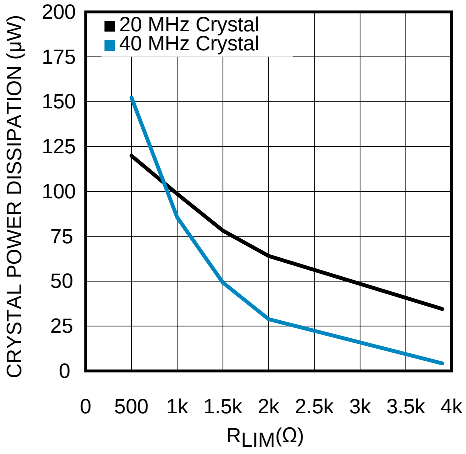


Figure 15.

APPLICATION INFORMATION

Driving the Clock Inputs

The LMK00334 has two universal inputs (CLKin0/CLKin0* and CLKin1/CLKin1*) that can accept DC-coupled 3.3V/2.5V LVPECL, LVDS, CML, SSTL, and other differential and single-ended signals that meet the input requirements specified in ELECTRICAL CHARACTERISTICS. The device can accept a wide range of signals due to its wide input common mode voltage range (V_{CM}) and input voltage swing (V_{ID}) / dynamic range. For 50% duty cycle and DC-balanced signals, AC coupling may also be employed to shift the input signal to within the V_{CM} range. Refer to Termination and Use of Clock Drivers for signal interfacing and termination techniques.

To achieve the best possible phase noise and jitter performance, it is mandatory for the input to have high slew rate of 3 V/ns (differential) or higher. Driving the input with a lower slew rate will degrade the noise floor and jitter. For this reason, a differential signal input is recommended over single-ended because it typically provides higher slew rate and common-mode-rejection. Refer to the "Noise Floor vs. CLKin Slew Rate" and "RMS Jitter vs. CLKin Slew Rate" plots in TYPICAL CHARACTERISTICS.

While it is recommended to drive the CLKin/CLKin* pair with a differential signal input, it is possible to drive it with a single-ended clock provided it conforms to the Single-Ended Input specifications for CLKin pins listed in the ELECTRICAL CHARACTERISTICS. For large single-ended input signals, such as 3.3V or 2.5V LVCMOS, a 50 Ω load resistor should be placed near the input for signal attenuation to prevent input overdrive as well as for line termination to minimize reflections. Again, the single-ended input slew rate should be as high as possible to minimize performance degradation. The CLKin input has an internal bias voltage of about 1.4 V, so the input can be AC coupled as shown in Figure 16. The output impedance of the LVCMOS driver plus Rs should be close to 50 Ω to match the characteristic impedance of the transmission line and load termination.

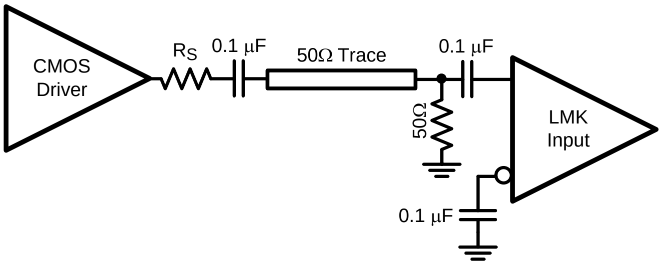


Figure 16. Single-Ended LVCMOS Input, AC Coupling

A single-ended clock may also be DC coupled to CLKinX as shown in Figure 17. A 50-Ω load resistor should be placed near the CLKin input for signal attenuation and line termination. Because half of the single-ended swing of the driver ($V_{O,PP}$ / 2) drives CLKinX, CLKinX* should be externally biased to the midpoint voltage of the attenuated input swing (($V_{O,PP}$ / 2) × 0.5). The external bias voltage should be within the specified input common voltage (V_{CM}) range. This can be achieved using external biasing resistors in the kΩ range (R_{B1} and R_{B2}) or another low-noise voltage reference. This will ensure the input swing crosses the threshold voltage at a point where the input slew rate is the highest.

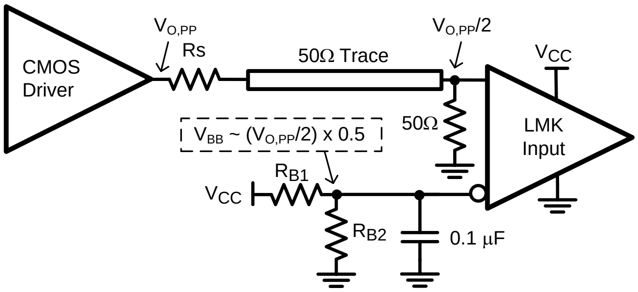


Figure 17. Single-Ended LVCMOS Input, DC Coupling with Common Mode Biasing

If the crystal oscillator circuit is not used, it is possible to drive the OSCin input with an single-ended external clock as shown in Figure 18. The input clock should be AC coupled to the OSCin pin, which has an internally-generated input bias voltage, and the OSCout pin should be left floating. While OSCin provides an alternative input to multiplex an external clock, it is recommended to use either universal input (CLKinX) since it offers higher operating frequency, better common mode and power supply noise rejection, and greater performance over supply voltage and temperature variations.

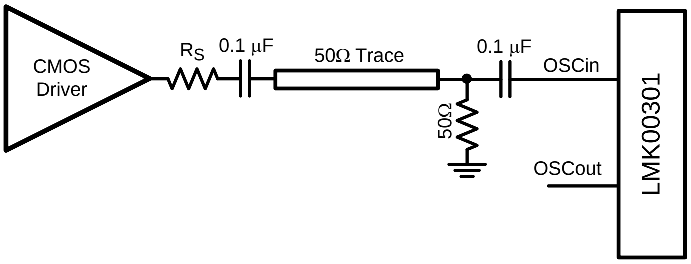


Figure 18. Driving OSCin with a Single-Ended Input

Crystal Interface

The LMK00334 has an integrated crystal oscillator circuit that supports a fundamental mode, AT-cut crystal. The crystal interface is shown in Figure 19.

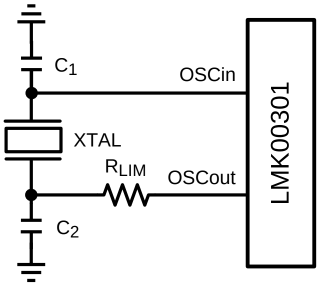


Figure 19. Crystal Interface

The load capacitance (C_L) is specific to the crystal, but usually on the order of 18 - 20 pF. While C_L is specified for the crystal, the OSCin input capacitance (C_{IN} = 1 pF typical) of the device and PCB stray capacitance (C_{STRAY} ~ 1~3 pF) can affect the discrete load capacitor values, C_1 and C_2.

For the parallel resonant circuit, the discrete capacitor values can be calculated as follows:

$$C_L = (C_1 * C_2) / (C_1 + C_2) + C_{IN} + C_{STRAY} \quad (1)$$

Typically, $C_1 = C_2$ for optimum symmetry, so Equation 1 can be rewritten in terms of C_1 only:

$$C_L = C_1^2 / (2 * C_1) + C_{IN} + C_{STRAY} \quad (2)$$

Finally, solve for C_1:

$$C_1 = (C_L - C_{IN} - C_{STRAY})*2 \quad (3)$$

ELECTRICAL CHARACTERISTICS provides crystal interface specifications with conditions that ensure start-up of the crystal, but it does not specify crystal power dissipation. The designer will need to ensure the crystal power dissipation does not exceed the maximum drive level specified by the crystal manufacturer. Overdriving the crystal can cause premature aging, frequency shift, and eventual failure. Drive level should be held at a sufficient level necessary to start-up and maintain steady-state operation.

The power dissipated in the crystal, P_{XTAL}, can be computed by:

$$P_{XTAL} = I_{RMS}{}^2 * R_{ESR}*(1 + C_0/C_L)^2 \quad (4)$$

where

- I_{RMS} is the RMS current through the crystal.
- R_{ESR} is the max. equivalent series resistance specified for the crystal
- C_L is the load capacitance specified for the crystal
- C_0 is the min. shunt capacitance specified for the crystal

I_{RMS} can be measured using a current probe (e.g. Tektronix CT-6 or equivalent) placed on the leg of the crystal connected to OSCout with the oscillation circuit active.

As shown in Figure 19, an external resistor, R_{LIM}, can be used to limit the crystal drive level, if necessary. If the power dissipated in the selected crystal is higher than the drive level specified for the crystal with R_{LIM} shorted, then a larger resistor value is mandatory to avoid overdriving the crystal. However, if the power dissipated in the crystal is less than the drive level with R_{LIM} shorted, then a zero value for R_{LIM} can be used. As a starting point, a suggested value for R_{LIM} is 1.5 kΩ.

Termination and Use of Clock Drivers

When terminating clock drivers keep in mind these guidelines for optimum phase noise and jitter performance:

- Transmission line theory should be followed for good impedance matching to prevent reflections.
- Clock drivers should be presented with the proper loads.
  - HCSL drivers are switched current outputs and require a DC path to ground via 50 Ω termination.
- Receivers should be presented with a signal biased to their specified DC bias level (common mode voltage) for proper operation. Some receivers have self-biasing inputs that automatically bias to the proper voltage level; in this case, the signal should normally be AC coupled.

Termination for DC Coupled Differential Operation

For DC coupled operation of an HCSL driver, terminate with 50 Ω to ground near the driver output as shown in Figure 20. Series resistors, Rs, may be used to limit overshoot due to the fast transient current. Because HCSL drivers require a DC path to ground, AC coupling is not allowed between the output drivers and the 50 Ω termination resistors.

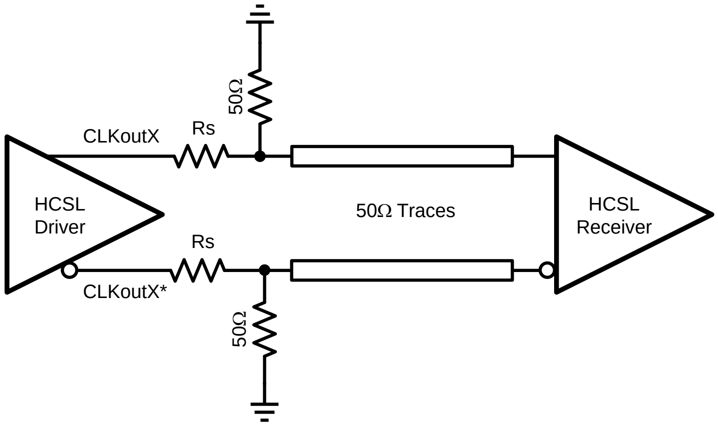


Figure 20. HCSL Operation, DC Coupling

Termination for AC Coupled Differential Operation

AC coupling allows for shifting the DC bias level (common mode voltage) when driving different receiver standards. Since AC coupling prevents the driver from providing a DC bias voltage at the receiver, it is important to ensure the receiver is biased to its ideal DC level.

Power Supply and Thermal Considerations

Current Consumption and Power Dissipation Calculations

The current consumption values specified in ELECTRICAL CHARACTERISTICS can be used to calculate the total power dissipation and IC power dissipation for any device configuration. The total V_{CC} core supply current (I_{CC_TOTAL}) can be calculated using Equation 5:

$$\mathbf{I_{CC\_TOTAL} = I_{CC\_CORE} + I_{CC\_BANKS} + I_{CC\_CMOS}}$$

where

- I_{CC_CORE} is the V_{CC} current for core logic and input blocks and depends on selected input (CLKinX or OSCin).
- I_{CC_HCSL} is the V_{CC} current for Banks A & B
- I_{CC_CMOS} is the V_{CC} current for the LVCMOS output (or 0 mA if REFout is disabled). (5)

Since the output supplies (V_{CCOA}, V_{CCOB}, V_{CCOC}) can be powered from 3 independent voltages, the respective output supply currents ($I_{CCO\_BANK\_A}$, $I_{CCO\_BANK\_B}$, and I_{CCO_CMOS}) should be calculated separately.

I_{CCO_BANK} for either Bank A or B may be taken as 50% of the corresponding output supply current specified for two banks (I_{CCO_HCSL}) **provided the output loading matches the specified conditions**. Otherwise, I_{CCO_BANK} should be calculated per bank as follows:

$$I_{CCO\_BANK} = I_{BANK\_BIAS} + (N * I_{OUT\_LOAD})$$

where

- I_{BANK_BIAS} is the output bank bias current (fixed value).
- I_{OUT_LOAD} is the DC load current per loaded output pair.
- N is the number of loaded output pairs (N = 0 to 2). (6)

Table 5 shows the typical I_{BANK_BIAS} values and I_{OUT_LOAD} expressions for HCSL.

Table 5. Typical Output Bank Bias and Load Currents

Current Parameter	HCSL
I_{BANK_BIAS}	2.4 mA
I_{OUT_LOAD}	V_{OH}/R_T

Once the current consumption is known for each supply, the total power dissipation (P_{TOTAL}) can be calculated:

$$\mathbf{P_{TOTAL} = (V_{CC}*I_{CC\_TOTAL}) + (V_{CCOA}*I_{CCO\_BANK}) + (V_{CCOB}*I_{CCO\_BANK}) + (V_{CCOC}*I_{CCO\_CMOS})} \quad (7)$$

If the device is configured with HCSL outputs, then it is also necessary to calculate the power dissipated in any termination resistors (P_{RT_HCSL}). The external power dissipation values can be calculated as follows:

$$\mathbf{P_{RT\_HCSL}\ (per\ HCSL\ pair) = V_{OH}^2 / R_T} \quad (8)$$

Finally, the IC power dissipation (P_{DEVICE}) can be computed by subtracting the external power dissipation values from P_{TOTAL} as follows:

$$\mathbf{P_{DEVICE} = P_{TOTAL} - N*P_{RT\_HCSL}}$$

where

- N is the number of HCSL output pairs with termination resistors to GND. (9)

Power Dissipation Example: Worst-Case Dissipation

This example shows how to calculate IC power dissipation for a configuration to estimate **worst-case power dissipation**. In this case, the maximum supply voltage and supply current values specified in ELECTRICAL CHARACTERISTICS are used.

- Max $V_{CC} = V_{CCO} = 3.465$ V. Max I_{CC} and I_{CCO} values.
- CLKin0/CLKin0* input is selected.
- Banks A and B are enabled, and all outputs are terminated with 50 Ω to GND.
- REFout is enabled with 5 pF load.
- $T_A = 85$ °C

Using the power calculations from the previous section and *maximum* supply current specifications, we can compute P_{TOTAL} and P_{DEVICE}.

- From Equation 5: I_{CC_TOTAL} = 10.5 mA + 58.5 mA + 5.5 mA = 74.5 mA
- From I_{CCO_HCSL} max spec: I_{CCO_BANK} = 50% of I_{CCO_HCSL} = 40.75 mA
- From Equation 7: P_{TOTAL} = (3.465 V * 74.5 mA) + (3.465 V * 40.75 mA)+ (3.465 V * 40.75 mA) + (3.465 V * 10 mA) = 575.2 mW
- From Equation 8: P_{RT_HCSL} = $(0.92V)^2$ / 50Ω = 16.9 mW (per output pair)
- From Equation 9: P_{DEVICE} = 575.2 mW - (4 * 16.9 mW) = 510.4 mW

In this worst-case example, the IC device will dissipate about 510.4 mW or 88.7% of the total power (575.2 mW), while the remaining 11.3% will be dissipated in the termination resistors (64.8 mW for 4 pairs). Based on θ_{JA} of 38.1 °C/W, the estimate die junction temperature would be about 19.4 °C above ambient, or 104.4 °C when T_A = 85 °C.

Power Supply Bypassing

The Vcc and Vcco power supplies should have a high-frequency bypass capacitor, such as 0.1 uF or 0.01 uF, placed very close to each supply pin. 1 uF to 10 uF decoupling capacitors should also be placed nearby the device between the supply and ground planes. All bypass and decoupling capacitors should have short connections to the supply and ground plane through a short trace or via to minimize series inductance.

Power Supply Ripple Rejection

In practical system applications, power supply noise (ripple) can be generated from switching power supplies, digital ASICs or FPGAs, etc. While power supply bypassing will help filter out some of this noise, it is important to understand the effect of power supply ripple on the device performance. When a single-tone sinusoidal signal is applied to the power supply of a clock distribution device, such as LMK00334, it can produce narrow-band phase modulation as well as amplitude modulation on the clock output (carrier). In the single-side band phase noise spectrum, the ripple-induced phase modulation appears as a phase spur level relative to the carrier (measured in dBc).

For the LMK00334, power supply ripple rejection, or PSRR, was measured as the single-sideband phase spur level (in dBc) modulated onto the clock output when a ripple signal was injected onto the Vcco supply. The PSRR test setup is shown in Figure 21.

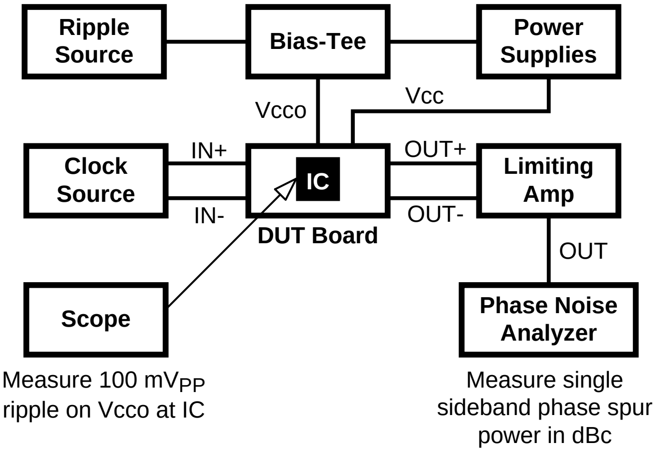


Figure 21. PSRR Test Setup

A signal generator was used to inject a sinusoidal signal onto the Vcco supply of the DUT board, and the peak-to-peak ripple amplitude was measured at the Vcco pins of the device. A limiting amplifier was used to remove amplitude modulation on the differential output clock and convert it to a single-ended signal for the phase noise analyzer. The phase spur level measurements were taken for clock frequencies of 156.25 MHz and 312.5 MHz under the following power supply ripple conditions:

- Ripple amplitude: 100 mVpp on Vcco = 2.5 V
- Ripple frequencies: 100 kHz, 1 MHz, and 10 MHz

Assuming no amplitude modulation effects and small index modulation, the peak-to-peak deterministic jitter (DJ) can be calculated using the measured single-sideband phase spur level (PSRR) as follows:

$$\text{DJ (ps pk-pk)} = [(2*10^{(\text{PSRR} / 20)}) / (\pi*f_{\text{CLK}})] * 10^{12} \quad (10)$$

The “PSRR vs. Ripple Frequency” plots in TYPICAL CHARACTERISTICS show the ripple-induced phase spur levels at 156.25 MHz and 312.5 MHz. The LMK00334 exhibits very good and well-behaved PSRR characteristics across the ripple frequency range. The phase spur levels for HCSL are below -72 dBc at 156.25 MHz and below -63 dBc at 312.5 MHz. Using Equation 10, these phase spur levels translate to Deterministic Jitter values of 1.02 ps pk-pk at 156.25 MHz and 1.44 ps pk-pk at 312.5 MHz. Testing has shown that the PSRR performance of the device improves for Vcco = 3.3 V under the same ripple amplitude and frequency conditions.

Thermal Management

Power dissipation in the LMK00334 device can be high enough to require attention to thermal management. For reliability and performance reasons the die temperature should be limited to a maximum of 125 °C. That is, as an estimate, T_A (ambient temperature) plus device power dissipation times θ_{JA} should not exceed 125 °C.

The package of the device has an exposed pad that provides the primary heat removal path as well as excellent electrical grounding to the printed circuit board. To maximize the removal of heat from the package a thermal land pattern including multiple vias to a ground plane must be incorporated on the PCB within the footprint of the package. The exposed pad must be soldered down to ensure adequate heat conduction out of the package.

A recommended land and via pattern is shown in Figure 22. More information on soldering WQFN packages can be obtained at: http://www.ti.com/packaging.

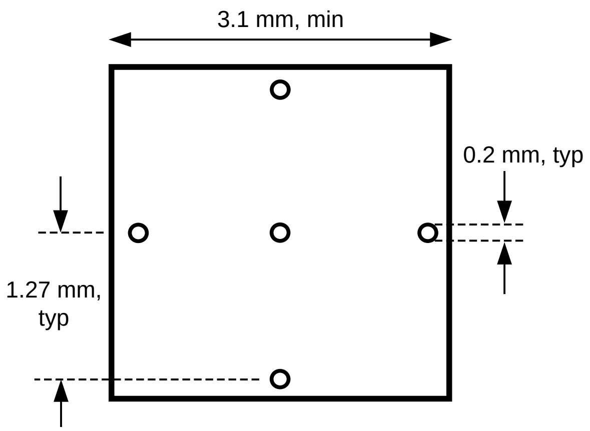


Figure 22. Recommended Land and Via Pattern

To minimize junction temperature it is recommended that a simple heat sink be built into the PCB (if the ground plane layer is not exposed). This is done by including a copper area of about 2 square inches on the opposite side of the PCB from the device. This copper area may be plated or solder coated to prevent corrosion but should not have conformal coating (if possible), which could provide thermal insulation. The vias shown in Figure 22 should connect these top and bottom copper layers and to the ground layer. These vias act as “heat pipes” to carry the thermal energy away from the device side of the board to where it can be more effectively dissipated.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMK00334RTVR	ACTIVE	WQFN	RTV	32	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	K00334	Samples
LMK00334RTVT	ACTIVE	WQFN	RTV	32	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	K00334	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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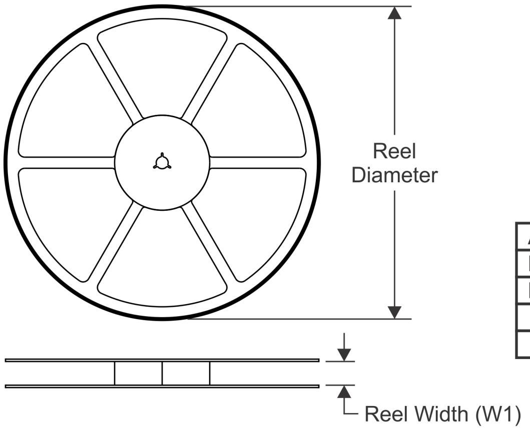
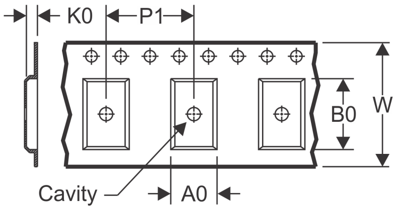
TAPE AND REEL INFORMATION

REEL DIMENSIONS

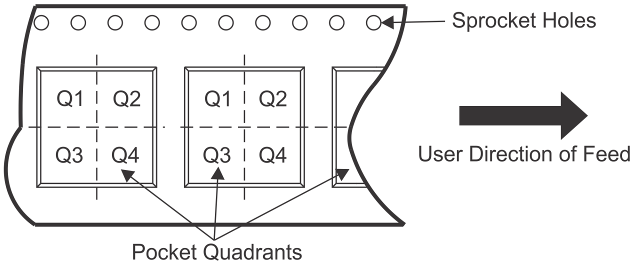


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

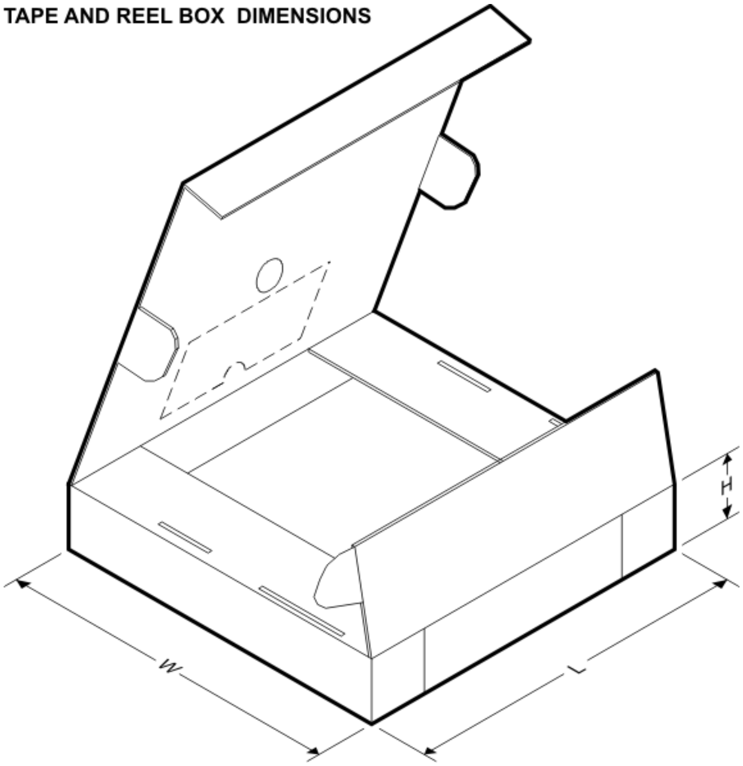
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMK00334RTVR	WQFN	RTV	32	1000	178.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1
LMK00334RTVT	WQFN	RTV	32	250	178.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1

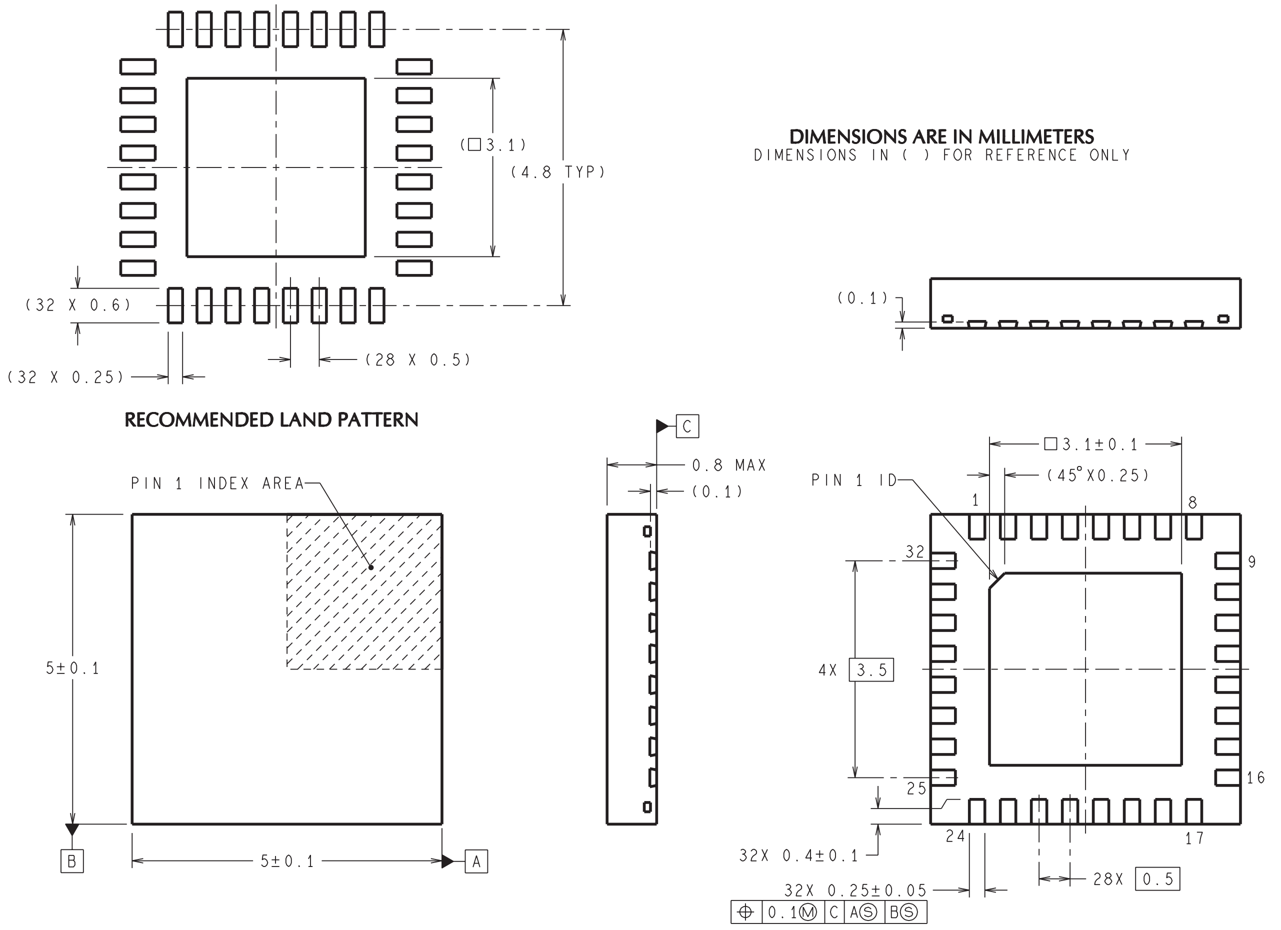
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMK00334RTVR	WQFN	RTV	32	1000	213.0	191.0	55.0
LMK00334RTVT	WQFN	RTV	32	250	213.0	191.0	55.0

RTV0032A



SQA32A (Rev B)

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

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