AT25M02

SPI Serial EEPROM
2-Mbit (262,144 x 8)

DATASHEET

Features

- Low-voltage and Standard-voltage Operation Available
  - 1.7V (V_{CC} = 1.7V to 5.5V)
  - 2.5V (V_{CC} = 2.5V to 5.5V)
- Serial Peripheral Interface (SPI) Compatible Interface
- Supports SPI Modes 0 (0,0) and 3 (1,1)
- High Speed Operation
  - 5MHz Clock Rate from 1.7V to 5.5V
- 256-byte Page Write Mode Support
  - Partial Page Writes Allowed
  - Byte Write Operation Supported
- Self-timed Write Cycle
  - All Write Operations Complete Within 10ms Max
- Block Write Protection
  - Ability to Protect the Upper Quarter, Upper Half, or the Entire Memory Array
- Multiple Write Protection Methods
  - Write Protect ($\overline{WP}$) Pin and Write Disable instructions for Both Hardware and Software Data Protection
- High Reliability
  - Endurance: 1,000,000 Write Cycles
  - Data Retention: 40 Years
- Green Package Options (Lead-free/Halide-free/RoHS Compliant)
  - 8-lead JEDEC SOIC and 8-ball Thin WLCSP
- Die Sale Options
  - Wafer form, Waffle Pack, and Bumped Die Available

Description

The Atmel® AT25M02 provides 2,097,152 bits of Serial Electrically Erasable Programmable Read-Only Memory (EEPROM) organized as 262,144 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation is essential. The device is available in space saving 8-lead JEDEC SOIC and 8-ball Thin WLCSP packages. In addition, the device operates from 1.7V to 5.5V.

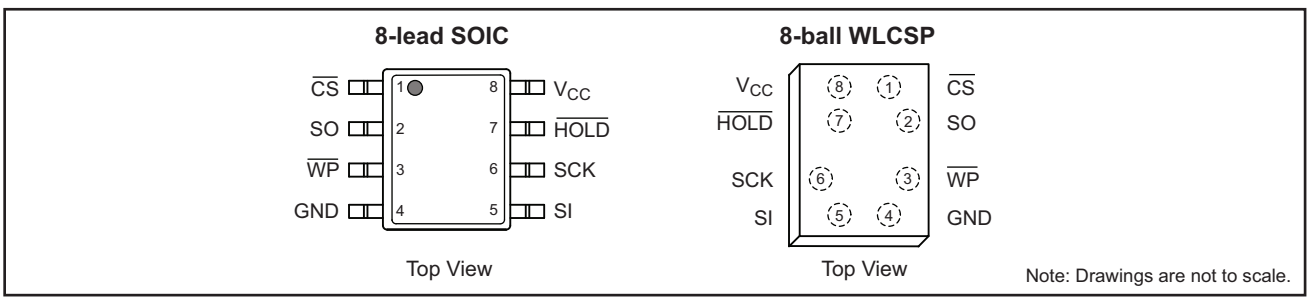
The AT25M02 is enabled through the Chip Select pin ($\overline{CS}$) and accessed via a 3-wire interface consisting of Serial Data Input (SI), Serial Data Output (SO), and Serial Clock (SCK). All programming cycles are completely self-timed and a separate erase cycle is not required before writing to the device.

Table of Contents

1. Pin Configurations and Pinouts

Table 1-1. Pin Description

Pin Number	Pin Symbol	Pin Name and Functional Description	Asserted State	Pin Type
1	CS	**Chip Select:** Asserting the $\overline{CS}$ pin selects the device. When the $\overline{CS}$ pin is deasserted, the device will be deselected and placed in standby mode and the SO pin will be in a high impedance state. When the device is deselected, data will not be accepted on the SI pin. A high-to-low transition on the $\overline{CS}$ pin is required to start an operation and a low-to-high transition is required to end an operation. When ending the internally self-timed write cycle, the device will not enter the standby mode until the completion of the operation.	Low	Input
2	SO	**Serial Data Output:** The SO pin is used to shift data out from the device. Data on the SO pin is always clocked out on the falling edge of SCK. The SO pin will be in a high impedance state whenever the device is deselected ($\overline{CS}$ is deasserted).	—	Output
3	$\overline{WP}$	**Write Protect:** The Write Protect ($\overline{WP}$) pin is used in conjunction with the block protection bits of the Status Register (see Table 4-3 on page 10) to inhibit writing to a portion of, or the entire memory array. The $\overline{WP}$ pin can also be used in conjunction with the WPEN bit to prevent inadvertent writing to the Status Register (see Table 4-4 on page 11). The protection is invoked by driving the $\overline{WP}$ pin to a low state.	Low	Input
4	GND	**Ground:** The ground reference for the device power supply (V_{CC}). GND should be connected to the system ground.	—	Power
5	SI	**Serial Data Input:** Instructions, addresses and data are latched by the AT25M02 on the rising edge of the Serial Clock (SCK) line via the Serial Data Input (SI) pin.	—	Input
6	SCK	**Serial Clock:** The Serial Clock (SCK) pin is used to provide a clock to the device and is used to synchronize the flow of data to and from the device. Instructions, addresses and data present on SI pin are always latched in on the rising edge of SCK, while output data on the SO pin is always clocked out on the falling edge of SCK.	—	Input
7	HOLD	**Hold:** When the device is selected and a serial sequence is underway, $\overline{Hold}$ can be used to pause the serial communication with the master device without resetting the serial sequence. To pause, the $\overline{HOLD}$ pin must be brought low while the SCK pin is low. To resume serial communication, the $\overline{HOLD}$ pin is brought high while the SCK pin is low (SCK may still toggle during $\overline{Hold}$). Inputs to the SI pin will be ignored and the SO pin will be in a high impedance state.	Low	Input
8	V_{CC}	**Device Power Supply:** The V_{CC} pin is used to supply the source voltage to the device. Operations at invalid V_{CC} voltages may produce spurious results and should not be attempted.	—	Power



2. Device Block Diagram and Bus Connections

Figure 2-1. Block Diagram

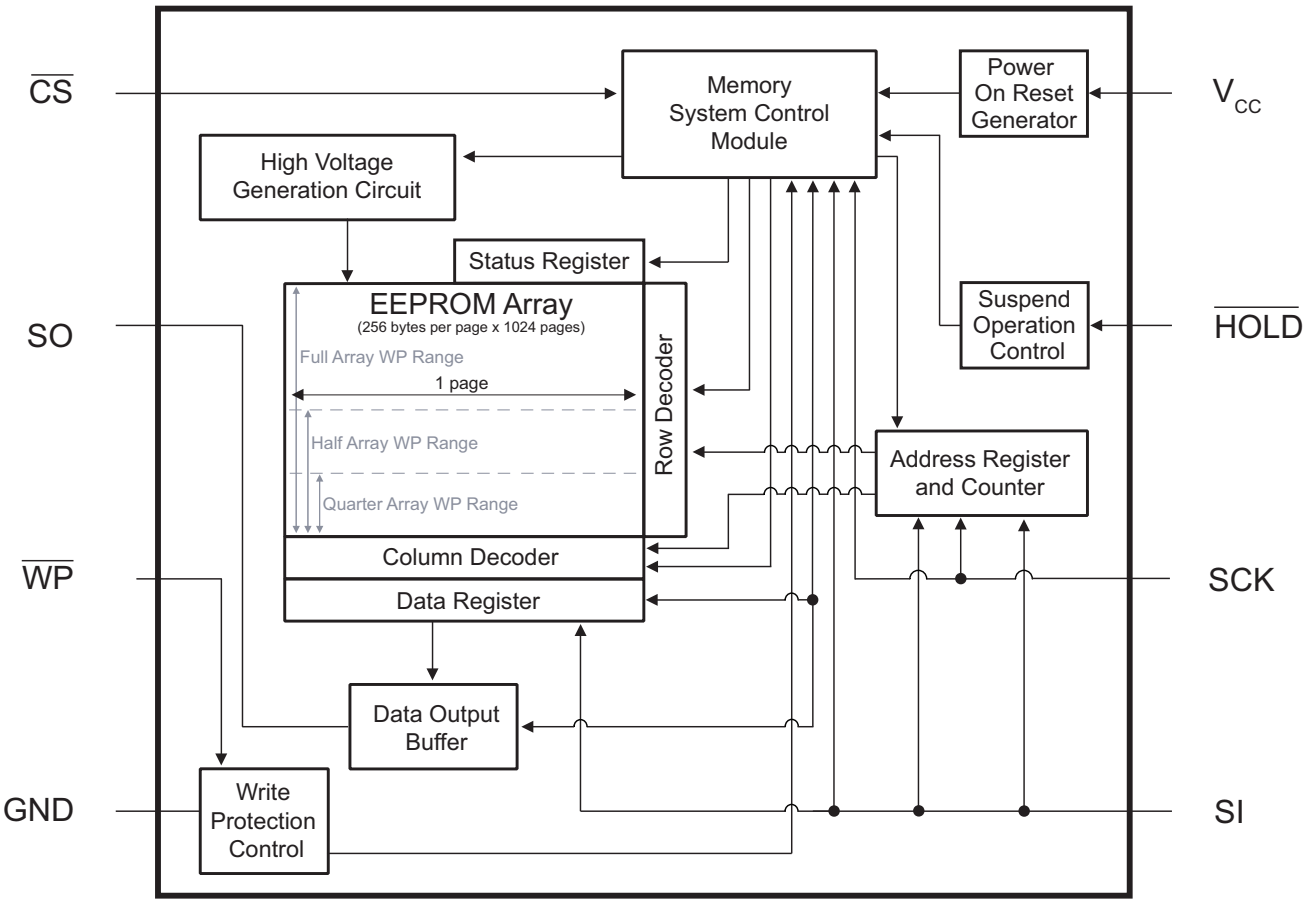
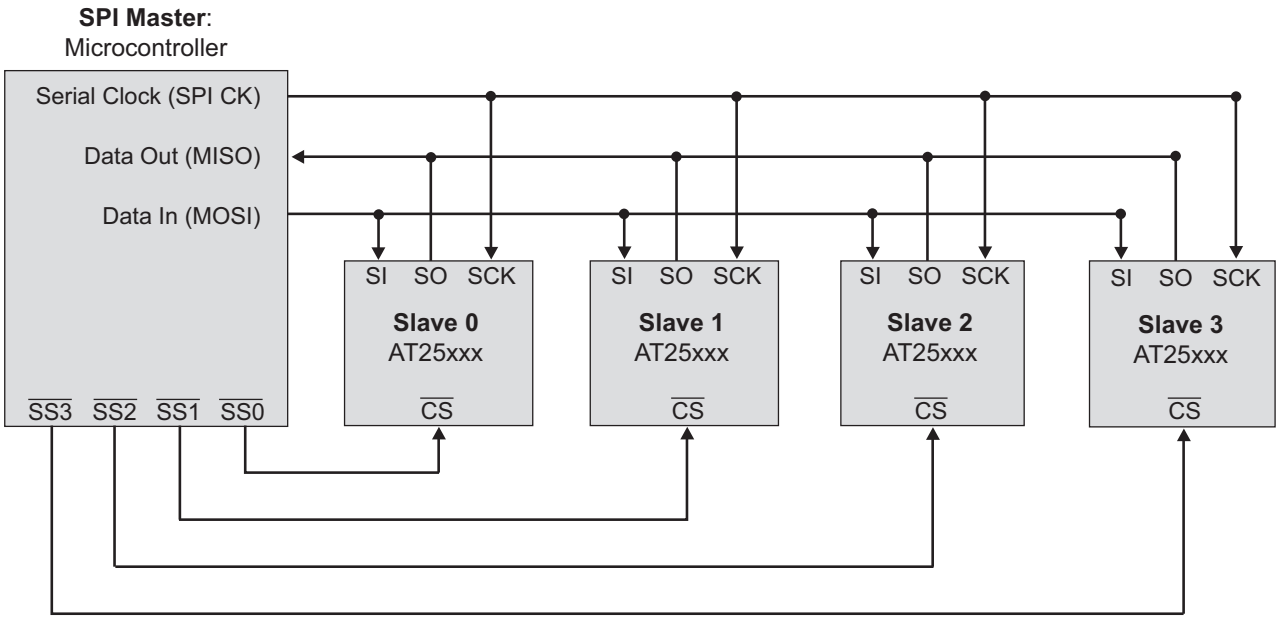


Figure 2-2. SPI Bus Master Connections to Serial EEPROMs

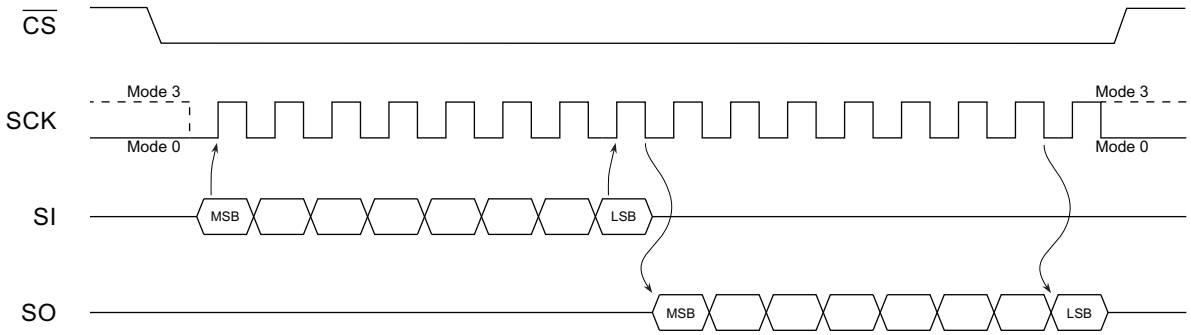


3. Device Operation

The AT25M02 is controlled by a set of instructions that are sent from a host controller, commonly referred to as the SPI Master. The SPI Master communicates with the AT25M02 via the SPI bus which is comprised of four signal lines: Chip Select ($\overline{CS}$), Serial Clock (SCK), Serial Input (SI), and Serial Output (SO).

The SPI protocol defines a total of four modes of operation (mode 0, 1, 2, or 3) with each mode differing in respect to the SCK polarity and phase and how the polarity and phase control the flow of data on the SPI bus. The AT25M02 supports the two most common modes, SPI Modes 0 and 3. With SPI Modes 0 and 3, data is always latched in on the rising edge of SCK and always output on the falling edge of SCK. The only difference between SPI Modes 0 and 3 is the polarity of the SCK signal when in the inactive state (when the SPI Master is in standby mode and not transferring any data). SPI Mode 0 is defined as a low SCK while $\overline{CS}$ is not asserted (at V_{CC}) and SPI Mode 3 has SCK high in the inactive state. The SCK idle state must match when the $\overline{CS}$ is deasserted both before and after the communication sequence in SPI Mode 0 and 3. The figures in this document depict Mode 0 with a solid line on SCK while $\overline{CS}$ is inactive and Mode 3 with a dotted line.

Figure 3-1. SPI Mode 0 and Mode 3



3.1 Interfacing the AT25M02 on the SPI Bus

Communication to and from the AT25M02 must be initiated by the SPI Master device, such as a microcontroller. The SPI Master device must generate the serial clock for the AT25M02 on the SCK pin. The AT25M02 always operates as a slave due to the fact that the Serial Clock pin (SCK) is always an input.

Selecting the Device: The AT25M02 is selected when the $\overline{CS}$ pin is low. When the device is not selected, data will not be accepted via the SI pin, and the SO pin will remain in a high impedance state.

Sending Data to the Device: The AT25M02 uses the Serial Data Input (SI) pin to receive information. All instructions, addresses and data input bytes are clocked into the device with the Most Significant Bit (MSB) first. The SI pin samples on the first rising edge of the SCK line after the $\overline{CS}$ has been asserted.

Receiving Data from the Device: Data output from the device is transmitted on the Serial Data Output (SO) pin, with the MSB output first. The SO data is latched on the first falling edge of SCK after the instruction has been clocked into the device, such as the Read from Memory Array and Read Status Register instructions. See Section 5. “Read Array Operation” on page 12 for more details.

3.2 Device Opcodes

Serial Opcode: After the device is selected by driving $\overline{CS}$ low, the first byte will be received on the SI pin. This byte contains the opcode that defines the operation to be performed. Please refer to Table 4-1 on page 7 for a list of all opcodes that the AT25M02 will respond to.

Invalid Opcode: If an invalid opcode is received, no data will be shifted into AT25M02 and the Serial Data Output (SO) pin will remain in a high impedance state until the falling edge of $\overline{CS}$ is detected again. This will reinitialize the serial communication.

3.3 Hold Function

The HOLD pin is used to pause the serial communication with the device without having to stop or reset the clock sequence. The Hold mode, however, does not have an effect on the internal write cycle. Therefore, if a write cycle is in progress, asserting the HOLD pin will not pause the operation and the write cycle will continue to completion.

The Hold mode can only be entered while the CS pin is asserted. The Hold mode is activated by asserting the HOLD pin during the SCK low pulse. If the HOLD pin is asserted during the SCK high pulse, then the Hold mode will not be started until the beginning of the next SCK low pulse. The device will remain in the Hold mode as long as the HOLD pin and CS pin are asserted.

While in Hold mode, the SO pin will be in a high impedance state. In addition, both the SI pin and the SCK pin will be ignored. The WP pin, however, can still be asserted or deasserted while in the Hold mode.

To end the Hold mode and resume serial communication, the HOLD pin must be deasserted during the SCK low pulse. If the HOLD pin is deasserted during the SCK high pulse, then the Hold mode will not end until the beginning of the next SCK low pulse.

If the CS pin is deasserted while the HOLD pin is still asserted, then any operation that may have been started will be aborted and the device will reset the WEL bit in the Status Register back to the Logic 0 state.

Figure 3-2. Hold Mode

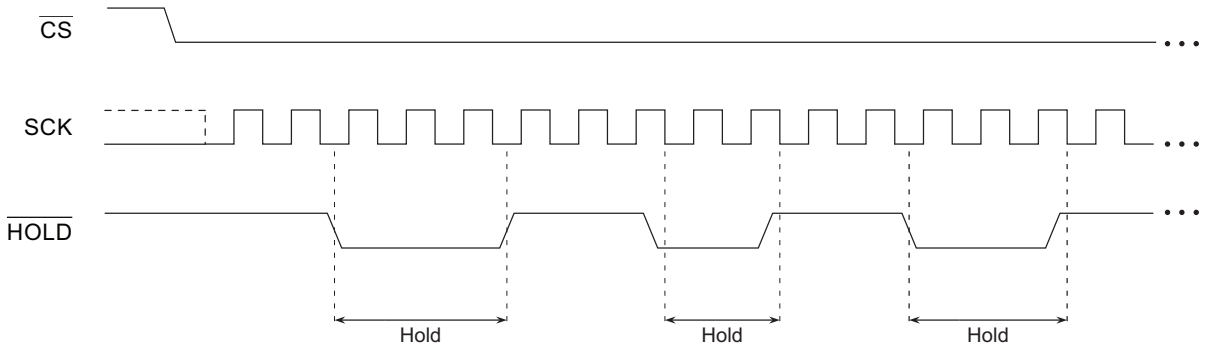
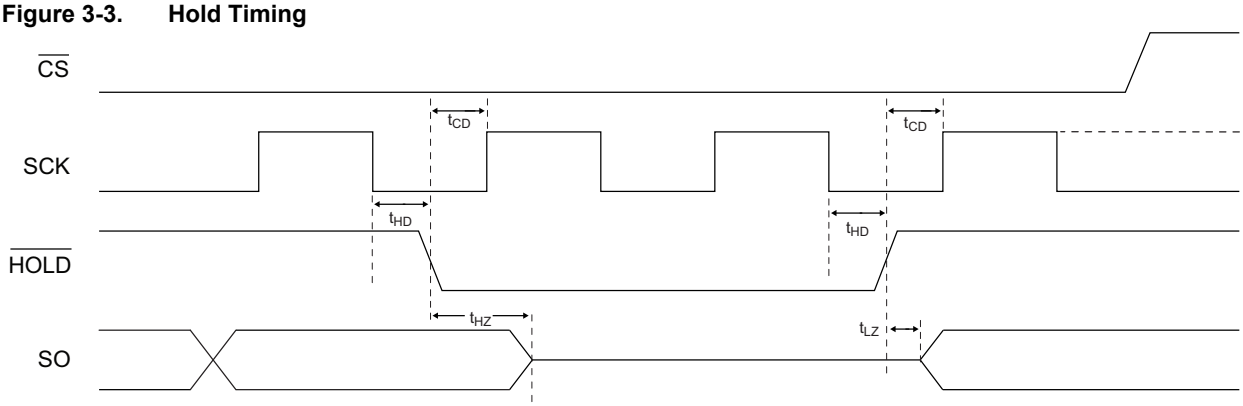


Figure 3-3. Hold Timing



3.4 Write Protection

The Write Protect (WP) pin will allow normal read/write operations when held high. When the WP pin is brought low and WPEN bit is a Logic 1, all write operations to the Status Register are inhibited. The WP pin going low while CS is still low will interrupt a Write to the Status Register. If the internal write cycle has already been initiated, WP going low will have no effect on any write operation to the Status Register. The WP pin function is blocked when the WPEN bit in the Status Register is a Logic 0. This will allow the user to install the AT25M02 device in a system with the WP pin tied to ground and still be able to write to the Status Register. All WP pin functions are enabled when the WPEN bit is set to a Logic 1.

4. Device Commands and Addressing

The AT25M02 is designed to interface directly with the synchronous Serial Peripheral Interface (SPI) of the 6800 type series of microcontrollers.

The AT25M02 utilizes an 8-bit instruction register. The list of instructions and their operation codes are contained in Table 4-1. All instructions, addresses, and data are transferred with the MSB first and start with a high-to-low $\overline{CS}$ transition.

Table 4-1. Instruction Set For the Atmel AT25M02

Instruction Name	Instruction Format	Operation Description	Operates On	Refer to Section
RDSR	0000 0101 (05h)	Read Status Register (SR)	Status Register	Section 4.2.1
LPWP	0000 1000 (08h)	Low Power Write Poll	Status Register	Section 4.2.2
WREN	0000 0110 (06h)	Set Write Enable Latch (WEL)	Status Register	Section 4.3.1
WRDI	0000 0100 (04h)	Reset Write Enable Latch (WEL)	Status Register	Section 4.3.2
WRSR	0000 0001 (01h)	Write Status Register (SR)	Status Register	Section 4.4
READ	0000 0011 (03h)	Read from Memory Array	Memory Array	Section 5.
WRITE	0000 0010 (02h)	Write to Memory Array	Memory Array	Section 6.
	0000 0111 (07h)			

4.1 Status Register Bit Definition and Function

The AT25M02 includes an 8-bit Status Register. The Status Register bits modulate various features of the device as shown in Table 4-2. These bits can be changed by specific instructions that are detailed in the following sections.

Table 4-2. Status Register Bit Definition

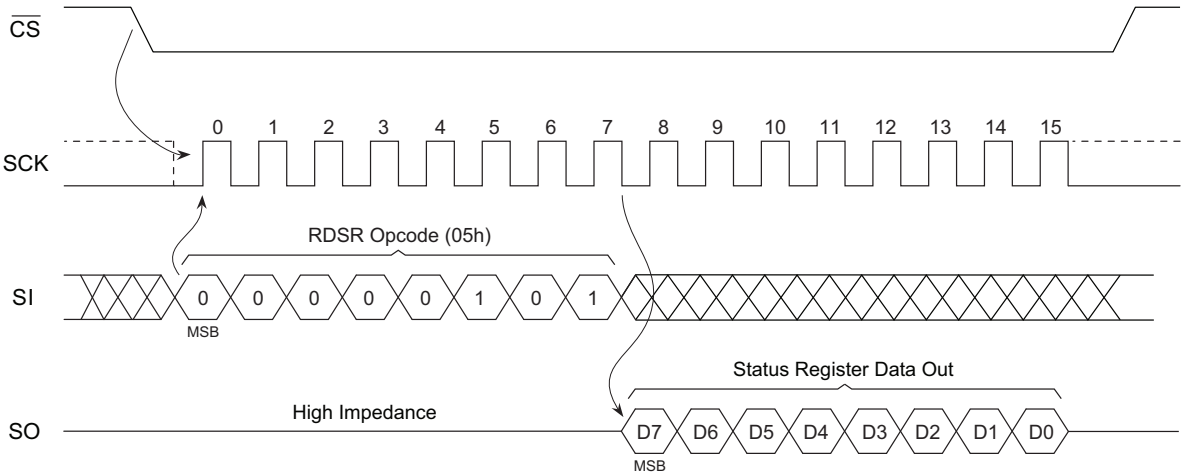
Bit	Name		Type	Description	
7	WPEN	Write Protect Enable	R/W	0	See Table 4-4 (Factory Default).
				1	See Table 4-4.
6:4	RFU	Reserved for Future Use	R	0	Reads as zeros when the device is not in a write cycle.
				1	Reads as ones when the device is in a write cycle.
3:2	BP1 BP0	Block Write Protection	R/W	00	No array write protection (Factory Default)
				01	Quarter memory array protection (see Table 4-3).
				10	Half memory array protection (see Table 4-3).
				11	Entire memory array protection (see Table 4-3).
1	WEL	Write Enable Latch	R/W	0	Device is not write enabled (Power-up Default).
				1	Device is write enabled.
0	$\overline{RDY}$/BSY	Ready/Busy Status	R	0	Device is ready for a new sequence.
				1	Device is busy with an internal operation.

4.2 Read Status Register (RDSR) and Low Power Write Poll (LPWP)

4.2.1 Read Status Register (RDSR)

The Read Status Register instruction provides access to the Status Register. The ready/busy and write enable status of the device can be determined by the RDSR instruction. Similarly, the Block Write Protection bits indicate the extent of memory array protection employed. The Status Register is read by asserting the $\overline{CS}$ pin, followed by sending in a 05h opcode on the SI pin. Upon completion of the opcode, the device will return the 8-bit Status Register value on the SO pin.

Figure 4-1. RDSR Waveform

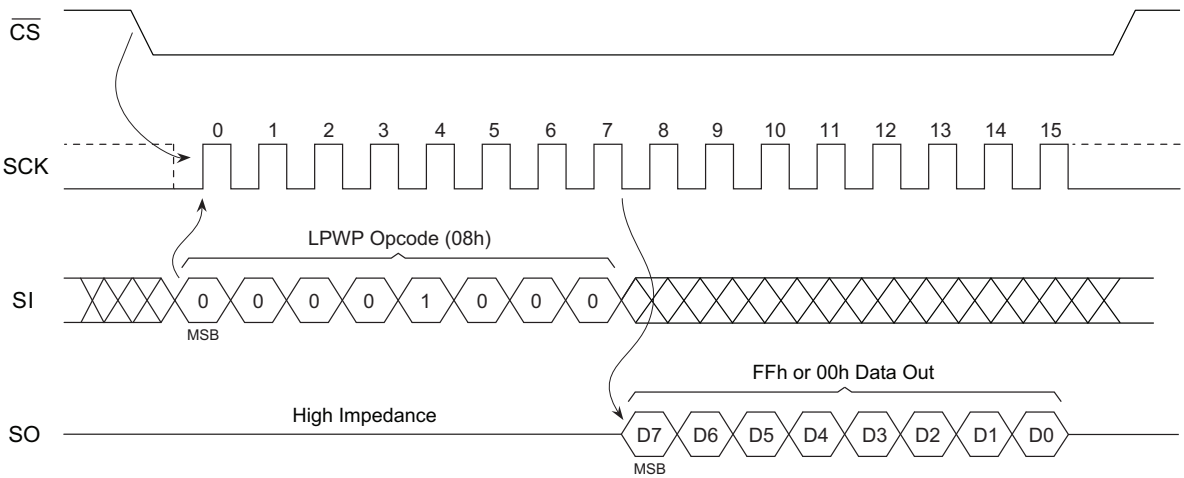


The Status Register can be continuously read for data by continuing to read beyond the first 8-bit value returned. The AT25M02 will update the Status Register value upon the completion of every 8 bits, thereby allowing new Status Register values to be read without having to issue a new RDSR instruction.

4.2.2 Low Power Write Poll (LPWP)

The Low Power Write Poll command can be used after any write command as a means to check if the device has completed its internal write cycle. The LPWP command requires an opcode of 08h and will return an FFh value when the part is still busy completing the write cycle. The LPWP command will return a 00h value if the part is no longer in a write cycle. Refer to section Section 6.2.1 on page 14 for a description on implementing a polling routine. Continuous reading of the LPWP state is supported and the value output by the device will be updated every eight bits.

Figure 4-2. LPWP Timing



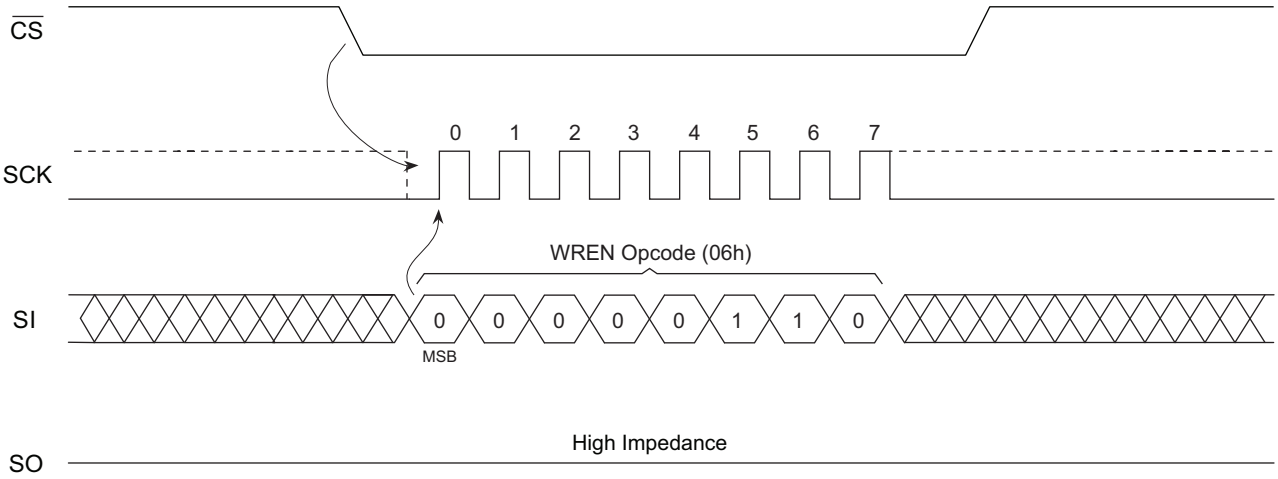
4.3 Write Enable (WREN) and Write Disable (WRDI)

Enabling and disabling writing to the Status Register and EEPROM array is accomplished through the Write Enable Instruction (WREN) and the Write Disable Instruction (WRDI). These functions change the status of the WEL bit in the Status Register.

4.3.1 Write Enable Instruction (WREN)

The Write Enable Latch (WEL) bit of the Status Register must be set to a Logic 1 prior to each WRSR and WRITE instruction. This is accomplished by sending a WREN (06h) command to the AT25M02. First, the $\overline{CS}$ pin is driven low to select the device and then a 06h instruction value is clocked in on the SI pin. Then the $\overline{CS}$ pin can be driven high and the WEL bit will be updated in the Status Register to a Logic 1. The device will power-up in the write disable state (WEL = 0).

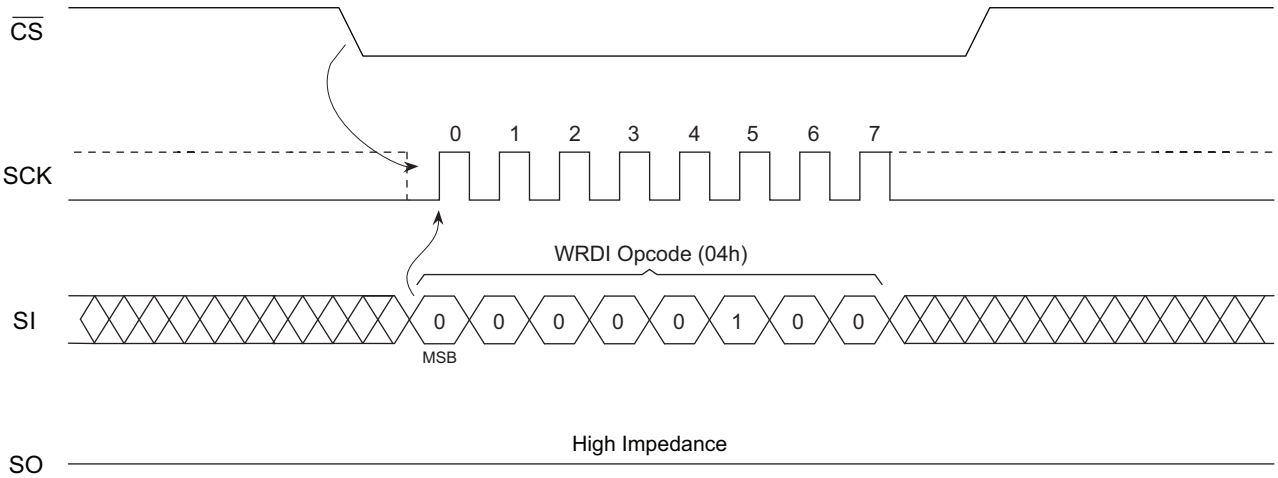
Figure 4-3. WREN Timing



4.3.2 Write Disable Instruction (WRDI)

To protect the device against inadvertent writes, the Write Disable instruction (opcode 04h) disables all programming modes by setting the WEL bit to a Logic 0. The WRDI instruction is independent of the status of the $\overline{WP}$ pin.

Figure 4-4. WRDI Timing



4.4 Write Status Register (WRSR)

The Write Status Register (WRSR) instruction enables the SPI Master to change selected bits of the Status Register. Before a WRSR sequence can be initiated, a WREN instruction must be executed to set the WEL to Logic 1. Upon completion of a WREN sequence, a WRSR sequence can be executed.

Note: The WRSR function has no effect on bit 6, bit 5, bit 4, bit 1 and bit 0 of the Status Register. Only bit 7, bit 3 and bit 2 can be changed via the WRSR sequence. These modifiable bits are the Write Protect Enable (WPEN) bit and Block Protect (BP1, BP0) bits. These three bits are non-volatile cells that have the same properties and functions as regular EEPROM cells. Their values are retained while power is removed from the device.

The AT25M02 will not respond to commands other than a RDSR after a WRSR sequence until the self-timed internal write cycle has completed. When the write cycle is completed, the WEL bit in the Status Register is reset to Logic 0.

4.4.1 Block Write Protect Function

The WRSR instruction allows the user to select one of four possible combinations as to how the memory array will be inhibited from writing through changing the Block Write Protect bits (BP1, BP0). The four levels of array protection are:

- None of the memory array is protected.
- Upper quarter (¼) address range is write protected meaning the highest order 512-Kbits are read-only.
- Upper half (½) address range is write protected meaning the highest order 1-Mbits are read-only.
- All of the memory array is write protected meaning all addresses are read-only.

The Block Write Protection levels and corresponding Status Register control bits are shown in Table 4-3.

Table 4-3. Block Write Protect Bits

Level	Status Register Bits <3:2>		Writeable Address Range	Write Protected / Read-Only Address Range
	BP1	BP0		
0	0	0	00000h – 3FFFFh	None
1 (¼)	0	1	00000h – 2FFFFh	30000h – 3FFFFh
2 (½)	1	0	00000h – 1FFFFh	20000h – 3FFFFh
3 (All)	1	1	None	00000h – 3FFFFh

4.4.2 Write Protect Enable Function

The WRSR instruction also allows the user to enable or disable the Write Protect ($\overline{WP}$) pin through the use of the Write Protect Enable (WPEN) bit. When the WPEN bit is set to Logic 0, the writability of the EEPROM array is dictated by the values of the Block Write Protect bits. The writability of the Status Register is controlled by the WEL bit. When the WPEN bit is set to Logic 1, the Status Register is read-only.

Hardware Write Protection is enabled when *both* the $\overline{WP}$ pin is at GND and the WPEN bit has been set to one. When the device is Hardware Write Protected, all writing to the Status Register, including the Block Write Protection bits, the WEL and the WPEN bit, and to the sections in the memory array selected by the Block Write Protection bits are disabled. When Hardware Write Protection is enabled, writes are only allowed to sections of the memory that are not block protected.

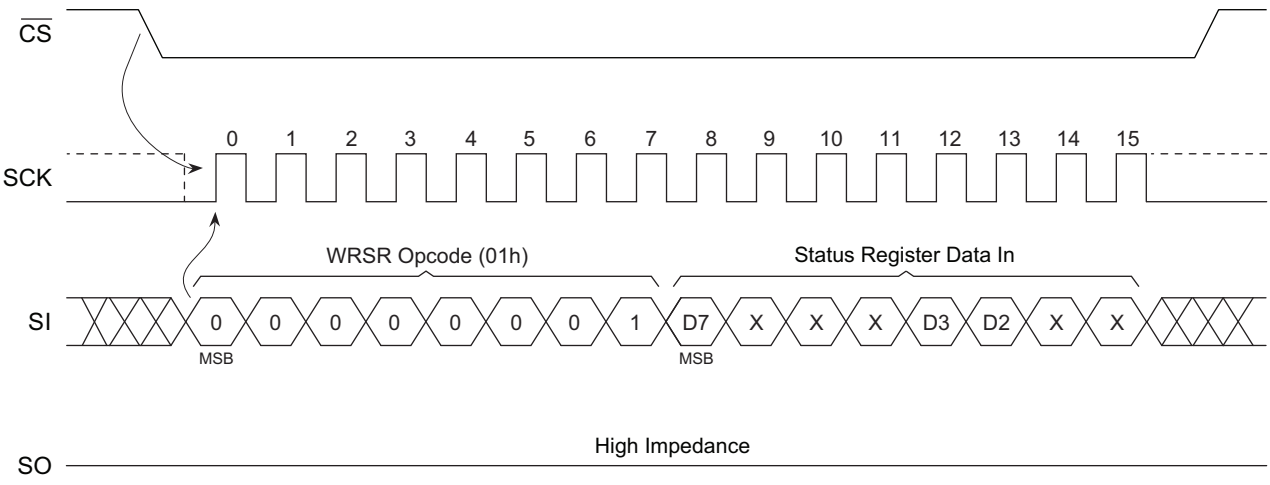
Hardware Write Protection is disabled when *either* the $\overline{WP}$ pin is at V_{CC} or the WPEN bit is zero. When Hardware Write Protection is disabled, writes are only allowed to sections of the memory that are not block protected.

Note: When the WPEN bit is hardware write protected, it cannot be changed back to zero, as long as the $\overline{WP}$ pin is held at GND.

Table 4-4. WPEN Operation

WPEN	$\overline{WP}$ Pin	WEL	Protected Blocks	Unprotected Blocks	Status Register
0	X	0	Protected	Protected	Protected
0	X	1	Protected	Writable	Writable
1	GND	0	Protected	Protected	Protected
1	GND	1	Protected	Writable	Protected
X	V_{CC}	0	Protected	Protected	Protected
X	V_{CC}	1	Protected	Writable	Writable

Figure 4-5. WRSR Waveform



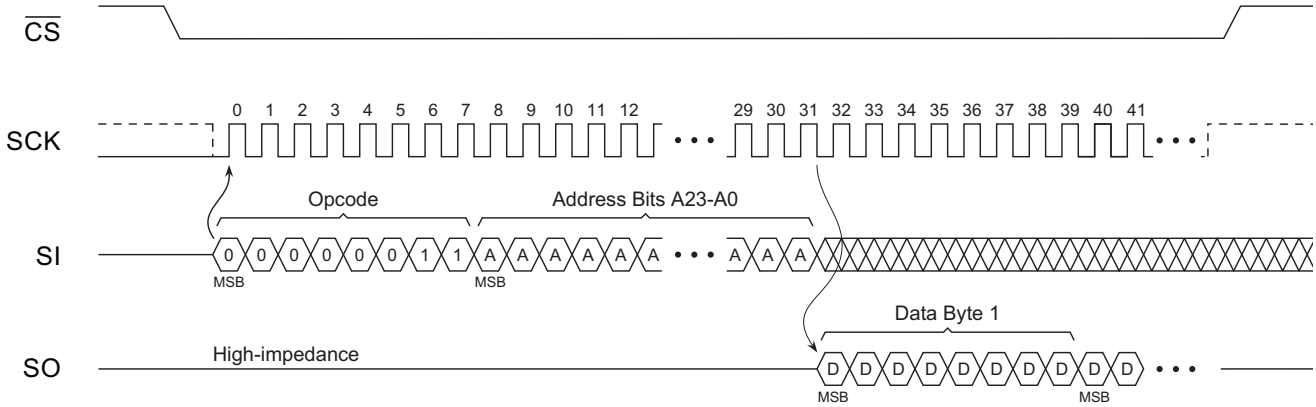
5. Read Array Operation

Reading the AT25M02 via the SO pin requires the following sequence. After the $\overline{CS}$ line is pulled low to select a device, the Read opcode 03h is transmitted via the SI line followed by the 24-bit address to be read.

Note: Address bits A23 through A18 are don't care bits as they do not fall within the 2-Mbit addressable range.

Upon completion of the 24-bit address, any data on the SI line will be ignored. The data (D7 – D0) at the specified address is then shifted out onto the SO line. If only one byte is to be read, the $\overline{CS}$ line should be driven high after the data comes out. The Read sequence can be continued since the byte address is automatically incremented and data will continue to be shifted out. When the highest address is reached (3FFFFh), the address counter will roll over to the lowest address (00000h) allowing the entire memory to be read in one continuous read cycle regardless of the starting address.

Figure 5-1. Read Array



6. Write Commands

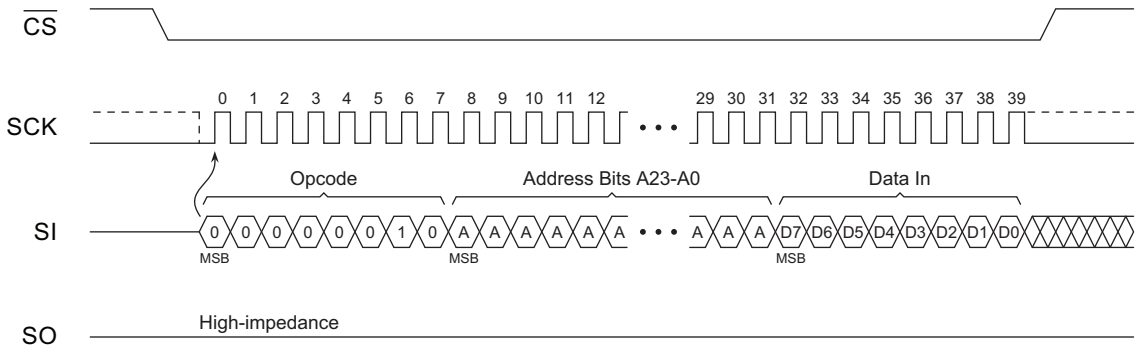
In order to program the AT25M02, two separate instructions must be executed. First, the device *must be write enabled* via the Write Enable instruction (WREN). Then, one of the two possible Write instructions described in Section 6.1 may be executed. The address of the memory location(s) to be programmed must be outside the protected address field location selected by the block write protection level. During an internal write cycle, all commands will be ignored except the RDSR instruction.

Note: If the device is not Write Enabled (WREN), the device will ignore the Write instruction and will return to the standby state when $\overline{CS}$ is brought high. A new $\overline{CS}$ assertion is required to re-initiate communication.

6.1 Byte Write

A Byte Write instruction requires the following sequence and is depicted in Figure 6-1. After the $\overline{CS}$ line is pulled low to select the device, the Write opcode (02h) is transmitted via the SI line followed by the 24-bit address and the data (D7 – D0) to be programmed. Programming will start after the $\overline{CS}$ pin is brought high. The low-to-high transition of the $\overline{CS}$ pin must occur during the SCK low time (Mode 0) and SCK high time (Mode 3) immediately after clocking in the D0 (LSB) data bit. The AT25M02 is automatically returned to the Write Disable state (Status Register bit WEL = 0) at the completion of a write cycle.

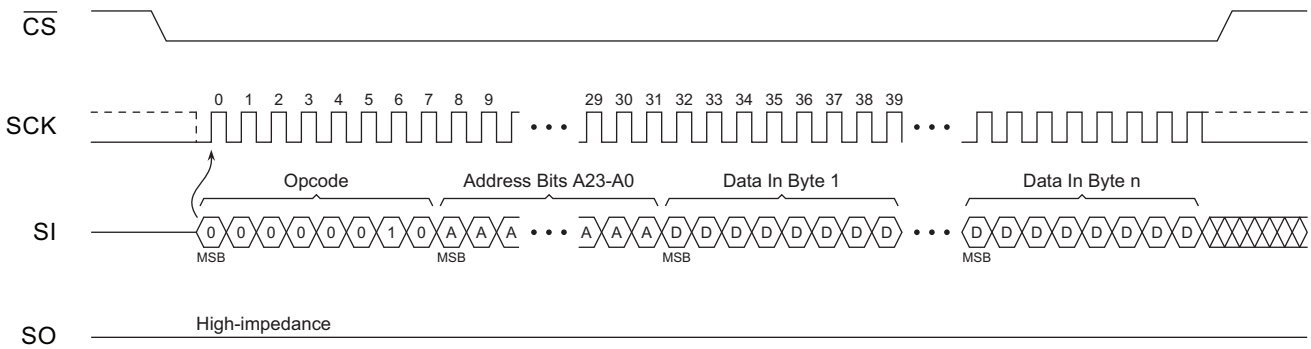
Figure 6-1. Byte Write



6.2 Page Write

A Page Write sequence allows up to 256 bytes to be written in the same write cycle, provided that all bytes are in the same row of the memory array (where addresses A17 through A8 are the same). Partial Page Writes of less than 256 bytes are allowed. After each byte of data is received, the eight lowest order address bits are internally incremented by one and the remaining address bits will remain constant. If more bytes of data are transmitted that what will fit to the end of that memory row, the address counter will “roll over” to the beginning of the same row. Due to the Internal Writing Methodology utilized in the device (see Section 6.2.1), creating a roll over event should be avoided as data in the page could become unintentionally altered during the write cycle. The AT25M02 is automatically returned to the Write Disable state (WEL = 0) at the completion of a write cycle.

Figure 6-2. Page Write



6.2.1 Internal Writing Methodology

The AT25M02 incorporates a built in error detection and correction (EDC) logic scheme. The EEPROM array is internally organized as a group of four connected 8-bit bytes plus an additional six ECC (Error Correction Code) bits of EEPROM. These 38 bits are referred to as the internal physical data word. During a read sequence, the EDC logic compares each 4-byte physical data word with its corresponding six ECC bits. If a single bit out of the 4-byte region happens to read incorrectly, the EDC logic will detect the bad bit and replace it with a correct value before the data is serially clocked out. This architecture significantly improves the reliability of the AT25M02 compared to an implementation that does not utilize EDC.

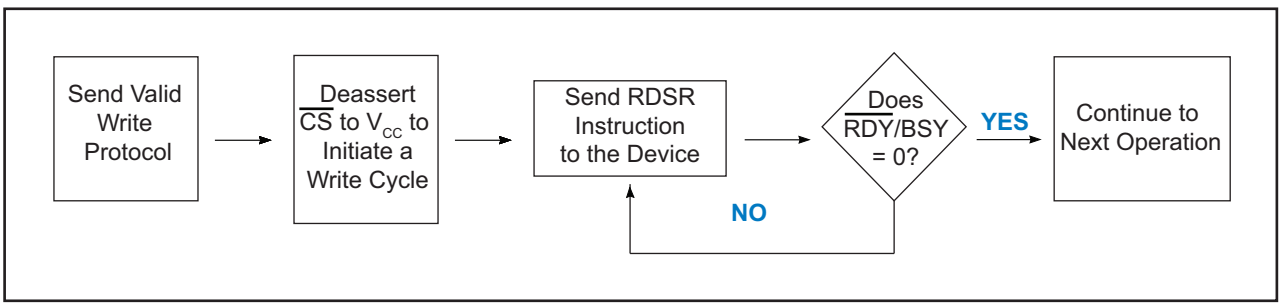
It is important to note that data is always physically written to the part at the internal physical data word level, regardless of the number of bytes written. Writing single bytes is still possible with the Byte Write operation, but internally, the other three bytes within the 4-byte location where the single byte was written, along with the six ECC bits will be updated. Due to this architecture, the AT25M02 EEPROM write endurance is rated at the internal physical data word level (4-byte word). The system designer needs to optimize the application writing algorithms to observe these internal word boundaries in order to reach the 1,000,000 cycle endurance rating.

6.2.2 Polling Routine

An polling routine can be implemented to optimize time sensitive applications that would not prefer to wait the fixed maximum write cycle time (t_{WC}). This method allows the application to know immediately when the Serial EEPROM write cycle has completed to start a subsequent operation.

Once the internally timed write cycle has started, a polling routine can be initiated. This involves repeatedly sending Read Status Register (RDSR) command to determine if the device has completed its self timed internal write cycle. If the $\overline{RDY}$/BSY bit (Bit 0) = 1, the write cycle is still in progress. If Bit 0 = 0, the write cycle has ended. If the $\overline{RDY}$/BSY bit = 1, repeated RDSR commands can be executed until the $\overline{RDY}$/BSY bit = 0, signaling that the device is ready to execute a new instruction. Only the Read Status Register instruction is enabled during the write programming cycle.

Figure 6-3. Polling Flow Chart



7. Electrical Specifications

7.1 Absolute Maximum Ratings*

Temperature under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Supply Voltage with respect to ground	-0.5V to +6.25V
Voltage on any pin with respect to ground	-1.0V to +7.0V
DC Output Current	5.0mA

Functional operation at the “Absolute Maximum Ratings” or any other conditions beyond those indicated in Section 7-1 is not implied or guaranteed. Stresses beyond those listed under “Absolute Maximum Ratings” and/or exposure to the “Absolute Maximum Ratings” for extended periods may affect device reliability and cause permanent damage to the device.

The voltage extremes referenced in the “Absolute Maximum Ratings” are intended to accommodate short duration undershoot/overshoot pulses that the device may be subjected to during the course of normal operation and does not imply or guarantee functional device operation at these levels for any extended period of time.

7.2 DC and AC Operating Range

Table 7-1. DC and AC Operating Range

		AT25M02
Operating Temperature (Case)	Industrial High Temperature	-40°C to +85°C
V_{CC} Power Supply	Low Voltage Grade	1.7V to 5.5V
	Standard Voltage Grade	2.5V to 5.5V

7.3 DC Characteristics

Table 7-2. DC Characteristics

Parameter are applicable over operating range in Section 7-1, unless otherwise noted.

Symbol	Parameter	Test Condition		Min	Typical[1]	Max	Units
V_{CC1}	Supply Voltage			1.7		5.5	V
V_{CC2}	Supply Voltage			2.5		5.5	V
I_{CC1}	Supply Current (Read)	V_{CC} = 1.8V[2], SCK = 1MHz, SO = Open			0.3	1.0	mA
		V_{CC} = 1.8V[2], SCK = 5MHz, SO = Open			0.5	1.0	mA
		V_{CC} = 5.0V, SCK = 1MHz, SO = Open			1.0	2.0	mA
		V_{CC} = 5.0V, SCK = 5MHz, SO = Open			2.0	3.0	mA
I_{CC2}	Supply Current (Write)	V_{CC} = 1.8V[2], SO = Open During t_{WC}, $\overline{CS}$ = V_{CC}			0.3	2.0	mA
		V_{CC} = 5.0V, SO = Open During t_{WC}, $\overline{CS}$ = V_{CC}			0.5	3.0	mA
I_{SB}	Standby Current	V_{CC} = 1.8V[2], $\overline{CS}$ = V_{CC}			0.08	1.0	µA
		V_{CC} = 2.5V, $\overline{CS}$ = V_{CC}			0.08	2.0	µA
		V_{CC} = 5.5V, $\overline{CS}$ = V_{CC}			0.15	3.0	µA
I_{IL}	Input Leakage	V_{IN} = 0V to V_{CC}		–3.0		3.0	µA
I_{OL}	Output Leakage	V_{IN} = 0V to V_{CC}, T_{AC} = 0°C to 70°C		–3.0		3.0	µA
V_{IL}[2]	Input Low-voltage			–1.0		V_{CC} x 0.3	V
V_{IH}[2]	Input High-voltage			V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL1}	Output Low-voltage	3.6 ≤ V_{CC} ≤ 5.5V	I_{OL} = 3.0mA			0.4	V
V_{OH1}	Output High-voltage		I_{OH} = –1.6mA	V_{CC} –0.8			V
V_{OL2}	Output Low-voltage	1.8V ≤ V_{CC} ≤ 3.6V	I_{OL} = 0.15mA			0.2	V
V_{OH2}	Output High-voltage		I_{OH} = –100µA	V_{CC} –0.2			V

Notes: 1. Typical values characterized at T_A = +25°C unless otherwise noted.
2. This parameter is characterized but is not 100% tested in production.

7.4 AC Characteristics

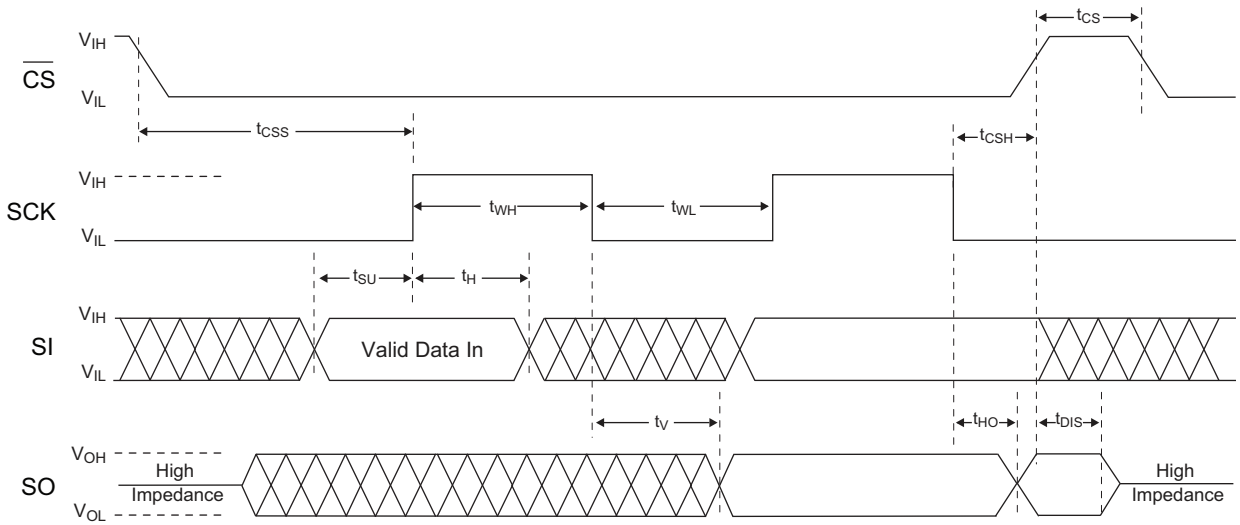
Table 7-3. AC Characteristics

Applicable over recommended operating range: T_{AI}= -40°C to +85°C, CL=1 TTL Gate and 30pF (unless otherwise noted).

Symbol	Parameter	V_{CC} = 1.7V to 5.5V		Units
		Min	Max	
f_{SCK}	SCK Clock Frequency	0	5	MHz
t_{RI} (1)	Input Rise Time	—	80	ns
t_{FI} (1)	Input Fall Time	—	80	ns
t_{WH}	SCK High Time	80	—	ns
t_{WL}	SCK Low Time	80	—	ns
t_{CS}	$\overline{CS}$ High Time	200	—	ns
t_{CSS}	$\overline{CS}$ Setup Time	200	—	ns
t_{CSH}	$\overline{CS}$ Hold Time	200	—	ns
t_{SU}	Data In Setup Time	20	—	ns
t_H	Data In Hold Time	20	—	ns
t_{HD}	$\overline{Hold}$ Setup Time	20	—	ns
t_{CD}	$\overline{Hold}$ Hold Time	20	—	ns
t_V	Output Valid	0	80	ns
t_{HO}	Output Hold Time	0	—	ns
t_{LZ}	$\overline{Hold}$ to Output Valid	—	100	ns
t_{HZ}	$\overline{Hold}$ to Output High Z	—	100	ns
t_{DIS}	Output Disable Time	—	100	ns
t_{WC}	Write Cycle Time	—	10	ms

Note: 1. This parameter is ensured by characterization only.

Figure 7-1. Synchronous Data Timing



7.5 Pin Capacitance

Table 7-4. Pin Capacitance[1]

Applicable over recommended operating range from T_A = 25°C, f = 1.0MHz, V_{CC} = 5.0V (unless otherwise noted).

Symbol	Test Conditions	Max	Units	Conditions
C_{OUT}	Output Capacitance (SO)	8	pF	V_{OUT} = 0V
C_{IN}	Input Capacitance ($\overline{CS}$, SCK, SI, $\overline{WP}$, $\overline{HOLD}$)	6	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

7.6 EEPROM Cell Performance Characteristics

Table 7-5. EEPROM Cell Performance Characteristics

Operation	Test Condition	Min	Max	Units
Write Endurance[1]	T_A = 25°C, V_{CC}(min)< V_{CC} < V_{CC}(max) Byte[2] or Page Write Mode	1,000,000	—	Write Cycles
Data Retention[3]	T_A = 55°C, V_{CC}(min)< V_{CC} < V_{CC}(max)	100	—	Years

Notes:
1. Write endurance performance is determined through characterization and the qualification process.
2. Due to the memory array architecture, the Write Cycle Endurance is specified for writes in groups of four data bytes. The beginning of any 4-byte boundaries can be determined by multiplying any integer (N) by four (i.e 4*N). The end address can be found by adding three to the beginning value (i.e. 4*N+3). See Section 6.2.1 “Internal Writing Methodology” on page 14 for more details on this implementation.
3. The data retention capability is determined through qualification and is checked on each device in production.

7.7 Power-Up Requirements, Reset, and Default Conditions

During a power-up sequence, the V_{CC} supplied to the AT25M02 should monotonically rise from GND to the minimum V_{CC} level as specified in Section 7-1 on page 15, with a slew rate no greater than of 1V/µs.

7.7.1 Device Reset

To prevent inadvertent write operations or other spurious events from happening during a power-up sequence, the AT25M02 includes a power-on-reset (POR) circuit. Upon power-up, the device will not respond to any commands until the V_{CC} level crosses the internal voltage threshold (V_{POR}) that brings the device out of reset and into standby mode.

The system designer must ensure that no instruction is sent to the device until the V_{CC} supply has reached a stable value greater than the minimum V_{CC} level. Once the V_{CC} has surpassed the minimum level, the SPI Master must wait at least t_{VCSL} before asserting the $\overline{CS}$ pin. See Table 7-6 for the values associated with these power-up parameters.

Table 7-6. Power-up Conditions[1]

Symbol	Parameter	Min	Max	Units
t_{VCSL}	Minimum V_{CC} to Chip Select Low Time	100		µs
V_{POR}	Power-On Reset Threshold Voltage		1.5	V
t_{POFF}	Minimum time at V_{CC} = 0V between power cycles	1		ms

Note: 1. These parameters are characterized but are not 100% tested in production.

If an event occurs in the system where the V_{CC} level supplied to the AT25M02 drops below the maximum V_{POR} level specified, it is recommended that a full power cycle sequence be performed by first driving the V_{CC} pin to GND, waiting at least the minimum t_{POFF} time, and then performing a new power-up sequence in compliance with the requirements defined in this section.

7.7.2 Software Reset

The SPI interface of the AT25M02 can be reset by toggling the $\overline{CS}$ input. If the $\overline{CS}$ line is already in the active state, it must a complete transition from the inactive state (≥ V_{IH}) to the active state (≤ V_{IL}), and then back to the inactive state (≥ V_{IH}) without sending clocks on the SCK line. Upon completion of this sequence, the device will be ready to receive a new opcode on the SI line.

7.7.3 Device Default State at Power-up

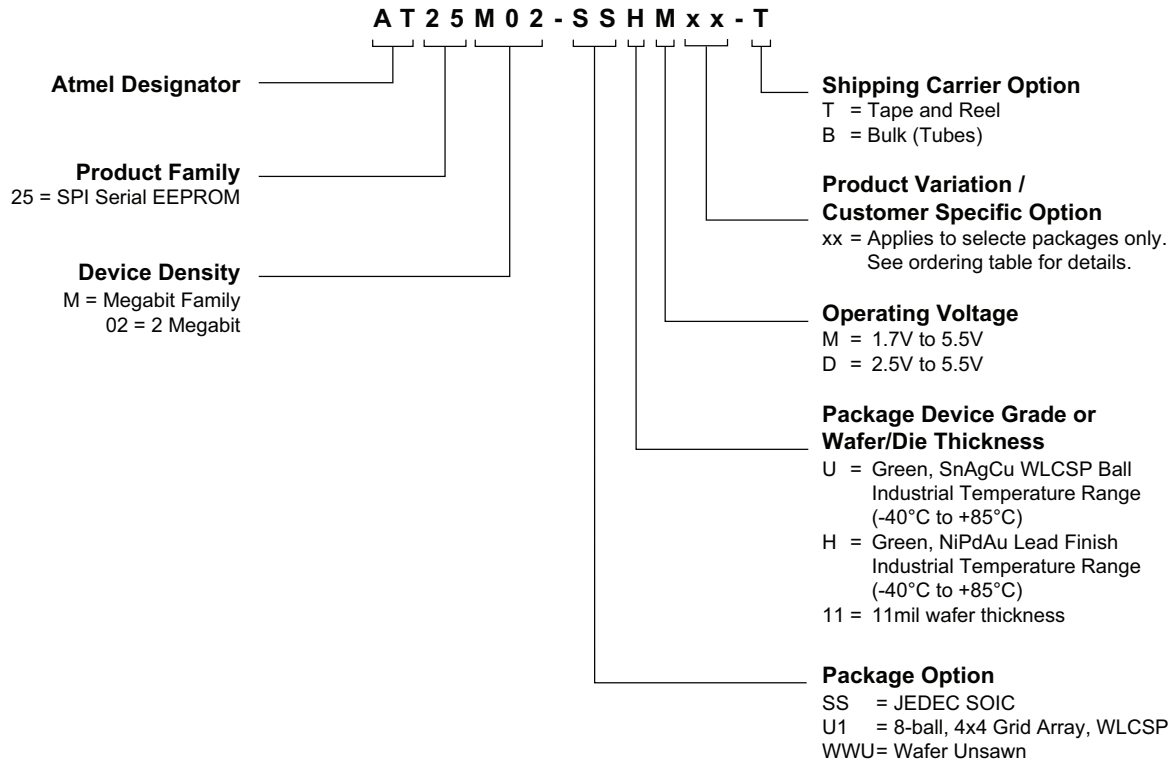
The AT25M02 default state upon power-up consists of:

- Standby Power mode.
- Write Enable Latch (WEL) bit in the Status Register = 0.
- $\overline{Ready}$/Busy bit in the Status Register = 0, indicating the device is ready to accept a new command.
- Device is not selected.
- Not in Hold condition.
- WPEN, BP1 and BP0 bits in the Status Register are unchanged from their previous state due to the fact that they are non-volatile values.

7.7.4 Device Default Condition from Atmel

The AT25M02 is shipped from Atmel to the customer with the EEPROM array set to an all FFh data pattern (Logic 1 state). The Write Protection Enable bit in the Status Register is set to Logic 0 (the ability of the EEPROM array to write is dictated by the values of the Block Write Protect bits while the SR ability to write is controlled by the WEL bit). The Block Write Protection bits in the Status Register are set to Logic 0 (no write protection selected).

8. Ordering Code Detail



9. Ordering Information

Additional package types that are not listed below may be available for order. Please contact Atmel for availability details.

Atmel Ordering Code	Lead Finish	Package	Voltage	Delivery Information		Operation Range
				Form	Quantity	
AT25M02-SSHM-T	NiPdAu (Lead-free/Halogen-free)	8S1	1.7V to 5.5V	Tape and Reel	4,000 per Reel	Industrial Temperature (-40°C to 85°C)
AT25M02-SSHM-B				Bulk (Tubes)	100 per Tube	
AT25M02-SSHD-T			2.5V to 5.5V	Tape and Reel	4,000 per Reel	
AT25M02-SSHD-B				Bulk (Tubes)	100 per Tube	
AT25M02-U1UM0B-T(1)	SnAgCu (Lead-free/Halogen-free)	8U-10	1.7V to 5.5V	Tape and Reel	5,000 per Reel	
AT25M02-WWU11M(2)	n/a	Wafer Sale		Note 2		

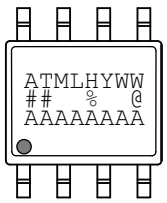
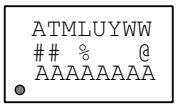
Notes: 1. WLCSP Package:
- This device includes a backside coating to increase product robustness.
- **CAUTION:** Exposure to ultraviolet (UV) light can degrade the data stored in EEPROM cells. Therefore, customers who use a WLCSP package must ensure that exposure to ultraviolet light does ***not*** occur.

2. For wafer sales, please contact Atmel Sales.

Package Type	
8S1	8-lead, 0.150" wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8U-10	4-ball, 4x4 Grid Array, Wafer Level Chip Scale Package (WLCSP)

10. Part Marking Scheme

AT25M02: Package Marking Information

8-lead SOIC	8-ball WLCSP
	

Note 1: ● designates pin 1
Note 2: Package drawings are not to scale

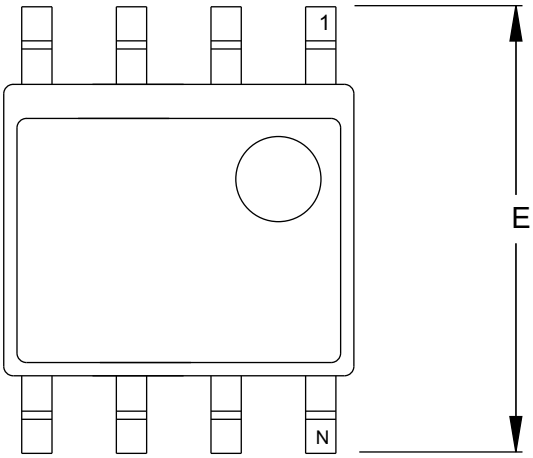
Catalog Number Truncation			
AT25M02		Truncation Code ##: 5H	
Date Codes			**Voltages**
Y = Year	M = Month	WW = Work Week of Assembly	% = Minimum Voltage
2: 2012 6: 2016 3: 2013 7: 2017 4: 2014 8: 2018 5: 2015 9: 2019	A: January B: February ... L: December	02: Week 2 04: Week 4 ... 52: Week 52	M: 1.7V min D: 2.5V min
Country of Assembly	**Lot Number**		**Grade/Lead Finish Material**
@ = Country of Assembly	AAA...A = Atmel Wafer Lot Number		U: Industrial/SnAgCu H: Industrial/NiPdAu
Trace Code			**Atmel Truncation**
XX = Trace Code (Atmel Lot Numbers Correspond to Code) Example: AA, AB.... YZ, ZZ			AT: Atmel ATM: Atmel ATML: Atmel

5/6/15

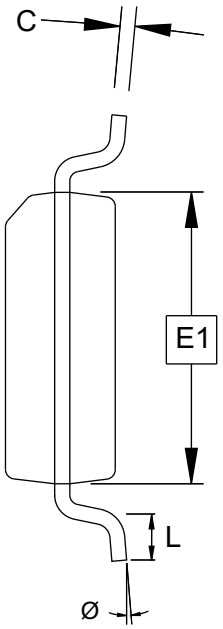
Atmel Package Mark Contact: DL-CSO-Assy_eng@atmel.com	**TITLE** **25M02SM**, AT25M02 Standard Package Marking Information	**DRAWING NO.** 25M02SM	**REV.** C

11. Packaging Information

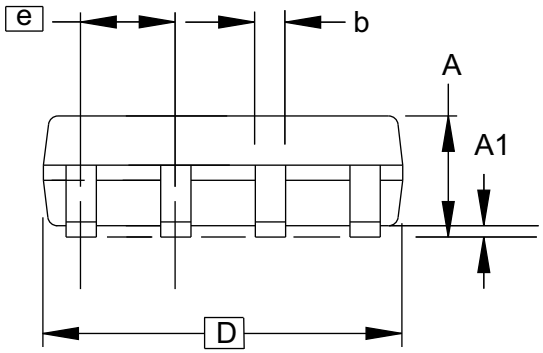
11.1 8S1 — 8-lead JEDEC SOIC



TOP VIEW



END VIEW



SIDE VIEW

Notes: This drawing is for general information only.
Refer to JEDEC Drawing MS-012, Variation AA
for proper dimensions, tolerances, datums, etc.

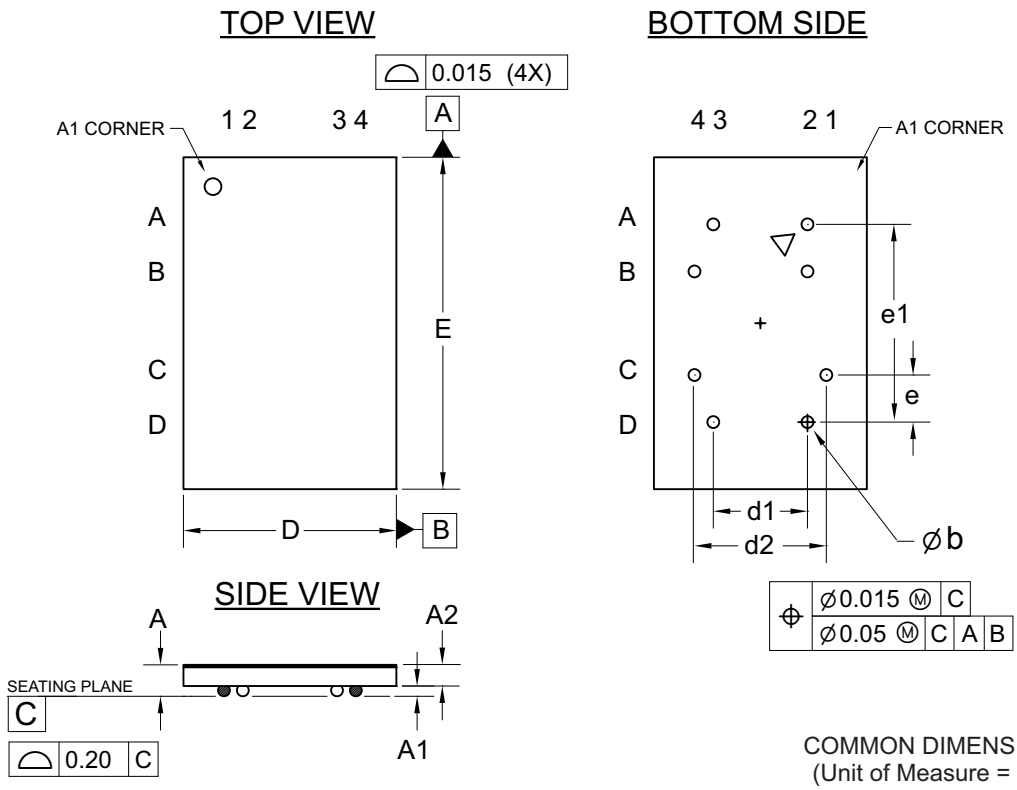
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D		4.90 BSC		
E		6.00 BSC		
E1		3.90 BSC		
e		1.27 BSC		
L	0.40	–	1.27	
Ø	0°	–	8°	

3/6/2015

Atmel Package Drawing Contact: packagedrawings@atmel.com	**TITLE** 8S1, 8-lead (0.150” Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC)	**GPC** SWB	**DRAWING NO.** 8S1	**REV.** H

11.2 8U-10 — 8-ball WLCSP



PIN ASSIGNMENT MATRIX

	1	2	3	4
A	n/a	V_{CC}	$\overline{CS}$	n/a
B	n/a	$\overline{HOLD}$	n/a	SO
C	SCK	n/a	n/a	$\overline{WP}$
D	n/a	SI	GND	n/a

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	TYP	MAX	NOTE
A	0.313	0.334	0.355	
A1	—	0.094	—	
A2	—	0.240	—	3
D	Contact Atmel for details			
d1	1.00 BSC			
d2	1.40 BSC			
E	Contact Atmel for details			
e	0.50 BSC			
e1	2.10 BSC			
b	0.170	0.185	0.200	

Note: 1. Dimensions are NOT to scale.
2. Solder ball composition is 95.5Sn-4.0Ag-0.5Cu.
3. Product offered with Back Side Coating

9/22/15

Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE 8U-11, 8-ball 4x4 Array, Custom Pitch Wafer Level Chip Scale Package (WLCSP)	GPC GAC	DRAWING NO. 8U-10	REV. E

12. Revision History

Doc. Rev.	Date	Comments
8832B	02/2016	Removed preliminary status and updated 8U-10 package drawing.
8832A	05/2015	Initial document release.

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