ADS1257 30-kSPS, 4-Channel, 24-Bit ADC with PGA in 5-mm × 5-mm VQFN Package

1 Features

- Up to 23-Bits Noise-Free Resolution
- Small 5-mm × 5-mm VQFN Package
- 4 Analog Inputs
  - 2 Differential or 3 Single-Ended Measurements
- Excellent DC Performance
  - Offset Drift: 4 nV/°C (Gain = 64)
  - Gain Drift: 0.8 ppm/°C
  - Nonlinearity: 3 ppm (Gain = 1)
- Programmable Data Rates: 2.5 SPS to 30 kSPS
- Single-Cycle Settled Conversions (≤ 1000 SPS)
- 50-Hz and 60-Hz Rejection
- High Impedance Input Buffer
- Differential-Input PGA
- Integrated Sensor Break Detection
- 2 General-Purpose Input/Outputs
- Power Supplies:
  - Analog: 5 V
  - Digital: 1.8 V to 3.6 V
- 5-V Tolerant SPI™-Compatible Serial Interface

2 Applications

- Factory Automation and Process Control
- Test and Measurement
- Medical Equipment
- Scientific Instrumentation

3 Description

The ADS1257 is a low-noise, 30-kSPS, 24-bit, delta-sigma (ΔΣ) analog-to-digital converter (ADC) with an integrated multiplexer, input buffer, and programmable gain amplifier (PGA) in a small 20-pin, 5-mm × 5-mm VQFN package. The combination of integration, high conversion rate, and 24-bit resolution together in a small package makes the device ideally suited for space-constrained applications.

The input multiplexer accepts either two differential or three single-ended input measurements. The sensor break circuit verifies the input connection continuity to the ADC. The selectable input buffer greatly increases the input impedance, and in many cases, eliminates the need for external buffers. The buffer input voltage range includes AGND. The low-noise PGA provides gains from 1 to 64 to accommodate a wide range of inputs (from ±78 mV to ±5 V). The programmable digital filter optimizes ADC resolution (up to 23 bits noise-free) and conversion rates (up to 30 kSPS). The digital filter provides single-cycle settled conversions, and rejection of 50-Hz and 60-Hz interference signals.

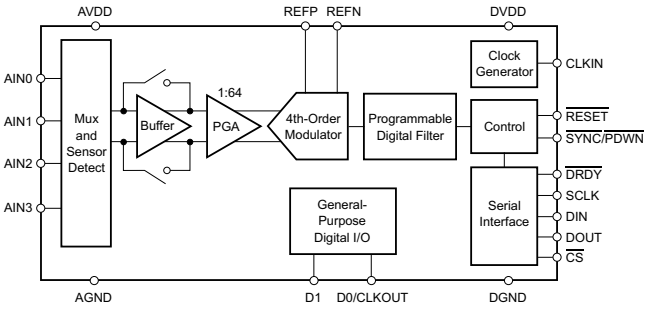
The SPI-compatible serial interface operates with as little as three wires, simplifying connections to external controllers. Integrated calibration features support both self and system correction of offset and gain errors for all PGA gain settings. Two bidirectional digital I/Os pins control external circuits.

Device Information[1]

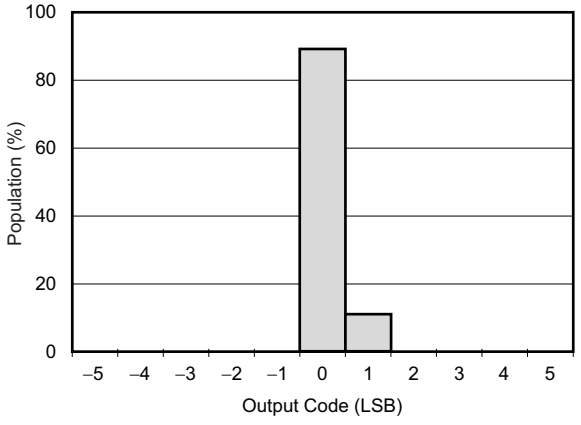
PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADS1257	VQFN (20)	5.00 mm × 5.00 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

Block Diagram



Output Data Histogram (256 readings, 2.5 SPS, Gain = 1)



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

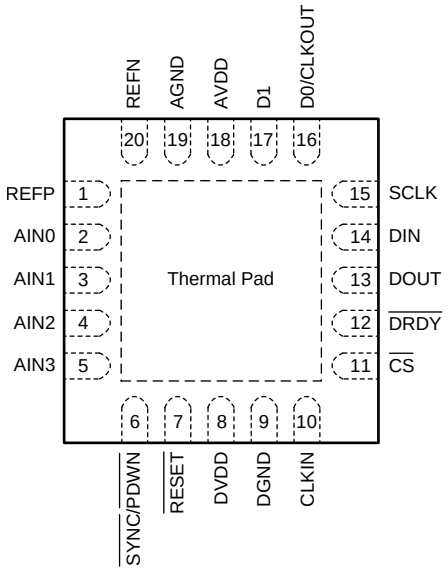
Changes from Original (September 2015) to Revision A	Page
• Changed from product preview to production data	1

5 Device Comparison Table

PART NUMBER	NUMBER OF INPUTS		NUMBER OF GPIOS	PACKAGE
	SINGLE-ENDED	DIFFERENTIAL		
ADS1255	2	1	2	20-pin SSOP
ADS1256	8	4	4	28-pin SSOP
ADS1257	3	2	2	20-pin QFN

6 Pin Configuration and Functions

RGW Package
20-Pin QFN
Top View (Not to Scale)



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	REFP	Analog input	Positive reference input
2	AIN0	Analog input	Analog input 0. Leave unconnected or connect to AVDD if not used.
3	AIN1	Analog input	Analog input 1. Leave unconnected or connect to AVDD if not used.
4	AIN2	Analog input	Analog input 2. Leave unconnected or connect to AVDD if not used.
5	AIN3	Analog input	Analog input 3. Leave unconnected or connect to AVDD if not used.
6	$\overline{\text{SYNC}}/\text{PDWN}$	Digital input(1)(2)	Synchronization or power down input; active low. Connect to DVDD if not used.
7	$\overline{\text{RESET}}$	Digital input(1)(2)	Reset input, active low. Connect to DVDD if not used.
8	DVDD	Digital	Digital power supply
9	DGND	Digital	Digital ground
10	CLKIN	Digital input(2)	External clock input
11	$\overline{\text{CS}}$	Digital input(1)(2)	Chip select; active low. Connect to DGND if not used.
12	$\overline{\text{DRDY}}$	Digital output	Data ready output; active low
13	DOUT	Digital output	Serial data output
14	DIN	Digital input(1)(2)	Serial data input
15	SCLK	Digital input(1)(2)	Serial clock input
16	D0/CLKOUT	Digital input/output(3)	General purpose digital I/O 0 or clock output
17	D1	Digital input/output(3)	General purpose digital I/O 1
18	AVDD	Analog	Analog power supply
19	AGND	Analog	Analog ground
20	REFN	Analog input	Negative reference input
Thermal Pad		—	Thermal power pad. Connect to AGND.

(1) Schmitt-trigger digital input.
(2) 5-V tolerant digital input.
(3) Schmitt-trigger digital input when the digital I/O is configured as an input.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
AVDD to AGND		–0.3	6.0	V
DVDD to DGND		–0.3	3.6	V
AGND to DGND		–0.3	0.3	V
Analog input voltage		AGND – 0.3	AVDD + 0.3	V
Digital input voltage	DIN, SCLK, $\overline{CS}$, $\overline{RESET}$, $\overline{SYNC}$/$\overline{PWDN}$, CLKIN	DGND – 0.3	DGND + 6.0	V
	D0/CLKOUT, D1	DGND – 0.3	DVDD + 0.3	
Input current, continuous	Any pins except power-supply pins	–10	10	mA
Operating temperature		–40	105	°C
Junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
	Analog power supply	AVDD to AGND	4.75	5	5.25	V
	Digital power supply	DVDD to DGND	1.8		3.6	V
	Analog to digital ground potential	AGND to DGND	–0.1	0	0.1	V
ANALOG INPUTS						
V_{IN}	Differential input voltage	$V_{IN} = V_{(AINP)} - V_{(AINN)}$	$-2 \cdot V_{ref}$ / Gain		$2 \cdot V_{ref}$ / Gain	V
$V_{(AINx)}$	Absolute input voltage	Buffer off	AGND – 0.1		AVDD + 0.1	V
		Buffer on	AGND		AVDD – 2.0	
VOLTAGE REFERENCE INPUTS						
V_{ref}	Differential reference input voltage	$V_{ref} = V_{(REFP)} - V_{(REFN)}$	0.5	2.5	2.6	V
$V_{(REFN)}$	Absolute negative reference input voltage	Buffer off	AGND – 0.1		$V_{(REFP)}$ – 0.5	V
		Buffer on(1)	AGND		$V_{(REFP)}$ – 0.5	
$V_{(REFP)}$	Absolute positive reference input voltage	Buffer off	$V_{(REFN)}$ + 0.5		AVDD + 0.1	V
		Buffer on(1)	$V_{(REFN)}$ + 0.5		AVDD – 2.0	
CLOCK SOURCE						
$f_{(CLKIN)}$	Clock frequency		0.1	7.68	10	MHz
	Duty cycle		40%	50%	60%	
DIGITAL INPUTS						
	Digital input voltage	$\overline{DIN}$, SCLK, $\overline{CS}$, $\overline{RESET}$, $\overline{SYNC}/\overline{PWDN}$, CLKIN	DGND		DGND + 5.25	V
		D0/CLKOUT, D1	DGND		DVDD	
TEMPERATURE						
T_A	Specified ambient temperature		–40		85	°C

(1) The reference input range with buffer on is restricted only if self-calibration or gain self-calibration is used. If using system calibration or writing calibration values directly to the registers, the entire buffer off range can be used.

7.4 Thermal Information

THERMAL METRIC(1)		RGW (QFN) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	24.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	10.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	10.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

Minimum and maximum specifications apply from T_A = −40°C to +85°C. Typical specifications are at T_A = 25°C. All specifications are at AVDD = 5 V, DVDD = 1.8 V, buffer on, $f_{(CLKIN)}$ = 7.68 MHz, gain = 1, and V_{ref} = 2.5 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
	PGA gain settings			1, 2, 4, 8, 16, 32, 64		V/V
	Differential input impedance	Buffer off, gain = 1, 2, 4, 8, 16		150 / Gain		kΩ
		Buffer off, gain = 32, 64		4.7		
		Buffer on, DR ≤ 50 SPS		80		MΩ
SYSTEM PERFORMANCE						
	Resolution	All data rates and PGA gain settings	24			Bit
DR	Data rate		2.5		30,000	SPS
INL	Integral nonlinearity	Differential input, gain = 1, buffer off		3	10	ppm
		Differential input, gain = 64, buffer off		7		
V_{IO}	Input offset voltage	After calibration		On the level of the noise		
	Offset drift	Gain = 1		100		nV/°C
		Gain = 64		4		
	Gain error	After calibration, gain = 1, buffer on		±0.005%		
		After calibration, gain = 64, buffer on		±0.03%		
	Gain drift	Gain = 1		0.8		ppm/°C
		Gain = 64		0.8		
CMRR	Common-mode rejection ratio	f_{CM} = 60 Hz, DR = 30 kSPS(1)	95	110		dB
PSRR	Analog power-supply rejection ratio	±5% Δ in AVDD	60	70		dB
PSRR	Digital power-supply rejection ratio	±10% Δ in DVDD		100		dB
VOLTAGE REFERENCE INPUTS						
	Reference input impedance			18.5		kΩ
SENSOR DETECT CURRENT SOURCES						
	Current settings			0.5, 2 ,10		µA
DIGITAL INPUTS/OUTPUTS						
V_{IH}	High-level input voltage	DIN, SCLK, CLKIN, $\overline{SYNC}$/PDWN, $\overline{CS}$, $\overline{RESET}$	0.8 DVDD		5.25	V
		D0/CLKOUT, D1	0.8 DVDD		DVDD	V
V_{IL}	Low-level input voltage		DGND		0.2 DVDD	
V_{OH}	High-level ouput voltage	I_{OH} = 4 mA	0.8 DVDD			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA			0.2 DVDD	V
	Input hysteresis			0.5		V
	Input leakage	0 < digital input voltage < DVDD	–10		+10	µA
POWER SUPPLY						
I_{AVDD}	Analog supply current	Power-down mode			5	µA
		Standby mode		20		µA
		Normal mode, gain = 1, buffer off		7	10	mA
		Normal mode, gain = 64, buffer off		16	24	mA
		Normal mode, gain = 1, buffer on		13	19	mA
		Normal mode, gain = 64, buffer on		36	50	mA
I_{DVDD}	Digital supply current	Power-down mode			5	µA
		Standby mode, CLKOUT off, DVDD = 3.3 V		95		µA
		Normal mode, CLKOUT off, DVDD = 3.3 V		0.9	2	mA
P_D	Power dissipation	Normal mode, gain = 1, buffer off, DVDD = 3.3 V		38	57	mW
		Standby mode, DVDD = 3.3 V		0.4		

(1) f_{CM} is the frequency of the common-mode input signal. Placing a notch of the digital filter at 60 Hz (setting DR = 60 SPS, 30 SPS, 15 SPS, 10 SPS, 5 SPS, or 2.5 SPS) further improves the common-mode rejection of this frequency.

8 Device and Documentation Support

8.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

8.2 Trademarks

E2E is a trademark of Texas Instruments.
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8.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS1257IRGWR	ACTIVE	VQFN	RGW	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS1257	Samples
ADS1257IRGWT	ACTIVE	VQFN	RGW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS1257	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

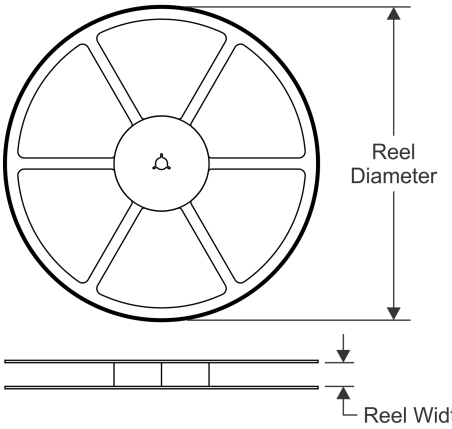
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

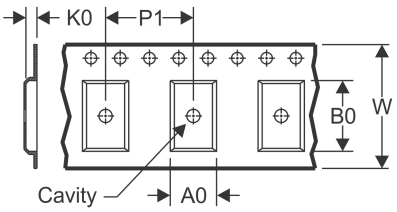
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

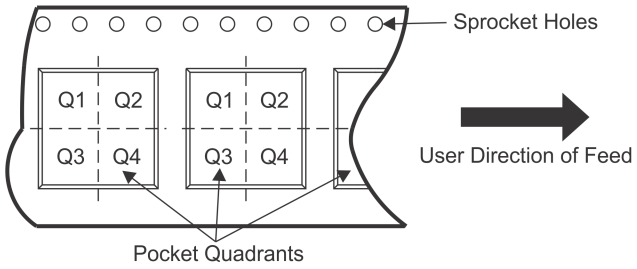


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

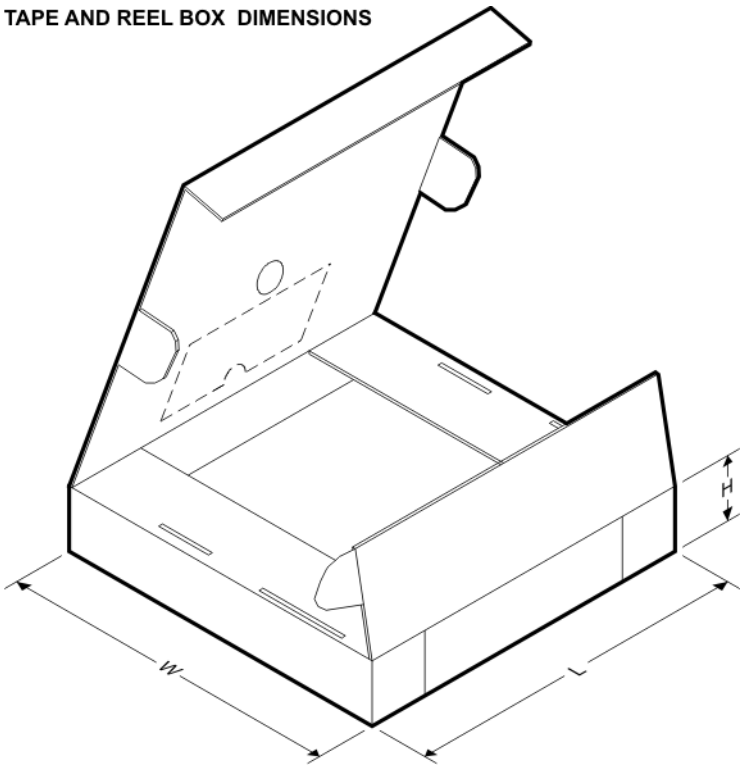
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS1257IRGWR	VQFN	RGW	20	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
ADS1257IRGWT	VQFN	RGW	20	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

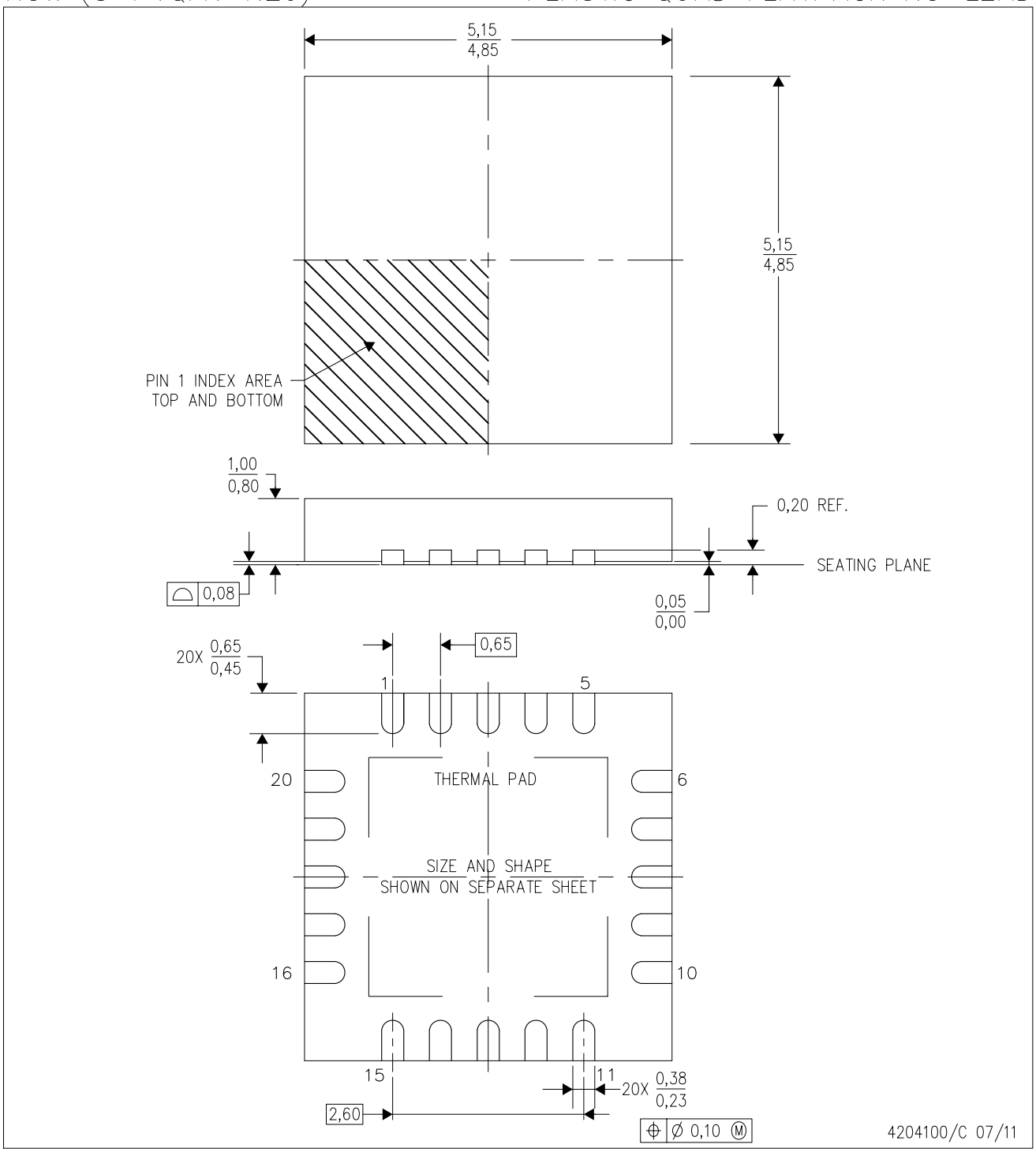
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS1257IRGWR	VQFN	RGW	20	3000	367.0	367.0	35.0
ADS1257IRGWT	VQFN	RGW	20	250	210.0	185.0	35.0

RGW (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flat pack, No–leads (QFN) package configuration
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

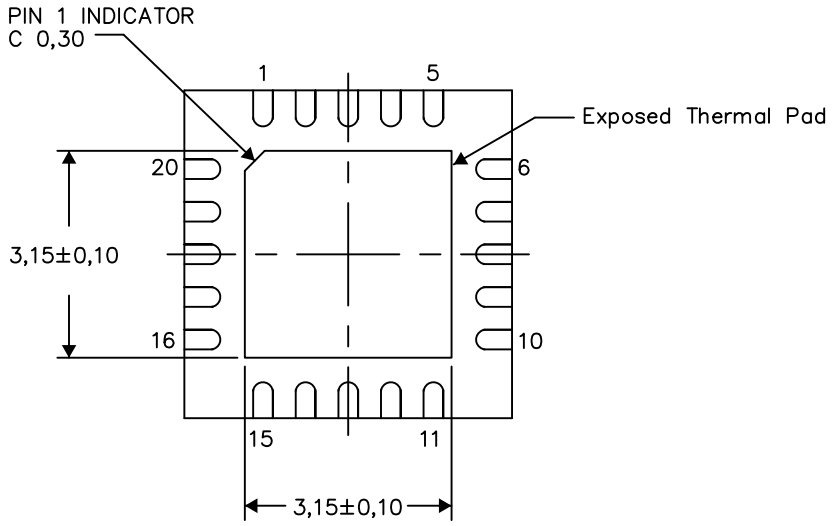
RGW (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



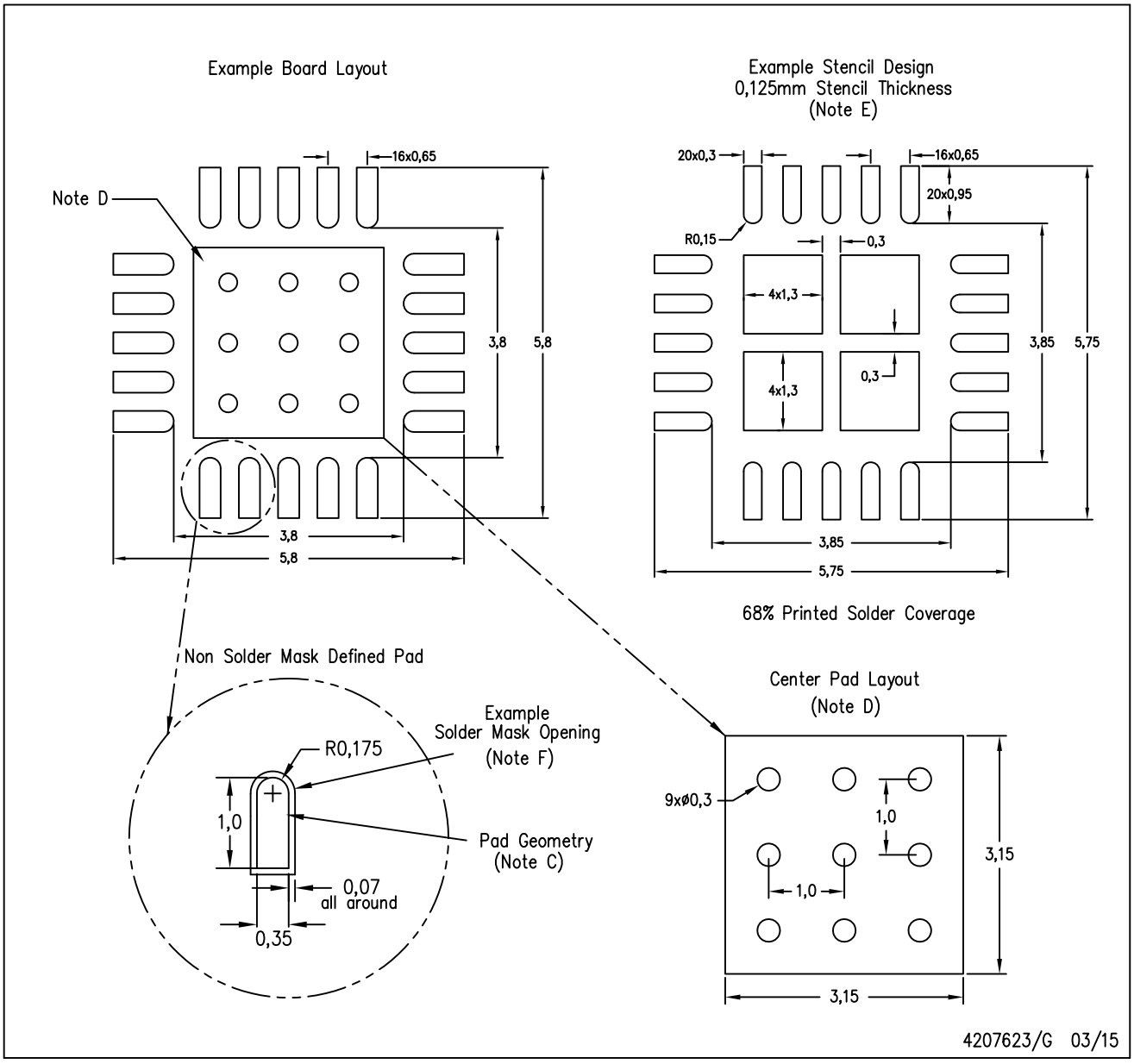
Bottom View

Exposed Thermal Pad Dimensions

4206352–2/M 06/15

NOTE: All linear dimensions are in millimeters

RGW (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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