Level 4 EMC Protected RS-485 Transceiver with Full ±42 V Fault Protection

Preliminary Technical Data

ADM3095E

FEATURES

- **Certified Level 4 EMC protection on RS-485 A and B bus pins**
  - **IEC 61000-4-5 surge protection (±4 kV)**
  - **IEC 61000-4-4 EFT protection (±2 kV)**
  - **IEC 61000-4-2 ESD protection**
    - **±8 kV contact discharge**
    - **±15 kV air-gap discharge**
- **RS-485 A and B bus pins HBM ESD >±30 kV**
- **±42 V ac/dc peak fault protection on RS-485 bus pins**
- **TIA/EIA RS-485/RS-422 compliant over full supply range**
  - **3 V to 5.5 V operating voltage range on V_{CC}**
  - **1.62 V to 5.5 V V_{IO} logic supply**
- **Common-mode input range: −25 V to +25 V**
- **Up to 2.5 Mbps data rate**
- **Half-duplex**
- **Profibus compliant at 4.5 V V_{CC}**
- **Receiver short circuit, open circuit, and floating input fail-safe**
- **Supports 256 bus nodes (96 kΩ receiver input impedance)**
- **−40°C to +125°C temperature option**
- **Glitch free power-up/power-down (hot swap)**
- **16-lead narrow body SOIC package**
- **Low Power shutdown current**

APPLICATIONS

- **HVAC networks**
- **Industrial field buses**
- **Building automation**
- **Utility networks**

GENERAL DESCRIPTION

The ADM3095E is a 3 V to 5.5 V, 2.5 Mbps, RS-485 transceiver that features up to ±42V ac/dc peak bus overvoltage fault protection on RS-485 bus pins. This device is designed to withstand overvoltage faults, such as shorts directly to power supplies, and overvoltage faults, such as 24 V ac supplies connected in error to the RS-485 A and B bus pins. The ADM3095E is an RS-485 transceiver that integrates IEC 61000-4-5 Level 4 surge protection, allowing up to ±4 kV protection on RS-485 bus pins. The device has IEC 61000-4-4 Level 4 electrical fast transient (EFT) protection up to ±2 kV and IEC 61000-4-2 Level 4 electrostatic discharge (ESD) protection on the bus pins allowing the device to withstand up to ±15 kV on the transceiver interface pins without latch up or damage.

These devices have an extended common-mode input range of ±25 V to improve data communication reliability in noisy environments over long cable lengths where ground loop voltages are possible. The combination of extended common-mode range, overvoltage fault protection, surge, EFT protection, and ESD protection provide a device that is a completely integrated electromagnetic compatibility (EMC) protected RS-485 transceiver.

The ADM3095E also features a logic supply pin, V_{IO}, for a flexible digital interface, operational to voltages as low as 1.62 V. The ADM3095E is Profibus compliant with a high driver differential output voltage, V_{OD}, of 2.1 V minimum at power supply voltages greater than 4.5 V. The device is fully characterized over extended operating temperature ranges, with options of −40°C to +125°C, and is available in a 16-lead, narrow body SOIC package.

FUNCTIONAL BLOCK DIAGRAM

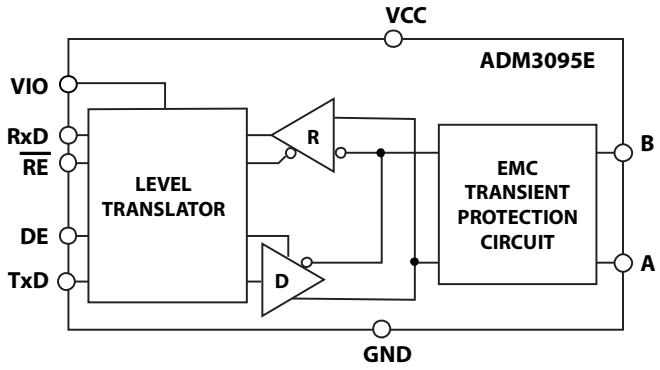

Figure 1.

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- ADM3095E: Level 4 EMC Protected RS-485 Transceiver with Full ±42 V Fault Protection Preliminary Data Sheet

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SPECIFICATIONS

V_{CC} = 3.0 V to 5.5 V, $T_A = T_{MIN}$ (−40°C), to T_{MAX} (125°C), unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER					
Differential Output Voltage, V_{OD}					
	1.5		5.0	V	$V_{CC} \geq 3.0$ V, R = 27 Ω or 50 Ω, Figure 21
	2.1		5.0	V	$V_{CC} \geq 4.5$ V, R = 27 Ω or 50 Ω, Figure 21
$\|V_{OD3}\|$	1.5		5.0	V	$V_{CC} \geq 3.0$ V, V_{CM} = −25 V to +25 V, see Figure 22
	2.1		5.0	V	$V_{CC} \geq 4.5$V, V_{CM} = −25V to +25 V, see Figure 22
$\Delta\|V_{OD}\|$ for Complementary Output States			0.2	V	R = 27 Ω or 50 Ω, see Figure 21
Common-Mode Output Voltage, V_{OC}			3	V	R = 27 Ω or 50 Ω, see Figure 21
$\Delta\|V_{OC}\|$ for Complementary Output States			0.2	V	R = 27 Ω or 50 Ω, see Figure 21
Output Short-Circuit Current, V_{OUT} = High	−250		+250	mA	$-42 \text{ V} \leq V_{SC} \leq +42$ V
Output Short-Circuit Current, V_{OUT} = Low	−250		+250	mA	$-42 \text{ V} \leq V_{SC} \leq +42$ V
DRIVER INPUT LOGIC					
Input Logic Threshold Low			0.33 V_{IO}	V	$1.62 \text{ V} \leq V_{IO} \leq 5.5$ V
Input Logic Threshold High	0.7 V_{IO}			V	$1.62 \text{ V} \leq V_{IO} \leq 5.5$ V
Logic Input Current (DI)			1	µA	$0 \leq V_{IN} \leq V_{IO}$
RECEIVER					
Differential Input Threshold Voltage, V_{TH}	−200	−125	−30	mV	$-25 \text{ V} \leq V_{CM} \leq +25$ V
Input Hysteresis		30		mV	$-25 \text{ V} \leq V_{CM} \leq +25$ V
Input Resistance (A, B)	96			kΩ	$-25 \text{ V} \leq V_{CM} \leq +25$ V
Input Capacitance (A, B)		150		pF	T_A = 25°C
Input Current (A, B)	−1.0		+1.0	mA	DE = 0 V, V_{CC} = 0 V/5 V, V_{IN} = ±25 V
	−1.0		+1.0		DE = 0 V, V_{CC} = 0 V/5 V, V_{IN} = ±42 V
Receiver Input Common-Mode Voltage	−25		+25	V	$V_{CC} \geq 3.0$ V
CMOS Logic Input Current ($\overline{RE}$)			±1	µA	
Output Voltage Low (V_{OL})			0.2	V	I_{OUT} = 300 µA
Output Voltage High(V_{OH})	V_{IO} − 0.2			V	$V_{IO} \geq 1.62$ V, I_{OUT} = −300 µA
Output Short-Circuit Current	3		85	mA	V_{OUT} = GND/V_{CC}, $\overline{RE}$ = 0 V, $V_{IO} \geq 3.0$V
			85	mA	V_{OUT} = GND/V_{CC}, $\overline{RE}$ = 0 V, V_{IO} < 3.0V
Three-State Output Leakage Current			±2	µA	$\overline{RE}$ = V_{IO}, RxD = 0 V or V_{IO}
POWER SUPPLY					
V_{IO}	1.62 V		V_{CC}	V	
Supply Current, I_{CC}					
TxD Data Rate = 2.5 Mbps			50	mA	No load, DE = V_{CC} = V_{IO}, $\overline{RE}$ = V_{CC} = V_{IO}
RxD Data Rate = 2.5 Mbps			3	mA	No load, DE = 0 V, $\overline{RE}$ = 0 V
			90	mA	No load, DE = V_{CC} = V_{IO}, $\overline{RE}$ = 0 V
TxD/RxD Data Rate = 2.5 Mbps			130	mA	R_L = 54 Ω, DE = V_{CC} = V_{IO}, $\overline{RE}$= 0 V
TxD/RxD Data Rate = 2.5 Mbps		95		mA	R_L = 54 Ω,DE = V_{CC} = V_{IO}, $\overline{RE}$ = 0 V, V_{CC} = 5.5 V
TxD/RxD Data Rate = 2.5 Mbps		45			R_L = 54 Ω,DE = V_{CC} = V_{IO}, $\overline{RE}$ = 0 V, V_{CC} = 3.0 V
Supply Current in Shutdown Mode			5	µA	DE = 0 V, $\overline{RE}$ = V_{CC} = V_{IO}

TIMING SPECIFICATIONS

V_{CC} = 3 V to 5.5 V, V_{IO} = 1.62 V to V_{CC}, T_A = T_{MIN} (−40°C), to T_{MAX} (125°C), unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER					
Maximum Data Rate	2.5			Mbps	
Propagation Delay, t_{PLH}, t_{PHL}		30	500	ns	R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF; see Figure 23 and Figure 27.
Differential Skew, t_{SKEW}		10	50	ns	R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF; see Figure 23 and Figure 27.
Rise/Fall Times, t_R, t_F		40	130	ns	R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF; see Figure 23 and Figure 27.
Enable Time, t_{ZH}, t_{ZL}		500	2500	ns	R_L = 110 Ω, C_L = 50 pF, see Figures 23, 28.
Disable Time, t_{HZ}, t_{LZ}		500	2500	ns	R_L = 110 Ω, C_L = 50 pF, see Figures 23, 28.
Enable Time from Shutdown		4000	4500	ns	R_L = 110 Ω, C_L = 50 pF, see Figures 23, 28.
RECEIVER					
Propagation Delay, t_{PLH}, t_{PHL}		120	200	ns	C_L = 15 pF, V_{ID} ≥ ± 1.5 V; see Figure 25 and Figure 28
		140	220	ns	C_L = 15 pF, V_{ID} ≥ ± 600 mV; see Figure 25 and Figure 28
Skew, t_{SKEW}		4	40	ns	C_L = 15 pF, V_{ID} ≥ ± 1.5 V; see Figure 25 and Figure 28
Enable Time		10	50	ns	R_L = 1 kΩ, C_L = 15 pF; see Figure 26 and Figure 30
Disable Time		10	50	ns	R_L = 1 kΩ, C_L = 15 pF; see Figure 26 and Figure 30
Enable Time from Shutdown		1700	4500	ns	R_L = 1 kΩ, C_L = 15 pF; see Figure 26 and Figure 30
Time to Shutdown	50	330	3000	ns	R_L = 1 kΩ, C_L = 15 pF; see Figure 26 and Figure 30
Rx, Pulse Width Distortion			40	ns	C_L = 15 pF, V_{ID} ≥ ± 1.5 V; see Figure 25 and Figure 28

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
V_{CC} to GND	−0.5 V to 7 V
V_{IO} to GND	−0.5V to 7 V
Digital Input/Output Voltage (DE, $\overline{RE}$, TxD, RxD)	−0.3 V to V_{IO} + 0.3 V
Driver Output/Receiver Input Voltage	±48 V
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Thermal Impedance	
θ_{JA}[1], Junction to Ambient	50.9°C/W
θ_{JC}[1], Junction to Case	18.9°C/W
Maximum Junction Temperature	150°C
Continuous Total Power Dissipation	400 mW
Lead Temperature	
Soldering (10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
ESD (A, B pins only)	
IEC 61000-4-2 contact discharge	±8 kV
IEC 61000-4-2 Air discharge	±15 kV
EFT (A and B pins only)	
IEC 61000-4-4 Level 4 EFT	±2 kV
Surge (A and B pins only)	
IEC 61000-4-5 Level 4 Surge	±4 kV
HBM ESD Protection (All Pins)	±6 kV
HBM ESD Protection (A and B Pins only)	> ±30 kV
Field-Induced Charged-Device Model ESD (FICDM)	±1.25 kV

[1] Thermal impedance simulated values are based on JEDEC 2S2P thermal test board with no vias. See JEDEC JESD51.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

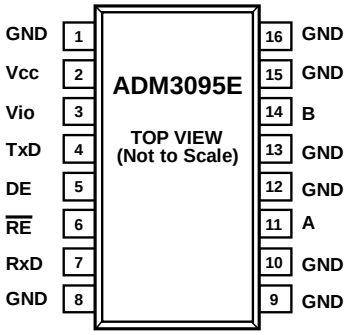


Figure 2. ADM3095E Pin Configuration

Table 4. ADM3095E Pin Descriptions

Pin No.	Mnemonic	Description
1	GND	Ground.
2	V_{CC}	3 V to 5.5 V Power Supply.
3	V_{IO}	1.62 V to 5.5 V V_{IO} Logic Supply.
4	TxD	Transmit Data Input. Data transmitted by the driver is applied to this input
5	DE	Driver Output Enable. A high level on this pin enables the A and B driver differential outputs. A low level places them into a high impedance state.
6	$\overline{RE}$	Receiver Enable Input. This is an active-low input. Driving this input low enables the receiver and driving the input high disables the receiver.
7	RxD	Receiver Output Data. This output is high when (A – B) > -50 mV and low when (A – B) < –200 mV.
8, 9, 10, 12, 13, 15, 16	GND	Ground.
11	A	Noninverting Driver Output/Receiver Input. When the driver is disabled, or when V_{CC} is powered down, Pin A is put into a high impedance state to avoid overloading the bus.
14	B	Inverting Driver Output/Receiver Input. When the driver is disabled, or when V_{CC} is powered down, Pin B is put into a high impedance state to avoid overloading the bus.

TYPICAL PERFORMANCE CHARACTERISTICS

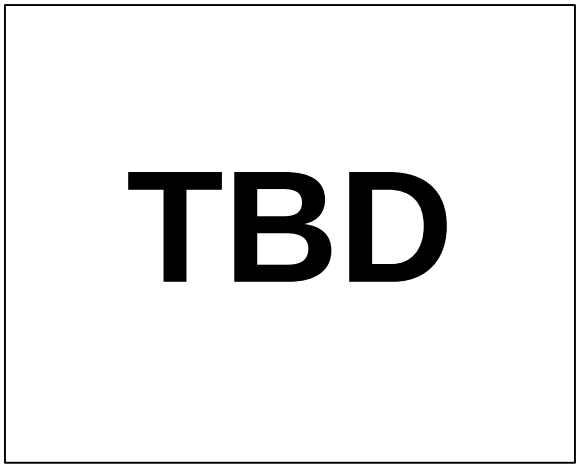


Figure 3. Supply Current (I_{CC} vs. Temperature), at RL = 54 Ω, and at RL = 120 Ω, and at RL = No Load, Data Rate = 2.5 Mbps, (V_{CC} = 5.5 V, V_{IO} = 5.5 V)

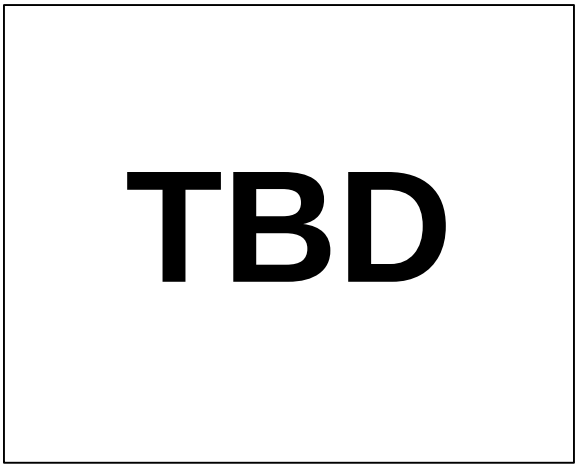


Figure 6. Driver Differential Output Current vs. Temperature

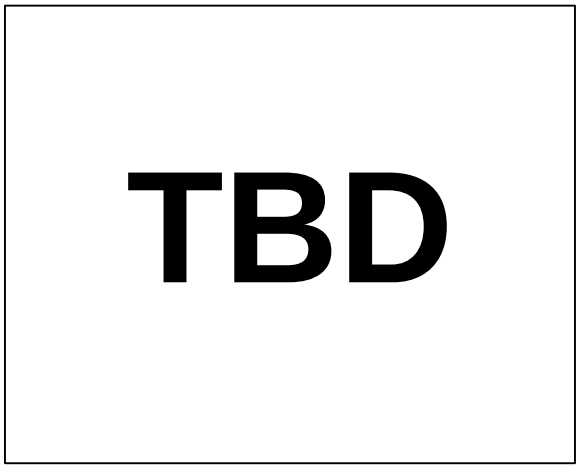


Figure 4. Supply Current (I_{CC} vs. Temperature), at RL = 54 Ω, and at RL = 120 Ω, and at RL = No Load, Data Rate = 2.5 Mbps, (V_{CC} = 3.0 V, V_{IO} = 1.62 V)

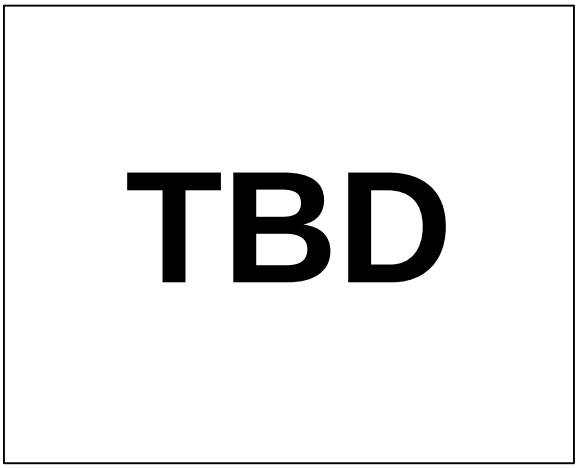


Figure 7. Driver Output Current vs. Driver Output High Voltage

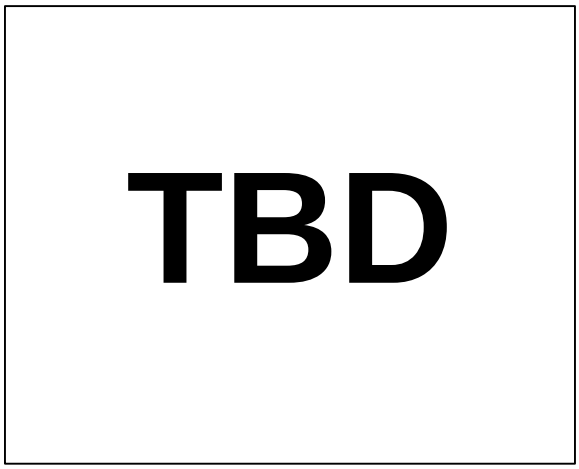


Figure 5. Driver Output Current vs. Differential Output Voltage

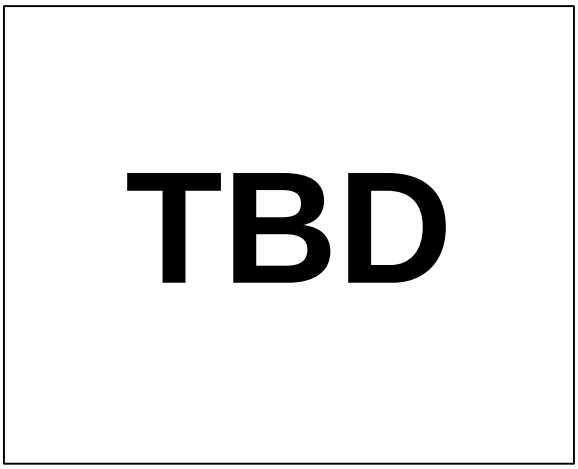


Figure 8. Driver Output Current vs. Driver Output Low Voltage

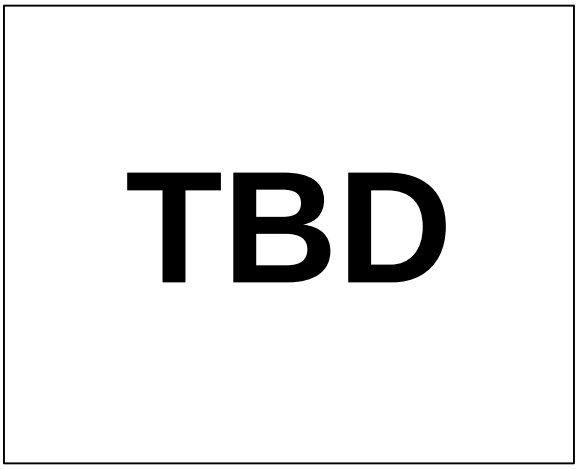


Figure 9. Driver Differential Propagation Delay vs. Temperature

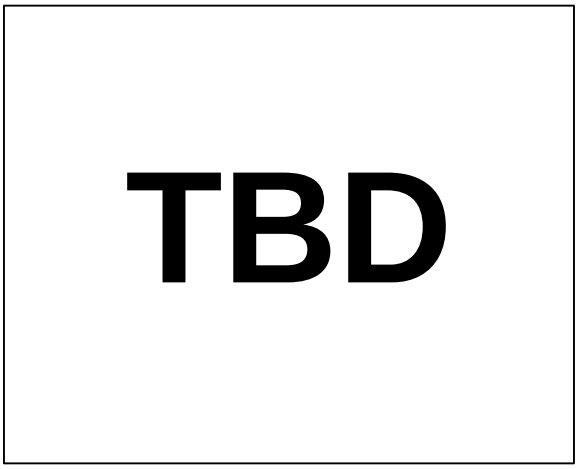


Figure 12. Receiver Output Current vs. Receiver Output Low Voltage

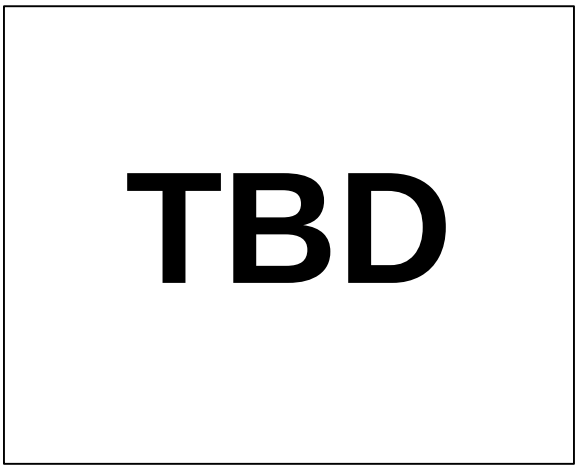


Figure 10. Driver Propagation Delay

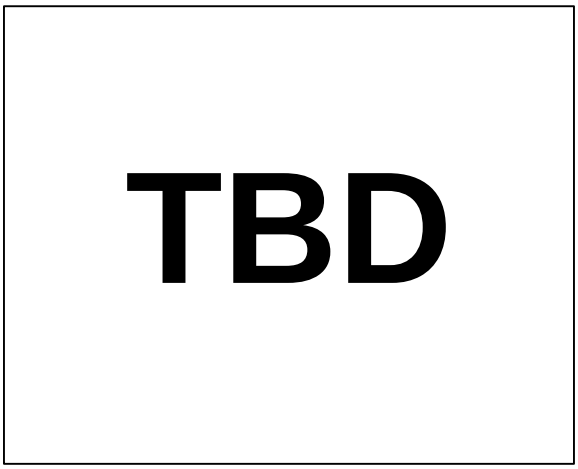


Figure 13. Receiver Output High Voltage vs. Temperature

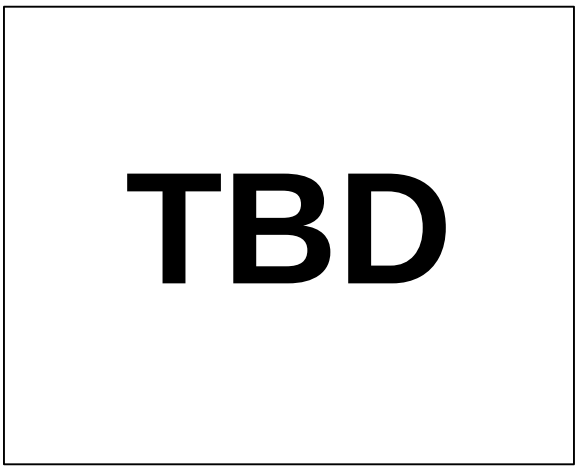


Figure 11. Receiver Output Current vs. Receiver Output High Voltage

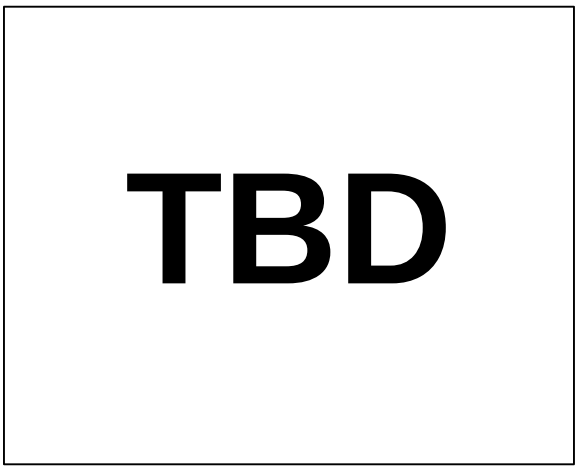


Figure 14. Receiver Output Low Voltage vs. Temperature

TBD

Figure 15. Receiver Propagation Delay

TBD

Figure 16. Receiver Propagation Delay vs. Temperature

TBD

Figure 17. Receiver Performance with Input Common-Mode Voltage of +25 V

TBD

Figure 18. Foldback Current over Fault Voltage Range

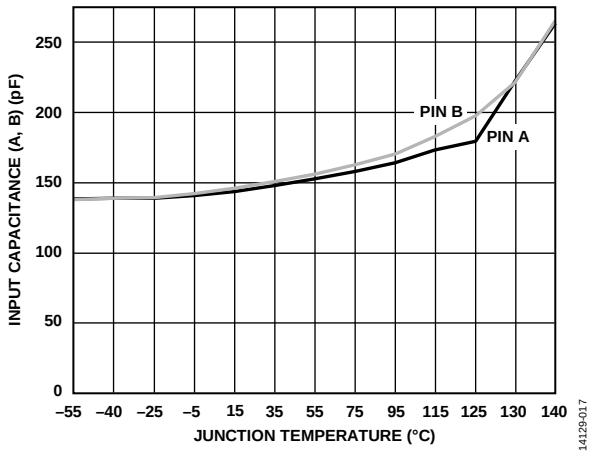


Figure 19. Input Capacitance (A and B Pin) vs. Junction Temperature

TBD

Figure 20. Receiver Input Differential Voltage (V_{ID}) vs. Signaling Rate

TEST CIRCUITS

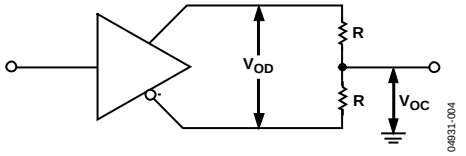


Figure 21. Driver Voltage Measurement

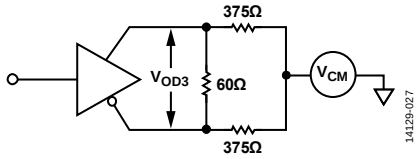


Figure 22. Driver Voltage Measurement over Common-Mode Voltage Range

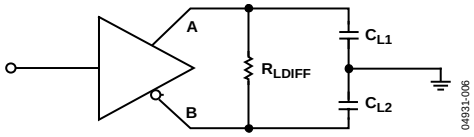


Figure 23. Driver Propagation Delay

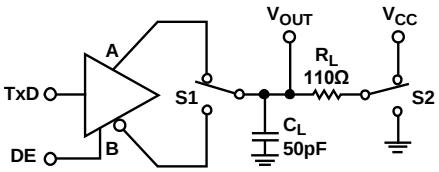


Figure 24. Driver Enable/Disable

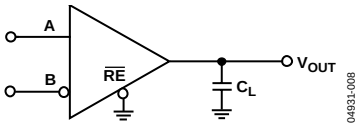


Figure 25. Receiver Propagation Delay

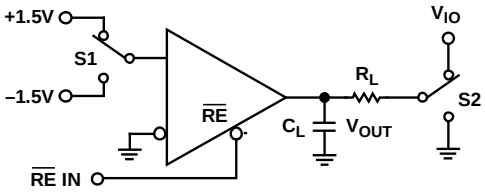


Figure 26. Receiver Enable/Disable

SWITCHING CHARACTERISTICS

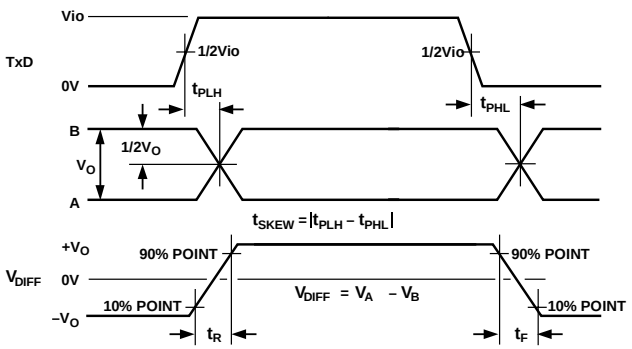


Figure 27. Driver Propagation Delay, Rise/Fall Timing

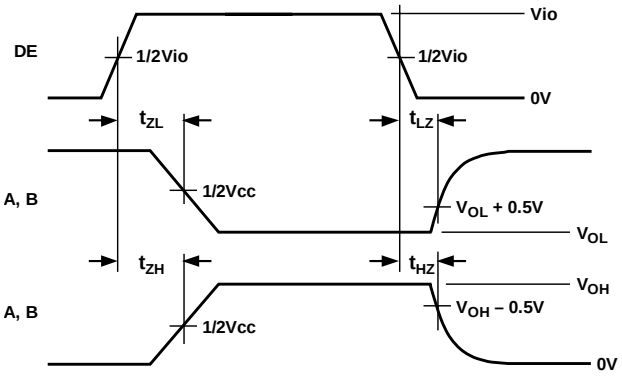


Figure 29. Driver Enable/Disable Timing

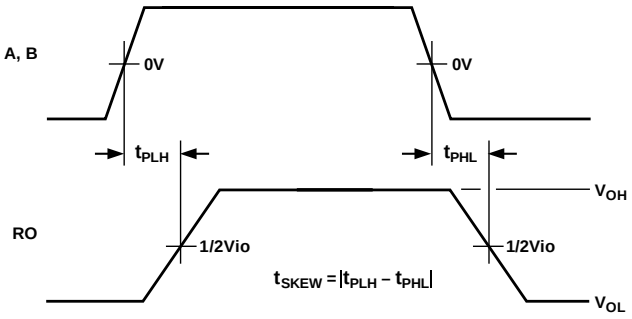


Figure 28. Receiver Propagation Delay

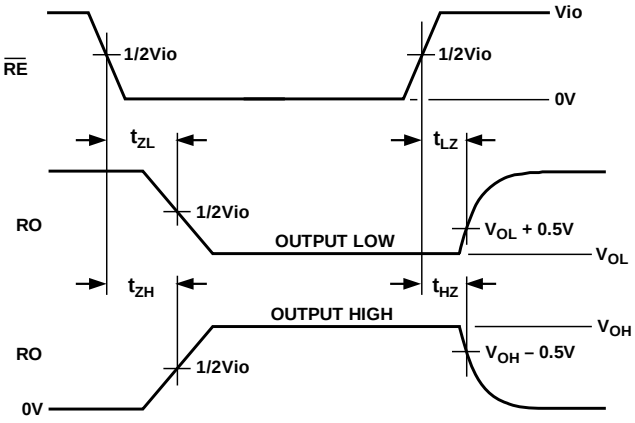


Figure 30. Receiver Enable/Disable Timing

THEORY OF OPERATION

RS-485 WITH INDUSTRY LEADING ROBUSTNESS

The ADM3095E is a 3 V to 5.5 V RS-485 transceiver with industry leading robustness that reduces system failures when operating in harsh application environments.

The ADM3095E is an RS-485 transceiver that integrates IEC 61000-4-5 Level 4 surge protection, allowing up to ±4 kV protection on RS-485 bus pins without the need for external protection components, such as transient voltage suppressors (TVS) or surge protectors (TISP). The ADM3095E has IEC 61000-4-4 Level 4 EFT protection up to ±2 kV, IEC 61000-4-2 Level 4 ESD protection, and IEC 61000-4-5 surge protection for the bus pins. The ADM3095E also offers a defined level of overvoltage fault protection

OFF THE SHELF CERTIFIED IEC EMC SOLUTION

The driver outputs/receiver inputs of RS-485 devices often experience high voltage faults from shorts to power supplies that exceed the −7 V to +12 V range, specified in the EIA/TIA-485 standard. Typically, RS-485 applications require costly external protection devices, such as positive temperature coefficient (PTC) fuses, for operation in harsh electrical environments. System designers must also consider common EMC problems in these harsh electrical environments, choosing components to provide IEC 61000-4-2 ESD, IEC 61000-4-4 EFT, and IEC 61000-4-5 surge protection for RS-485 bus pins.

When choosing suitable EMC protection components, achieving EMC regulations compliance and matching the EMC protection dynamic breakdown characteristics to the RS-485 transceiver can be challenging. To overcome these challenges, the designer may have to run multiple design, test, and PCB board iterations, leading to a slower time to market and project budget overruns.

To reduce system cost and design complexity, the ADM3095E provides integrated EMC and overvoltage fault protection. The ADM3095E integrated EMC and overvoltage fault protection circuits are optimally performance matched, saving the circuit designer significant design and testing time.

Figure 31 shows an EMC protected RS-485 circuit layout, which targets IEC 61000-4-2 ESD Level 4, IEC 61000-4-4 EFT Level 4, and IEC 61000-4-5 surge protection to Level 4 for RS-485 bus pins. This circuit uses several discrete components, including two totally integrated surge suppressors (TISPs), two transient blocking units (TBUs), and one dual-transient voltage suppressor (TVS). Due to the integrated protection components of the ADM3095E, the PCB area is significantly reduced when compared to a solution with discrete EMC and overvoltage fault protection components.

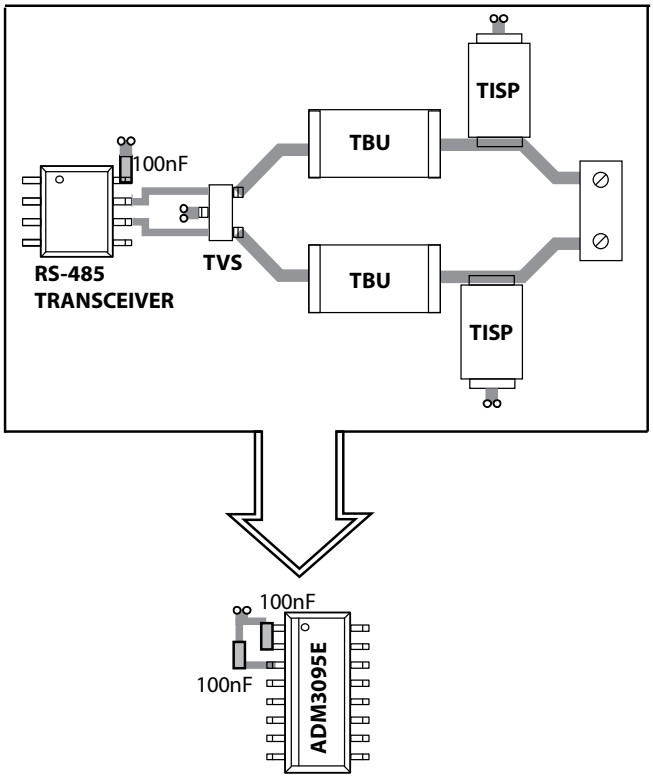


Figure 31. EMC Protected RS-485 Circuit Layout

OVERVOLTAGE FAULT PROTECTION

The ADM3095E is an RS-485 transceiver that offers fault protection over a 3 V to 5.5 V V_{CC} operating range without close examination of the RS-485 transceiver logic pin state (TxD input and DE/$\overline{RE}$). The transceiver is also fault protected over the entire extended common-mode operating range of ±25 V.

The ADM3095E RS-485 driver outputs/receiver inputs are protected from short circuits to any voltage within the −42 V to +42 V ac/dc peak range. The maximum current in a fault condition is ±250 mA. The RS-485 driver includes a foldback current limiting circuit that reduces the driver current at voltages above the ±25 V common-mode range limit of the transceiver (see Figure 18). Due to the foldback feature, this current reduction allows better management of power dissipation and heating effects.

±42 V MISWIRE PROTECTION

The ADM3095E is protected against high voltage miswire events when it operates on a bus that does not have RS-485 termination or bus biasing resistors installed. A typical miswire event is when a high voltage 24 V ac/dc power supply is connected directly to RS-485 bus pin connectors. The ADM3095E can withstand miswiring faults of up to ±42V peak on RS-485 bus pins with respect to ground (GND) without damage.

Miswiring protection is guaranteed on the ADM3095E RS-485 bus A and B pins and during a hot swap of connectors to the bus pins. Table 5 provides a summary of the high voltage miswire protection offered by the ADM3095E. The ADM3095E is tested with ±42 V dc and to ±24 V ±20% rms 50 Hz/60 Hz, with both a hot plug and dc ramp test waveforms. The test is performed in both powered and unpowered/floating power supply cases and at a range of different states for the RS-485 TxD input and DE/$\overline{RE}$ enable pins. The RS-485 bus pins survive a high voltage miswire from Pin A to GND, from Pin B to GND, and between Pin A and Pin B.

Table 5. High Voltage Miswire Protection

Supply[1]		Inputs[2]			Miswire Protection at RS-485 Output Pins[3, 4]
V_{CC}	V_{IO}	DE	$\overline{RE}$	TxD	
X	X	H/L	H/L	H/L	−42 V dc ≤ V_A ≤ +42 V dc
X	X	H/L	H/L	H/L	−42 V dc ≤ V_B ≤ +42 V dc
X	X	H/L	H/L	H/L	−42 V ac ≤ V_A ≤ +42 V ac
X	X	H/L	H/L	H/L	−42 V ac ≤ V_B ≤ +42 V ac

[1] X means on or off power supply state.
[2] H means high level for logic pin; L means low level for logic pin.
[3] This is the ac/dc peak miswire voltage between Pin A and GND, Pin B and GND, or between Pin A and Pin B.
[4] V_A refers to the voltage on Pin A and V_B refers to the voltage on Pin B.

RS-485 NETWORK BIASING AND TERMINATION

For a high voltage miswire on RS-485 A and B bus pins with biasing and termination resistors installed, there is a current path through the biasing network to the ADM3095E power supply V_{CC} pin. To protect the ADM3095E for this scenario the device has an integrated V_{CC} protection circuit. This means the current path through the R1 pull-up resistor (see Figure 32) does not cause damage to the V_{CC} pin, although the pull-up resistor can be damaged if not appropriately power rated. The R1 pull-up resistor power rating depends on the miswire voltage and the resistance value.

For the scenario where there is a miswire between the A and B pins, the ADM3095E bus setup (see Figure 32) is protected, but the RT bus termination resistor is damaged if not appropriately power rated. The RT termination resistor power rating depends on the miswire voltage and the resistance value.

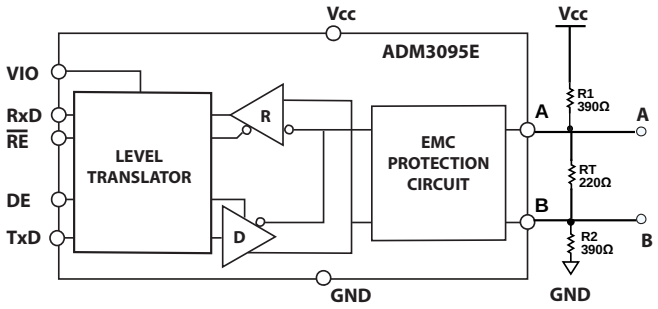


Figure 32. High Voltage Miswiring Protection for the ADM3095E with Bus Termination and Biasing Resistors

IEC ESD, EFT, AND SURGE PROTECTION

Electrical and electronic equipment must be designed to meet system level IEC standards. The following are example system level IEC standards:

- IEC 61131-2—process control and automation
- IEC 61800-3—motor control
- IEC 60730-1—building automation

For data communication lines, these system level standards specify varying levels of protection against the following three types of high voltage transients:

- IEC 61000-4-2 ESD
- IEC 61000-4-4 EFT
- IEC 61000-4-5 surge

Each of these specifications defines a test method to assess the immunity of electronic and electrical equipment against the defined phenomenon. The following sections summarize each of these tests. The ADM3095E is fully tested in accordance with these IEC EMC specifications and is certified EMC compliant.

Electrostatic Discharge (ESD)

ESD is the sudden transfer of electrostatic charge between bodies at different potentials caused by near contact or induced by an electric field. It has the characteristics of high current in a short time period. The primary purpose of the IEC 61000-4-2 test is to determine the immunity of systems to external ESD events outside the system during operation. IEC 61000-4-2 describes testing using two coupling methods. These are known as contact discharge and air-gap discharge.

Contact discharge implies a direct contact between the discharge gun and the equipment under test (EUT). During air discharge testing, the charged electrode of the discharge gun moves toward the EUT until a discharge occurs as an arc across the air gap. The discharge gun does not make direct contact with the EUT.

A number of factors affect the results and repeatability of the air discharge test, including humidity, temperature, barometric pressure, distance, and rate of approach to the EUT This method is a better representation of an actual ESD event but is not as repeatable. Therefore, contact discharge is the preferred test method.

During testing, the data port is subjected to at least 10 positive and 10 negative single discharges with a one second interval between each pulse. Selection of the test voltage is dependent on the system end environment.

The ADM3095E is robust to IEC 61000-4-2 events and passes the highest level recognized in the standard Level 4, which defines a contact discharge voltage of ±8 kV and an air discharge voltage of ±15 kV.

Figure 33 shows the 8 kV contact discharge current waveform as described in the specification. Some of the key waveform parameters are rise times of less than 1 ns and pulse widths of approximately 60 ns.

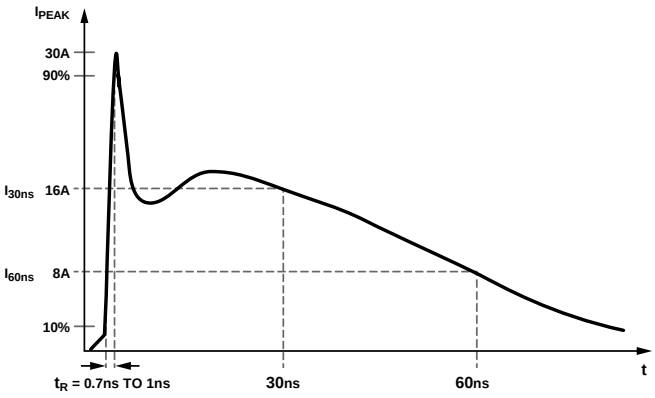


Figure 33. IEC 61000-4-2 ESD Waveform (8 kV)

Figure 16 shows the 8 kV contact discharge current waveform from the IEC 61000-4-2 standard compared to the human body model (HBM) ESD 8 kV waveform. The two standards specify a different waveform shape and peak current. The peak current associated with a IEC 61000-4-2 8 kV pulse is 30 A, while the corresponding peak current for HBM ESD is more than five times less at 5.33 A. The other difference is the rise time of the initial voltage spike, with IEC 61000-4-2 ESD having a much faster rise time of 1 ns, compared to the 10 ns associated with the HBM ESD waveform. The amount of power associated with an IEC 61000-4-2 ESD waveform is much greater than that of an HBM ESD waveform (see Figure 34).

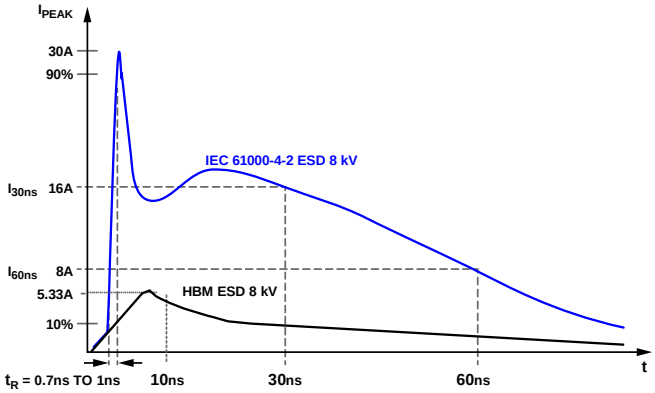


Figure 34. IEC 61000-4-2 ESD Waveform (8 kV) compared to HBM ESD Waveform (8 kV)

These factors combined mean that it is strongly recommended to system designers to choose devices such as the ADM3095E with IEC 61000-4-2 ESD ratings for operation in harsh environments, rather than some competitive devices, which state varying levels of HBM ESD protection. Table 6 summarizes the certified IEC 61000-4-2 ESD test results. Testing was performed in normal transceiver operation, with the ADM3095E clocking data at 2.5 Mbps.

Table 6. IEC 61000-4-2 Certified Test Results

ESD Gun Connected to	IEC 61000-4-2 Test Result	Certified Result
GND	±15 kV (air), ±8 kV (contact), Level 4 protection	Yes

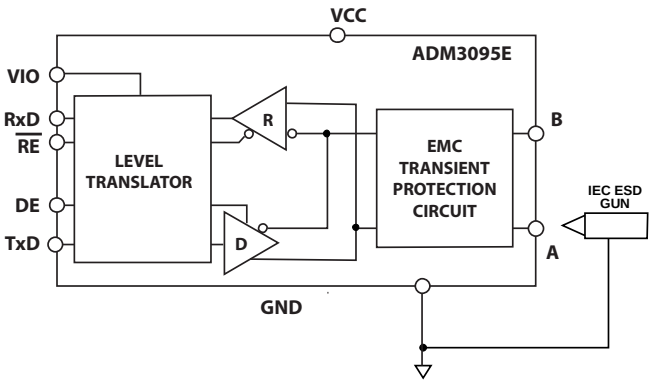


Figure 35. IEC 61000-4-2 ESD Testing Diagram

Electrical Fast Transients (EFT)

Electrical fast transient testing involves coupling a number of extremely fast transient impulses onto the signal lines to represent transient disturbances associated with external switching circuits that are capacitively coupled onto the communication ports, which can include relay and switch contact bounce or transients originating from the switching of inductive or capacitive loads—all of which are very common in industrial environments. The EFT test defined in IEC 61000-4-4 attempts to simulate the interference resulting from these types of events.

Figure 16 shows the EFT 50 Ω load waveform. The EFT waveform is described in terms of a voltage across 50 Ω impedance from a generator with 50 Ω output impedance. The output waveform consists of a 15 ms burst of 2.5 kHz to 5 kHz high voltage transients repeated at 300 ms intervals (see Figure 36). Each individual pulse has a rise time of 5 ns and pulse duration of 50 ns, measured between the 50% point on the rising and falling edges of the waveform.

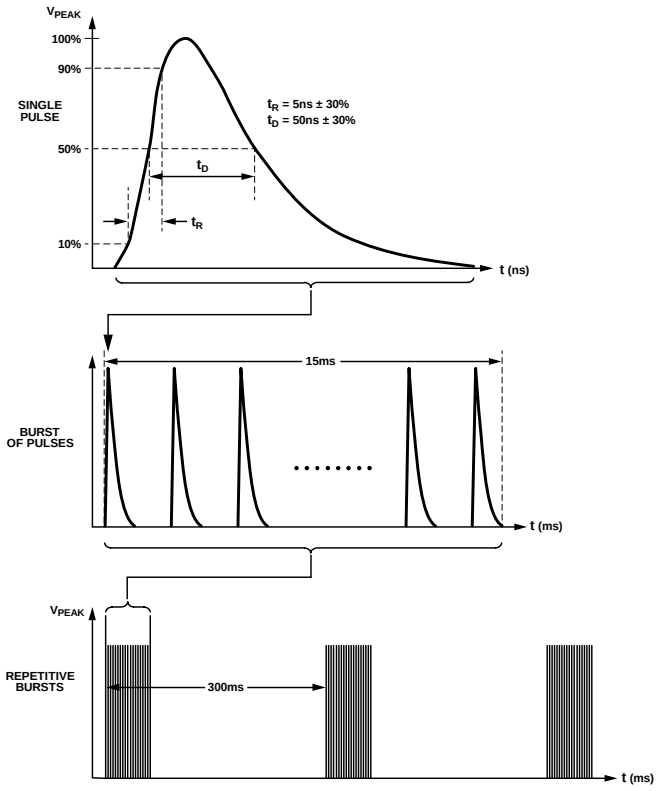


Figure 36. IEC 61000-4-4 EFT 50 Ω Load Waveforms

The total energy in a single EFT pulse is similar to that in an ESD pulse. The total energy in a single pulse is typically 4 mJ.

The ADM3095E is robust to IEC 61000-4-4 events and passes the highest level recognized in the standard Level 4, defining a voltage level of 2 kV.

During testing, these EFT fast burst transients are coupled onto the communication lines using a capacitive clamp. The EFT is capacitively coupled onto the communication lines by the clamp rather than direct contact. This also reduces the loading caused by the low output impedance of the EFT generator. The coupling capacitance between the clamp and cable depends on cable diameter, shielding, and insulation on the cable. Testing was performed in normal transceiver operation, with the ADM3095E clocking data at 2.5 Mbps. Table 7 summarizes the certified test results.

Table 7. IEC 61000-4-4 Certified Test Results

EFT Clamp Connected to	IEC 61000-4-4 Test Result	Certified Result
GND	±2 kV Level 4 protection	Yes

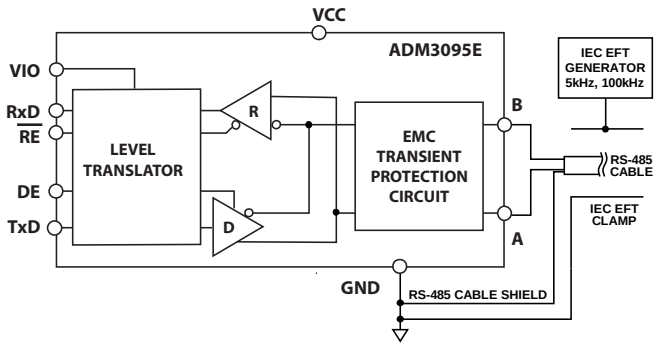


Figure 37. IEC 61000-4-4 EFT Testing Diagram

Surge

Surge transients are caused by overvoltage from switching or lightning transients. Switching transients can result from power system switching, load changes in power distribution systems or various system faults, such as short circuits. Lightning transients can be a result of high currents and voltages injected into the circuit from nearby lightning strikes. IEC 61000-4-5 defines waveforms, test methods, and test levels for evaluating immunity against these destructive surges.

The waveforms are specified as the outputs of a waveform generator in terms of open circuit voltage and short circuit current. Two waveforms are described. The 10 µs/700 µs combination waveform tests ports intended for connection to symmetrical communication lines, for example, telephone exchange lines. The 1.2 µs/50 µs combination waveform generator is used in all other cases, in particular, short distance signal connections. For RS-485 ports, the 1.2 µs/50 µs waveform is predominantly used.. The waveform generator has an effective output impedance of 2 Ω; hence, the surge transient has high currents associated with it.

Figure 17 shows the 1.2 µs/50 µs surge transient waveform. ESD and EFT have similar rise times, pulse widths, and energy levels; however, the surge pulse has a rise time of 1.25 µs and the pulse width is 50 µs (see Figure 38). Additionally, the surge pulse energy can reach almost 90 J, which is three to four orders of magnitude larger than the energy in an ESD or EFT pulse. Therefore, the surge transient is considered the most severe of the EMC transients.

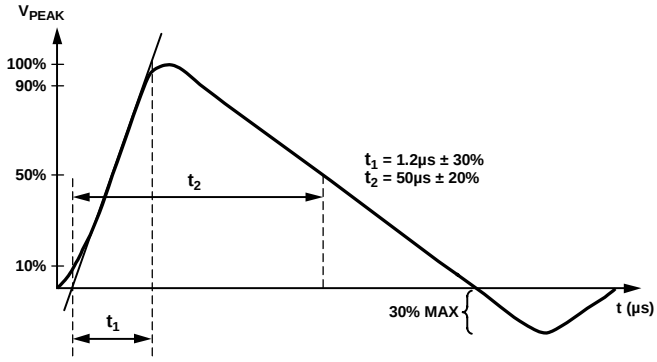


Figure 38. IEC 61000-4-5 Surge 1.2/50 µs Waveform

The ADM3095E is robust to IEC 61000-4-5 events and passes the highest level recognized in the standard Level 4, which defines a peak voltage of 4 kV.

During testing, resistors couple the surge transient onto the communication line. The coupling network for a half-duplex RS-485 device consists of an 80 Ω resistor on both the A and B lines. The total parallel sum of the resistance is 40 Ω. During the surge test, five positive and five negative pulses are applied to the data ports with a maximum time interval of one minute between each pulse. The standard states the device must be set up in normal operating conditions for the duration of the test.

Testing was performed in normal transceiver operation, with the ADM3095E clocking data at 2.5 Mbps. Table 8 summarizes the certified test results.

Table 8. IEC 61000-4-5 Certified Test Results

Surge Generator Connected to	IEC 61000-4-5 Test Result	Certified Result
GND	±4 kV Level 4 protection	Yes

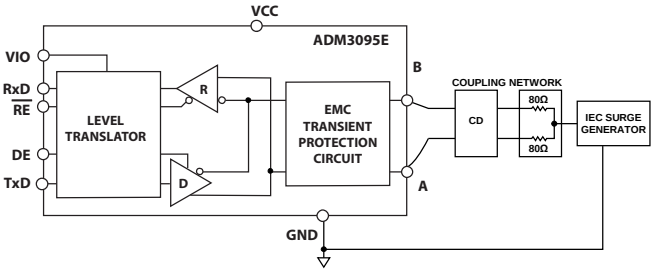


Figure 39. IEC 61000-4-5 Surge Testing Diagram

FULLY RS-485 COMPLIANT OVER AN EXTENDED ±25 V COMMON-MODE RANGE

The ADM3095E is also an RS-485 transceiver that offers an extended common-mode input range of ±25 V across an operating voltage range of 3 V to 5 V, while still meeting or exceeding compliance with the TIA/EIA-845-A standard. These standards specify a bus differential voltage of at least 1.5 V across common-mode range. Additionally, when powered at greater than 4.5 V V_{CC}, the ADM3095E driver output is a minimum 2.1 V V_{OD}, meeting the requirements for a Profibus compliant RS-485 driver.

The extended common-mode input range of ±25 V improves system robustness over long cable lengths, where large differences in ground potential between RS-485 transceivers are possible. The extended common-mode input range of ±25V improves data communication reliability in noisy environments over long cable lengths where ground loop voltages are possible.

1.62 V TO 5.5 V V_{IO} LOGIC SUPPLY

The ADM3095E features a logic supply pin, V_{IO}, for flexible digital interface operational to voltages as low as 1.62 V. The V_{IO} pin powers the logic inputs (TxD input and DE/$\overline{RE}$control pins) and the RxD output.

These pins interface with logic devices such as universal asynchronous receivers/transmitters (UARTs), application-specific integrated circuits (ASICs), and μControllers. Many of these devices use power supplies significantly lower than 5 V.

TRUTH TABLES

V_{IO} supplies DE, TxD, $\overline{RE}$, and RxD interfaces only.

Table 9. Transmitting Truth Table

Supply Status		Inputs[1]		Outputs[1]	
V_{CC}	V_{IO}	DE	TxD	A	B
On	On	H	H	H	L
On	On	H	L	L	H
On	On	L	X	Z	Z
On	Off	H	H	I	I
On	Off	H	L	I	I
On	Off	L	X	I	I
Off	On	X	X	Z	Z
Off	Off	X	X	Z	Z

[1] H means high level; I means indeterminate; L means low level; X means any state; Z means high impedance (off); NC means disconnected.

Table 10. Receiving Truth Table

Supply Status		Inputs[1]		Outputs[1]
V_{CC}	V_{IO}	A – B	$\overline{RE}$	RxD
On	On	>−0.05 V	L	H
On	On	<−0.2 V	L	L
On	Off	>−0.05 V	L	I
On	Off	<−0.2 V	L	I
On	On	−0.2 V < A – B < −0.05 V	L	I
On	Off	−0.2 V < A – B < −0.05 V	L	I
On	On	Inputs open/shorted	L	H
On	Off	Inputs open/shorted	L	I
On	On	X	H	Z
On	Off	X	H	I
Off	Off	X	H	I
Off	Off	X	L or NC	I

[1] H means high level; I means indeterminate; L means low level; X means any state; Z means high impedance (off); NC means disconnected.

RECEIVER FAIL-SAFE

The receiver input includes a fail-safe feature that guarantees a logic high RxD output when the A and B inputs are floating, open-circuited, or shorted. A logic high RxD output is guaranteed in a terminated transmission line with all drivers disabled. This is done by setting the receiver input threshold between −50 mV and −200 mV. If the differential receiver input voltage (A − B) is greater than or equal to −50 mV, RxD is logic high. If A − B is less than or equal to −200 mV, RxD is logic low. In the case of a terminated bus with all transmitters disabled, the receiver differential input voltage is pulled to 0 V by the termination. With the receiver thresholds of the ADM3095E, this results in a logic high with a 50 mV minimum noise margin.

The receiver fail-safe feature (logic high RxD) is also guaranteed under any bus capacitance value, or pull-up resistor configuration on the RxD pin.

RS-485 DATA RATE AND BUS CAPACITANCE

The data rate and bus node capability of the ADM3095E are dependent on the operating temperature of the device. As the operating temperature of the ADM3095E increases, the capacitance of the ADM3095E integrated EMC protection circuitry also increases. The driver output structures of the ADM3095E can be simplified as low pass filter structures, with a given resistance and capacitance. As the operating temperature increases the capacitance increases, so the low pass filter effectively works to decrease the maximum data rate that can be driven on the RS-485 bus pins.

HOT SWAP CAPABILITY

When a circuit board is inserted into a hot (or powered) backplane, differential disturbances to the data bus can lead to data errors. The ADM3095E was lab tested to ensure that the RS-485 A, B bus pins do not output spurious data during a V_{CC} power up/power down event, which simulates a PCB hot insertion. The V_{CC} ramp test rates were 0 V to 5 V in 300 µs (fast ramp rate), and 0 V to 5 V in 9.5 ms (slow ramp rate). For these ramp rates, the RS-485 A and B outputs were monitored and no output glitches were observed.

APPLICATIONS INFORMATION

ROBUST HALF-DUPLEX RS-485 NETWORK

Figure 40 shows a robust RS-485 communications network, with bus communications running over 1000 feet of cabling. Over long cable runs with multiple RS-485 nodes, a number of hazards can either corrupt data communication or even cause permanent damage to the RS-485 interface.

The ADM3095E provides robust protection against high voltage faults to bus power supplies and EMC transients, such as an IEC 61000-4-5 surge. In addition, the ADM3095E has an extended common-mode input range of ±25 V, which allows±25 V of ground potential difference between the GND pins of two or more ADM3095E devices.

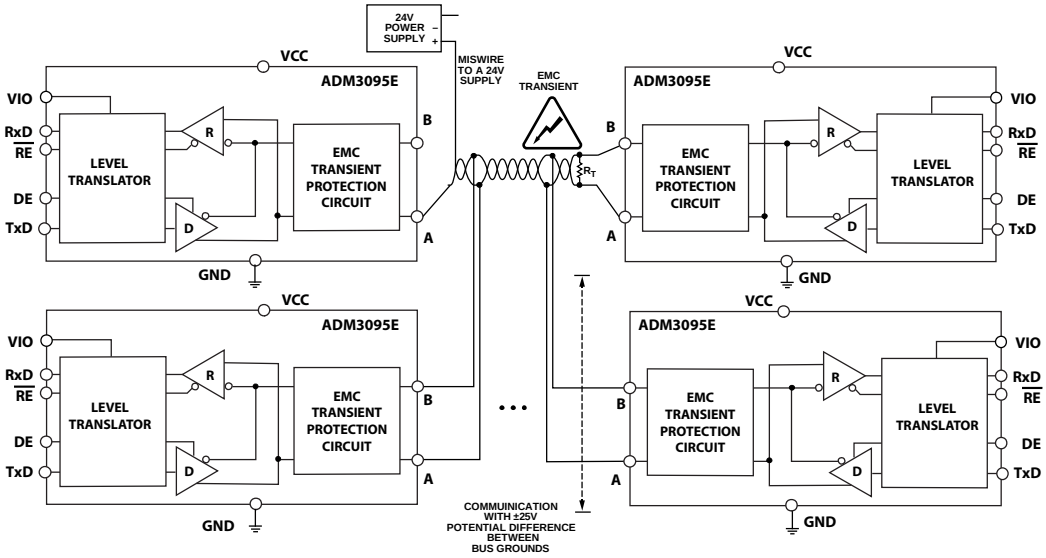
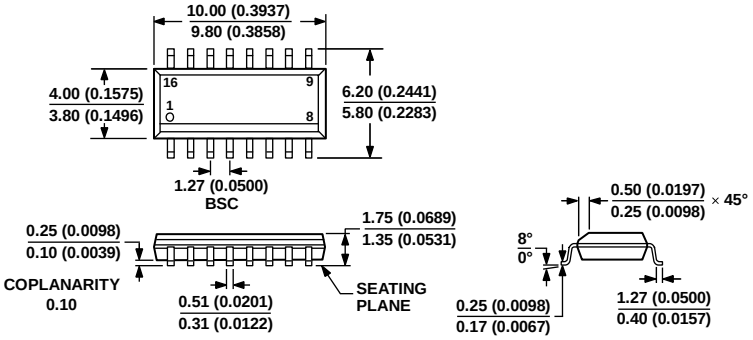


Figure 40. RS-485 Communications Network

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AC

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

060606-A

Figure 41. 16-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-16)
Dimensions shown in millimeters and (inches)

PR14685-0-10/16(PrA)