

DRV8884 1.0-A Stepper Motor Driver With Integrated Current Sense

1 Features

- PWM Microstepping Stepper Motor Driver
 - Up to 1/16 Microstepping
 - Non-Circular and Standard ½ Step Modes
- Integrated Current Sense Functionality
 - No Sense Resistors Required
 - ±6.25% Full-Scale Current Accuracy
- Slow and Mixed Decay Options
- 8.0- to 37-V Operating Supply Voltage Range
- Low $R_{DS(ON)}$: 1.4 Ω HS + LS at 24 V, 25°C
- High Current Capacity
 - 1.0-A Full Scale per Bridge
 - 0.7-A rms per Bridge
- Fixed Off-Time PWM Chopping
- Simple STEP/DIR Interface
- Low-Current Sleep Mode (20 μ A)
- Small Package and Footprint
 - 24 HTSSOP (PowerPAD™)
- Protection Features
 - VM Undervoltage Lockout (UVLO)
 - Charge Pump Undervoltage (CPUV)
 - Overcurrent Protection (OCP)
 - Thermal Shutdown (TSD)
 - Fault Condition Indication Pin (nFAULT)

2 Applications

- Multi-Function Printers and Scanners
- Laser Beam Printers
- 3D Printers
- Automatic Teller and Money Handling Machines
- Video Security Cameras
- Office Automation Machines
- Factory Automation and Robotics

3 Description

The DRV8884 device is a stepper motor driver for industrial equipment applications. The device has two N-channel power MOSFET H-bridge drivers, a microstepping indexer, and integrated current sense. The DRV8884 is capable of driving up to 1.0-A full scale or 0.7-A rms output current (depending on proper PCB ground plane for thermal dissipation and at 24 V and $T_A = 25^\circ\text{C}$).

The DRV8884 integrated current sense functionality eliminates the need for two external sense resistors.

The STEP/DIR pins provide a simple control interface. The device can be configured in full-step up to 1/16 step modes. A low-power sleep mode is provided for very-low quiescent current standby using a dedicated nSLEEP pin.

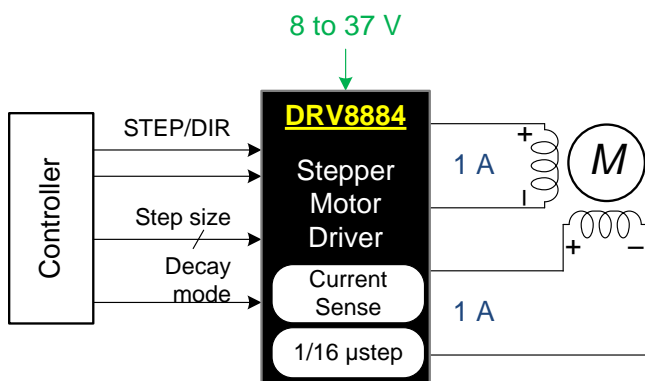
Internal protection functions are provided for undervoltage, charge pump faults, overcurrent, short circuits, and overtemperature. Fault conditions are indicated by an nFAULT pin.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8884	HTSSOP (24)	7.80 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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Microstepping Current Waveform

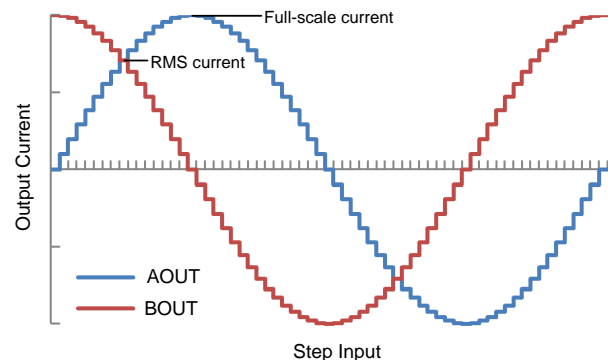


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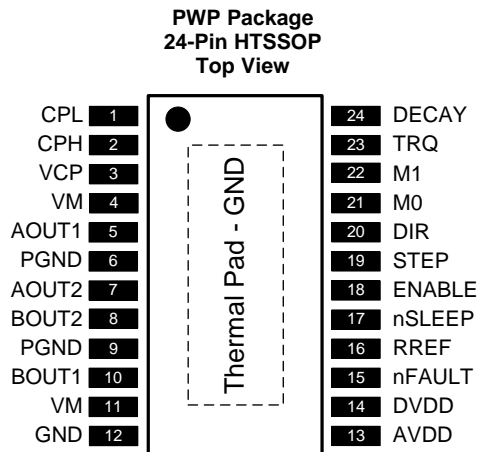
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2016) to Revision B	Page
• Updated R_{PD} and R_{PU} values.....	6
• Fixed chopping current equation	18
• Added "Controlling RREF with a PWM Resource"	18
• Fixed resistance values in tri-level input pin diagram.....	25

Changes from Original (January 2016) to Revision A	Page
• Changed the device status from <i>Product Preview</i> to <i>Production Data</i>	1

5 Pin Configuration and Functions



Pin Functions

PIN		TYPE	DESCRIPTION	
NAME	PWP			
CPL	1	—	Charge pump output	Connect a 0.022- μ F ceramic capacitor rated for VM from CPH to CPL
CPH	2			
VCP	3	O	Charge pump output	Connect a 16-V, 0.22- μ F ceramic capacitor to VM
VM	4	PWR	Power supply	Connect to motor supply voltage; bypass to GND with two 0.01- μ F capacitors (one for each pin) plus a bulk capacitor rated for VM
	11			
AOUT1	5	O	Winding A output	Connect to stepper motor winding
AOUT2	7			
PGND	6	O	Power FET ground	Must be connected to ground
	9			
BOUT2	8	O	Winding B output	Connect to stepper motor winding
BOUT1	10			
GND	12	PWR	Device ground	Must be connected to ground
AVDD	13	—	Internal regulator	Internal supply voltage; bypass to GND with a 6.3-V, 0.47- μ F ceramic capacitor
DVDD	14	—	Internal regulator	Internal supply voltage; bypass to GND with a 6.3-V, 0.47- μ F ceramic capacitor
nFAULT	15	O	Fault indication pin	Pulled logic low with fault condition; open-drain output requires an external pullup
RREF	16	I	Current limit analog input	Connect resistor to ground to set full-scale chopping current
nSLEEP	17	I	Sleep mode input	Logic high to enable device; logic low to enter low-power sleep mode; internal pulldown
ENABLE	18	I	Enable driver input	Logic high to enable device outputs and internal indexer; logic low to disable; internal pulldown
STEP	19	I	Step input	A rising edge causes the indexer to advance one step; internal pulldown
DIR	20	I	Direction input	Logic level sets the direction of stepping; internal pulldown
M0	21	I	Microstepping mode setting pins	Sets the step mode; tri-level pins.set the step mode; internal pulldown
M1	22			
TRQ	23	I	Current scaling control pin	Scales the output current; tri-level pin
DECAY	24	I	Decay mode setting pin	Sets the decay mode; see the Decay Modes section

External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C_{VM}	VM	GND	Two 0.01- μ F ceramic capacitors rated for VM
C_{VM}	VM	GND	Bulk electrolytic capacitor rated for VM
C_{VCP}	VCP	VM	16-V, 0.22- μ F ceramic capacitor
C_{SW}	CPH	CPL	0.022- μ F X7R capacitor rated for VM
C_{AVDD}	AVDD	GND	6.3-V, 0.47- μ F ceramic capacitor
C_{DVDD}	DVDD	GND	6.3-V, 0.47- μ F ceramic capacitor
R_{nFAULT}	VCC ⁽¹⁾	nFAULT	>4.7 k Ω
R_{REF}	RREF	GND	Resistor to limit chopping current must be installed. See the <i>Typical Application</i> section for value selection.

- (1) VCC is not a pin on the DRV8884, but a VCC supply voltage pullup is required for open-drain output nFAULT; nFAULT may be pulled up to DVDD

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

	MIN	MAX	UNIT
Power supply voltage (VM)	-0.3	40	V
Power supply voltage ramp rate (VM)	0	2	V/ μ s
Charge pump voltage (VCP, CPH)	-0.3	VM + 7	V
Charge pump negative switching pin (CPL)	-0.3	VM	V
Internal regulator voltage (DVDD)	-0.3	3.8	V
Internal regulator current output (DVDD)	0	1	mA
Internal regulator voltage (AVDD)	-0.3	5.7	V
Control pin voltage (STEP, DIR, ENABLE, nFAULT, M0, M1, DECAY, TRQ, nSLEEP)	-0.3	5.7	V
Open drain output current (nFAULT)	0	10	mA
Current limit input pin voltage (RREF)	-0.3	6.0	V
Continuous phase node pin voltage (AOUT1, AOUT2, BOUT1, BOUT2)	-0.7	VM + 0.7	V
Peak drive current (AOUT1, AOUT2, BOUT1, BOUT2)		1.7	A
Operating junction temperature, T_J	-40	150	$^{\circ}$ C
Storage temperature, T_{stg}	-65	150	$^{\circ}$ C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

	VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	\pm 2000
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	\pm 500

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
VM	Power supply voltage	8	37	V
VCC	Logic level input voltage	0	5.3	V
f_{PWM}	Applied STEP signal (STEP)	0	100 ⁽¹⁾	kHz
I_{DVDD}	DVDD external load current	0	1 ⁽²⁾	mA
I_{FS}	Motor full scale current	0	1.0	A
I_{rms}	Motor rms current	0	0.7	A
T_A	Operating ambient temperature	-40	125	°C

(1) STEP input can operate up to 500 kHz, but system bandwidth is limited by the motor load

(2) Power dissipation and thermal limits must be observed

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾	DRV8884	UNIT	
	PWP (HTSSOP)		
	24 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	36.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	18.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	15.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (VM, DVDD, AVDD)						
V _{VM}	VM operating voltage		8		37	V
I _{VM}	VM operating supply current	VM ≈ 8 to 35 V, ENABLE = 1, nSLEEP = 1, No motor load		5	8	mA
I _{VMQ}	VM sleep mode supply current	nSLEEP = 0; T _A = 25°C			20	μA
		nSLEEP = 0; T _A = 125°C ⁽¹⁾			40	
t _{SLEEP}	Sleep time	nSLEEP = 0 to sleep-mode		50	200	μs
t _{WAKE}	Wake-up time	nSLEEP = 1 to output transition		0.85	1.5	ms
t _{ON}	Turn-on time	VM > UVLO to output transition		0.85	1.5	ms
V _{DVDD}	Internal regulator voltage	0- to 1-mA external load	2.9	3.3	3.6	V
V _{AVDD}	Internal regulator voltage	No external load	4.5	5.0	5.5	V
CHARGE PUMP (VCP, CPH, CPL)						
V _{VCP}	VCP operating voltage	VM > 8 V		VM + 5.5		V
LOGIC-LEVEL INPUTS (STEP, DIR, ENABLE, nSLEEP, M1)						
V _{IL}	Input logic low voltage		0		0.8	V
V _{IH}	Input logic high voltage		1.6		5.3	V
V _{HYS}	Input logic hysteresis		100			mV
I _{IL}	Input logic low current	V _{IN} = 0 V	-1		1	μA
I _{IH}	Input logic high current	V _{IN} = 5.0 V			100	μA
R _{PD}	Pulldown resistance	To GND		100		kΩ
t _{PD}	Propagation delay	STEP to current change			1.2	μs
TRI-LEVEL INPUT (M0, TRQ)						
V _{IL}	Tri-level input logic low voltage		0		0.65	V
V _{IZ}	Tri-level input Hi-Z voltage			1.1		V
V _{IH}	Tri-level input logic high voltage		1.5		5.3	V
I _{IL}	Tri-level input logic low current	V _{IN} = 0 V	-80			μA
I _{IZ}	Tri-level input Hi-Z current	V _{IN} = 1.3 V	-5		5	μA
I _{IH}	Tri-level input logic high current	V _{IN} = 5.0 V			155	μA
R _{PD}	Tri-level pulldown resistance	To GND	18	32	50	kΩ
R _{PU}	Tri-level pullup resistance	To DVDD	30	60	90	kΩ
QUAD-LEVEL INPUT (DECAY)						
V _{I1}	Quad-level input voltage 1	5% resistor 5 kΩ to GND	0.07	0.11	0.13	V
V _{I2}	Quad-level input voltage 2	5% resistor 15 kΩ to GND	0.24	0.32	0.40	V
V _{I3}	Quad-level input voltage 3	5% resistor 45 kΩ to GND	0.71	0.97	1.20	V
V _{I4}	Quad-level input voltage 4	5% resistor 135 kΩ to GND	2.12	2.90	3.76	V
I _O	Output current	To GND	14	22	30	μA
CONTROL OUTPUTS (nFAULT)						
V _{OL}	Output logic low voltage	I _O = 1 mA, R _{PULLUP} = 4.7 kΩ			0.5	V
I _{OH}	Output logic high leakage	V _O = 5.0 V, R _{PULLUP} = 4.7 kΩ	-1		+1	μA

(1) Not tested in production; limits are based on characterization data

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MOTOR DRIVER OUTPUTS (AOUT1, AOUT2, BOUT1, BOUT2)						
R _{DS(ON)}	High-side FET on resistance	VM = 24 V, I = 1 A, T _A = 25°C		716	798	mΩ
R _{DS(ON)}	Low-side FET on resistance	VM = 24 V, I = 1 A, T _A = 25°C		684	749	mΩ
t _{RISE} ⁽²⁾	Output rise time			100		ns
t _{FALL} ⁽²⁾	Output fall time			100		ns
t _{DEAD} ⁽²⁾	Output dead time			200		ns
V _d ⁽²⁾	Body diode forward voltage	I _{OUT} = 0.5 A		0.7	1.0	V
PWM CURRENT CONTROL (RREF)						
A _{RREF}	RREF transimpedance gain		28.1	30	31.9	kAΩ
V _{RREF}	RREF voltage	RREF = 27 to 132 kΩ	1.18	1.232	1.28	V
t _{OFF}	PWM off-time			20		μs
C _{RREF}	Equivalent capacitance on RREF				10	pF
t _{BLANK}	PWM blanking time	I _{RREF} = 1.0 A, 63% to 100% current setting		1.5		μs
		I _{RREF} = 1.0 A, 0% to 63% current setting		1.0		
ΔI _{TRIP}	Current trip accuracy	I _{RREF} = 1.0 A, 10% to 20% current setting, 1% reference resistor	-25%		25%	
		I _{RREF} = 1.0 A, 20% to 63% current setting, 1% reference resistor	-12.5%		12.5%	
		I _{RREF} = 1.0 A, 71% to 100% current setting, 1% reference resistor	-6.25%		6.25%	
PROTECTION CIRCUITS						
V _{UVLO}	VM UVLO	VM falling; UVLO report			7.8	V
		VM rising; UVLO recovery			8.0	
V _{UVLO,HYS}	Undervoltage hysteresis	Rising to falling threshold		100		mV
V _{CPUV}	Charge pump undervoltage	VCP falling; CPUV report		VM + 2.0		V
I _{OCP}	Overcurrent protection trip level	Current through any FET	1.7			A
t _{OCP}	Overcurrent deglitch time		1.3	1.9	2.8	μs
t _{RETRY}	Overcurrent retry time		1		1.6	ms
T _{TSD} ⁽²⁾	Thermal shutdown temperature	Die temperature T _J	150			°C
T _{HYS} ⁽²⁾	Thermal shutdown hysteresis	Die temperature T _J		20		°C

(2) Not tested in production; limits are based on characterization data

6.6 Indexer Timing Requirements

$T_A = 25^\circ\text{C}$, over recommended operating conditions unless otherwise noted

NO.			MIN	MAX	UNIT
1	f_{STEP}	Step frequency		500 ⁽¹⁾	kHz
2	$t_{\text{WH}}(\text{STEP})$	Pulse duration, STEP high	970		ns
3	$t_{\text{WL}}(\text{STEP})$	Pulse duration, STEP low	970		ns
4	$t_{\text{SU}}(\text{DIR, Mx})$	Setup time, DIR or USMx to STEP rising	200		ns
5	$t_{\text{H}}(\text{DIR, Mx})$	Hold time, DIR or USMx to STEP rising	200		ns

(1) STEP input can operate up to 500 kHz, but system bandwidth is limited by the motor load

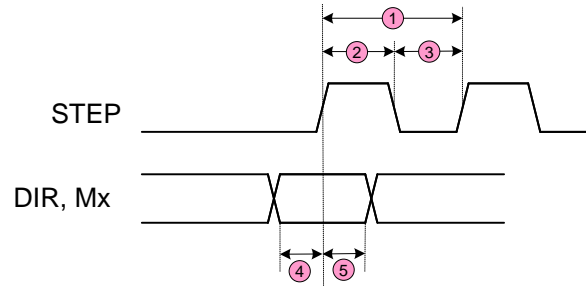


Figure 1. Timing Diagram

6.7 Typical Characteristics

Over recommended operating conditions (unless otherwise noted)

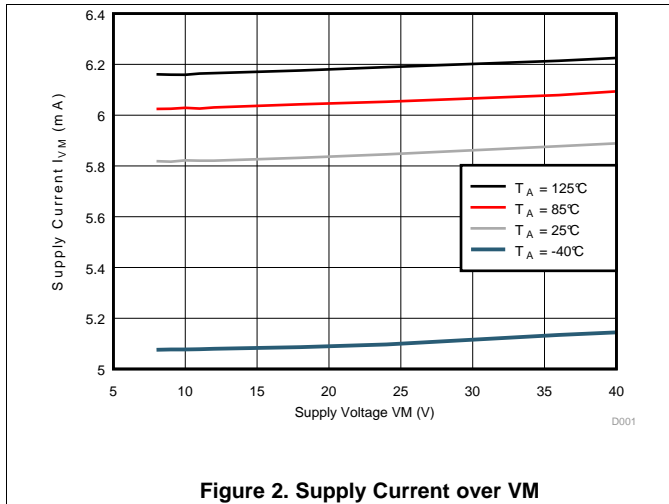


Figure 2. Supply Current over VM

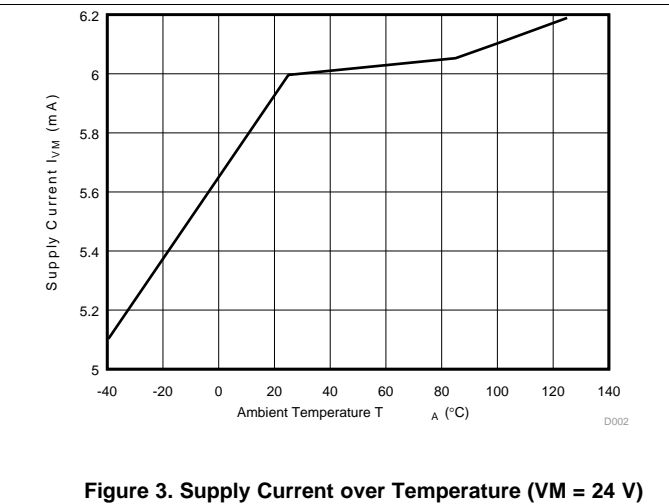


Figure 3. Supply Current over Temperature (VM = 24 V)

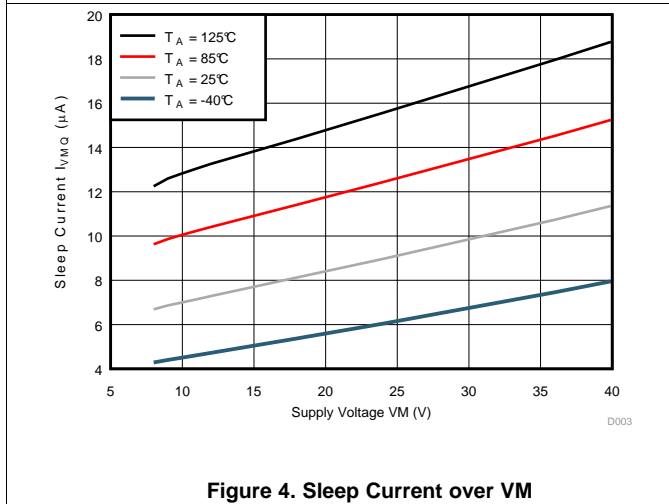


Figure 4. Sleep Current over VM

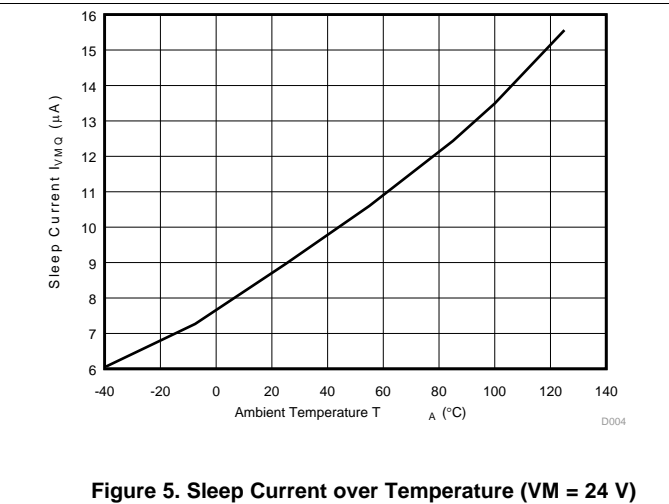


Figure 5. Sleep Current over Temperature (VM = 24 V)

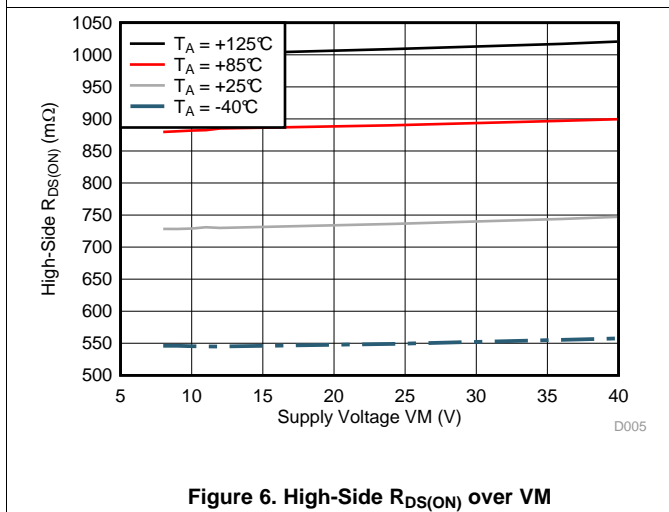


Figure 6. High-Side $R_{DS(ON)}$ over VM

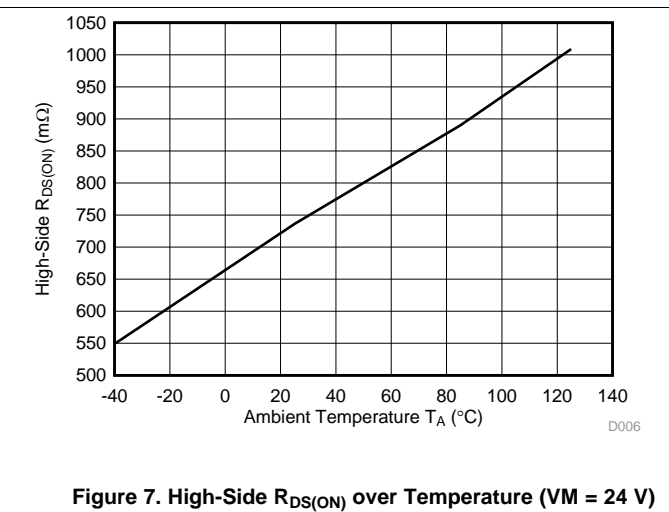
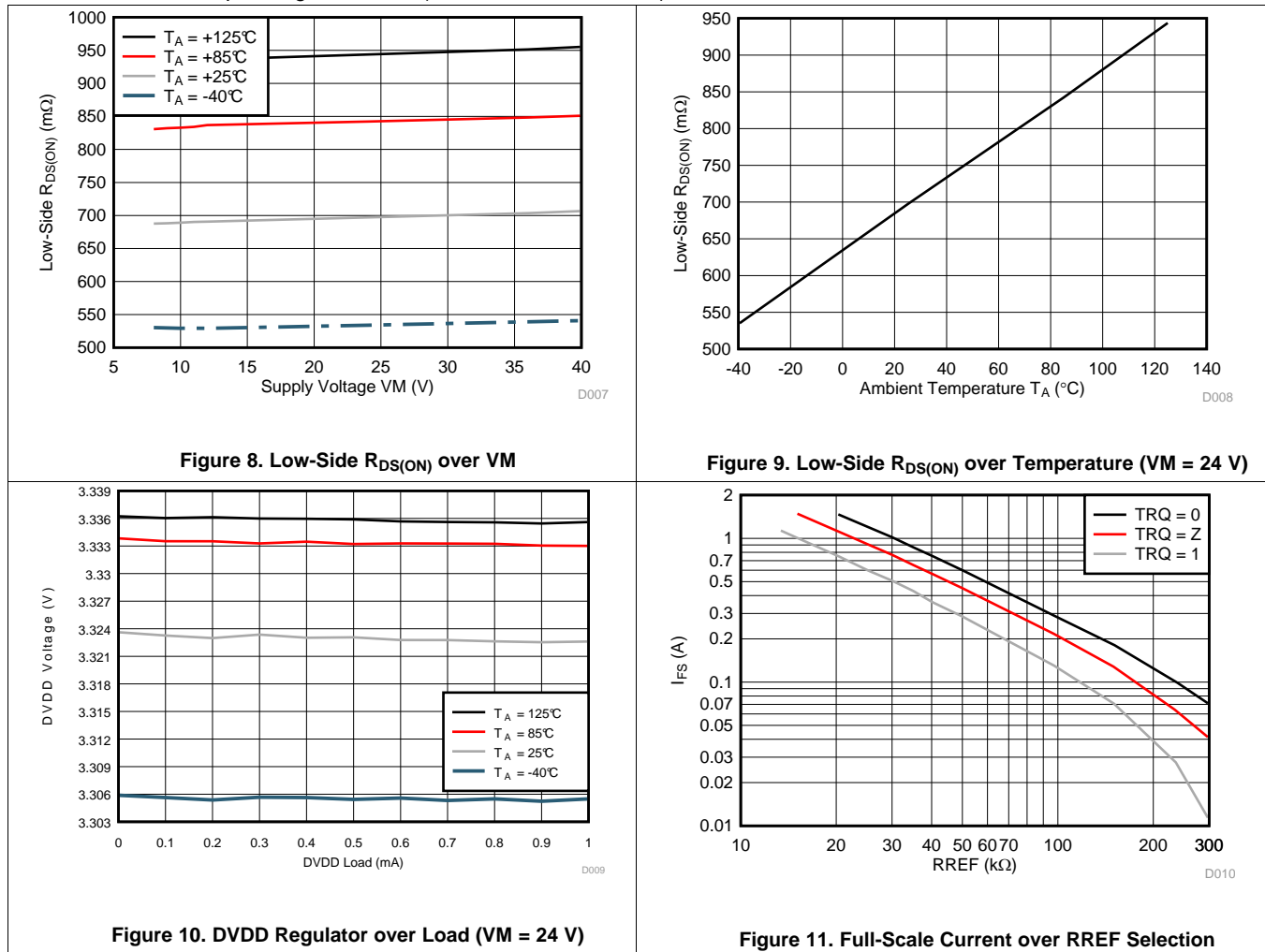


Figure 7. High-Side $R_{DS(ON)}$ over Temperature (VM = 24 V)

Typical Characteristics (continued)

Over recommended operating conditions (unless otherwise noted)



7 Detailed Description

7.1 Overview

The DRV8884 is an integrated motor driver solution for bipolar stepper motors. The device integrates two NMOS H-bridges, integrated current sense and regulation circuitry, and a microstepping indexer. The DRV8884 can be powered with a supply voltage between 8 and 37 V, and is capable of providing an output current with up to 1.7-A peak, 1.0-A full-scale, or 0.7-A rms. Actual full-scale and rms current depends on ambient temperature, supply voltage, and PCB ground plane size.

The DRV8884 integrates current sense functionality, which eliminates the need for high-power external sense resistors. This integration does not dissipate the external sense resistor power, because the current sense functionality is not implemented using a resistor-based architecture. This functionality helps improve component cost, board size, PCB layout, and system power consumption.

A simple STEP/DIR interface allows easy interfacing to the controller circuit. The internal indexer is able to execute high-accuracy microstepping without requiring the processor to control the current level. The indexer is capable of full step and half step as well as microstepping to 1/4, 1/8, and 1/16. In addition to the standard half-stepping mode, a non-circular 1/2-stepping mode is available for increased torque output at higher motor rpm.

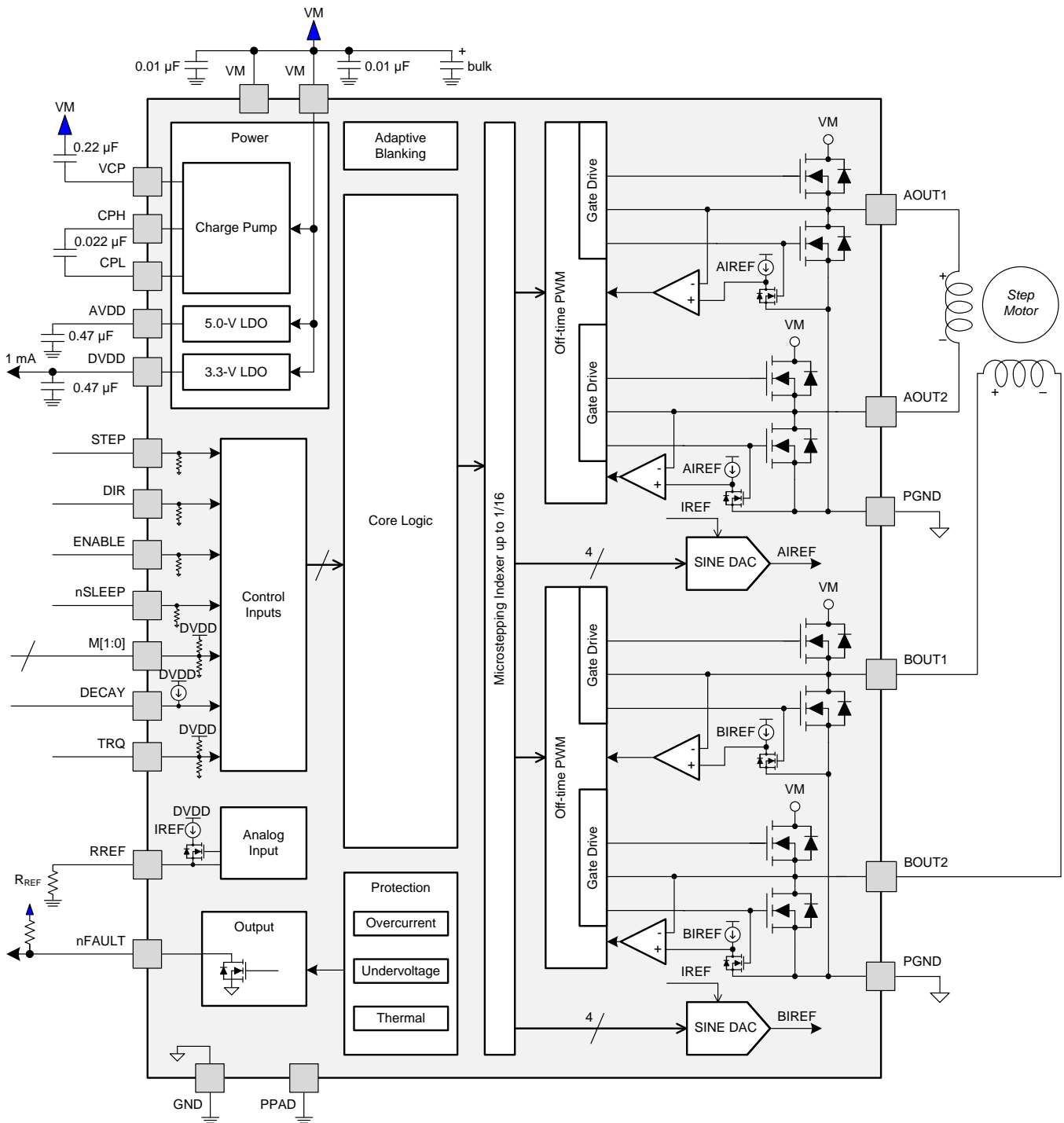
The current regulation is configurable with several decay modes of operation. The decay mode can be selected as a fixed slow, slow/mixed, or mixed decay. The slow/mixed decay mode uses slow decay on increasing steps and mixed decay on decreasing steps.

An adaptive blanking time feature automatically scales the minimum drive time with output current. This helps alleviate zero-crossing distortion by limiting the drive time at low-current steps.

A torque DAC feature allows the controller to scale the output current without needing to scale the reference resistor. The torque DAC is accessed using a digital input pin. This allows the controller to save power by decreasing the current consumption when not high current is not required.

A low-power sleep mode is included that allows the system to save power when not driving the motor.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Stepper Motor Driver Current Ratings

Stepper motor drivers can be classified using three different numbers to describe the output current: peak, rms, and full-scale.

7.3.1.1 Peak Current Rating

The peak current in a stepper driver is limited by the overcurrent protection trip threshold, I_{OCP} . The peak current describes any transient duration current pulse, for example when charging capacitance, when the overall duty cycle is very low. In general, the minimum value of I_{OCP} specifies the peak current rating of the stepper motor driver. For the DRV8884, the peak current rating is 1.7 A per bridge.

7.3.1.2 RMS Current Rating

The rms (average) current is determined by the thermal considerations of the IC. The rms current is calculated based on the $R_{DS(ON)}$, rise and fall time, PWM frequency, device quiescent current, and package thermal performance in a typical system at 25°C. The real operating rms current may be higher or lower depending on heatsinking and ambient temperature. For the DRV8884, the rms current rating is 0.7 A per bridge.

7.3.1.3 Full-Scale Current Rating

The full-scale current describes the top of the sinusoid current waveform while microstepping. Because the sinusoid amplitude is related to the rms current, the full-scale current is also determined by the thermal considerations of the IC. The full-scale current rating is approximately $\sqrt{2} \times I_{rms}$. The full-scale current is set by VREF, the sense resistor, and torque DAC when configuring the DRV8884 (see [Current Regulation](#) for details). For the DRV8884, the full-scale current rating is 1.0 A per bridge.

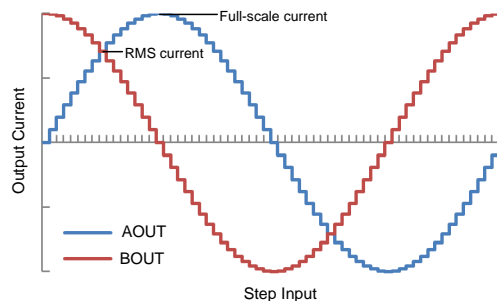


Figure 12. Full-Scale and rms Current

Feature Description (continued)

7.3.2 PWM Motor Drivers

The DRV8884 contains drivers for two full H-bridges. [Figure 13](#) shows a block diagram of the circuitry.

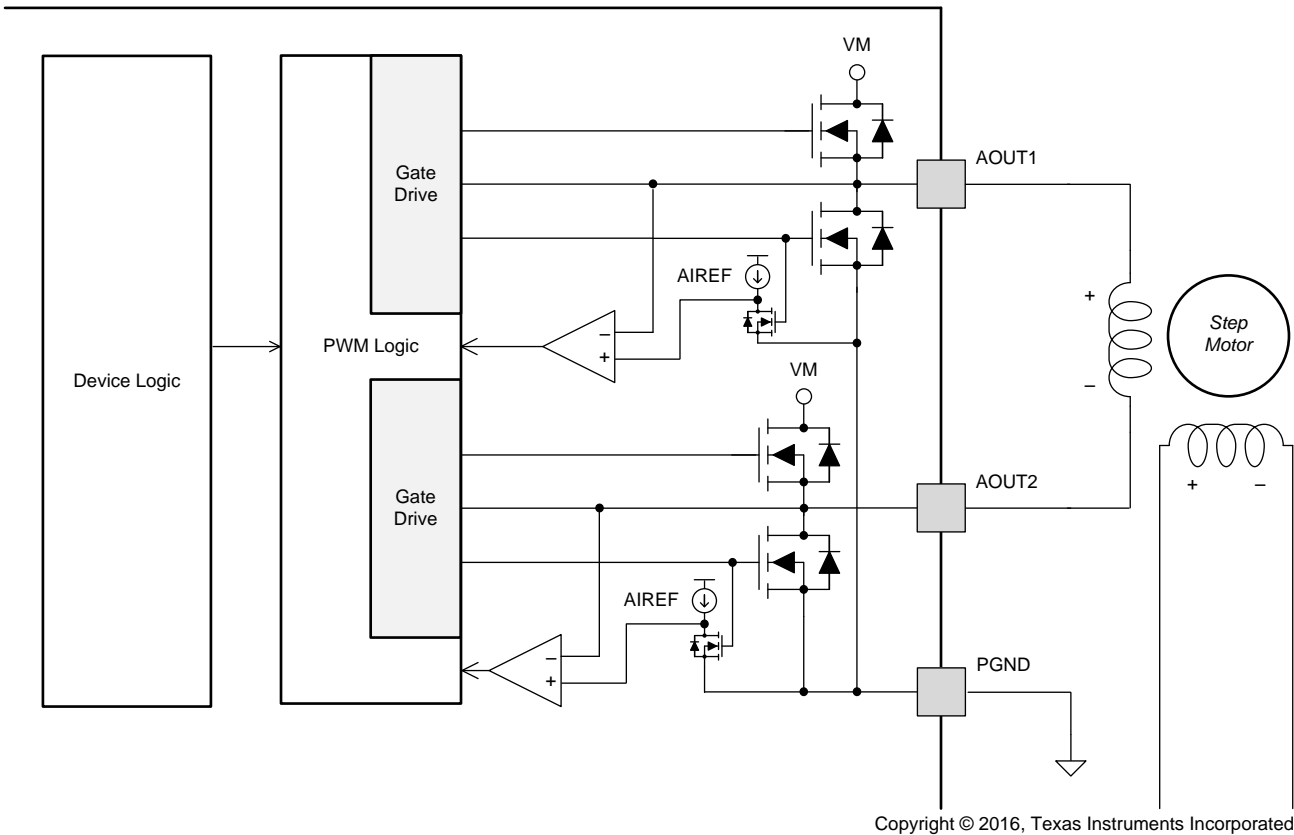


Figure 13. PWM Motor Driver Block Diagram

7.3.3 Microstepping Indexer

Built-in indexer logic in the DRV8884 allows a number of different stepping configurations. The Mx pins are used to configure the stepping format as shown in [Table 1](#).

Table 1. Microstepping Settings

M1	M0	STEP MODE
0	0	Full step (2-phase excitation) with 71% current
0	1	1/16 step
1	0	1/2 step
1	1	1/4 step
0	Z	1/8 step
1	Z	Non-circular 1/2 step

[Table 2](#) shows the relative current and step directions for full-step through 1/16-step operation. The AOUT current is the sine of the electrical angle; BOUT current is the cosine of the electrical angle. Positive current is defined as current flowing from xOUT1 to xOUT2 while driving.

At each rising edge of the STEP input the indexer travels to the next state in the table (see [Table 2](#)). The direction is shown with the DIR pin logic high. If the DIR pin is logic low, the sequence is reversed.

On power-up or when exiting sleep mode, keep the STEP pin logic low, otherwise the indexer will advance one step.

Note that if the step mode is changed from full, 1/2, 1/4, 1/8, or 1/16 to full, 1/2, 1/4, 1/8, or 1/16 while stepping, the indexer will advance to the next valid state for the new MODE setting at the rising edge of STEP. If the step mode is changed from or to non-circular 1/2 step, the indexer will immediately go to the valid state for that mode.

The home state is an electrical angle of 45°. This state is entered after power-up, after exiting logic undervoltage lockout (UVLO), or after exiting sleep mode. [Table 2](#) shows this state with the cells outlined in red.

Table 2. Microstepping Relative Current per Step (DIR = 1)

FULL STEP	1/2 STEP	1/4 STEP	1/8 STEP	1/16 STEP	ELECTRICAL ANGLE (DEGREES)	AOUT CURRENT (% FULL-SCALE)	BOUT CURRENT (% FULL-SCALE)
	1	1	1	1	0.000°	0%	100%
				2	5.625°	10%	100%
			2	3	11.250°	20%	98%
				4	16.875°	29%	96%
		2	3	5	22.500°	38%	92%
				6	28.125°	47%	88%
			4	7	33.750°	56%	83%
				8	39.375°	63%	77%
1	2	3	5	9	45.000°	71%	71%
				10	50.625°	77%	63%
			6	11	56.250°	83%	56%
				12	61.875°	88%	47%
		4	7	13	67.500°	92%	38%
				14	73.125°	96%	29%
			8	15	78.750°	98%	20%
				16	84.375°	100%	10%
	3	5	9	17	90.000°	100%	0%
				18	95.625°	100%	-10%
			10	19	101.250°	98%	-20%
				20	106.875°	96%	-29%
		6	11	21	112.500°	92%	-38%
				22	118.125°	88%	-47%
			12	23	123.750°	83%	-56%
				24	129.375°	77%	-63%
2	4	7	13	25	135.000°	71%	-71%
				26	140.625°	63%	-77%
			14	27	146.250°	56%	-83%
				28	151.875°	47%	-88%
		8	15	29	157.500°	38%	-92%
				30	163.125°	29%	-96%
			16	31	168.750°	20%	-98%
				32	174.375°	10%	-100%
	5	9	17	33	180.000°	0%	-100%
				34	185.625°	-10%	-100%
			18	35	191.250°	-20%	-98%
				36	196.875°	-29%	-96%
		10	19	37	202.500°	-38%	-92%
				38	208.125°	-47%	-88%
			20	39	213.750°	-56%	-83%
				40	219.375°	-63%	-77%

Table 2. Microstepping Relative Current per Step (DIR = 1) (continued)

FULL STEP	1/2 STEP	1/4 STEP	1/8 STEP	1/16 STEP	ELECTRICAL ANGLE (DEGREES)	AOUT CURRENT (% FULL-SCALE)	BOUT CURRENT (% FULL-SCALE)
3	6	11	21	41	225.000°	-71%	-71%
				42	230.625°	-77%	-63%
			22	43	236.250°	-83%	-56%
				44	241.875°	-88%	-47%
		12	23	45	247.500°	-92%	-38%
				46	253.125°	-96%	-29%
			24	47	258.750°	-98%	-20%
				48	264.375°	-100%	-10%
	7	13	25	49	270.000°	-100%	0%
				50	275.625°	-100%	10%
			26	51	281.250°	-98%	20%
				52	286.875°	-96%	29%
		14	27	53	292.500°	-92%	38%
				54	298.125°	-88%	47%
			28	55	303.750°	-83%	56%
				56	309.375°	-77%	63%
4	8	15	29	57	315.000°	-71%	71%
				58	320.625°	-63%	77%
			30	59	326.250°	-56%	83%
				60	331.875°	-47%	88%
		16	31	61	337.500°	-38%	92%
				62	343.125°	-29%	96%
			32	63	348.750°	-20%	98%
				64	354.375°	-10%	100%
	1	1	1	1	360.000°	0%	100%

Non-circular 1/2-step operation is shown in [Table 3](#). This stepping mode consumes more power than circular 1/2-step operation, but provides a higher torque at high motor rpm.

Table 3. Non-Circular 1/2-Stepping Current

NON-CIRCULAR 1/2 STEP	AOUT CURRENT (% FULL-SCALE)	BOUT CURRENT (% FULL-SCALE)	ELECTRICAL ANGLE (°)
1	0	100	0
2	100	100	45
3	100	0	90
4	100	-100	135
5	0	-100	180
6	-100	-100	225
7	-100	0	270
8	-100	100	315

7.3.4 Current Regulation

The current through the motor windings is regulated by an adjustable fixed-off-time PWM current regulation circuit. When an H-bridge is enabled, current rises through the winding at a rate dependent on the DC voltage, inductance of the winding, and the magnitude of the back EMF present. After the current hits the current chopping threshold, the bridge enters a decay mode for a fixed 20-μs period of time to decrease the current. After the off time expires, the bridge is re-enabled, starting another PWM cycle.

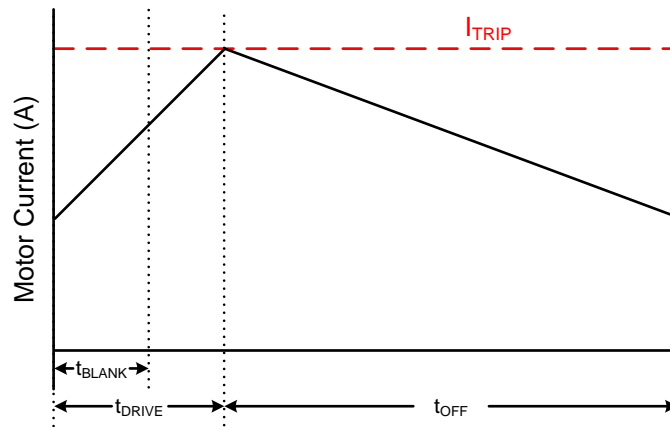


Figure 14. Current Chopping Waveform

The PWM chopping current is set by a comparator which looks at the voltage across current sense FETs in parallel with the low-side drivers. The current sense FETs are biased with a reference current that is the output of a current-mode sine-weighted DAC whose full-scale reference current is set by the current through the RREF pin. An external resistor is placed from the RREF pin to GND in order to set the reference current. In addition, the TRQ pin can further scale the reference current.

The chopping current is calculated as shown in Equation 1.

$$I_{FS} \text{ (A)} = \frac{A_{RREF} \text{ (k}\Omega\text{)}}{RREF \text{ (k}\Omega\text{)}} \times \text{TRQ (\%)} = \frac{30 \text{ (k}\Omega\text{)}}{RREF \text{ (k}\Omega\text{)}} \times \text{TRQ (\%)} \quad (1)$$

Example: If a 30-kΩ resistor is connected to the RREF pin, the chopping current will be 1 A (TRQ at 100%).

The TRQ pin is the input to a DAC used to scale the output current. The current scalar value for different inputs is shown in Table 4.

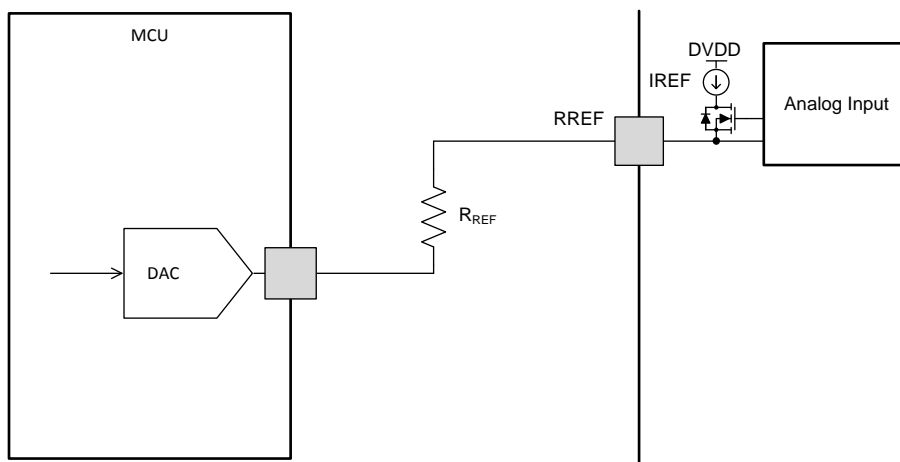
Table 4. Torque DAC Settings

TRQ	CURRENT SCALAR (TRQ)
0	100%
Z	75%
1	50%

7.3.5 Controlling RREF With an MCU DAC

In some cases, the full-scale output current may need to be changed on the fly between many different values, depending on motor speed and loading. The RREF pin reference current can be adjusted in system by tying the RREF resistor to a DAC output instead of GND.

In this mode of operation, as the DAC voltage increases, the reference current will decrease, and therefore, the full-scale current will decrease as well. For proper operation, the output of the DAC should not rise above V_{RREF} .



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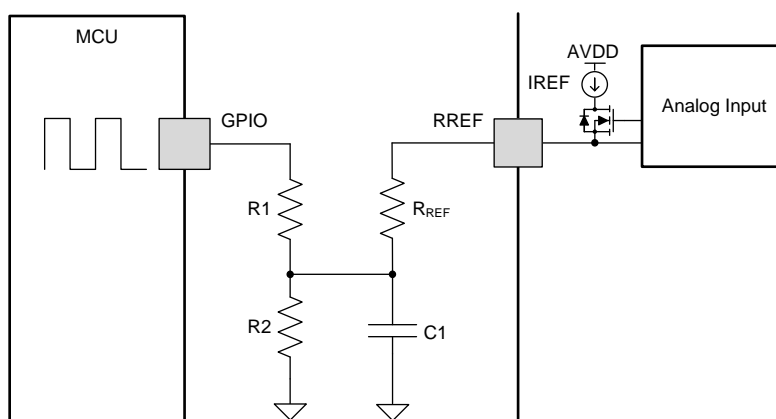
Figure 15. Controlling RREF With a DAC

The chopping current as controlled by a DAC is calculated as in [Equation 2](#).

$$I_{FS} (A) = \frac{A_{RREF} (k\Omega) \times [V_{RREF} (V) - V_{DAC} (V)]}{V_{RREF} (V) \times R_{REF} (k\Omega)} \times TRQ (\%) \quad (2)$$

Example: If a 20-k Ω resistor is connected from the RREF pin to the DAC, and the DAC is outputting 0.74 V, the chopping current will be 600 mA (TRQ at 100%).

RREF can also be adjusted using a PWM signal and low-pass filter.



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Figure 16. Controlling RREF with a PWM Resource

7.3.6 Decay Modes

The DRV8884 decay mode is selected by setting the quad-level DECAY pin to the voltage range in [Table 5](#).

Table 5. Decay Mode Settings

DECAY	INCREASING STEPS	DECREASING STEPS
100 mV Can be tied to ground	Slow decay	Mixed decay: 30% fast
300 mV, 15 kΩ to GND	Mixed decay: 30% fast	Mixed decay: 30% fast
1.0 V, 45 kΩ to GND	Mixed decay: 60% fast	Mixed decay: 60% fast
2.9 V Can be tied to DVDD	Slow decay	Slow decay

Increasing and decreasing current are defined in [Figure 17](#). For the slow/mixed decay mode, the decay mode is set as slow during increasing current steps and mixed decay during decreasing current steps. In full-step mode, the decreasing steps decay mode is always used.

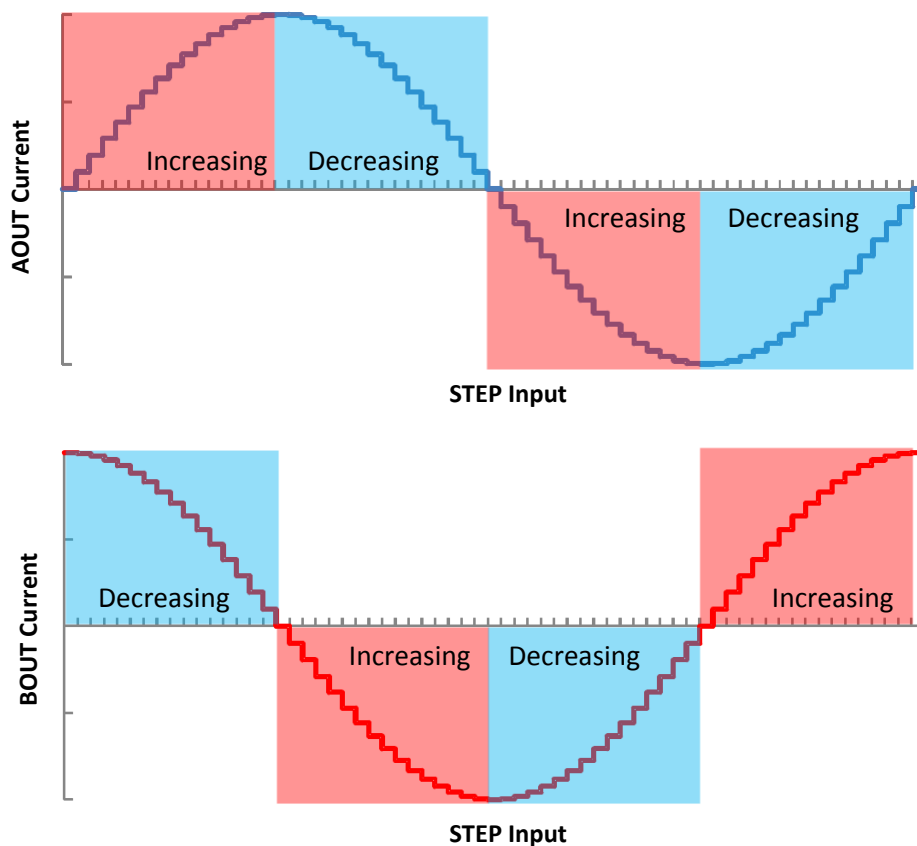
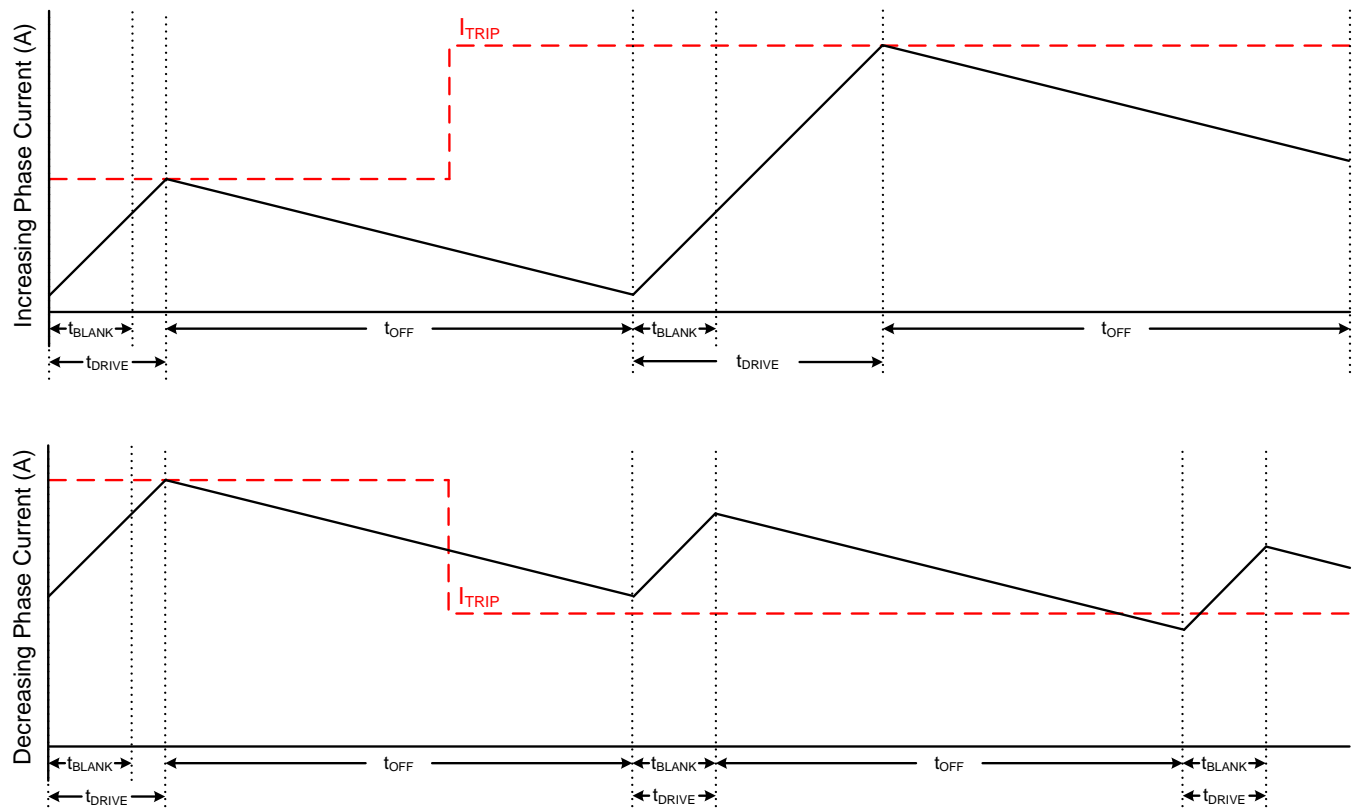


Figure 17. Definition of Increasing and Decreasing Steps

7.3.6.1 Mode 1: Slow Decay for Increasing and Decreasing Current

Figure 18. Slow/Slow Decay Mode

During slow decay, both of the low-side FETs of the H-bridge are turned on, allowing the current to be recirculated.

Slow decay exhibits the least current ripple of the decay modes for a given t_{OFF} . However, on decreasing current steps, slow decay takes a long time to settle to the new I_{TRIP} level because the current decreases very slowly.

7.3.6.2 Mode 2: Slow Decay for Increasing Current, Mixed Decay for Decreasing Current

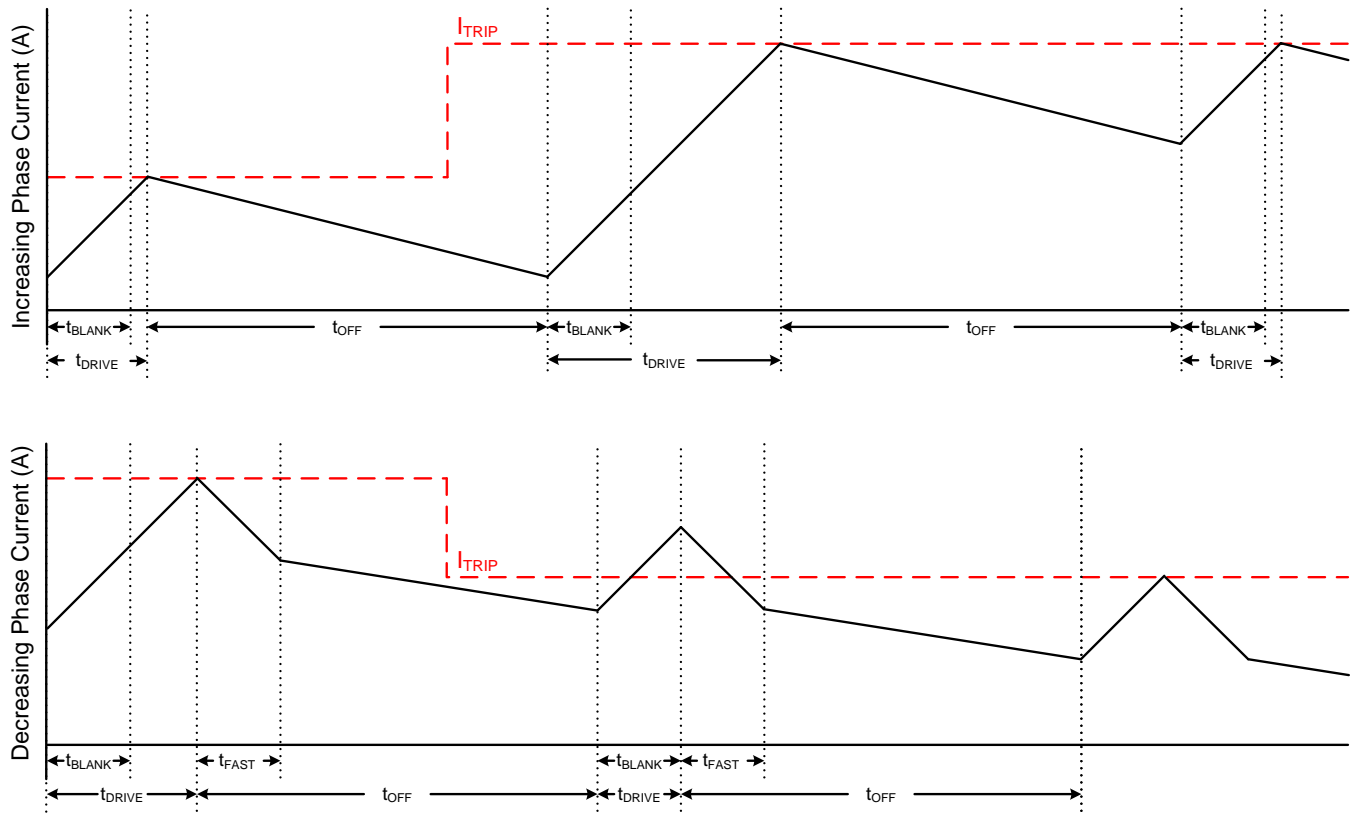


Figure 19. Slow/Mixed Decay Mode

Mixed decay begins as fast decay for a time, followed by slow decay for the remainder of t_{OFF} . In this mode, mixed decay only occurs during decreasing current. Slow decay is used for increasing current.

This mode exhibits the same current ripple as slow decay for increasing current, since for increasing current, only slow decay is used. For decreasing current, the ripple is larger than slow decay, but smaller than fast decay. On decreasing current steps, mixed decay settles to the new I_{TRIP} level faster than slow decay.

7.3.6.3 Mode 3: Mixed Decay for Increasing and Decreasing Current

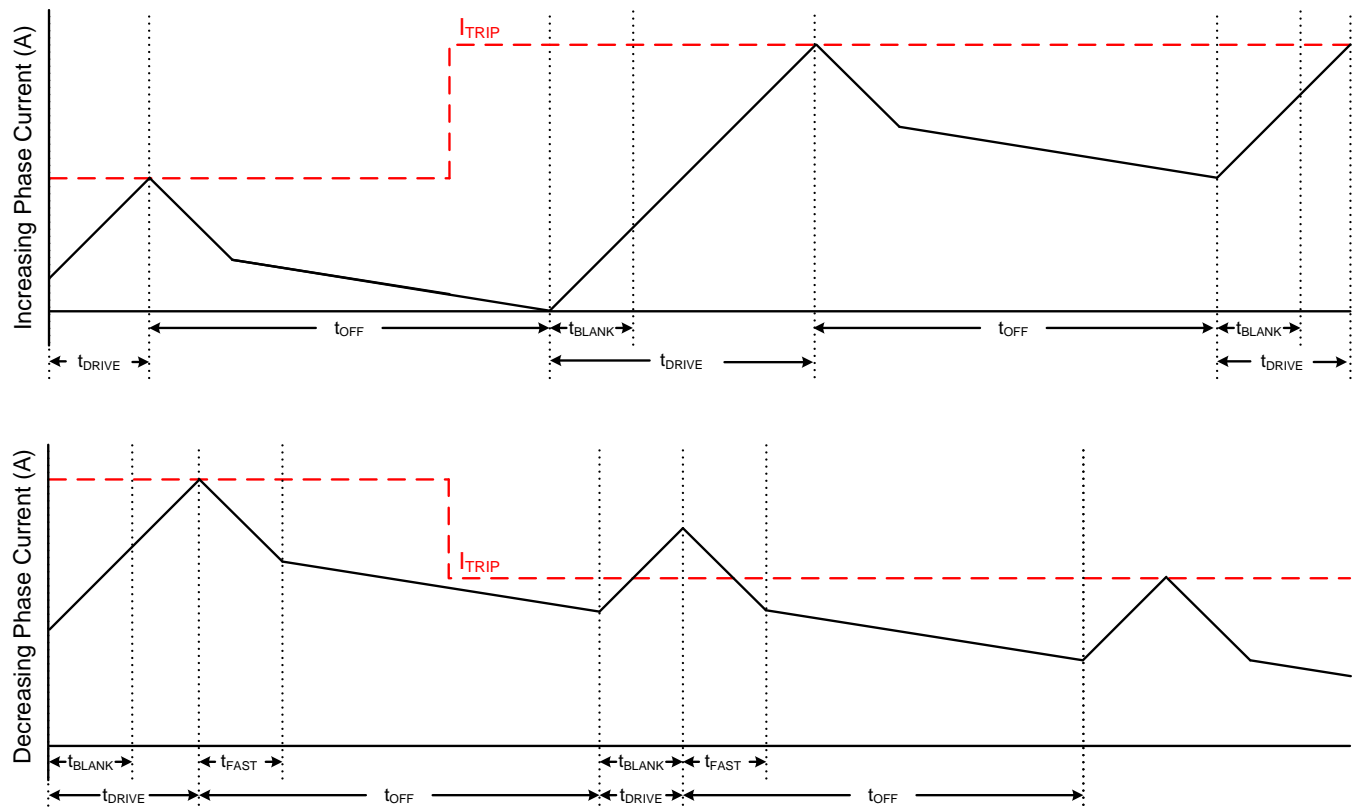


Figure 20. Mixed/Mixed Decay Mode

Mixed decay begins as fast decay for a time, followed by slow decay for the remainder of t_{OFF} . In this mode, mixed decay occurs for both increasing and decreasing current steps.

This mode exhibits ripple larger than slow decay, but smaller than fast decay. On decreasing current steps, mixed decay settles to the new I_{TRIP} level faster than slow decay.

In cases where current is held for a long time (no input in the STEP pin) or at very low stepping speeds, slow decay may not properly regulate current because no back-EMF is present across the motor windings. In this state, motor current can rise very quickly, and requires an excessively large off-time. Increasing/decreasing mixed decay mode allows the current level to stay in regulation when no back-EMF is present across the motor windings.

7.3.7 Blanking Time

After the current is enabled in an H-bridge, the current sense comparator is ignored for a period of time (t_{BLANK}) before enabling the current sense circuitry. Note that the blanking time also sets the minimum drive time of the PWM. Table 6 shows the blanking time based on the sine table index and the torque DAC setting. Note that the torque DAC index is not the same as one step as given in Table 2.

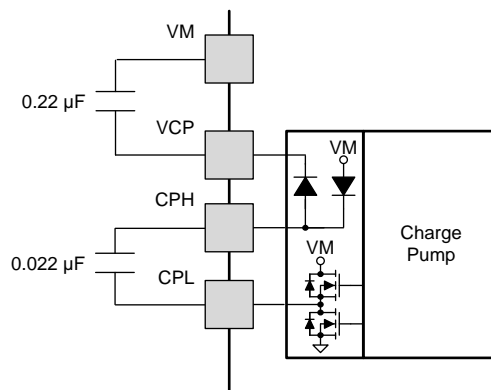
Table 6. Adaptive Blanking Time over Torque DAC and Microsteps

$t_{blank} = 1.5 \mu s$ $t_{blank} = 1.0 \mu s$

SINE INDEX	TORQUE DAC (TRQ)		
	100%	75%	50%
16	100%	75%	50%
15	98%	73.5	49%
14	96%	72%	48%
13	92%	69%	46%
12	88%	66%	44%
11	83%	62.3%	41.5%
10	77%	57.8%	38.5%
9	71%	53.3%	35.5%
8	63%	47.3%	31.5%
7	56%	42%	28%
6	47%	35.3	23.5%
5	38%	28.5	19%
4	29%	21.8%	14.5%
3	20%	15%	10%
2	10%	7.5%	5%
1	0%	0%	0%

7.3.8 Charge Pump

A charge pump is integrated in order to supply a high-side NMOS gate drive voltage. The charge pump requires a capacitor between the VM and VCP pins. Additionally, a low-ESR ceramic capacitor is required between pins CPH and CPL.



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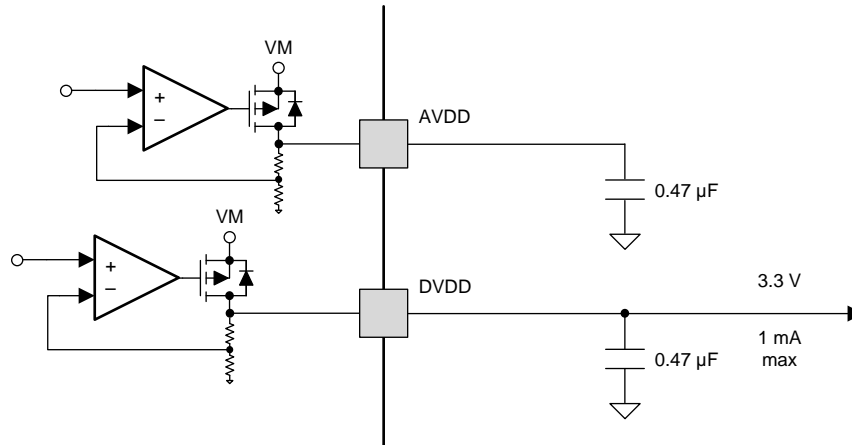
Figure 21. Charge Pump Diagram

7.3.9 LDO Voltage Regulator

An LDO regulator is integrated into the DRV8884. DVDD can be used to provide a reference voltage. For proper operation, bypass DVDD to GND using a ceramic capacitor.

The DVDD output is nominally 3.3 V. When the DVDD LDO current load exceeds 1 mA, the output voltage drops significantly.

The AVDD pin also requires a bypass capacitor to GND. This LDO is for DRV8884 internal use only.



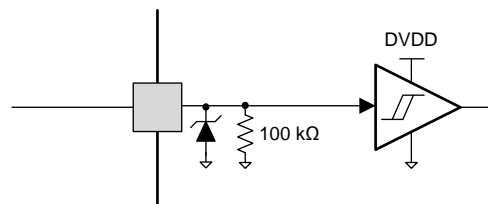
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Figure 22. LDO Diagram

If a digital input needs to be tied permanently high (that is, Mx, DECAY, or TRQ), it is preferable to tie the input to DVDD instead of an external regulator. This saves power when VM is not applied or in sleep mode; DVDD is disabled and current will not be flowing through the input pull-down resistors. For reference, logic level inputs have a typical pull-down of 100 kΩ, and tri-level inputs have a typical pull-down of 60 kΩ.

7.3.10 Logic and Multi-Level Pin Diagrams

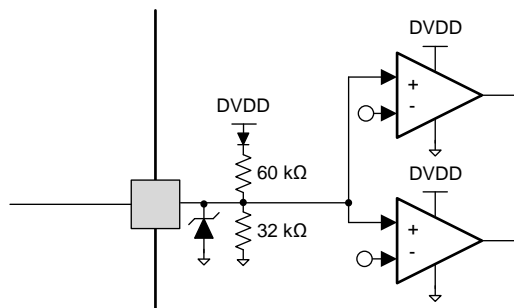
Figure 23 gives the input structure for logic-level pins STEP, DIR, ENABLE, nSLEEP, and M1.



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Figure 23. Logic-level Input Pin Diagram

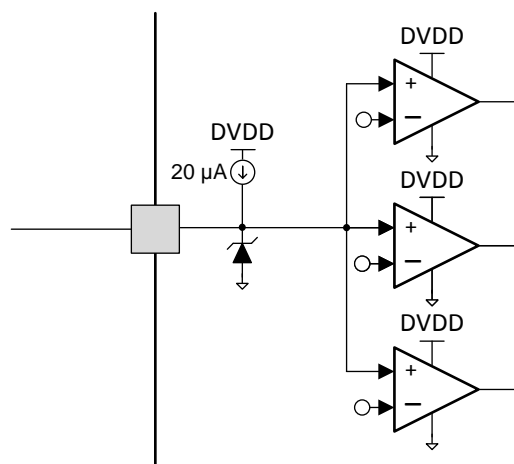
Tri-level logic pins M0 and TRQ have the following structure shown in Figure 24.



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Figure 24. Tri-level Input Pin Diagram

Quad-level logic pin DECAY has the following structure shown in [Figure 25](#).



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Figure 25. Quad-level Input Pin Diagram

7.3.11 Protection Circuits

The DRV8884 is fully protected against undervoltage, charge pump undervoltage, overcurrent, and overtemperature events.

7.3.11.1 VM UVLO

If at any time the voltage on the VM pin falls below the VM UVLO threshold voltage (V_{UVLO}), all FETs in the H-bridge will be disabled, the charge pump will be disabled, the logic will be reset, the DVDD regulator is disabled, and the nFAULT pin will be driven low. Operation resumes when VM rises above the UVLO threshold. The nFAULT pin is released after operation has resumed. Decreasing VM below this undervoltage threshold will reset the indexer position.

7.3.11.2 VCP Undervoltage Lockout (CPUV)

If at any time the voltage on the VCP pin falls below the charge pump UVLO threshold voltage, all FETs in the H-bridge will be disabled and the nFAULT pin will be driven low. Operation resumes when VCP rises above the CPUV threshold. The nFAULT pin is released after operation has resumed.

7.3.11.3 Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than t_{OCP} , all FETs in the H-bridge will be disabled and nFAULT will be driven low.

The driver is re-enabled after the OCP retry period (t_{RETRY}) has passed. nFAULT becomes high again after the retry time. If the fault condition is still present, the cycle repeats. If the fault is no longer present, normal operation resumes and nFAULT remains deasserted.

7.3.11.4 Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge will be disabled and the nFAULT pin will be driven low. After the die temperature has fallen to a safe level, operation automatically resumes. The nFAULT pin is released after operation has resumed.

Table 7. Fault Condition Summary

FAULT	CONDITION	ERROR REPORT	H-BRIDGE	CHARGE PUMP	INDEXER	DVDD	RECOVERY
VM undervoltage (UVLO)	$VM < V_{UVLO}$ (max 7.8 V)	nFAULT	Disabled	Disabled	Disabled	Disabled	$VM > V_{UVLO}$ (max 8.0 V)
VCP undervoltage (CPUV)	$VCP < V_{CPUV}$ (typ VM + 2.0 V)	nFAULT	Disabled	Operating	Operating	Operating	$VCP > V_{CPUV}$ (typ VM + 2.7 V)
Overcurrent (OCP)	$I_{OUT} > I_{OCP}$ (min 1.7 A)	nFAULT	Disabled	Operating	Operating	Operating	t_{RETRY}
Thermal Shutdown (TSD)	$T_J > T_{TSD}$ (min 150°C)	nFAULT	Disabled	Operating	Operating	Operating	$T_J < T_{TSD} - T_{HYS}$ (T_{HYS} typ 20°C)

7.4 Device Functional Modes

The DRV8884 is active unless the nSLEEP pin is brought logic low. In sleep mode, the charge pump is disabled, the H-bridge FETs are disabled Hi-Z, and the V3P3 regulator is disabled. Note that t_{SLEEP} must elapse after a falling edge on the nSLEEP pin before the device is in sleep mode. The DRV8884 is brought out of sleep mode automatically if nSLEEP is brought logic high. Note that t_{WAKE} must elapse before the outputs change state after wake-up.

TI recommends to keep the STEP pin logic low when coming out of nSLEEP or when applying power.

If the ENABLE pin is brought logic low, the H-bridge outputs are disabled, but the internal logic will still be active. A rising edge on STEP will advance the indexer, but the outputs will not change state until ENABLE is deasserted.

Table 8. Functional Modes Summary

	CONDITION	H-BRIDGE	CHARGE PUMP	INDEXER	V3P3
Operating	$8\text{ V} < VM < 40\text{ V}$ nSLEEP pin = 1 ENABLE pin = 1	Operating	Operating	Operating	Operating
Disabled	$8\text{ V} < VM < 40\text{ V}$ nSLEEP pin = 1 ENABLE pin = 0	Disabled	Operating	Operating	Operating
Sleep mode	$8\text{ V} < VM < 40\text{ V}$ nSLEEP pin = 0	Disabled	Disabled	Disabled	Disabled
Fault encountered	VM undervoltage (UVLO)	Disabled	Disabled	Disabled	Disabled
	VCP undervoltage (CPUV)	Disabled	Operating	Operating	Operating
	Overcurrent (OCP)	Disabled	Operating	Operating	Operating
	Thermal shutdown (TSD)	Disabled	Operating	Operating	Operating

8 Application and Implementation

NOTE

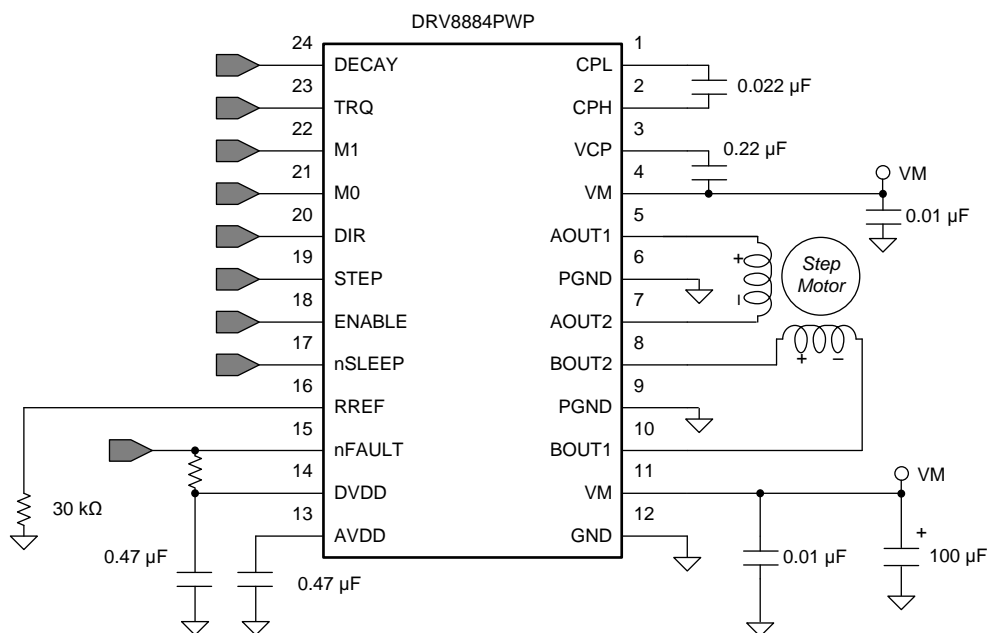
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8884 is used in bipolar stepper control.

8.2 Typical Application

The following design procedure can be used to configure the DRV8884.



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Figure 26. Typical Application Schematic

8.2.1 Design Requirements

Table 9 gives design input parameters for system design.

Table 9. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply voltage	VM	24 V
Motor winding resistance	R_L	2.6 Ω /phase
Motor winding inductance	L_L	1.4 mH/phase
Motor full step angle	θ_{step}	1.8°/step
Target microstepping level	n_m	1/8 step
Target motor speed	v	120 rpm
Target full-scale current	I_{FS}	1.0 A

8.2.2 Detailed Design Procedure

8.2.2.1 Stepper Motor Speed

The first step in configuring the DRV8884 requires the desired motor speed and microstepping level. If the target application requires a constant speed, then a square wave with frequency f_{step} must be applied to the STEP pin.

If the target motor speed is too high, the motor will not spin. Make sure that the motor can support the target speed.

For a desired motor speed (v), microstepping level (n_m), and motor full step angle (θ_{step}),

$$f_{\text{step}} \text{ (steps / s)} = \frac{v \text{ (rpm)} \times 360 \text{ (}^\circ \text{ / rot)}}{\theta_{\text{step}} \text{ (}^\circ \text{ / step)} \times n_m \text{ (steps / microstep)} \times 60 \text{ (s / min)}} \quad (3)$$

θ_{step} can be found in the stepper motor data sheet, or written on the motor itself.

For the DRV8884, the microstepping level is set by the Mx pins and can be any of the settings in [Table 10](#). Higher microstepping will mean a smoother motor motion and less audible noise, but will increase switching losses and require a higher f_{step} to achieve the same motor speed.

Table 10. Microstepping Indexer Settings

M1	M0	STEP MODE
0	0	Full step (2-phase excitation) with 71% current
0	1	1/16 step
1	0	1/2 step
1	1	1/4 step
0	Z	1/8 step
1	Z	Non-circular 1/2 step

Example: Target 120 rpm at 1/8 microstep mode. The motor is 1.8°/step

$$f_{\text{step}} \text{ (steps / s)} = \frac{120 \text{ rpm} \times 360^\circ \text{ / rot}}{1.8^\circ \text{ / step} \times 1/8 \text{ steps / microstep} \times 60 \text{ s / min}} = 3.2 \text{ kHz} \quad (4)$$

8.2.2.2 Current Regulation

In a stepper motor, the full-scale current (I_{FS}) is the maximum current driven through either winding. This quantity will depend on the RREF resistor and the TRQ setting. During stepping, I_{FS} defines the current chopping threshold (I_{TRIP}) for the maximum current step.

$$I_{\text{FS}} \text{ (A)} = \frac{A_{\text{RREF}} \text{ (k}\Omega\text{)}}{R_{\text{REF}} \text{ (k}\Omega\text{)}} = \frac{30 \text{ (k}\Omega\text{)} \times \text{TRQ}\%}{R_{\text{REF}} \text{ (k}\Omega\text{)}} \quad (5)$$

Note that I_{FS} must also follow [Equation 6](#) in order to avoid saturating the motor. VM is the motor supply voltage, and R_L is the motor winding resistance.

$$I_{\text{FS}} \text{ (A)} < \frac{VM \text{ (V)}}{R_L \text{ (}\Omega\text{)} + 2 \times R_{\text{DS(ON)}} \text{ (}\Omega\text{)}} \quad (6)$$

8.2.2.3 Decay Modes

The DRV8884 supports three different decay modes: slow decay, slow/mixed and all mixed decay. The current through the motor windings is regulated using an adjustable fixed-time-off scheme. This means that after any drive phase, when a motor winding current has hit the current chopping threshold (I_{TRIP}), the DRV8884 will place the winding in one of the three decay modes for t_{OFF} . After t_{OFF} , a new drive phase starts.

The blanking time t_{BLANK} defines the minimum drive time for the PWM current chopping. I_{TRIP} is ignored during t_{BLANK} , so the winding current may overshoot the trip level.

8.2.3 Application Curves

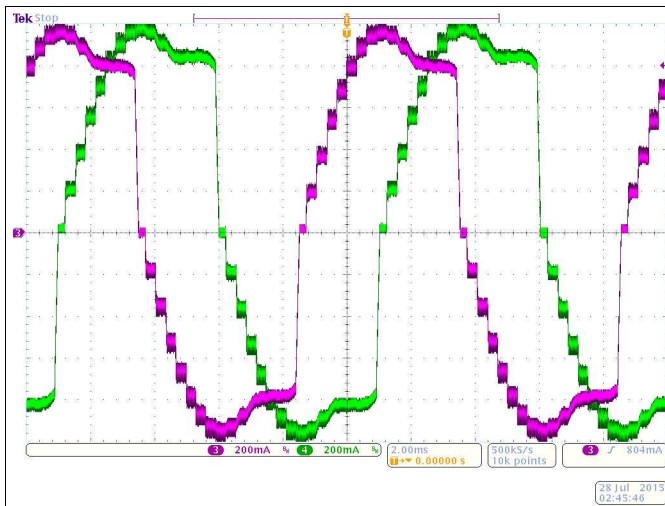


Figure 27. Microstepping Using Slow Decay on Increasing and Decreasing Steps; Current Loses Regulation on Falling Steps

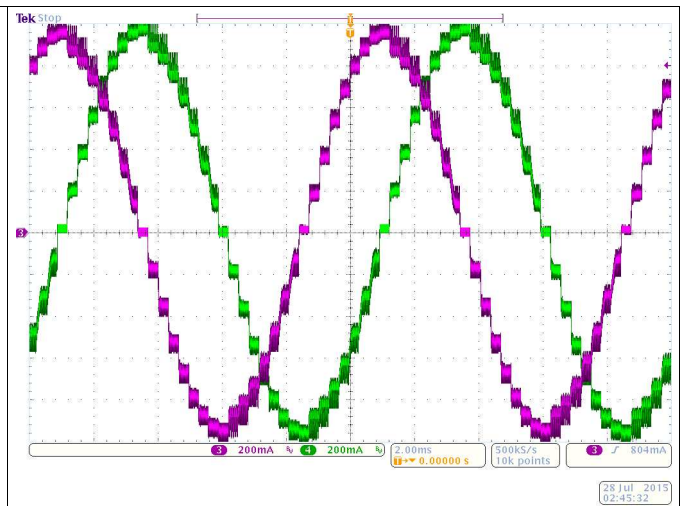


Figure 28. Microstepping Using Slow Decay on Increasing Steps and Mixed 30% Fast Decay on Decreasing Steps

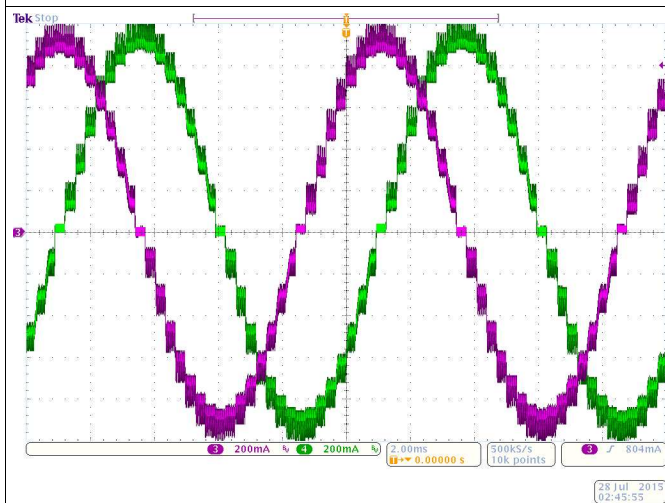


Figure 29. Microstepping Using Mixed 30% Fast Decay on Increasing and Decreasing Steps

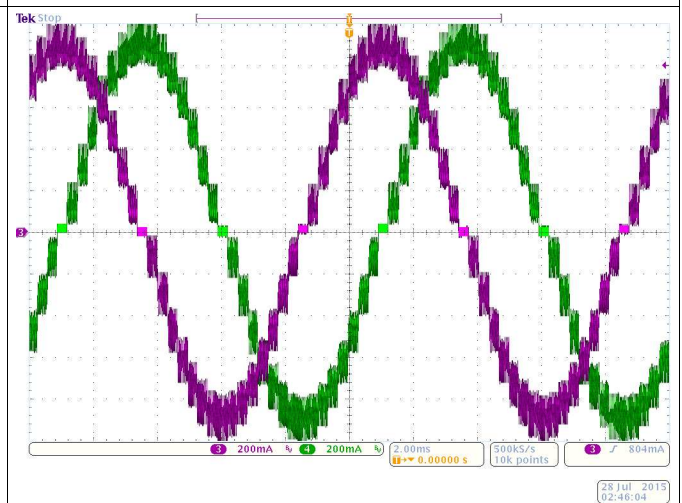


Figure 30. Microstepping Using Mixed 60% Fast Decay on Increasing and Decreasing Steps

9 Power Supply Recommendations

The DRV8884 is designed to operate from an input voltage supply (VM) range between 8 and 35 V. A 0.01- μF ceramic capacitor rated for VM must be placed at each VM pin as close to the DRV8884 as possible. In addition, a bulk capacitor must be included on VM.

9.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

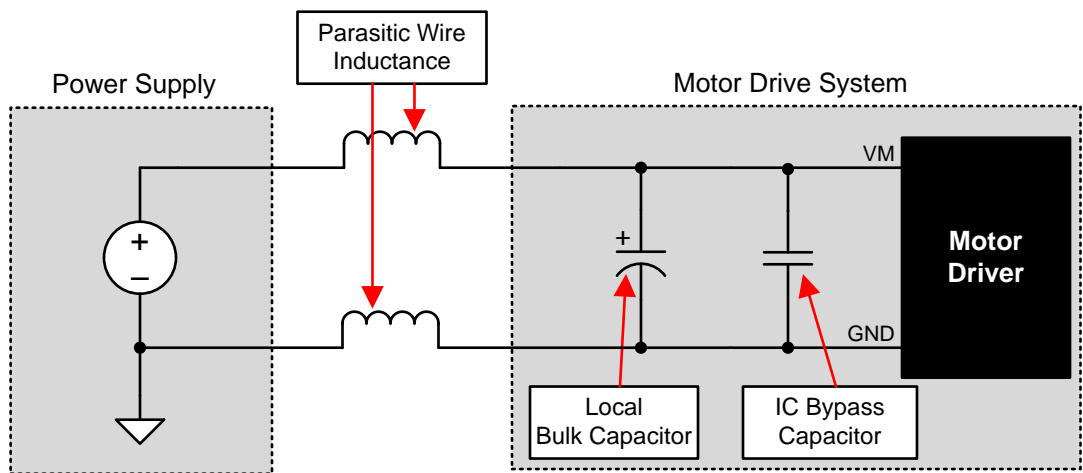
The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The power supply's capacitance and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed DC, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.



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Figure 31. Example Setup of Motor Drive System With External Power Supply

10 Layout

10.1 Layout Guidelines

The VM terminal should be bypassed to GND using a low-ESR ceramic bypass capacitor with a recommended value of 0.01 μF rated for VM. This capacitor should be placed as close to the VM pin as possible with a thick trace or ground plane connection to the device GND pin.

The VM pin must be bypassed to ground using a bulk capacitor rated for VM. This component may be an electrolytic.

A low-ESR ceramic capacitor must be placed in between the CPL and CPH pins. TI recommends a value of 0.022 μF rated for VM. Place this component as close as possible to the pins.

A low-ESR ceramic capacitor must be placed in between the VM and VCP pins. TI recommends a value of 0.22 μF rated for 16 V. Place this component as close as possible to the pins.

Bypass AVDD and DVDD to ground with a ceramic capacitor rated 6.3 V. Place this bypassing capacitor as close as possible to the pin.

10.2 Layout Example

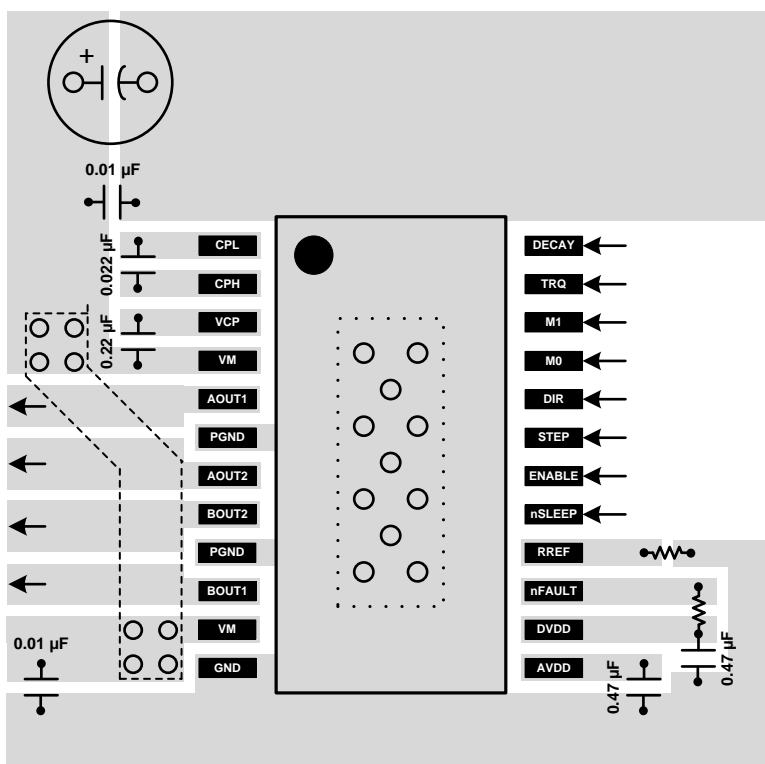


Figure 32. Layout Recommendation

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

- *PowerPAD™ Thermally Enhanced Package*, [SLMA002](#)
- *PowerPAD™ Made Easy*, [SLMA004](#)
- *Current Recirculation and Decay Modes*, [SLVA321](#)
- *Calculating Motor Driver Power Dissipation*, [SLVA504](#)
- *Understanding Motor Driver Current Ratings*, [SLVA505](#)

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments. All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8884PWP	ACTIVE	HTSSOP	PWP	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8884	Samples
DRV8884PWPR	ACTIVE	HTSSOP	PWP	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8884	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8884PWPR	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8884PWPR	HTSSOP	PWP	24	2000	367.0	367.0	38.0

MECHANICAL DATA

PWP (R-PDSO-G24)

PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

THERMAL PAD MECHANICAL DATA

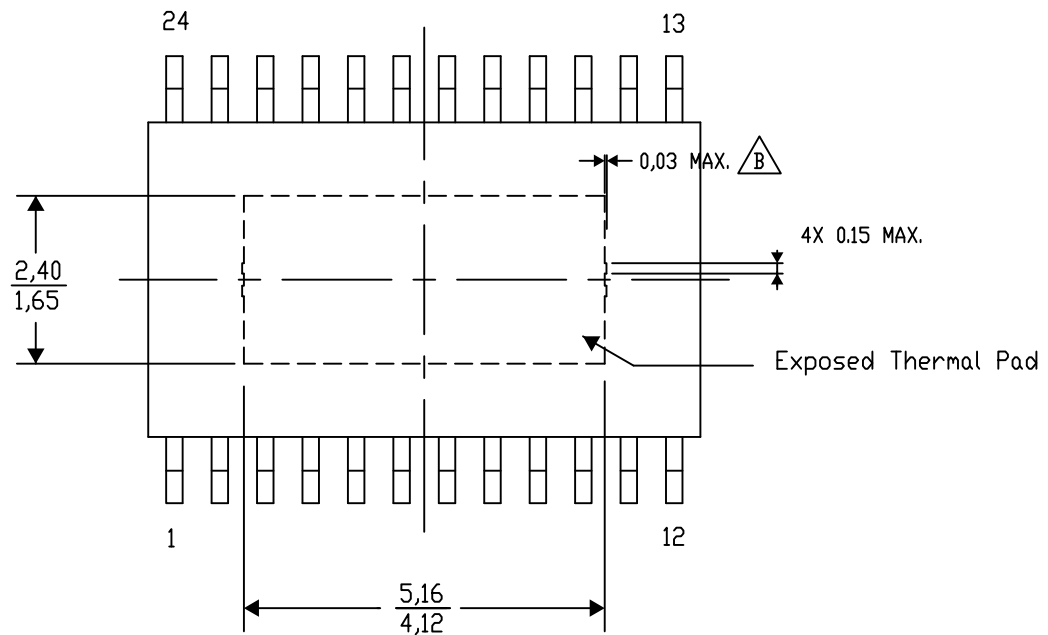
PWP (R-PDSO-G24) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332-29/AO 01/16

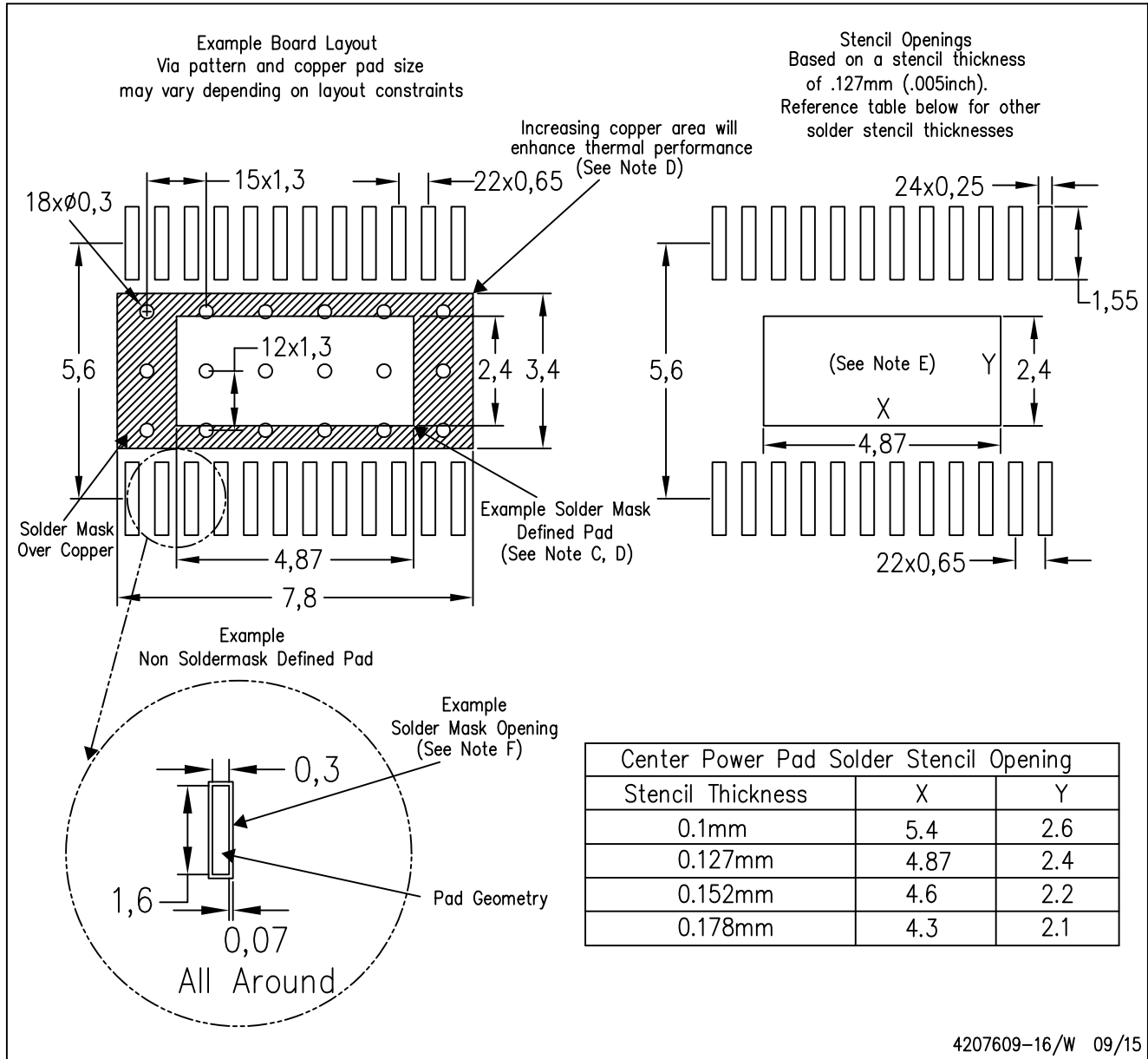
NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R-PDSO-G24)

PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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