- Electronic point-of-sale terminals
- Patient-monitoring devices

Features of the i.MX25 processor include the following:

- Advanced power management—The heart of the device is a level of power management throughout the IC that enables the multimedia features and peripherals to achieve minimum system power consumption in both active and various low-power modes. Power management techniques allow the designer to deliver a feature-rich product that requires levels of power that are far lower than typical industry expectations.
- Multimedia powerhouse—The multimedia performance of the i.MX25 processor is boosted by a 16 KB L1 instruction and data cache system, and further enhanced by an LCD controller (with alpha blending), CMOS image sensor interface, A/D controller (integrated touchscreen controller), and a programmable smart DMA (SDMA) controller.
- 128 Kbytes on-chip SRAM—The additional 128 Kbyte on-chip SRAM makes the device ideal for eliminating external RAM in applications with small footprint RTOS. The on-chip SRAM allows the designer to enable an ultra low power LCD refresh.
- Interface flexibility—The device interface supports connection to all common types of external memories: MobileDDR, DDR, DDR2, NOR Flash, PSRAM, SDRAM and SRAM, NAND Flash, and managed NAND/moviNAND™ (via the enhanced secured digital host controller (eSDHC)). Designers seeking to provide products that deliver a rich multimedia experience will find a full suite of on-chip peripherals: LCD controller and CMOS sensor interface, A/D controller (integrated touchscreen controller), parallel ATA, USB 2.0 high-speed on-the-go and full-speed host PHYs, multiple expansion card ports (high-speed MMC/SDIO host and others), fast Ethernet controller, and a variety of other common interfaces including UART, CSPI, I2C, FlexCAN, and SIM card.
- Increased security—Because the need for advanced security for tethered and untethered devices continues to increase, the i.MX25 processor delivers hardware-enabled security features that enable secure e-commerce, digital rights management (DRM), information encryption, robust tamper detection, secure boot, and secure software downloads.
- On-chip PHY—The device includes an HS USB OTG PHY and FS USB PHY.
- Fast Ethernet—For rapid external communication a fast Ethernet controller (FEC) is included.

1.1 Ordering Information

Table 1 provides the ordering information for the i.MX25.

Table 1. Non-Production Engineering Ordering Information

Part Number	Silicon Version	Projected Temperature Range (°C)	Package
PCIMX255CVM4	1.1	–40 to +85	17 x 17 mm, 0.8 mm pitch, MAPBGA-400
MCIMX253DVM4	1.1	–20 to +70	17 x 17 mm, 0.8 mm pitch, MAPBGA-400

Table 1. Non-Production Engineering Ordering Information (continued)

Part Number	Silicon Version	Projected Temperature Range (°C)	Package
MCIMX257DVM4	1.1	–20 to +70	17 x 17 mm, 0.8 mm pitch, MAPBGA-400
MCIMX257CVM4	1.1	–40 to +85	17 x 17 mm, 0.8 mm pitch, MAPBGA-400
MCIMX258CVM4	1.1	–40 to +85	17 x 17 mm, 0.8 mm pitch, MAPBGA-400

1.2 Block Diagram

Figure 1 shows the i.MX25 simplified interface block diagram.

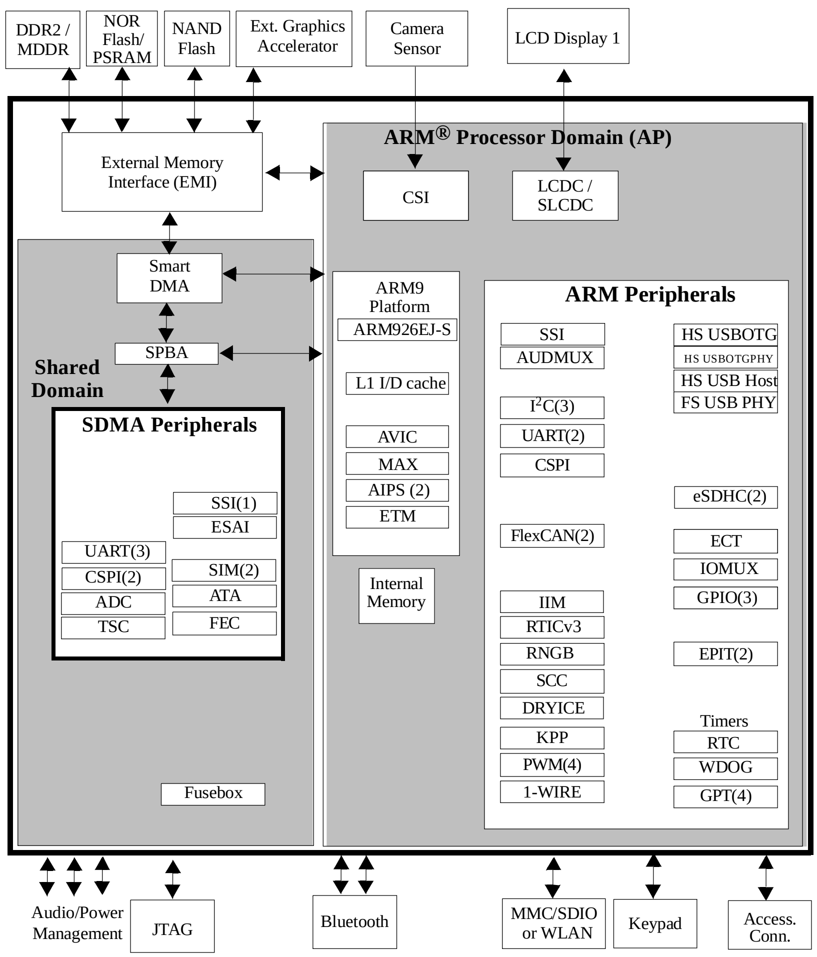


Figure 1. i.MX25 Simplified Interface Block Diagram

2 Features

Table 2 describes the digital and analog modules of the device.

Table 2. i.MX25 Digital and Analog Modules

Block Mnemonic	Block Name	Subsystem	Brief Description
1-WIRE	1-Wire Interface	Connectivity peripherals	1-Wire support provided for interfacing with an on-board EEPROM, and smart battery interfaces, for example: Dallas DS2502.
ARM9 or ARM926	ARM926 platform and memory	ARM®	The ARM926 Platform consists of the ARM926EJ-S™ core, the ETM real-time debug modules, a 5x5 Multi-Layer AHB crossbar switch, and a “primary AHB” complex. It contains the 16-Kbyte L1 instruction cache, 16-Kbyte L1 data cache, 32-Kbyte ROM and 128-Kbyte RAM.
ATA	ATA module	Connectivity peripherals	The ATA module is an AT attachment host interface. Its main use is to interface with IDE hard disc drives and ATAPI optical disc drives. It interfaces with the ATA device over a number of ATA signals.
AUDMUX	Digital audio mux	Multimedia peripherals	The AUDMUX is a programmable interconnect for voice, audio, and synchronous data routing between host serial interfaces (SSIs) and peripheral serial interfaces (audio codecs). The AUDMUX has two sets of interfaces: internal ports to on-chip peripherals, and external ports to off-chip audio devices. Data is routed by configuring the appropriate internal and external ports.
CCM	Clock control module	Clocks	This block generates all clocks for the iMX25 system. The CCM also manages the ARM926 Platform's low-power modes (wait, stop, and doze) by disabling peripheral clocks appropriately for power conservation.
CSPI(3)	Configurable serial peripheral interface	Connectivity peripherals	This module is a serial interface equipped with data FIFOs. Each master/slave-configurable SPI module is capable of interfacing to both serial port interface master and slave devices. The CSPI ready (SPI_RDY) and slave select (SS) control signals enable fast data communication with fewer software interrupts.
DRYICE	DRYICE module	Security	DRYICE provides volatile key storage for point-of-sale (POS) terminals, and a trusted time source for digital rights management (DRM) schemes. Several tamper-detect circuits are also provided to support key erasure and time invalidation in the event of tampering. Alarms and/or interrupts can also assert if tampering is detected.
EMI	External memory interface	Connectivity peripherals	The external memory interface (EMI) module provides access to external memory for the ARM and other masters. It is composed of four main submodules: • M3IF provides arbitration between multiple masters requesting access to the external memory. • Enhanced SDRAM/LPDDR memory controller (ESDCTL) interfaces to DDR2 and SDR interfaces. • NAND Flash controller (NFC) provides an interface to NAND Flash memories. • Wireless external interface memory controller (WEIM) interfaces to NOR Flash and PSRAM.

Table 2. i.MX25 Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
EPIT(2)	Enhanced periodic interrupt timer	Timer peripherals	Each enhanced periodic interrupt timer (EPIT) is a 32-bit set-and-forget timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler to adjust the input clock frequency to the required time setting for the interrupts, and the counter value can be programmed on the fly.
ESAI	Enhanced serial audio interface	Connectivity peripherals	ESAI provides a full-duplex serial port for serial communication with a variety of serial devices, including industry-standard codecs, SPDIF transceivers, and other DSPs. The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator.
eSDHC(2)	Enhanced multimedia card/ secure digital host controller	Connectivity peripherals	The features of the eSDHC module, when serving as host, include the following: • Conforms to the SD host controller standard specification version 2.0 • Compatible with the JEDEC MMC system specification version 4.2 • Compatible with the SD memory card specification version 2.0 • Compatible with the SDIO specification version 1.2 • Designed to work with SD memory, miniSD memory, SDIO, miniSDIO, SD combo, MMC and MMC RS cards • Configurable to work in one of the following modes: —SD/SDIO 1-bit, 4-bit —MMC 1-bit, 4-bit, 8-bit • Full-/high-speed mode • Host clock frequency variable between 32 kHz and 52 MHz • Up to 200-Mbps data transfer for SD/SDIO cards using four parallel data lines • Up to 416-Mbps data transfer for MMC cards using eight parallel data lines
FEC	Fast ethernet controller	Connectivity peripherals	The Ethernet media access controller (MAC) is designed to support both 10- and 100-Mbps Ethernet networks compliant with IEEE 802.3® standard. An external transceiver interface and transceiver function are required to complete the interface to the media
FlexCAN(2)	Controller area network module	Connectivity peripherals	The controller area network (CAN) protocol is primarily designed to be used as a vehicle serial data bus running at 1 MBps.
GPIO(4)	General purpose I/O modules	System control peripherals	Used for general purpose input/output to external ICs. Each GPIO module supports 32 bits of I/O.
GPT(4)	General purpose timers	Timer peripherals	Each GPT is a 32-bit free-running or set-and-forget mode timer with programmable prescaler and compare and capture register. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in set-and-forget mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.

Table 2. i.MX25 Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
I^2C(3)	I^2C module	Connectivity peripherals	Inter-IC Communication (I^2C) is an industry-standard, bidirectional serial bus that provides a simple, efficient method of data exchange, minimizing the interconnection between devices. I^2C is suitable for applications requiring occasional communications over a short distance between many devices. The interface operates up to 100 kbps with maximum bus loading and timing. The I^2C system is a true multiple-master bus, including arbitration and collision detection that prevents data corruption if multiple devices attempt to control the bus simultaneously. This feature supports complex applications with multiprocessor control and can be used for rapid testing and alignment of end products through external connections to an assembly-line computer.
IIM	IC Identification Module	Security	The IIM provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, and various control signals requiring a fixed value.
IOMUX	I/O multiplexer	Pins	Each I/O multiplexer provides a flexible, scalable multiplexing solution: • Up to eight output sources multiplexed per pin • Up to four destinations for each input pin • Unselected input paths are held at constant level for reduced power consumption
KPP	Keypad port	Connectivity peripherals	KPP can be used for either keypad matrix scanning or general purpose I/O.
LCDC	LCD Controller	Multimedia peripherals	LCDC provides display data for external gray-scale or color LCD panels. LCDC is capable of supporting black-and-white, gray-scale, passive-matrix color (passive color or CSTN), and active-matrix color (active color or TFT) LCD panels.
MAX	ARM platform multilayer AHB crossbar switch	ARM platform	MAX concurrently supports up to five simultaneous connections between master ports and slave ports. MAX allows for concurrent transactions to occur from any master port to any slave port.
PWM(4)	Pulse width modulation	Connectivity peripherals	The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images. It can also generate tones. The PWM uses 16-bit resolution and a 4x16 data FIFO to generate sound.
SDMA	Smart DMA engine	System control	The SDMA provides DMA capabilities inside the processor. It is a shared module that implements 32 DMA channels.
SIM(2)	Subscriber identity module interface	Connectivity peripherals	The SIMv2 is an asynchronous interface with additional features for allowing communication with smart cards conforming to the ISO/IEC 7816 specification. The SIM is designed to facilitate communication to SIM cards or pre-paid phone cards.
SJC	Secure JTAG interface	System control peripherals	The system JTAG controller (SJC) provides debug and test control with maximum security.
SLCD	Smart LCD controller	Multimedia peripherals	The SLCDC module transfers data from the display memory buffer to the external display device.
SPBA	Shared peripheral bus arbiter	System control	The SPBA controls access to the shared peripherals. It supports shared peripheral ownership and access rights to an owned peripheral.

Table 2. i.MX25 Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SSI(2)	I2S/SSI/AC97 interface	Connectivity peripherals	The SSI is a full-duplex serial port that allows the processor to communicate with a variety of serial protocols, including the Freescale Semiconductor SPI standard and the inter-IC sound bus standard (I2S). The SSIs interface to the AUDMUX for flexible audio routing.
TSC (and ADC)	Touchscreen controller (and A/D converter)	Multimedia peripherals	The touchscreen controller and associated analog-to-digital converter (ADC) together provide a resistive touchscreen solution. The module implements simultaneous touchscreen control and auxiliary ADC operation for temperature, voltage, and other measurement functions.
UART(5)	UART interface	Connectivity peripherals	Each of the UART modules supports the following serial data transmit/receive protocols and configurations: • 7- or 8-bit data words, one or two stop bits, programmable parity (even, odd, or none) • Programmable baud rates up to 4 MHz. This is a higher maximum baud rate than the 1.875 MHz specified by the TIA/EIA-232-F standard and previous Freescale UART modules. 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud • IrDA-1.0 support (up to SIR speed of 115200 bps) • Option to operate as 8-pins full UART, DCE, or DTE
USBOTG USBHOST	High-speed USB on-the-go	Connectivity peripherals	The USB module provides high-performance USB On-The-Go (OTG) and host functionality (up to 480 Mbps), compliant with the USB 2.0 specification, the OTG supplement, and the ULPI 1.0 Low Pin Count specification. The module has DMA capabilities for handling data transfer between internal buffers and system memory. An OTG HS PHY and HOST FS PHY are also integrated.

2.1 Special Signal Considerations

Special signal considerations are listed in Table 3. The package contact assignment is found in Section 4, "Package Information and Contact Assignment." Signal descriptions are provided in the reference manual.

Table 3. Signal Considerations

Signal	Description
BAT_VDD	DryIce backup power supply input.
CLK0	Clock-out pin; renders the internal clock visible to users for debugging. The clock source is controllable through CRM registers. This pin can also be configured (via muxing) to work as a normal GPIO.
CLK_SEL	Used to select the ARM clock source from MPLL out or from external EXT_ARMCLK. In normal operation, CLK_SEL should be connected to GND.
EXT_ARMCLK	Primarily for Freescale factory use. There is no internal on-chip pull-up/down on this pin, so it must be externally connected to GND or VDD. Aside from factory use, this pin can also be configured (via muxing) to work as a normal GPIO.
MESH_C, MESH_D	Wire-mesh tamper detect pins that can be routed at the PCB board to detect attempted tampering of a protected wire. When security measures are implemented, MESH_C should be pulled-up to NVCC_DRYICE and triggers a tamper event when floating or when connected to MESH_D. MESH_D should be pulled-down to GND and triggers an event when floating or connected to MESH_C. These pins can be left unconnected if the DryIce security features are not being used.

Table 3. Signal Considerations (continued)

Signal	Description
NVCC_DRYICE	DryIce power supply output. Source can be SoC supply or backup supply. This pin can be used to power external components (external tamper detect, wire-mesh tamper detect).
OSC_BYP	The 32 kHz oscillator bypass-control pin. If this signal is pulled down, then OSC32K_EXTAL and OSC32K_XTAL analog pins should be tied to the external 32.768 kHz crystal circuit. If on the other hand the signal is pulled up, then the external 32 kHz oscillator output clock must be connected to OSC32K_EXTAL analog pin, and OSC32K_XTAL can be no connect (NC).
OSC32K_EXTAL OSC32K_XTAL	These analog pins are connected to an external 32 kHz CLK circuit depending on the state of OSC_BYP pin (see the description of OSC_BYP under the preceding bullet). The 32 kHz reference CLK is required for normal operation.
POWER_FAIL	An interrupt from PMIC, which should be connected to a low-battery detection circuit. This signal is internally connected to an on-chip 100 kΩ pull-down device. If there is no low-battery detection, then users can tie this pin to GND via a pull-down resistor, or leave the signal as NC. This pin can also be configured to work as a normal GPIO.
REF	External ADC reference voltage (2.5 V). REF may be left floating if the internally generated 2.5 V supply is enabled. Use of an external 2.5 V reference voltage is recommended.
SJC_MOD	Must be externally connected to GND for normal operation. Termination to GND through an external pull-down resistor (such as 1 kΩ) is allowed, but the value should be much smaller than the on-chip 100-kΩ pull-up.
TAMPER_A, TAMPER _B	DryIce external tamper detect pins, active high. If either TAMPER_A or TAMPER_B asserted, then external tampering is detected. These pins can be left unconnected if the DryIce security features are not being used.
TEST_MODE	For Freescale factory use only. This signal is internally connected to an on-chip pull-down device. Users must either float this signal or tie it to GND.
UPLL_BYPCLK	Primarily for Freescale factory use. There is no internal on-chip pull-up/down on this pin, so it must be externally connected to GND or VDD. Aside from factory use, this pin can also be configured (via muxing) to work as a normal GPIO.
USBPHY1_RREF	Determines the reference current for the USB PHY1 bandgap reference. An external 10 kΩ 1% resistor to GND is required.
USBPHY2_DM USBPHY2_DP	The output impedance of these signals is expected at 10 Ω. It is recommended to also have on-board 33 Ω series resistors (close to the pins).

3 Electrical Characteristics

This section provides the device-level and module-level electrical characteristics for the i.MX25.

3.1 i.MX25 Chip-Level Conditions

This section provides the chip-level electrical characteristics for the IC.

3.1.1 DC Absolute Maximum Ratings

Table 4 provides the DC absolute maximum operating conditions.

CAUTION

- Stresses beyond those listed under Table 4 may cause permanent damage to the device.
- Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- Table 4 gives stress ratings only—functional operation of the device is not implied beyond the conditions indicated in Table 5.

Table 4. DC Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply voltage	QV_{DD}	–0.5	1.52	V
Supply voltage (level shift i/o)	$V_{DDIOmax}$	–0.5	3.6	V
ESD damage immunity:	V_{esd}			V
Human body model (HBM)		—	2000[1]	
Charge device model (CDM)		—	500[1]	
Input voltage range	V_{Imax}	–0.5	NV_{DD} + 0.3	V
Storage temperature range	$T_{storage}$	–40	105	°C

[1] ESD values will be verified during qualification.

3.1.2 DC Operating Conditions

Table 5 provides the DC recommended operating conditions.

Table 5. DC Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Core supply voltage (at 266 MHz)	QV_{DD}	1.15[1]	1.34	1.52	V
Core supply voltage (at 400 MHz)	QV_{DD}	1.38[1]	1.45	1.52	V
Coin battery[2] BAT_VDD	V_{DD_BAT}	1.15	—	1.55	V
I/O supply voltage, GPIO NFC,CSI,SDIO	NV_{DD_GPIO1}	1.75	—	3.6	V

Table 5. DC Operating Conditions (continued)

Parameter	Symbol	Min.	Typ.	Max.	Units
I/O supply voltage, GPIO CRM,LCDC,JTAG,MISC	NV_{DD_GPIO2}	3.0	3.3	3.6	—
I/O supply voltage DDR (Mobile DDR mode) EMI1, EMI2	NV_{DD_MDDR}	1.75	—	1.95	V
I/O supply voltage DDR (DDR2 mode) EMI1,EMI2	NV_{DD_DDR2}	1.75	—	1.9	V
I/O supply voltage DDR (SDRAM mode) EMI1,EMI2	NV_{DD_SDRAM}	1.75	—	3.6	V
Supply of USBPHY1 (HS) USBPHY1_VDDA_BIAS, USBPHY1_UPLL_VDD,USBPHY1_VDDA	$V_{DD\_usbphy1}$	3.17	3.3	3.43	V
Supply of USBPHY2 (FS) USBPHY2_VDD	$V_{DD\_usbphy2}$	3.0	3.3	3.6	V
Supply of OSC24M OSC24M_VDD	V_{DD_OSC24M}	3.0	3.3	3.6	V
Supply of PLL MPLL_VDD,UPLL_VDD	V_{DD_PLL}	1.4	—	1.65	V
Supply of touchscreen ADC NVCC_ADC	V_{DD_tsc}	3.0	3.3	3.6	V
External reference of touchscreen ADC Ref	Vref	2.5	V_{DD_tsc}	V_{DD_tsc}	V
Fusebox program supply voltage FUSE_VDD[3]	$FUSEV_{DD}$ (program mode)	—	3.6	—	V
Supply output[4] NVCC_DRYICE	$V_{DD\_}$	1.0	—	1.55	V
Operating ambient temperature	T_A	–40	—	85	°C

1 Values must be verified

2 V_{DD_BAT} must always be powered by battery in security application. In non-security case, V_{DD_BAT} can be connected to QV_{DD}.

3 The fusebox read supply is connected to supply of the full speed USBPHY2_VDD. FUSE_VDD is only used for programming. It is recommended that FUSE_VDD be connected to ground when not being used for programming. See Table 6 for current parameters.

4 NVCC_DRYICE is supply output. A 0.1-µF external capacitor should be connected to it.

3.1.3 Fusebox Supply Current Parameters

Table 6 lists the fusebox supply current parameters.

Table 6. Fusebox Supply Current Parameters

Parameter	Symbol	Min.	Typ.	Max.	Units
eFuse program current[1] Current to program one eFuse bit The associated VDD_FUSE supply = 3.6 V	$I_{program}$	26	35	62	mA
eFuse read current[2] Current to read an 8-bit eFuse word	I_{read}	—	12.5	15	mA

[1] The current $I_{program}$ is during program time ($t_{program}$).
[2] The current I_{read} is present for approximately 50 ns of the read access to the 8-bit word.

3.1.4 Interface Frequency Limits

Table 7 provides information for interface frequency limits.

Table 7. Interface Frequency Limits

Parameter	Min.	Typ.	Max.	Units
JTAG: TCK Frequency of Operation	DC	5	10	MHz
OSC24M_XTAL Oscillator	—	24	—	MHz
OSC32K_XTAL Oscillator	—	32.768	—	KHz

3.1.5 USB_PHY Current Consumption

Table 8 provides information for USB_PHY current consumption.

Table 8. USB PHY Current Consumption[1]

Parameter	Conditions		Typ. (@Typ. Temp)	Max. (@Max. Temp)	Unit
Analog supply USBPHY1_VDDA_BIAS, USBPHY1_UPLL_VDD, USBPHY1_VDDA (3.3 V)	Full speed	Rx	11.4	—	mA
		Tx	22,6	—	
	High speed	Rx	21.5	—	
		Tx	33.8	—	
	Suspend	—	0.6		µA
Analog supply USBPHY2_VDD (3.3 V)	Full Speed	Rx	120	—	µA
		Tx	25	—	mA
	Low Speed	Rx	252	—	µA
		Tx	5.5	—	mA
All supplies	Suspend		50	100	µA

[1] Values must be verified

3.1.6 Power Modes

Table 9 describes the core, clock, and module settings for the different power modes of the processor.

Table 9. i.MX25 Power Mode Settings[1]

Core/Clock/Module	Power Mode				
	Doze	Wait	Stop/Sleep[2]	Run (266 MHz)	Run (400 MHz)
ARM core	Platform clock is off	In wait-for-interrupt mode	—	Active @ 266 MHz	Active @ 400 MHz
Well bias	On	Off	On	Off	Off
MCU PLL	On	On	Off	On	On
USB PLL	Off	Off	Off	On	On
OSC24M	On	On	Off	On	On
OSC32K	On	On	On	On	On
Other modules	Off	Off	Off	On	On

1 Values must be verified.

2 Sleep mode differs from stop mode in that the core voltage is reduced to 1 V.

Table 10 describes the current consumption for the various power supplies under the various power modes.

Table 10. i.MX25 Power Mode Current Consumption

Power Group	Power Supplies	Voltage Setting	Current Consumption for Power Modes					
			Doze[1]	Wait[1]	Stop[1]	Sleep[1]	Run @266 MHz[1]	Run @400 MHz[1]
FUSE_VDD	FUSE_VDD	1.8 V	0.04 mA	0.04 mA	0.04 mA	—	—	—
NVCC_EMI	NVCC_EMI1 NVCC_EMI2	1.8 V	10.12 mA	10.11 mA	0.09 mA	—	—	—
NVCC_CRM	NVCC_CRM	3.3 V	0.35 mA	0.35 mA	0.15 mA	—	—	—
NVCC_OTHER	NVCC_SDIO NVCC_CSI NVCC_NFC NVCC_JTAG NVCC_LCDC NVCC_MISC	3.3 V	0.4 mA	0.4 mA	0.04 mA	—	—	—
NVCC_ADC	NVCC_ADC	3.3 V	0.03 mA	0.03 mA	0.03 mA	—	—	—
OSC24M	OSC24M_VDD	3.3 V	0.6 mA	0.6 mA	0.04 mA	—	—	—
PLL_VDD	MPLL_VDD UPLL_VDD	1.5 V	10.5 mA	9.75 mA	0.08 mA	—	—	—
QVDD	QVDD	1.2 V	396 µA	620 µA	396 µA[1]	222 µA	84 mA	136 mA
USBPHY1_VDDA	USBPHY1_VDDA	3.3 V	—	—	—	—	—	—
USBPHY1_VDDA_VBIAS	USBPHY1_VDDA_VBIAS	3.3 V	—	—	—	—	—	—
USBPHY1_UPLL_VDD	USBPHY1_UPLL_VDD	3.3 V	—	—	—	—	—	—
USBPHY2	USBPHY2_VDD	3.3 V	0.16 mA	0.16 mA	0.16 mA	—	—	—
TOTAL		—	—	—	—	—	—	—

[1] Values must be verified.

3.2 Supply Power-Up/Power-Down Requirements and Restrictions

Any i.MX25 board design must comply with the power-up and power-down sequence guidelines given in this section to ensure reliable operation of the device. Recommended power-up and power-down sequences are given in the following subsections.

CAUTION

Deviations from the guidelines in this section may result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting
- Irreversible damage to the i.MX25 (worst-case scenario)

NOTE

For security applications, the coin battery must be connected during both power-up and power-down sequences to ensure that security keys are not unintentionally erased.

3.2.1 Power-Up Sequence

The following power-up sequence is recommended:

1. Assert power on reset (POR).
2. Turn on digital logic domain and I/O power supplies VDD*n* and NVCC*x*.
3. Turn on all other analog power supplies, including USBPHY1_VDDA_BIAS, USBPHY1_UPLL_VDD, USBPHY1_VDDA, USBPHY2_VDD, OSC24M_VDD, MPPLL_VDD, UPLL_VDD, NVCC_ADC, and FUSEVDD (FUSEVDD is tied to GND if fuses are not being programmed). The minimum time between turning on each power supply is the time it takes for the previous supply to be stable.
4. Negate the POR signal.

NOTE

- The user is advised to connect FUSEVDD to GND except when fuses are being programmed, in order to prevent unintentional blowing of fuses.
- Other power-up sequences may be possible; however, the above sequence has been verified and is recommended.

Figure 2 shows the power-up sequence diagram. After POR_B is asserted, Core VDD and NVDDx can be powered up. After Core VDD and NVDDx are stable, the analog supplies can be powered up.

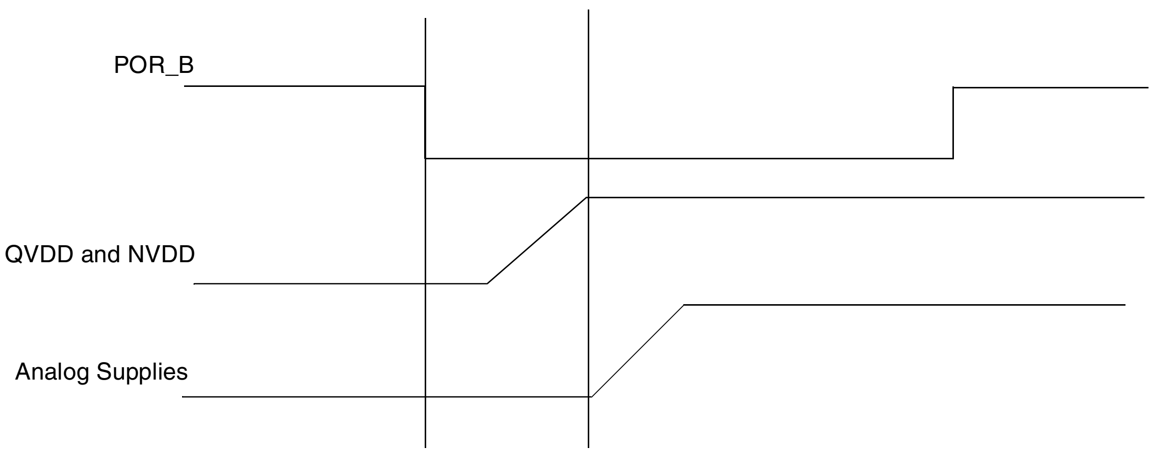


Figure 2. Power-Up Sequence Diagram

3.2.2 Power-Down Sequence

There are no special requirements for the power-down sequence. All power supplies can be shut down at the same time.

3.3 Thermal Characteristics

The thermal resistance characteristics for the device are given in Table 11. These values were measured under the following conditions:

- Two-layer substrate
- Substrate solder mask thickness: 0.025 mm
- Substrate metal thicknesses: 0.016 mm
- Substrate core thickness: 0.200 mm
- Core via I.D: 0.118 mm, Core via plating 0.016 mm.
- Flag: Trace style with ground balls under the die connected to the flag
- Die Attach: 0.033 mm non-conductive die attach, k = 0.3 W/m K
- Mold compound: Generic mold compound; k = 0.9 W/m K

Table 11. Thermal Resistance Data

Rating	Condition	Symbol	Value	Unit
Junction to ambient[1] natural convection	Single layer board (1s)	R_{eJA}	55	°C/W
Junction to ambient[1] natural convection	Four layer board (2s2p)	R_{eJA}	33	°C/W
Junction to ambient[1] (@200 ft/min)	Single layer board (1s)	R_{eJMA}	46	°C/W
Junction to ambient[1] (@200 ft/min)	Four layer board (2s2p)	R_{eJMA}	29	°C/W
Junction to boards[2]	—	R_{eJB}	22	°C/W
Junction to case (top)[3]	—	R_{eJCtop}	13	°C/W
Junction to package top[4]	Natural convection	Ψ_{JT}	2	°C/W

1 Junction-to-ambient thermal resistance determined per JEDC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

2 Junction-to-board thermal resistance determined per JEDC JESD51-8. Thermal test board meets JEDEC specification for this package.

3 Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

4 Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, this thermal characterization parameter is written as Psi-JT.

3.4 I/O DC Parameters

This section includes the DC parameters of the following I/O types:

- DDR I/O: Mobile DDR (mDDR), double data rate (DDR2), or Synchronous dynamic random access memory (SDRAM)
- General purpose I/O (GPIO)

NOTE

The term 'OVDD' in this section refers to the associated supply rail of an input or output. The association is shown in the "Signal Multiplexing" chapter of the reference manual.

3.4.1 DDR I/O DC Parameters

The DDR pad type is configured by the IOMUXC_SW_PAD_CTL_GRP_DDRTYPE register (see the External Signals and Pin Multiplexing chapter of the *i.MX25 Reference Manual* for details).

3.4.1.1 DDR_TYPE = 00 Standard Setting DDR I/O DC Parameters

Table 12 shows the I/O parameters for mobile DDR. These settings are suitable for mDDR and DDR2 1.8V (± 5%) applications.

Table 12. Mobile DDR I/O DC Electrical Characteristics

DC Electrical Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units	Notes
High-level output voltage	Voh	I_{OH} = –1mA I_{OH} = Specified Drive	OVDD – 0.08 0.8 × OVDD	—	—	V	1
Low-level output voltage	Vol	I_{OL} = 1mA I_{OL} = Specified Drive	—	—	0.08 0.2 × OVDD	V	
High-level output current	I Ioh	Voh = 0.8 × OVDDV Standard Drive High Drive Max. Drive	–3.6 –7.2 –10.8	—	—	mA	—
Low-level output current	I Iol	Vol = 0.2 × OVDDV Standard Drive High Drive Max. Drive	3.6 7.2 10.8	—	—	mA	—
High-level DC CMOS input voltage	VIH	—	0.7 × OVDD	OVDD	OVDD+0.3	V	—
Low-level DC CMOS input voltage	VIL	—	–0.3	0	0.3 × OVDD	V	
Differential receiver VTH+	VTH+	—		—	100	mV	
Differential receiver VTH-	VTH-		–100	—	—	mV	
Input current (no pull-up/down)	IIN	VI = 0 VI = OVDD	—	—	110 60	nA	2, 3
High-impedance I/O supply current	Icc-ovdd	VI = OVDD or 0	—	—	990	nA	2, 3
High-impedance core supply current	Icc-vddi	VI = VDD or 0	—	—	1220	nA	

Note:

1. Simulation circuit for parameters Voh and Vol for I/O cells is below
2. Minimum condition: BCS model, 1.95 V, and –40 °C. Typical condition: typical model, 1.8 V, and 25 °C. Maximum condition: wcs model, 1.65 V, and 105 °C.
3. Typical condition: typical model, 1.8 V, and 25 °C. Maximum condition: BCS model, 1.95 V, and 105 °C.

3.4.1.2 DDR_TYPE = 01 SDRAM I/O DC Parameters

Table 13 shows the DC I/O parameters for SDRAM.

Table 13. SDRAM DC Electrical Characteristics

DC Electrical Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units	Notes
High-level output voltage	Voh	Ioh = Specified Drive (Ioh = –4, –8, –12, –16mA)	2.4	—	—	V	1
Low-level output voltage	Vol	Ioh = Specified Drive (Ioh = 4, 8, 12, 16mA)	—	—	0.4	V	1
High-level output current	I Ioh	Standard Drive High Drive Max. Drive	–4.0 –8.0 –12.0	—	—	mA	—
Low-level output current	I Iol	Standard Drive High Drive Max. Drive	4.0 8.0 12.0	—	—	mA	—
High-level DC input voltage	VIH	—	2.0	—	3.6	V	—
Low-level DC input voltage	VIL	—	–0.3 V	—	0.8	V	
Input current (no pull-up/down)	IIN	VI = 0 VI = OVDD	—	—	150 80	nA	2, 3
High-impedance I/O supply current	Icc-ovdd	VI = OVDD or 0	—	—	1180	nA	2, 3
High-impedance core supply current	Icc-vddi	VI = VDD or 0	—	—	1220	nA	

Note:

1. Simulation circuit for parameters Voh and Vol for I/O cells is below
2. Minimum condition: bcs model, OVDD = 3.6 V, and –40 °C. Typical condition: typical model, OVDD = 3.3 V, and 25 °C. Maximum condition: wcs model, OVDD = 3.0 V, and 105 °C.
3. Typical condition: typical model, OVDD = 3.3 V, and 25 °C. Maximum condition: bcs model, OVDD = 3.6 V, and 105 °C.

3.4.1.3 DDR_TYPE = 10 Max Setting DDR I/O DC Parameters

Table 14 shows the I/O parameters for DDR2 (SSTL_18).

Table 14. DDR2 (SSTL_18) I/O DC Electrical Characteristics

DC Electrical Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units	Notes
High-level output voltage	Voh	—	OVDD – 0.28	—	—	V	—
Low-level output voltage	Vol	—	—	—	0.28	V	
Output min. source current	Iloh	—	–13.4	—	—	mA	1
Output min. sink current	Ilol	—	13.4	—	—	mA	2
DC input logic high	VIH(dc)	—	OVDD/2 + 0.125	—	OVDD + 0.3	V	—
DC input logic low	VIL(dc)	—	–0.3 V	—	OVDD/2 – 0.125	V	—

Table 14. DDR2 (SSTL_18) I/O DC Electrical Characteristics (continued)

DC Electrical Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units	Notes
DC input signal voltage(for differential signal)	Vin(dc)	—	–0.3	—	OVDD + 0.3	V	3
DC differential input voltage	Vid(dc)	—	0.25	—	OVDD+0.6	V	4
Termination voltage	Vtt	—	OVDD/2 – 0.04	OVDD/2	OVDD/2 + 0.04		5
Input current (no pull-up/down)	IIN	VI = 0 VI = OVDD	—	—	110 60	nA	9
High-impedance I/O supply current	Icc-ovdd	VI = OVDD or 0	—	—	980	nA	9
High-impedance core supply current	Icc-vddi	VI = VDD or 0	—	—	1210	nA	

Note:

1. OVDD = 1.7 V; V_{out} = 1.42 V. (V_{out}-OVDD)/IOH must be less than 21 W for values of V_{out} between OVDD and OVDD-0.28 V.
2. OVDD = 1.7 V; V_{out} = 280 mV. V_{out}/IOL must be less than 21 W for values of V_{out} between 0 V and 280 mV. Simulation circuit for parameters V_{oh} and V_{ol} for I/O cells is below
3. Vin(dc) specifies the allowable DC excursion of each differential input
4. Vid(dc) specifies the input differential voltage required for switching. The minimum value is equal to Vih(dc) - Vil(dc).
5. Vtt is expected to track OVDD/2.
6. Minimum condition: BCS model, 1.95 V, and –40 °C. Typical condition: typical model, 1.8 V, and 25 °C. Maximum condition: wcs model, 1.65 V, and 105 °C.
7. Typical condition: typical model, 1.8 V, and 25 °C. Maximum condition: BCS model, 1.95 V, and 105 °C.
8. The JEDEC SSTL_18 specification (JESD8-15a) for a SSTL interface for class II operation supersedes any specification in this document.

3.4.2 GPIO I/O DC Parameters

Table 15 shows the I/O parameters for GPIO.

Table 15. GPIO DC Electrical Characteristics

DC Electrical Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units	Notes
High-level output voltage	Voh	Ioh=–1mA Ioh = Specified Drive	OVDD – 0.15 0.8 × OVDD	—	—	V	1
Low-level output voltage	Vol	Iol=1mA Iol=Specified Drive	—	—	0.15 0.2 × OVDD	V	1
High-level output current for slow mode	I Ioh	Voh=0.8 × OVDD Standard Drive High Drive Max. Drive	 –2.0 –4.0 –8.0	—	—	mA	—
High-level output current for fast mode	I Ioh	Voh=0.8 × OVDD Standard Drive High Drive Max. Drive	 –4.0 –6.0 –8.0	—	—	mA	—

Table 15. GPIO DC Electrical Characteristics (continued)

DC Electrical Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units	Notes
Low-level output current for slow mode	I Iol	Voh=0.2 × OVDD Standard Drive High Drive Max. Drive	 2.0 4.0 8.0	—	—	mA	—
Low-level output current for fast mode	I Iol	Voh=0.2 × OVDD Standard Drive High Drive Max. Drive	 4.0 6.0 8.0	—	—	mA	—
High-level DC input voltage	VIH	—	0.7 × OVDD	—	OVDD	V	—
Low-level DC input voltage	VIL	—	–0.3 V	—	0.3 × OVDD	V	
Input hysteresis	VHYS	OVDD = 3.3 V OVDD = 1.8V	370 290	—	420 320	mV	—
Schmitt trigger VT+	VT+	—	0.5 × OVDD	—	—	V	2
Schmitt trigger VT–	VT–	—	—	—	0.5 × OVDD	V	
Pull-up resistor (22 kΩ PU)	Rpu	Vi=0	18.5	22	25.6	KΩ	3
Pull-up resistor (47 kΩ PU)	Rpu	Vi=0	41	47	55	KΩ	
Pull-up resistor (100 kΩ PU)	Rpu	Vi=0	85	100	120	KΩ	
Pull-down resistor (100 kΩ PD)	Rpd	VI = OVDD	85	100	120	KΩ	
Input current (no pull-up/down)	IIN	VI = 0, OVDD = 3.3 V VI = OVDD = 3.3 V VI = 0, OVDD = 1.8 V VI = OVDD = 1.8 V	—	—	100 60 77 50	nA	4
Input current (22 kΩ PU)	IIN	VI = 0, OVDD = 3.3 V VI = OVDD = 3.3 V VI = 0, OVDD = 1.8 V VI = OVDD = 1.8 V	117 0.0001 64 0.0001	—	184 0.0001 104 0.0001	µA	

Table 15. GPIO DC Electrical Characteristics (continued)

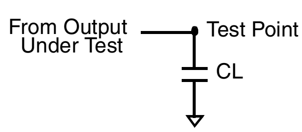
DC Electrical Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units	Notes
Input current (47 kΩ PU)	IIN	VI = 0, OVDD = 3.3 V VI = OVDD = 3.3 V VI = 0, OVDD = 1.8 V VI = OVDD = 1.8 V	54 0.0001 30 0.0001	—	88 0.0001 49 0.0001	µA	4
Input current (100 kΩ PU)	IIN	VI = 0, OVDD = 3.3 V VI = OVDD = 3.3 V VI = 0, OVDD = 1.8 V VI = OVDD = 1.8 V	25 0.0001 14 0.0001	—	42 0.0001 23 0.0001	µA	
Input current (100 kΩ PD)	IIN	VI = 0, OVDD = 3.3 V VI = OVDD = 3.3 V VI = 0, OVDD = 1.8 V VI = OVDD = 1.8 V	25 0.0001 14 0.0001	—	42 0.001 23 0.0001	µA	
High-impedance I/O supply current	Icc–ovdd	VI = 0, OVDD = 3.3 V VI = OVDD = 3.3 V VI = 0, OVDD = 1.8 V VI = OVDD = 1.8 V	—	—	688 688 560 560	nA	4
High-impedance core supply current	Icc–vddi	VI = 0, OVDD = 3.3 V VI = OVDD = 3.3 V VI = 0, OVDD = 1.8 V VI = OVDD = 1.8 V	—	—	490 490 410 410	nA	

1. Simulation circuit for parameters Voh and Vol for I/O cells is below
2. Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled.
3. Minimum condition: bcs model, OVDD = 3.6 V / 1.95 V and –40 °C. Typical condition: typical model, OVDD = 3.3 V / 1.8 V, and 25 °C. Maximum condition: wcs model, OVDD = 3.0 V, and 105 °C.
4. Typical condition: typical model, OVDD=3.3 V / 1.8 V, and 25 °C. Maximum condition: bcs model, OVDD=3.6 V / 1.95 V, and 105 °C.

3.5 AC Electrical Characteristics

This section provides the AC parameters for slow and fast I/O.

Figure 3 shows the load circuit for output. Figure 4 through Figure 6 show the output transition time and propagation waveforms.



CL includes package, probe and jig capacitance

Figure 3. Load Circuit for Output

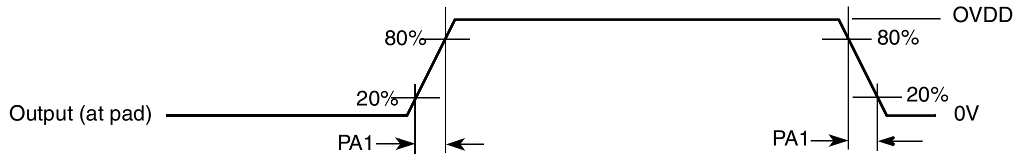


Figure 4. Output Pad Transition Time Waveform

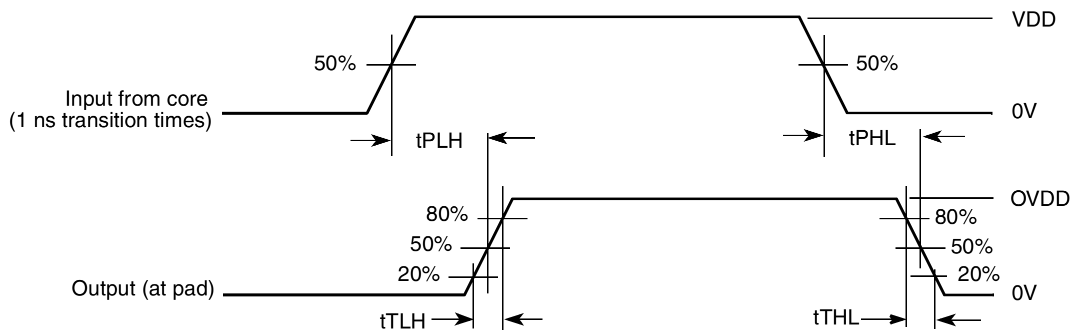


Figure 5. Output Pad Propagation and Transition Time Waveform

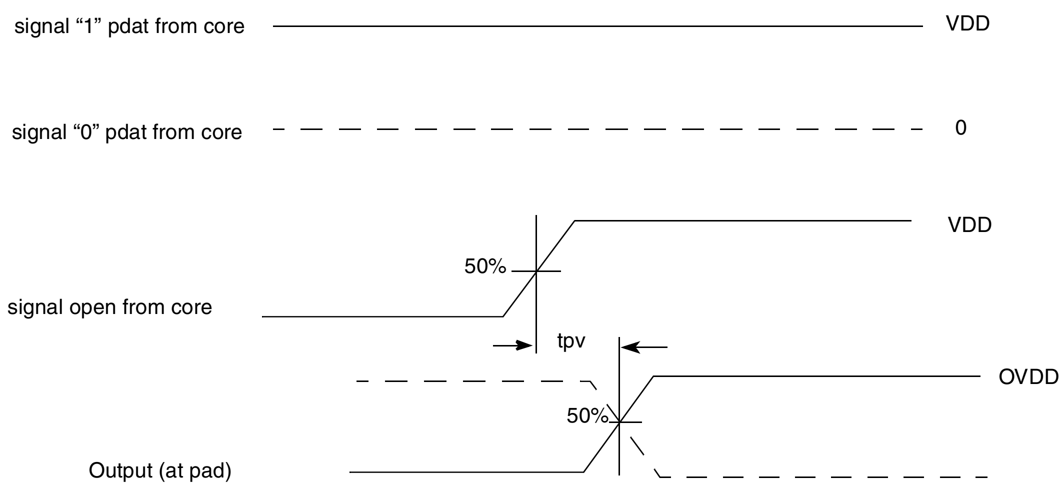


Figure 6. Output Enable to Output Valid

3.5.1 Slow I/O AC Parameters

Table 16 shows the slow I/O AC parameters.

Table 16. Slow I/O AC Parameters

Parameter	Symbol	Test Voltage	Test Capacitance	Min. Rise/Fall	Typ. Rise/Fall	Max. Rise/Fall	Units	Notes
Duty cycle	Fduty	—	—	40	—	60	%	—
Output pad transition times (max. drive)	tpr	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	0.95/0.84 1.58/1.37 2.70/2.50 3.40/3.20	1.36/1.11 2.19/1.77 1.80/1.40 2.80/2.14	2.06/1.60 3.20/2.47 3.01/2.37 4.63/3.38	ns	1
Output pad transition times (high drive)	tpr	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	1.60/1.39 2.94/2.51 1.85/1.48 2.93/2.37	2.23/1.79 4.05/3.17 2.90/2.17 4.56/3.40	3.26/2.50 5.72/4.27 4.75/3.43 7.33/5.26		
Output pad transition times (standard drive)	tpr	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	3.07/2.62 5.82/4.95 3.04/2.47 5.37/4.40	4.22/3.30 7.94/6.19 4.73/3.50 7.70/8.10	6.03/4.48 11.28/8.28 3.01/2.36 4.63/3.38		
Output pad propagation delay (max. drive), 50%–50%	tpo	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	1.92/2.1 2.44/2.53 2.05/2.27 2.71/2.84	2.96/2.96 3.7/3.64 3.32/3.67 4.39/4.51	4.47/4.38 5.54/5.31 5.27/5.85 7.00/7.15	ns	1
Output pad propagation delay (high drive), 50%–50%	tpo	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	2.35/2.49 3.31/3.43 2.58/2.69 3.62/3.60	3.58/3.61 4.9/4.786 4.17/4.27 5.86/5.61	5.35/5.24 7.19/6.8 6.64/6.74 9.34/8.76		
Output pad propagation delay (standard drive), 50%–50%	tpo	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	3.39/3.51 5.28/5.35 3.71/3.68 5.52/5.32	5.03/4.89 7.6/7.14 6.03/5.75 8.80/7.96	7.39/6.95 10.97/9.45 9.64/8.97 13.9/11.3		
Output pad propagation delay (max. drive), 40%–60%	tpo	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	1.942/2.04 2.378/2.48 2.03/2.28 2.59/2.73	2.923/2.95 3.541/3.53 3.19/3.59 4.10/4.33	4.33/4.3 5.29/5.09 4.97/5.64 6.43/6.77	ns	1
Output pad propagation delay (high drive), 40%–60%	tpo	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	2.29/2.44 3.05/3.20 2.45/2.62 3.36/3.39	3.42/3.49 4.46/4.45 3.86/4.07 5.34/5.22	5.05/5.02 6.53/6.3 6.02/6.35 8.40/8.08		
Output pad propagation delay (standard drive), 40%–60%	tpo	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	3.12/3.26 4.60/4.73 3.43/3.46 4.89/4.79	4.58/4.53 6.61/6.32 5.48/5.34 7.75/7.16	6.69/6.42 9.5/8.32 8.65/8.26 12.2/9.97		

Table 16. Slow I/O AC Parameters (continued)

Parameter	Symbol	Test Voltage	Test Capacitance	Min. Rise/Fall	Typ. Rise/Fall	Max. Rise/Fall	Units	Notes
Output enable to output valid delay (max. drive), 50%–50%	tpv	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	2.13/2.01 2.65/2.46 2.31/2.45 2.95/3.01	3.3/3.045 4.038/3.639 3.76/4.00 4.81/4.82	5.072/4.609 6.142/5.423 6.11/6.47 7.81/7.73	ns	1
Output enable to output valid delay (high drive), 50%–50%	tpv	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	2.56/2.43 3.55/3.21 2.85/2.90 3.87/3.78	3.91/3.604 5.21/4.598 4.65/4.64 6.31/5.95	5.937/5.36 7.776/6.694 7.58/7.44 10.3/9.43		
Output enable to output valid delay (standard drive), 50%–50%	tpv	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	3.60/3.28 5.50/4.81 4.04/3.94 5.85/5.56	5.35/4.70 7.93/6.603 6.65/6.21 9.47/8.49	7.97/6.836 11.58/9.338 10.9/9.22 15.5/13.3		
Output enable to output valid delay (max. drive), 40%–60%	tpv	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	2.152/1.7 2.6/2.07 2.28/2.46 2.83/2.93	3.25/2.68 3.88/3.17 3.62/3.92 4.50/4.62	4.93/4.162 5.842/4.846 5.77/6.24 7.20/7.32	ns	1
Output enable to output valid delay (high drive), 40%–60%	tpv	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	2.497/2.036 3.254/2.647 2.71/2.81 3.59/3.56	3.75/3.135 4.8/3.9 4.31/4.23 5.75/5.54	5.633/4.782 7.117/5.84 6.89/7.01 9.23/8.71		
Output enable to output valid delay (standard drive), 40%–60%	tpv	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	3.326/2.7 4.81/3.85 3.73/3.69 5.16/4.99	4.9/3.9 6.9/5.4 6.04/5.77 8.28/7.61	7.269/5.95 10.12/7.86 9.81/9.11 13.4/11.8		
Output pad slew rate (max. drive)	tps	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	0.79/1.12 0.49/0.73 0.30/0.42 0.20/0.29	1.30/1.77 0.84/1.23 0.54/0.73 0.35/0.50	2.02/2.58 1.19/1.58 0.91/1.20 0.60/0.80	V/ns	2
Output pad slew rate (high drive)	tps	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	0.48/0.72 0.27/0.42 0.19/0.28 0.12/0.18	0.76/1.10 0.41/0.62 0.34/0.49 0.34/0.49	1.17/1.56 0.63/0.86 0.58/0/79 0.36/0.49		
Output pad slew rate (standard drive)	tps	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	0.25/0.40 0.14/0.21 0.12/0.18 0.07/0.11	0.40/0.59 0.21/0.32 0.20/0.30 0.11/0.17	0.60/0.83 0.32/0.44 0.34/0.47 0.20/0.27		

Table 16. Slow I/O AC Parameters (continued)

Parameter	Symbol	Test Voltage	Test Capacitance	Min. Rise/Fall	Typ. Rise/Fall	Max. Rise/Fall	Units	Notes
Output pad dI/dt (max. drive)	tdit	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	15 16 7 7	36 38 21 22	76 80 56 58	mA /ns	3
Output pad dI/dt (high drive)	tdit	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	8 9 5 5	20 21 14 15	45 47 38 40		
Output pad dI/dt (standard drive)	tdit	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	4 4 2 2	10 10 7 7	22 23 18 19		
Input pad propagation delay without hysteresis, 50%–50%	tpi	—	1.6 pF	0.82/0.47 0.74/1	1.1/0.76 1.1/1.5	1.6/1.04 1.75/2.16	ns	4
Input pad propagation delay with hysteresis, 50%–50%	tpi	—	1.6 pF	1.1/1.3 1.75/1.63	1.43/1.6 2.67/2.22	2/2 2.92/3		
Input pad propagation delay without hysteresis, 40%–60%	tpi	—	1.6 pF	1.62/1.28 1.82/1.55	1.9/1.56 2.28/1.87	2.38/1.82 2.95/2.54		
Input pad propagation delay with hysteresis, 40%–60%	tpi	—	1.6 pF	1.88/2.1 2.4/2.6	2.2/2.4 3/3.07	2.7/2.75 3.77/3.71		
Input pad transition times without hysteresis	trfi	—	1.6 pF	0.16/0.12	0.23/0.18	0.33/0.29		
Input pad transition times with hysteresis	trfi		1.6 pF	0.16/0.13	0.22/0.18	0.33/0.29		
Maximum input transition times	trm	—	—	—	—	25	ns	5

Note:

1. Maximum condition for tpr, tpo, and tpv: wcs model, 1.1 V, I/O 3.0 V (3.0–3.6 V range) or 1.65 V (1.65–1.95 V range), and 105 °C. Minimum condition for tpr, tpo, and tpv: bcs model, 1.3 V, I/O 3.6 V (3.0–3.6 V range) or 1.95 V (1.65–1.95 V range), and –40 °C. Input transition time from core is 1 ns (20%–80%).
2. Minimum condition for tps: wcs model, 1.1 V, I/O 3.0 V (3.0–3.6 V range) or 1.65 V (1.65–1.95 V range), and 105 °C. tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.
3. Maximum condition for tdit: bcs model, 1.3 V, I/O 3.6 V (3.0–3.6 V range) or 1.95 V (1.65–1.95 V range), and –40 °C.
4. Maximum condition for tpi and trfi: wcs model, 1.1 V, I/O 3.0 V (3.0–3.6 V range) or 1.65 V (1.65–1.95 V range), and 105 °C. Minimum condition for tpi and trfi: bcs model, 1.3 V, I/O 3.6 V or 1.95 V (1.65–1.95 V range), and –40 °C. Input transition time from pad is 5 ns (20%–80%).
5. Hysteresis mode is recommended for input with transition time greater than 25 ns.

3.5.2 Fast I/O AC Parameters

Table 17 shows the fast I/O AC parameters for OVDD = 1.65–1.95 V.

Table 17. Fast I/O AC Parameters for OVDD = 1.65–1.95 V

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units	Notes
Duty cycle	Fduty	—	40	—	60	%	—
Output pad transition times (max. drive)	tpr	25 pF 50 pF	0.88/0.77 1.45/1.24	1.36/1.10 2.20/1.80	2.10/1.70 3.50/2.70	ns	1
Output pad transition times (high drive)	tpr	25 pF 50 pF	1.10/0.92 1.84/1.54	1.65/1.33 2.80/2.20	2.64/2.10 4.40/3.30	ns	
Output pad transition times (standard drive)	tpr	25 pF 50 pF	1.60/1.35 2.74/2.26	2.47/1.95 4.20/3.20	3.99/3.10 6.56/4.86	ns	
Output pad propagation delay (max. drive), 50%–50%	tpo	25 pF 50 pF	1.64/1.53 2.15/2.01	2.68/2.41 3.47/3.08	4.25/3.74 5.50/4.77	ns	1
Output pad propagation delay (high drive), 50%–50%	tpo	25 pF 50 pF	1.82/1.71 2.46/2.29	2.98/2.66 3.96/3.49	4.74/4.13 6.27/5.37	ns	
Output pad propagation delay (standard drive), 50%–50%	tpo	25 pF 50 pF	2.24/2.06 3.17/2.92	3.63/3.15 5.09/4.41	5.73/4.84 8.06/6.75	ns	
Output pad propagation delay (max. drive), 40%–60%	tpo	25 pF 50 pF	1.67/1.58 2.09/1.98	2.63/2.38 3.30/2.97	4.06/3.63 5.14/4.51	ns	1
Output pad propagation delay (high drive), 40%–60%	tpo	25 pF 50 pF	1.94/1.73 2.34/2.22	2.89/2.61 3.69/3.30	4.49/3.97 5.76/5.01	ns	
Output pad propagation delay (standard drive), 40%–60%	tpo	25 pF 50 pF	2.15/1.99 2.94/2.74	3.39/2.99 4.65/4.07	5.28/4.53 7.28/6.13	ns	
Output enable to output valid delay (max. drive), 50%–50%	tpv	25 pF 50 pF	1.87/1.70 2.36/2.16	3.06/2.71 3.83/3.37	4.97/4.30 6.18/5.30	ns	1
Output enable to output valid delay (high drive), 50%–50%	tpv	25 pF 50 pF	2.05/1.88 2.68/2.45	3.67/2.98 4.32/3.78	5.46/4.72 6.98/5.92	ns	
Output enable to output valid delay (standard drive), 50%–50%	tpv	25 pF 50 pF	2.49/2.25 3.40/3.08	4.06/3.50 5.50/4.73	6.57/5.49 8.88/7.37	ns	
Output enable to output valid delay (max. drive), 40%–60%	tpv	25 pF 50 pF	1.90/1.74 2.30/2.13	3.00/2.69 3.65/3.24	4.76/4.18 5.79/5.02	ns	1
Output enable to output valid delay (high drive), 40%–60%	tpv	25 pF 50 pF	2.06/1.90 2.56/2.37	3.28/2.33 4.04/3.59	5.21/4.54 6.43/5.54	ns	
Output enable to output valid delay (standard drive), 40%–60%	tpv	25 pF 50 pF	2.39/2.18 3.16/2.89	3.80/3.18 5.03/4.37	6.05/5.14 8.02/6.72	ns	
Output pad slew rate (max. drive)	tps	25 pF 50 pF	0.40/0.57 0.25/0.36	0.72/0.97 0.43/0.61	1.2/1.5 0.72/0.95	V/ns	2
Output pad slew rate (high drive)	tps	25 pF 50 pF	0.38/0.48 0.20/0.30	0.59/0.81 0.34/0.50	0.98/1.27 0.56/0.72	V/ns	
Output pad slew rate (standard drive)	tps	25 pF 50 pF	0.23/0.32 0.13/0.20	0.40/0.55 0.23/0.34	0.66/0.87 0.38/0.52	V/ns	

Table 17. Fast I/O AC Parameters for OVDD = 1.65–1.95 V (continued)

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units	Notes
Output pad dI/dt (max. drive)	tdit	25 pF 50 pF	7 7	43 46	112 118	mA/ns	3
Output pad dI/dt (high drive)	tdit	25 pF 50 pF	11 12	31 33	81 85	mA/ns	
Output pad dI/dt (standard drive)	tdit	25 pF 50 pF	9 10	27 28	71 74	mA/ns	
Input pad propagation delay without hysteresis, 50%–50%	tpi	1.6 pF	0.74/1	1.1/1.5	1.75/2.16	ns	4
Input pad propagation delay with hysteresis, 50%–50%	tpi	1.6 pF	1.75/1.63	2.67/2.22	2.92/3	ns	
Input pad propagation delay without hysteresis, 40%–60%	tpi	1.6 pF	1.82/1.55	2.28/1.87	2.95/2.54	ns	
Input pad propagation delay with hysteresis, 40%–60%	tpi	1.6 pF	2.4/2.6	3/3.07	3.77/3.71	ns	
Input pad transition times without hysteresis	trfi	1.6 pF	0.16/0.12	0.30/0.18	0.33/0.29	ns	
Input pad transition times with hysteresis	trfi	1.6 pF	0.16/0.13	0.30/0.18	0.33/0.29	ns	
Maximum input transition times	trm	—	—	—	25	ns	5

Note:

1. Maximum condition for tpr, tpo, and tpv: wcs model, 1.1 V, I/O 1.65 V, and 105 °C. Minimum condition for tpr, tpo, and tpv: bcs model, 1.3 V, I/O 1.95 V, and –40 °C. Input transition time from core is 1 ns (20%–80%).
2. Minimum condition for tps: wcs model, 1.1 V, I/O 1.65 V and 105 °C. tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.
3. Maximum condition for tdit: bcs model, 1.3 V, I/O 1.95 V and –40 °C.
4. Maximum condition for tpi and trfi: wcs model, 1.1 V, I/O 1.65 V and 105 °C. Minimum condition for tpi and trfi: bcs model, 1.3 V, I/O 1.95 V and –40 °C. Input transition time from pad is 5 ns (20%–80%).
5. Hysteresis mode is recommended for input with transition time greater than 25 ns.

Table 18 shows the fast I/O AC parameters for OVDD = 3.0–3.6 V.

Table 18. Fast I/O AC Parameters for OVDD = 3.0–3.6 V

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units	Notes
Duty Cycle	Fduty		40		60	%	
Output Pad Transition Times (Max Drive)	tpr	25 pF 50 pF	0.80/0.70 1.40/1.60	1.12/2.51 1.60/2.39	1.64/1.32 2.84/2.10	ns	
Output Pad Transition Times (High Drive)	tpr	25 pF 50 pF	1.00/0.90 1.95/1.66	1.43/1.16 2.66/2.09	2.05/1.60 3.70/2.80	ns	1
Output Pad Transition Times (Standard Drive)	tpr	25 pF 50 pF	1.50/1.30 2.90/2.50	2.09/1.67 3.40/3.09	3.00/2.30 5.56/4.12	ns	
Output Pad Propagation Delay (Max Drive), 50%–50%	tpo	25 pF 50 pF	1.20/1.28 1.67/1.75	1.74/1.73 2.39/2.32	2.67/2.52 3.58/3.33	ns	
Output Pad Propagation Delay (High Drive), 50%–50%	tpo	25 pF 50 pF	1.35/1.42 1.98/2.04	1.95/1.91 2.81/2.68	2.96/2.76 4.16/3.78	ns	1
Output Pad Propagation Delay (Standard Drive), 50%–50%	tpo	25 pF 50 pF	1.77/1.85 2.70/2.78	2.54/2.48 3.82/3.62	3.80/3.60 5.62/5.10	ns	
Output Pad Propagation Delay (Max Drive), 40%–60%	tpo	25 pF 50 pF	1.37/1.50 1.74/1.88	1.94/2.05 2.46/2.55	2.95/3.07 3.71/3.75	ns	
Output Pad Propagation Delay (High Drive), 40%–60%	tpo	25 pF 50 pF	1.48/1.61 1.98/2.10	2.11/2.19 2.78/2.81	3.19/3.26 4.14/4.09	ns	1
Output Pad Propagation Delay (Standard Drive), 40%–60%	tpo	25 pF 50 pF	1.84/1.97 2.58/2.71	2.61/2.67 3.62/3.58	3.95/3.95 5.36/5.15	ns	
Output Enable to Output Valid Delay (Max Drive), 50%–50%	tpv	25 pF 50 pF	1.34/1.32 1.81/1.79	1.91/1.81 2.56/2.40	2.92/2.67 3.83/3.47	ns	
Output Enable to Output Valid Delay (High Drive), 50%–50%	tpv	25 pF 50 pF	1.48/1.47 2.12/2.1	2.12/2.00 2.98/2.76	3.21/2.92 4.41/3.94	ns	1
Output Enable to Output Valid Delay (Standard Drive), 50%–50%	tpv	25 pF 50 pF	1.90/1.90 2.85/2.83	2.70/2.60 4.00/3.70	4.07/3.74 5.86/5.24	ns	
Output Enable to Output Valid Delay (Max Drive), 40%–60%	tpv	25 pF 50 pF	1.55/1.42 1.93/1.81	2.25/2.08 2.77/2.58	3.50/3.31 4.24/3.99	ns	
Output Enable to Output Valid Delay (High Drive), 40%–60%	tpv	25 pF 50 pF	1.67/1.54 2.16/2.03	2.41/2.23 3.08/2.86	3.74/3.51 4.66/4.34	ns	1
Output Enable to Output Valid Delay (Standard Drive), 40%–60%	tpv	25 pF 50 pF	2.02/1.90 2.76/2.63	2.91/2.71 3.91/3.62	4.48/4.21 5.85/5.39	ns	
Output Pad Slew Rate (Max Drive)	tps	25 pF 50 pF	0.96/1.40 0.54/0.83	1.54/2.10 0.85/1.24	2.30/3.00 1.26/1.70	V/ns	
Output Pad Slew Rate (High Drive)	tps	25 pF 50 pF	0.76/1.10 0.41/0.64	1.19/1.71 0.63/0.95	1.78/2.39 0.95/1.30	V/ns	2
Output Pad Slew Rate (Standard Drive)	tps	25 pF 50 pF	0.52/0.78 0.28/0.44	0.80/1.19 0.43/0.64	1.20/1.60 0.63/0.87	V/ns	

Table 18. Fast I/O AC Parameters for OVDD = 3.0–3.6 V (continued)

Output Pad di/dt (Max Drive)	didt	25 pF 50 pF	46 49	108 113	250 262	mA/ns	
Output Pad di/dt (High Drive)	didt	25 pF 50 pF	35 37	82 86	197 207	mA/ns	3
Output Pad di/dt (Standard Drive)	didt	25 pF 50 pF	22 23	52 55	116 121	mA/ns	
Input Pad Propagation Delay without Hysteresis, 50%–50%	tpi	1.6pF	0.729/0.458	0.97/0.0649	1.404/0.97	ns	
Input Pad Propagation Delay with Hysteresis, 50%–50%	tpi	1.6pF	1.203/0.938	1.172/1.187	1.713/1.535	ns	
Input Pad Propagation Delay without Hysteresis, 40%–60%	tpi	1.6pF	0.879/0.977	1.434/1.12	1.854/1.427	ns	4
Input Pad Propagation Delay with Hysteresis, 40%–60%	tpi	1.6pF	1.353/1.457	1.637/1.659	2.163/1.991	ns	
Input Pad Transition Times without Hysteresis	trfi	1.6pF	0.16/0.12	0.23/0.18	0.33/0.29	ns	
Input Pad Transition Times with Hysteresis	trfi	1.6pF	0.16/0.13	0.22/0.18	0.33/0.29	ns	
Maximum Input Transition Times	trm	—	—	—	—	ns	5

Note:

1. Maximum condition for tpr, tpo, and tpv: wcs model, 1.1 V, IO 3.0 V and 105 °C. Min condition for tpr, tpo, and tpv: bcs model, 1.3 V, IO 3.6 V and –40 °C. Input transition time from core is 1ns (20%–80%).
2. Minimum condition for tps: wcs model, 1.1 V, IO 3.0 V and 105 °C. tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.
3. Maximum condition for tdit: bcs model, 1.3 V, IO 3.6 V and –40 °C.
4. Maximum condition for tpi and trfi: wcs model, 1.1 V, IO 3.0 V and 105 °C. Minimum condition for tpi and trfi: bcs model, 1.3 V, IO 3.6 V and –40 °C. Input transition time from pad is 5ns (20%–80%).
5. Hysteresis mode is recommended for input with transition time greater than 25 ns.

3.5.3 DDR I/O AC Parameters

The DDR pad type is configured by the IOMUXC_SW_PAD_CTL_GRP_DDRTYPE register (see Chapter 4, “External Signals and Pin Multiplexing,” in the *i.MX25 Multimedia Applications Processor Reference Manual*).

3.5.3.1 DDR_TYPE = 00 Standard Setting I/O AC Parameters and Requirements

Table 19 shows AC parameters for mobile DDR I/O. These settings are suitable for mDDR and DDR2 1.8V (± 5%) applications.

Table 19. AC Parameters for Mobile DDR I/O

Parameter	Symbol	Load Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units	Notes
Duty cycle	Fduty	—	40	50	60	%	—
Clock frequency	f	—	—	—	133	MHz	1
Output pad transition times (max. drive)	tpr	25 pF 50 pF	0.52/0.51 0.98/0.96	0.79/0.72 1.49/1.34	1.25/1.09 2.31/1.98	ns	1
Output pad transition times (high drive)	tpr	25 pF 50 pF	1.13/1.10 2.15/2.10	1.74/1.55 3.28/2.92	2.71/2.30 5.11/4.31	ns	
Output pad transition times (standard drive)	tpr	25 pF 50 pF	2.26/2.19 4.30/4.18	3.46/3.07 6.59/5.79	5.39/4.56 10.13/8.55	ns	
Output pad propagation delay (max. drive), 50%–50%	tpo	15 pF 35 pF	0.80/1.03 1.06/1.32	1.36/1.50 1.76/1.90	2.21/2.40 2.83/2.82	ns	1
Output pad propagation delay (high drive), 50%–50%	tpo	15 pF 35 pF	1.04/1.27 1.63/1.90	1.74/1.83 2.63/2.69	2.79/2.70 4.18/3.86	ns	
Output pad propagation delay (standard drive), 50%–50%	tpo	15 pF 35 pF	1.55/1.80 2.72/3.06	2.53/2.57 4.31/4.29	4.03/3.76 6.80/6.19	ns	
Output pad propagation delay (max. drive), 40%–60%	tpo	15 pF 35 pF	0.80/0.91 1.06/1.12	1.44/1.59 1.76/1.91	2.24/2.29 2.74/2.75	ns	1
Output pad propagation delay (high drive), 40%–60%	tpo	15 pF 35 pF	1.04/1.09 1.63/1.56	1.73/1.83 2.43/2.52	2.69/2.62 3.79/3.62	ns	
Output pad propagation delay (standard drive), 40%–60%	tpo	15 pF 35 pF	1.50/1.74 2.73/2.42	2.36/2.41 3.77/3.78	3.67/3.46 5.86/5.37	ns	
Output enable to output valid delay (max. drive), 50%–50%	tpv	15 pF 35 pF	1.17/1.01 1.43/1.30	1.93/1.61 2.33/2.00	3.06/2.55 3.69/3.13	ns	1
Output enable to output valid delay (high drive), 50%–50%	tpv	15 pF 35 pF	1.38/1.28 1.97/1.92	2.25/1.99 3.16/2.86	3.58/3.10 5.01/4.39	ns	
Output enable to output valid delay (standard drive), 50%–50%	tpv	15 pF 35 pF	1.92/1.57 3.12/3.16	3.11/2.79 4.97/4.59	4.98/4.13 7.97/6.98	ns	
Output enable to output valid delay (max. drive), 40%–60%	tpv	15 pF 35 pF	1.28/1.12 1.49/1.36	2.01/1.70 2.33/2.01	3.09/2.60 3.60/3.06	ns	1
Output enable to output valid delay (high drive), 40%–60%	tpv	15 pF 35 pF	1.43/1.33 1.90/1.84	2.24/1.99 2.96/2.68	3.47/3.02 4.59/4.03	ns	
Output enable to output valid delay (standard drive), 40%–60%	tpv	15 pF 35 pF	1.85/1.78 2.80/2.81	2.91/2.62 4.37/4.53	4.54/3.96 6.88/6.05	ns	

Table 19. AC Parameters for Mobile DDR I/O (continued)

Parameter	Symbol	Load Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units	Notes
Output pad slew rate (max. drive)	tps	25 pF 50 pF	0.80/0.92 0.43/0.50	1.35/1.50 0.72/0.81	2.23/2.27 1.66/1.68	V/ns	2
Output pad slew rate (high drive)	tps	25 pF 50 pF	0.37/0.43 0.19/0.23	0.62/0.70 0.33/0.37	1.03/1.05 0.75/0.77	V/ns	
Output pad slew rate (standard drive)	tps	25 pF 50 pF	0.18/0.22 0.10/0.12	0.31/0.35 0.16/0.18	0.51/0.53 0.38/0.39	V/ns	
Output pad dI/dt (max. drive)	tdit	25 pF 50 pF	64 69	171 183	407 432	mA/ns	3
Output pad dI/dt (high drive)	tdit	25 pF 50 pF	37 39	100 106	232 246	mA/ns	
Output pad di/dt (standard drive)	tdit	25 pF 50 pF	18 20	50 52	116 123	mA/ns	
Input pad transition times	trfi	1.0 pF	0.07/0.08	0.11/0.13	0.16/0.20	ns	4
Input pad propagation delay, 50%–50%	tpi	1.0 pF	0.77/1.00	1.22/1.45	1.89/2.21	ns	
Input pad propagation delay, 40%–60%	tpi	1.0 pF	1.59/1.82	2.04/2.27	2.69/3.01	ns	

Note:

1. Maximum condition for tpr, tpo, tpi, and tpv: wcs model, 1.1 V, I/O 1.65 V, and 105 °C. Minimum condition for tpr, tpo, and tpv: bcs model, 1.3 V, I/O 1.95 V and –40 °C. Input transition time from core is 1 ns (20%–80%).
2. Minimum condition for tps: wcs model, 1.1 V, I/O 1.65 V, and 105 °C. tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.
3. Maximum condition for tdit: bcs model, 1.3 V, I/O 1.95 V, and –40 °C.
4. Maximum condition for tpi and trfi: wcs model, 1.1 V, I/O 1.65 V and 105 °C. Minimum condition for tpi and trfi: bcs model, 1.3 V, I/O 1.95 V and –40 °C. Input transition time from pad is 5 ns (20%–80%).

Table 20 shows the AC parameters for mobile DDR pbijtov18_33_ddr_clk I/O.

Table 20. AC Parameters for Mobile DDR pbijtov18_33_ddr_clk I/O

Parameter	Symbol	Load Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units	Notes
Duty cycle	Fduty	—	40	50	60	%	—
Clock frequency	f	—	—	—	133	MHz	1
Output pad transition times (max. drive)	tpr	25 pF 50 pF	0.52/0.51 0.98/0.96	0.79/0.72 1.49/1.34	1.25/1.09 2.31/1.98	ns	1
Output pad transition times (high drive)	tpr	25 pF 50 pF	1.13/1.10 2.15/2.10	1.74/1.55 3.28/2.92	2.71/2.30 5.11/4.31	ns	
Output pad transition times (standard drive)	tpr	25 pF 50 pF	2.26/2.19 4.30/4.18	3.46/3.07 6.59/5.79	5.39/4.56 10.13/8.55	ns	

Table 20. AC Parameters for Mobile DDR pbijtov18_33_ddr_clk I/O (continued)

Parameter	Symbol	Load Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units	Notes
Output pad propagation delay (max. drive), 50%–50% input signals and crossing of output signals	tpo	15 pF 35 pF	1.28/1.19 1.56/1.47	1.97/1.83 2.37/2.23	2.98/2.78 3.57/3.37	ns	1
Output pad propagation delay (high drive), 50%–50% input signals and crossing of output signals	tpo	15 pF 35 pF	1.54/1.43 2.14/2.04	2.34/2.20 3.22/3.08	3.54/3.33 4.85/4.65	ns	
Output pad propagation delay (standard drive), 50%–50% input signals and crossing of output signals	tpo	15 pF 35 pF	2.05/1.94 3.27/3.16	3.11/2.96 4.86/4.72	4.70/4.50 7.33/7.12	ns	
Output pad propagation delay (max. drive), 40%–60% input signals and crossing of output signals	tpo	15 pF 35 pF	1.45/1.36 1.73/1.64	2.13/2.00 2.53/2.40	3.14/2.94 3.74/3.54	ns	1
Output pad propagation delay (high drive), 40%–60% input signals and crossing of output signals	tpo	15 pF 35 pF	1.70/1.60 2.31/2.21	2.51/2.37 3.38/3.24	3.70/3.50 5.02/4.82	ns	
Output pad propagation delay (standard drive), 40%–60% input signals and crossing of output signals	tpo	15 pF 35 pF	2.22/2.11 3.43/3.32	3.27/3.13 5.02/4.88	4.87/4.66 7.49/7.29	ns	
Output enable to output valid delay (max. drive), 50%–50%	tpv	15 pF 35 pF	1.16/1.12 1.42/1.41	1.91/1.81 2.31/2.20	3.10/2.89 3.72/3.47	ns	1
Output enable to output valid delay (high drive), 50%–50%	tpv	15 pF 35 pF	1.39/1.39 1.98/2.02	2.28/2.18 3.18/3.04	3.69/3.43 5.08/4.69	ns	
Output enable to output valid delay (standard drive), 50%–50%	tpv	15 pF 35 pF	1.90/1.94 3.07/3.20	3.09/2.94 4.88/4.66	4.95/4.55 7.73/7.05	ns	
Output enable to output valid delay (max. drive), 40%–60%	tpv	15 pF 35 pF	1.28/1.24 1.49/1.47	2.00/1.90 2.32/2.21	3.14/2.93 3.64/3.41	ns	1
Output enable to output valid delay (high drive), 40%–60%	tpv	15 pF 35 pF	1.45/1.44 1.92/1.95	2.28/2.19 2.99/2.87	3.60/3.36 4.69/4.36	ns	
Output enable to output valid delay (standard drive), 40%–60%	tpv	15 pF 35 pF	1.85/1.88 2.78/2.88	2.92/2.79 4.34/4.16	4.5894.25 6.79/6.24	ns	
Output pad slew rate (max. drive)	tps	25 pF 50 pF	0.37/0.45 0.30/0.36	0.64/0.79 0.52/0.61	1.14/1.36 0.90/1.02	V/ns	2
Output pad slew rate (high drive)	tps	25 pF 50 pF	0.30/0.37 0.21/0.25	0.51/0.63 0.36/0.42	091/1.06 0.63/0.67	V/ns	
Output pad slew rate (standard drive)	tps	25 pF 50 pF	0.22/0.26 0.13/0.16	0.37/0.44 0.23/0.26	0.65/0.72 0.39/0.40	V/ns	

Table 20. AC Parameters for Mobile DDR pbijtov18_33_ddr_clk I/O (continued)

Parameter	Symbol	Load Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units	Notes
Output pad dI/dt (max. drive)	tdit	25 pF 50 pF	65 70	171 183	426 450	mA/ns	3
Output pad dI/dt (high drive)	tdit	25 pF 50 pF	31 33	82 87	233 245	mA/ns	
Output pad dI/dt (standard drive)	tdit	25 pF 50 pF	16 17	43 46	115 120	mA/ns	
Input pad transition times	trfi	1.0 pF	0.07/0.08	0.11/0.13	0.16/0.20	ns	4
Input pad propagation delay, 50%–50%	tpi	1.0 pF	0.84/0.84	1.40/1.34	2.25/2.16	ns	
Input pad propagation delay, 40%–60%	tpi	1.0 pF	1.66/1.66	2.22/2.16	3.06/2.97	ns	

Note:

1. Maximum condition for tpr, tpo, tpi, and tpv: wcs model, 1.1 V, I/O 1.65 V, and 105 °C. Minimum condition for tpr, tpo, and tpv: bcs model, 1.3 V, I/O 1.95 V and –40 °C. Input transition time from core is 1 ns (20%–80%).
2. Minimum condition for tps: wcs model, 1.1 V, I/O 1.65 V, and 105 °C. tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.
3. Maximum condition for tdit: bcs model, 1.3 V, I/O 1.95 V, and –40 °C.
4. Maximum condition for tpi and trfi: wcs model, 1.1 V, I/O 1.65 V and 105 °C. Minimum condition for tpi and trfi: bcs model, 1.3 V, I/O 1.95 V and –40 °C. Input transition time from pad is 5 ns (20%–80%).

Table 21 shows the AC requirements for mobile DDR I/O.

Table 21. AC Requirements for Mobile DDR I/O

Parameter	Symbol	Min.	Max.	Units
AC input logic high	VIH(ac)	0.8 × OVDD	OVDD+0.3	V
AC input logic low	VIL(ac)	–0.3	0.2 × OVDD	V
AC differential input voltage	Vid(ac)	0.6 × OVDD	OVDD+0.6	V
AC differential cross point voltage for input	Vix(ac)	0.4 × OVDD	OVDD+0.6	V

3.5.3.2 DDR_TYPE = 01 SDRAM I/O AC Parameters and Requirements

Table 22 shows AC parameters for SDRAM I/O.

Table 22. AC Parameters for SDRAM I/O

Parameter	Symbol	Load Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units	Notes
Duty cycle	Fduty	—	40	50	60	%	—
Clock frequency	f	—	—	—	125	MHz	1

Table 22. AC Parameters for SDRAM I/O (continued)

Parameter	Symbol	Load Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units	Notes
Output pad transition times (max. drive)	tpr	25 pF 50 pF	0.82/0.87 1.56/1.67	1.14/1.13 2.13/2.09	1.62/1.50 3.015/2.77	ns	1
Output pad transition times (high drive)	tpr	25 pF 50 pF	1.23/1.31 2.31/2.47	1.71/1.68 3.22/3.12	2.39/2.22 4.53/4.16	ns	
Output pad transition times (standard drive)	tpr	25 pF 50 pF	2.44/2.60 4.65/4.99	3.38/3.27 6.38/6.23	4.73/4.38 9.05/8.23	ns	
Output pad propagation delay (max. drive), 50%–50%	tpo	15 pF 35 pF	0.97/1.19 2.85/3.21	1.69/0.75 2.02/2.30	2.17/2.46 2.93/3.27	ns	1
Output pad propagation delay (high drive), 50%–50%	tpo	15 pF 35 pF	1.15/1.39 3.57/3.91	1.72/1.93 2.54/2.85	2.51/2.77 3.66/3.97	ns	
Output pad propagation delay (standard drive), 50%–50%	tpo	15 pF 35 pF	2.01/1.57 5.73/6.05	2.45/2.69 4.10/4.51	3.54/3.77 5.84/6.13	ns	
Output pad propagation delay (max. drive), 40%–60%	tpo	15 pF 35 pF	1.06/1.26 1.38/1.38	1.53/1.73 1.96/2.23	2.18/2.47 2.78/3.12	ns	1
Output pad propagation delay (high drive), 40%–60%	tpo	15 pF 35 pF	1.15/1.20 1.75/1.67	1.72/1.93 2.37/2.66	2.45/2.71 3.35/3.67	ns	
Output pad propagation delay (standard drive), 40%–60%	tpo	15 pF 35 pF	1.91/2.01 2.88/2.56	2.30/2.52 3.59/3.97	3.26/3.50 5.06/5.36	ns	
Output enable to output valid delay (max. drive), 50%–50%	tpv	15 pF 35 pF	0.90/1.27 1.07/1.77	1.44/1.89 1.66/2.51	2.19/2.87 2.51/3.69	ns	1
Output enable to output valid delay (high drive), 50%–50%	tpv	15 pF 35 pF	1.01/1.48 1.37/2.33	1.58/2.16 2.06/3.09	2.38/3.23 3.06/4.46	ns	
Output enable to output valid delay (standard drive), 50%–50%	tpv	15 pF 35 pF	1.32/2.14 2.04/3.67	2.02/3.00 3.00/4.91	3.01/4.36 4.40/6.90	ns	
Output enable to output valid delay (max. drive), 40%–60%	tpv	15 pF 35 pF	1.03/1.34 1.16/1.74	1.54/1.94 1.74/2.44	2.26/2.88 2.55/3.54	ns	—
Output enable to output valid delay (high drive), 40%–60%	tpv	15 pF 35 pF	1.11/1.51 1.39/2.10	1.65/2.15 2.03/2.89	2.43/3.16 2.95/4.13	ns	
Output enable to output valid delay (standard drive), 40%–60%	tpv	15 pF 35 pF	1.35/2.03 1.91/3.23	1.99/2.83 2.76/4.30	2.89/4.03 3.98/6.01	ns	
Output pad slew rate (max. drive)	tps	25 pF 50 pF	1.11/1.20 0.97/0.65	1.74/1.75 0.92/0.94	2.42/2.46 1.39/1.30	V/ns	2
Output pad slew rate (high drive)	tps	25 pF 50 pF	0.76/0.80 0.40/0.43	1.16/1.19 0.61/0.63	1.76/1.66 0.93/0.87	V/ns	
Output pad slew rate (standard drive)	tps	25 pF 50 pF	0.38/0.41 0.20/0.22	0.59/0.60 0.31/0.32	0.89/0.82 0.47/0.43	V/ns	

Table 22. AC Parameters for SDRAM I/O (continued)

Parameter	Symbol	Load Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units	Notes
Output pad dI/dt (max. drive)	tdit	25 pF 50 pF	89 94	198 209	398 421	mA/ns	3
Output pad dI/dt (high drive)	tdit	25 pF 50 pF	59 62	132 139	265 279	mA/ns	
Output pad dI/dt (standard drive)	tdit	25 pF 50 pF	29 31	65 69	132 139	mA/ns	
Input pad transition times	trfi	1.0 pF	0.07/0.08	0.11/0.12	0.16/0.20	ns	4
Input pad propagation delay, 50%–50%	tpi	1.0 pF	0.35/1.17	0.63/1.53	1.16/2.04	ns	
Input pad propagation delay, 40%–60%	tpi	—	1.18/1.99	1.45/2.35	1.97/2.85	—	

Note:

1. Maximum condition for tpr, tpo, tpi, and tpv: wcs model, 1.1 V, I/O 3.0 V, and 105 °C. Minimum condition for tpr, tpo, and tpv: bcs model, 1.3 V, I/O 3.6 V and –40 °C. Input transition time from core is 1 ns (20%–80%).
2. Minimum condition for tps: wcs model, 1.1 V, I/O 3.0 V, and 105 °C. tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.
3. Maximum condition for tdit: bcs model, 1.3 V, I/O 3.6 V, and –40 °C.
4. Maximum condition for tpi and trfi: wcs model, 1.1 V, I/O 3.0 V and 105 °C. Minimum condition for tpi and trfi: bcs model, 1.3 V, I/O 3.6 V and –40 °C. Input transition time from pad is 5 ns (20%–80%).

Table 23 shows AC parameters for SDRAM pbijtov18_33_ddr_clk I/O.

Table 23. AC Parameters for SDRAM pbijtov18_33_ddr_clk I/O

Parameter	Symbol	Load Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units	Notes
Duty cycle	Fduty	—	40	50	60	%	—
Clock frequency	f	—	—	—	125	MHz	1
Output pad transition times (max. drive)	tpr	25 pF 50 pF	0.82/0.87 1.56/1.67	1.14/1.13 2.13/2.09	1.62/1.50 3.015/2.77	ns	1
Output pad transition times (high drive)	tpr	25 pF 50 pF	1.23/1.31 2.31/2.47	1.71/1.68 3.22/3.12	2.39/2.22 4.53/4.16	ns	
Output pad transition times (standard drive)	tpr	25 pF 50 pF	2.44/2.60 4.65/4.99	3.38/3.27 6.38/6.23	4.73/4.38 9.05/8.23	ns	
Output pad propagation delay (max. drive), 50%–50% input signals and crossing of output signals	tpo	15 pF 35 pF	1.50/1.40 1.95/1.85	2.23/2.07 2.81/2.66	3.28/3.04 4.06/3.82	ns	1
Output pad propagation delay (high drive), 50%–50% input signals and crossing of output signals	tpo	15 pF 35 pF	1.69/1.59 2.35/2.25	2.48/2.32 3.35/3.19	3.63/3.38 4.80/4.56	ns	
Output pad propagation delay (standard drive), 50%–50% input signals and crossing of output signals	tpo	15 pF 35 pF	2.26/2.15 3.59/3.49	3.24/3.08 4.98/4.82	4.66/4.42 7.00/6.75	ns	

Table 23. AC Parameters for SDRAM pbijtov18_33_ddr_clk I/O (continued)

Parameter	Symbol	Load Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units	Notes
Output pad propagation delay (max. drive), 40%–60% input signals and crossing of output signals	tpo	15 pF 35 pF	1.67/1.57 2.11/2.02	2.39/2.24 2.97/2.82	3.45/3.21 4.23/3.99	ns	1
Output pad propagation delay (high drive), 40%–60% input signals and crossing of output signals	tpo	15 pF 35 pF	1.85/1.75 2.52/2.42	2.65/2.49 3.51/3.36	3.79/3.55 4.97/4.72	ns	
Output pad propagation delay (standard drive), 40%–60% input signals and crossing of output signals	tpo	15 pF 35 pF	2.42/2.32 3.76/3.66	3.40/3.25 5.15/4.99	4.83/4.59 7.17/6.92	ns	
Output enable to output valid delay (max. drive), 50%–50%	tpv	15 pF 35 pF	1.37/1.34 1.77/1.83	2.22/2.02 2.77/2.63	3.53/3.12 4.30/3.92	ns	1
Output enable to output valid delay (high drive), 50%–50%	tpv	15 pF 35 pF	1.55/1.56 2.15/2.29	2.46/2.30 3.28/3.21	3.87/3.47 5.02/4.67	ns	
Output enable to output valid delay (standard drive), 50%–50%	tpv	15 pF 35 pF	2.07/2.18 3.28/3.65	3.20/3.08 4.84/4.90	4.92/4.50 7.21/6.89	ns	
Output enable to output valid delay (max. drive), 40%–60%	tpv	15 pF 35 pF	1.46/1.42 1.77/1.81	2.28/2.07 2.71/2.56	3.54/3.13 4.15/3.78	ns	
Output enable to output valid delay (high drive), 40%–60%	tpv	15 pF 35 pF	1.60/1.59 2.07/2.18	2.47/2.30 3.12/3.02	3.82/3.41 4.72/4.37	ns	
Output enable to output valid delay (standard drive), 40%–60%	tpv	15 pF 35 pF	2.01/2.09 2.96/3.26	3.05/2.91 4.34/4.37	4.64/4.23 6.45/6.13	ns	
Output pad slew rate (max. drive)	tps	25 pF 50 pF	1.11/1.20 0.60/0.65	1.74/1.75 0.93/0.95	2.63/2.48 1.39/1.29	V/ns	2
Output pad slew rate (high drive)	tps	25 pF 50 pF	0.75/0.81 0.40/0.43	1.16/1.18 0.62/0.64	1.76/1.65 094/0.87	V/ns	
Output pad slew rate (standard drive)	tps	25 pF 50 pF	0.38/0.41 0.20/0.22	0.59/0.61 0.31/0.32	0.89/0.83 0.47/0.43	V/ns	
Output pad dI/dt (max. drive)	tdit	25 pF 50 pF	89 95	202 213	435 456	mA/ns	3
Output pad dI/dt (high drive)	tdit	25 pF 50 pF	60 63	135 142	288 302	mA/ns	
Output pad dI/dt (standard drive)	tdit	25 pF 50 pF	29 31	67 70	144 150	mA/ns	
Input pad transition times	trfi	1.0 pF	0.07/0.08	0.11/0.12	0.16/0.20	ns	4
Input pad propagation delay, 50%–50%	tpi	1.0 pF	0.56/0.69	0.87/1.08	1.37/1.62	ns	
Input pad propagation delay, 40%–60%	tpi		1.38/1.51	1.68/1.89	2.18/2.42		

Note:

1. Maximum condition for tpr, tpo, tpi, and tpv: wcs model, 1.1 V, I/O 3.0 V, and 105 °C. Minimum condition for tpr, tpo, and tpv: bcs model, 1.3 V, I/O 3.6 V and –40 °C. Input transition time from core is 1 ns (20%–80%).
2. Minimum condition for tps: wcs model, 1.1 V, I/O 3.0 V, and 105 °C. tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.

3. Maximum condition for tdit: bcs model, 1.3 V, I/O 3.6 V, and –40 °C.
4. Maximum condition for tpi and trfi: wcs model, 1.1 V, I/O 3.0 V and 105 °C. Minimum condition for tpi and trfi: bcs model, 1.3 V, I/O 3.6 V and –40 °C. Input transition time from pad is 5 ns (20%–80%).

3.5.3.3 DDR_TYPE = 10 Max Setting I/O AC Parameters and Requirements

Table 24 shows AC parameters for DDR2 I/O.

Table 24. AC Parameters for DDR2 I/O

Parameter	Symbol	Load Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units	Notes
Duty cycle	Fduty	—	40	50	60	%	—
Clock frequency	f	—	—	—	133	MHz	—
Output pad transition times	tpr	25 pF 50 pF	0.53/0.52 1.01/0.98	0.80/0.72 1.49/1.34	1.19/1.04 2.21/1.90	ns	1
Output pad propagation delay, 50%–50%	tpo	25 pF 50 pF	0.93/1.25 1.26/1.54	1.56/1.70 2.07/2.19	2.52/2.53 3.29/3.24	ns	1
Output pad propagation delay, 40%–60%	tpo	25 pF 50 pF	1.01/1.17 1.27/1.53	1.60/1.75 2.00/2.14	2.49/2.52 3.11/3.10	ns	1
Output enable to output valid delay, 50%–50%	tpv	25 pF 50 pF	1.30/1.19 1.62/1.54	2.17/1.81 2.56/2.29	3.35/2.84 3.35/2.54	ns	1
Output enable to output valid delay, 40%–60%	tpv	25 pF 50 pF	1.39/1.27 1.64/1.55	2.13/1.86 2.62/2.23	3.38/2.83 4.14/2.38	ns	1
Output pad slew rate	tps	25 pF 50 pF	0.86/0.98 0.46/054	1.35/1.5 0.72/0.81	2.15/2.19 1.12/1.16	V/ns	2
Output pad dI/dt	tdit	25 pF 50 pF	65 70	157 167	373 396	mA/ns	3
Input pad transition times	trfi	1.0 pF	0.07/0.08	0.10/0.12	0.17/0.20	ns	4
Input pad propagation delay, 50%–50%	tpi	1.0 pF	0.83/0.99	1.23/1.49	1.79/2.04	ns	
Input pad propagation delay, 40%–60%	tpi	1.0 pF	1.65/1.81	2.05/2.31	2.60/2.84	ns	

Note:
1. Maximum condition for tpr, tpo, tpi, and tpv: wcs model, 1.1 V, I/O 1. V, and 105 °C. Minimum condition for tpr, tpo, and tpv: bcs model, 1.3 V, I/O 1.9 V and –40 °C. Input transition time from core is 1 ns (20%–80%).
2. Minimum condition for tps: wcs model, 1.1 V, I/O 1.7 V, and 105 °C. tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.
3. Maximum condition for tdit: bcs model, 1.3 V, I/O 1.9 V, and –40 °C.
4. Maximum condition for tpi and trfi: wcs model, 1.1 V, I/O 1.7 V and 105 °C. Minimum condition for tpi and trfi: bcs model, 1.3 V, I/O 1.9 V and –40 °C. Input transition time from pad is 5 ns (20%–80%).

Table 25 shows AC parameters for DDR2 pbijtov18_33_ddr_clk I/O.

Table 25. AC Parameters for DDR2 pbijtov18_33_ddr_clk I/O

Parameter	Symbol	Load Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units	Notes
Duty cycle	Fduty	—	40	50	60	%	—
Clock frequency	f	—	—	—	133	MHz	—
Output pad transition times	tpr	25 pF 50 pF	0.53/0.52 1.01/0.98	0.80/0.72 1.49/1.34	1.19/1.04 2.21/1.90	ns	1
Output pad propagation delay, 50%–50% input signals and crossing of output signals	tpo	25 pF 50 pF	1.3/1.21 1.59/1.5	1.97/1.84 2.37/2.24	2.91/2.71 3.48/3.28	ns	1
Output pad propagation delay, 40%–60% input signals and crossing of output signals	tpo	25 pF 50 pF	1.47/1.38 1.75/1.67	2.13/2.00 2.54/2.40	3.072/2.87 3.65/3.45	ns	1
Output enable to output valid delay, 50%–50%	tpv	25 pF 50 pF	1.32/1.28 1.66/1.65	2.11/2.00 2.61/2.50	3.31/3.12 4.06/3.81	ns	1
Output enable to output valid delay, 40%–60%	tpv	25 pF 50 pF	1.40/1.37 1.67/1.66	2.16/2.06 2.56/2.45	3.30/3.13 3.89/3.67	ns	1
Output pad slew rate	tps	25 pF 50 pF	0.86/0.98 0.46/054	1.35/1.5 0.72/0.81	2.15/2.19 1.12/1.16	V/ns	2
Output pad dI/dt	tdit	25 pF 50 pF	72 77	172 183	400 422	mA/ns	3
Input pad transition times	trfi	1.0 pF	0.07/0.08	0.10/0.12	0.17/0.20	ns	4
Input pad propagation delay, 50%–50%	tpi	1.0 pF	0.89/0.87	1.41/1.37	2.16/2.07	ns	
Input pad propagation delay, 40%–60%	tpi	1.0 pF	1.71/1.69	2.22/2.18	2.98/2.88	ns	

Note:

1. Maximum condition for tpr, tpo, tpi, and tpv: wcs model, 1.1 V, I/O 1. V, and 105 °C. Minimum condition for tpr, tpo, and tpv: bcs model, 1.3 V, I/O 1.9 V and –40 °C. Input transition time from core is 1 ns (20%–80%).
2. Minimum condition for tps: wcs model, 1.1 V, I/O 1.7 V, and 105 °C. tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.
3. Maximum condition for tdit: bcs model, 1.3 V, I/O 1.9 V, and –40 °C.
4. Maximum condition for tpi and trfi: wcs model, 1.1 V, I/O 1.7 V and 105 °C. Minimum condition for tpi and trfi: bcs model, 1.3 V, I/O 1.9 V and –40 °C. Input transition time from pad is 5 ns (20%–80%).

Table 26 shows the AC requirements for DDR2 I/O.

Table 26. AC Requirements for DDR2 I/O

Parameter[1]	Symbol	Min.	Max.	Units
AC input logic high	VIH(ac)	OVDD/2 + 0.25	OVDD + 0.3	V
AC input logic low	VIL(ac)	–0.3	OVDD/2 – 0.25	V
AC differential input voltage[2]	Vid(ac)	0.5	OVDD + 0.6	V
AC differential cross point voltage for input[3]	Vix(ac)	OVDD/2–0.175	OVDD/2 + 0.175	V
AC differential cross point voltage for output[4]	Vox(ac)	OVDD/2–0.125	OVDD/2 + 0.125	V

1 Note that the Jedec SSTL_18 specification (JESD8-15a) for an SSTL interface for class II operation supersedes any specification in this document.

2 Vid(ac) specifies the input differential voltage |Vtr–Vcp| required for switching, where Vtr is the "true" input signal and Vcp is the "complementary" input signal. The minimum value is equal to Vih(ac)–Vil(ac)

3 The typical value of Vix(ac) is expected to be about 0.5 × OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

4 The typical value of Vox(ac) is expected to be about 0.5 × OVDD and Vox(ac) is expected to track variation in OVDD. Vox(ac) indicates the voltage at which differential output signal must cross. Cload = 25 pF.

3.6 Module Timing and Electrical Parameters

This section contains the timing and electrical parameters for i.MX25 modules.

3.6.1 1-Wire Timing Parameters

Figure 7 shows the reset and presence pulses (RPP) timing for 1-Wire, and Table 27 lists the RPP timing parameters.

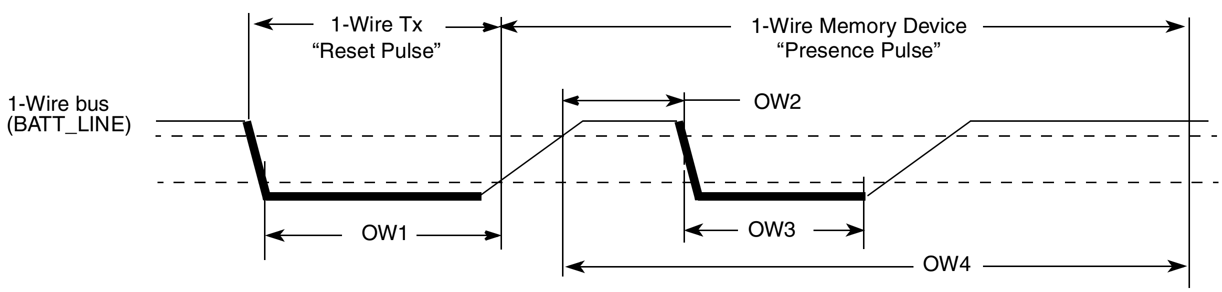


Figure 7. 1-Wire RPP Timing Diagram

Table 27. RPP Sequence Delay Comparisons Timing Parameters

ID	Parameters	Symbol	Min.	Typ.	Max.	Units
OW1	Reset Time Low	t_{RSTL}	480	511	—	us
OW2	Presence Detect High	t_{PDH}	15	—	60	us
OW3	Presence Detect Low	t_{PDL}	60	—	240	us
OW4	Reset Time High	t_{RSTH}	480	512	—	us

Figure 8 shows write 0 sequence timing, and Table 28 describes the timing parameters (OW5–OW6) that are shown in the figure.

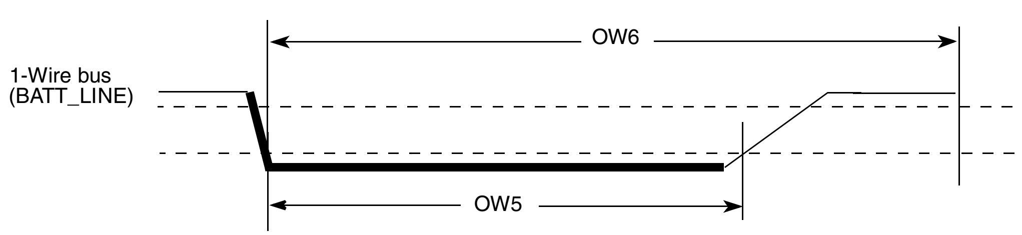


Figure 8. Write 0 Sequence Timing Diagram

Table 28. WR0 Sequence Timing Parameters

ID	Parameter	Symbol	Min.	Typ.	Max.	Units
OW5	Write 0 Low Time	t_{WR0_low}	60	100	120	µs
OW6	Transmission Time Slot	t_{SLOT}	OW5	117	120	µs

Figure 9 and Figure 10 show write 1 and read sequence timing, respectively. Table 29 describes the timing parameters (OW7–OW8) that are shown in the figure.

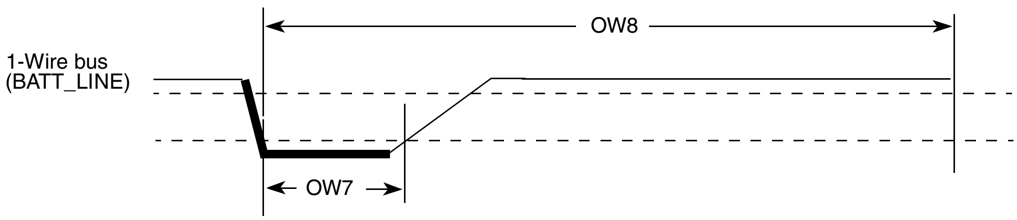


Figure 9. Write 1 Sequence Timing Diagram

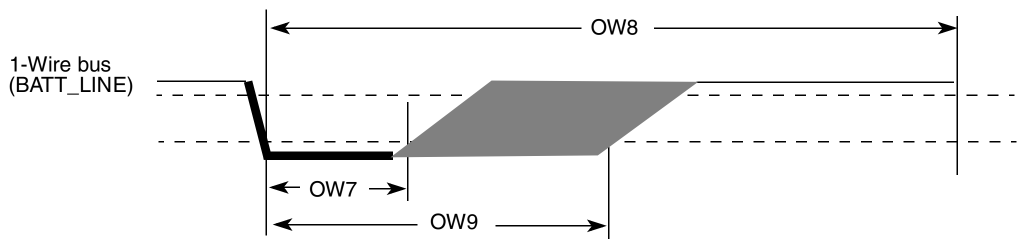


Figure 10. Read Sequence Timing Diagram

Table 29. WR1 /RD Timing Parameters

ID	Parameter	Symbol	Min.	Typ.	Max.	Units
OW7	Write 1 / read low time	t_{LOW1}	1	5	15	µs
OW8	Transmission time slot	t_{SLOT}	60	117	120	µs
OW9	Release time	$t_{RELEASE}$	15	—	45	µs

3.6.2 ATA Timing Parameters

Table 30 shows parameters used to specify the ATA timing. These parameters depend on the implementation of the ATA interface on silicon, the bus buffer used, the cable delay and cable skew.

Table 30. Timing Parameters

Name	Description	Value/Contributing Factor
T	Bus clock period	Peripheral clock frequency
ti_ds	Set-up time **ata_data** to **ata_iordy** edge (UDMA-in only) UDMA0 UDMA1 UDMA2,UDMA3 UDMA4 UDMA5	 15 ns 10 ns 7 ns 5 ns 4 ns
ti_dh	Hold time ata_iordy edge to ata_data (UDMA-in only) UDMA0,UDMA1,UDMA2,UDMA3,UDMA4 UDMA5	 5.0 ns 4.6 ns
tco	Propagation delay bus clock L-to-H to ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_dior, ata_diow, ata_dmack, ata_data, ata_buffer_en	12.0 ns
tsu	Set-up time **ata_data** to bus clock L-to-H	8.5 ns
tsui	Set-up time **ata_iordy** to bus clock H-to-L	8.5 ns
thi	Hold time **ata_iordy** to bus clock H-to-L	2.5 ns
tskew1	Maximum difference in propagation delay bus clock L-to-H to any of the following signals **ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_dior, ata_diow, ata_dmack, ata_data** (write), **ata_buffer_en**	7 ns
tskew2	Maximum difference in buffer propagation delay for any of the following signals **ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_dior, ata_diow, ata_dmack, ata_data** (write), **ata_buffer_en**	Transceiver
tskew3	Maximum difference in buffer propagation delay for any of the following signals **ata_iordy, ata_data** (read)	Transceiver
tbuf	Maximum buffer propagation delay	Transceiver
tcable1	cable propagation delay for **ata_data**	Cable
tcable2	cable propagation delay for control signals **ata_dior**, **ata_diow**, **ata_iordy**, **ata_dmack**	Cable
tskew4	Maximum difference in cable propagation delay between **ata_iordy** and **ata_data** (read)	Cable
tskew5	Maximum difference in cable propagation delay between (**ata_dior**, **ata_diow**, **ata_dmack**) and **ata_cs0**, **ata_cs1**, **ata_da2**, **ata_da1**, **ata_da0**, **ata_data**(write)	Cable
tskew6	Maximum difference in cable propagation delay without accounting for ground bounce	Cable

3.6.2.1 PIO Mode Timing Parameters

Figure 11 shows a timing diagram for PIO read mode.

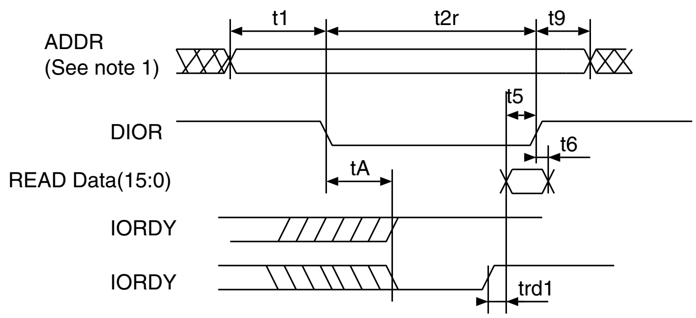


Figure 11. PIO Read Mode Timing

To meet PIO read mode timing requirements, a number of timing parameters must be controlled. Table 31 shows timing parameters and their determining relations, and indicates parameters that can be adjusted to meet required conditions.

Table 31. Timing Parameters for PIO Read Mode

ATA Parameter	PIO Read Mode Timing Parameter[1]	Relation	Adjustable Parameter
t1	t1	t1(min.) = time_1 × T – (tskew1 + tskew2 + tskew5)	time_1
t2	t2r	t2(min.) = time_2r × T – (tskew1 + tskew2 + tskew5)	time_2r
t9	t9	t9(min.) = time_9 × T – (tskew1 + tskew2 + tskew6)	time_9
t5	t5	t5(min.) = tco + tsu + tbuf + tbuf + tcable1 + tcable2	If not met, increase time_2
t6	t6	0	—
tA	tA	tA(min.) = (1.5 + time_ax) × T – (tco + tsui + tcable2 + tcable2 + 2 × tbuf)	time_ax
trd	trd1	trd1(max.) = (–trd) + (tskew3 + tskew4) trd1(min.) = (time_pio_rdx – 0.5) × T – (tsu + thi) (time_pio_rdx – 0.5) × T > tsu + thi + tskew3 + tskew4	time_pio_rdx
t0	—	t0(min.) = (time_1 + time_2 + time_9) × T	time_1, time_2r, time_9

[1] See Figure 11.

Figure 12 gives timing waveforms for PIO write mode.

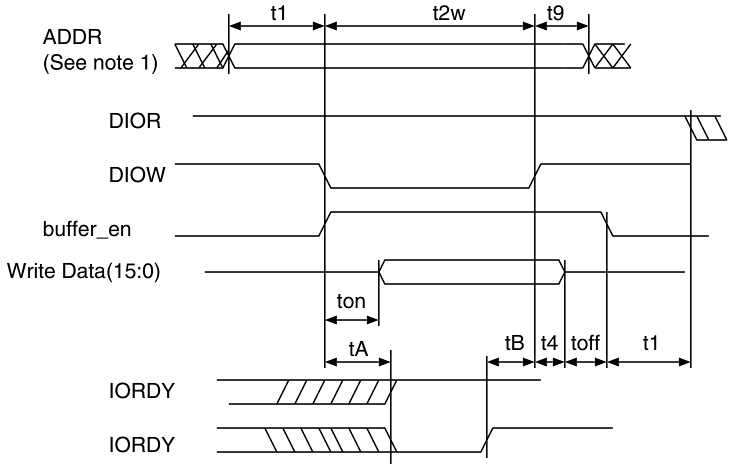


Figure 12. PIO Write Mode Timing

To meet PIO write mode timing requirements, a number of timing parameters must be controlled. Table 32 shows timing parameters and their determining relations, and indicates parameters that can be adjusted to meet required conditions.

Table 32. Timing Parameters for PIO Write Mode

ATA Parameter	PIO Write Mode Timing Parameter[1]	Relation	Adjustable Parameter(s)
t1	t1	t1(min.) = time_1 × T – (tskew1 + tskew2 + tskew5)	time_1
t2	t2w	t2(min.) = time_2w × T – (tskew1 + tskew2 + tskew5)	time_2w
t9	t9	t9(min.) = time_9 × T – (tskew1 + tskew2 + tskew6)	time_9
t3	—	t3(min.) = (time_2w – time_on) × T – (tskew1 + tskew2 +tskew5)	if not met, increase time_2w
t4	t4	t4(min.) = time_4 × T – tskew1	time_4
tA	tA	tA = (1.5 + time_ax) × T – (tco + tsui + tcable2 + tcable2 + 2 × tbuf)	time_ax
t0	—	t0(min.) = (time_1 + time_2 + time_9) × T	time_1, time_2r, time_9
—	—	Avoid bus contention when switching buffer on by making ton long enough	—
—	—	Avoid bus contention when switching buffer off by making toff long enough	—

[1] See Figure 12.

3.6.2.2 Multiword DMA (MDMA) Mode Timing

Figure 13 and Figure 14 show the timing for MDMA read and write modes, respectively.

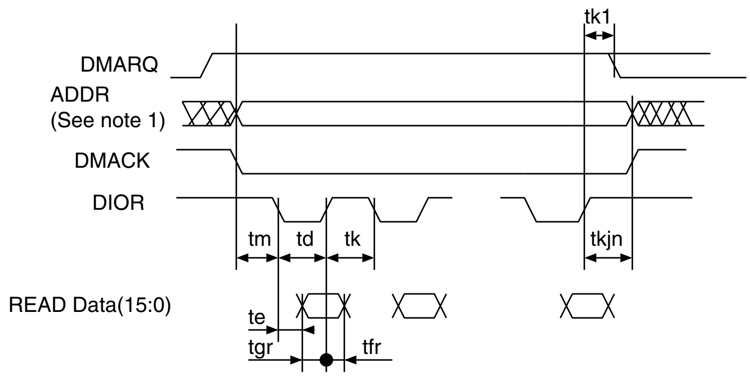


Figure 13. MDMA Read Mode Timing

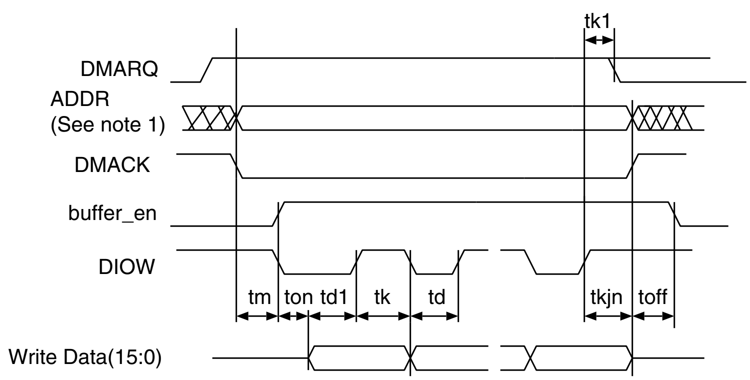


Figure 14. MDMA Write Mode Timing

To meet timing requirements, a number of timing parameters must be controlled. See Table 33 for details on timing parameters for MDMA read and write modes.

Table 33. Timing Parameters for MDMA Read and Write Modes

ATA Parameter	MDMA Read[1] and Write[2] Timing Parameters	Relation	Adjustable Parameter(s)
tm, ti	tm	tm(min.) = ti(min.) = time_m × T – (tskew1 + tskew2 + tskew5)	time_m
td	td, td1	td1(min.) = td(min.) = time_d × T – (tskew1 + tskew2 + tskew6)	time_d
tk	tk	tk(min.) = time_k × T – (tskew1 + tskew2 + tskew6)	time_k
t0	—	t0(min.) = (time_d + time_k) × T	time_d, time_k
tg(read)	tgr	tgr(min.–read) = tco + tsu + tbuf + tbuf + tcable1 + tcable2 tgr(min.–drive) = td – te(drive)	time_d
tf(read)	tfr	tfr(min.–drive) =0 k	—
tg(write)	—	tg(min.–write) = time_d × T –(tskew1 + tskew2 + tskew5)	time_d

Table 33. Timing Parameters for MDMA Read and Write Modes (continued)

ATA Parameter	MDMA Read[1] and Write[2] Timing Parameters	Relation	Adjustable Parameter(s)
tf(write)	—	tf(min.–write) = time_k × T – (tskew1 + tskew2 + tskew6)	time_k
tL	—	tL(max.) = (time_d + time_k–2) × T – (tsu + tco + 2 × tbuf + 2 × tcable2)	time_d, time_k[3]
tn, tj	tkjn	tn= tj= tkjn = (max.(time_k,. time_jn) × T – (tskew1 + tskew2 + tskew6)	time_jn
—	ton toff	ton = time_on × T – tskew1 toff = time_off × T – tskew1	—

[1] See Figure 13.

[2] See Figure 14.

[3] tk1 in the UDMA figures equals (tk –2 × T).

3.6.2.3 Ultra DMA (UDMA) Mode Timing

UDMA mode timing is more complicated than PIO mode or MDMA mode. In this section, timing diagrams for UDMA in- and out-transfers are provided.

3.6.2.3.1 UDMA In-Transfer Timing

Figure 15 shows the timing for UDMA in-transfer start.

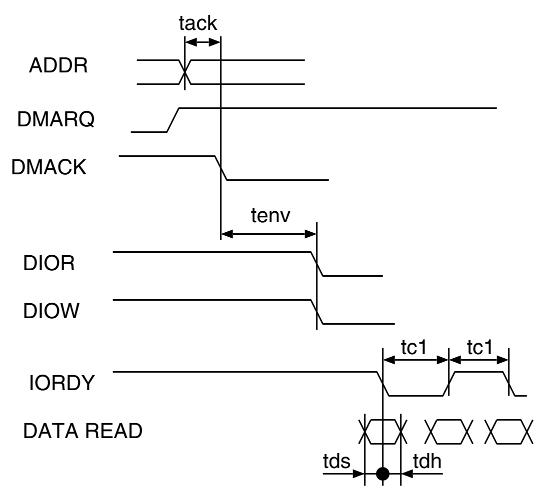


Figure 15. Timing for UDMA In-Transfer Start

Figure 16 shows the timing for host-terminated UDMA in-transfer.

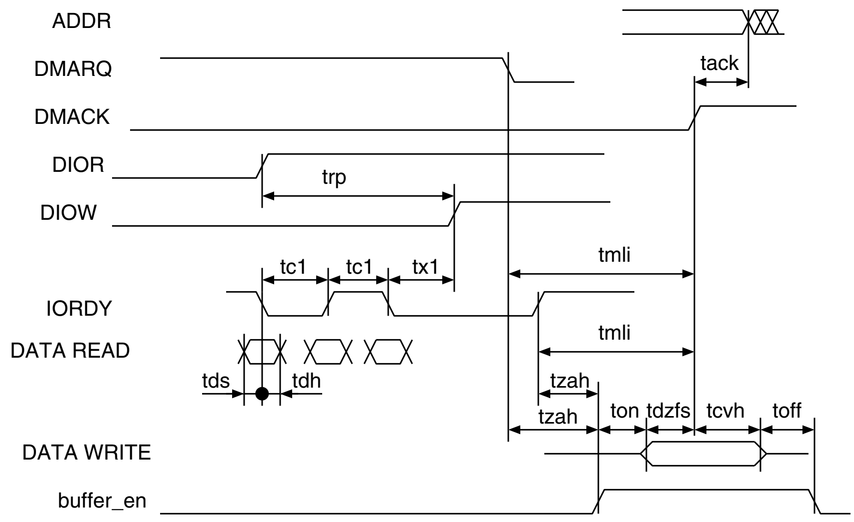


Figure 16. Timing for Host-Terminated UDMA In-Transfer

Figure 17 shows timing for device-terminated UDMA in-transfer.

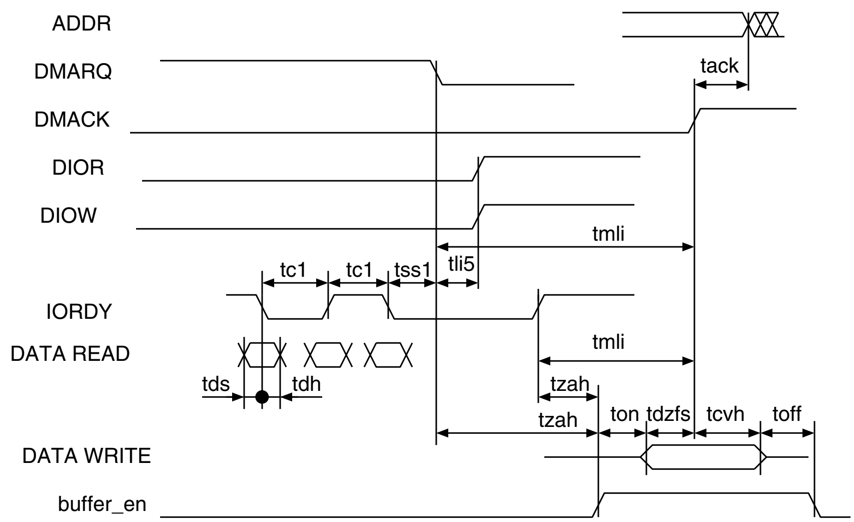


Figure 17. Timing for Device-Terminated UDMA Transfer

Timing parameters for UDMA in-burst are listed in Table 34.

Table 34. Timing Parameters for UDMA In-Burst

ATA Parameter	Spec. Parameter	Value	Required Conditions
tack	tack	tack(min.) = (time_ack × T) – (tskew1 + tskew2)	time_ack
tenv	tenv	tenv(min.) = (time_env × T) – (tskew1 + tskew2) tenv(max.) = (time_env × T) + (tskew1 + tskew2)	time_env
tds	tds1	tds – (tskew3) – ti_ds > 0	tskew3, ti_ds, ti_dh should be low enough
tdh	tdh1	tdh – (tskew3) –ti_dh > 0	
tcyc	tc1	(tcyc – tskew) > T	T big enough
trp	trp	trp(min.) = time_rp × T – (tskew1 + tskew2 + tskew6)	time_rp
—	tx1[1]	(time_rp × T) – (tco + tsu + 3T + 2 × tbuf + 2 × tcable2) > trfs (drive)	time_rp
tmli	tmli1	tmli1(min.) = (time_mlix + 0.4) × T	time_mlix
tzah	tzah	tzah(min.) = (time_zah + 0.4) × T	time_zah
tdzfs	tdzfs	tdzfs = (time_dzfs × T) – (tskew1 + tskew2)	time_dzfs
tcvh	tcvh	tcvh = (time_cvh × T) – (tskew1 + tskew2)	time_cvh
—	ton toff	ton = time_on × T – tskew1 toff = time_off × T – tskew1	—

1 There is a special timing requirement in the ATA host that requires the internal DIOW to go only high three clocks after the last active edge on the DSTROBE signal. The equation given on this line tries to capture this constraint.

Make t_{on} and t_{off} big enough to avoid bus contention.

3.6.2.4 UDMA Out-Transfer Timing

Figure 18 shows the timing for start of UDMA out-transfer.

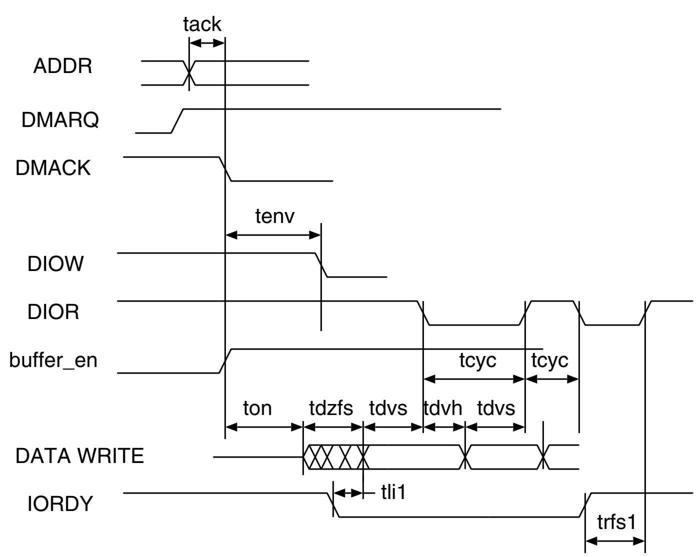


Figure 18. Timing for UDMA Out-Transfer Start

Figure 19 shows timing for host-terminated UDMA out-transfer.

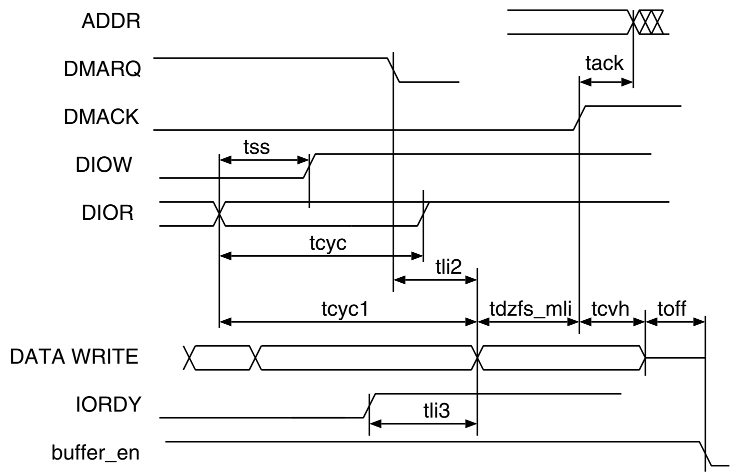


Figure 19. Timing for Host-Terminated UDMA Out-Transfer

Timing parameters for UDMA out-bursts are listed in Table 35.

Table 35. Timing Parameters UDMA Out-Bursts

ATA Parameter	Spec Parameter	Value	How to Meet?
tack	tack	tack(min.) = (time_ack × T) – (tskew1 + tskew2)	time_ack
tenv	tenv	tenv(min.) = (time_env × T) – (tskew1 + tskew2) tenv(max.) = (time_env × T) + (tskew1 + tskew2)	time_env
tdvs	tdvs	tdvs = (time_dvs × T) – (tskew1 + tskew2)	time_dvs
tdvh	tdvh	tdvs = (time_dvh × T) – (tskew1 + tskew2)	time_dvh
tcyc	tcyc	tcyc = time_cyc × T – (tskew1 + tskew2)	time_cyc
t2cyc	—	t2cyc = time_cyc × 2 × T	time_cyc
trfs1	trfs	trfs = 1.6 × T + tsui + tco + tbuf + tbuf	—
—	tdzfs	tdzfs = time_dzfs × T – (tskew1)	time_dzfs
tss	tss	tss = time_ss × T – (tskew1 + tskew2)	time_ss
tmli	tdzfs_mli	tdzfs_mli =max.(time_dzfs, time_mli) × T – (tskew1 + tskew2)	—
tli	tli1	tli1 > 0	—
tli	tli2	tli2 > 0	—
tli	tli3	tli3 > 0	—
tcvh	tcvh	tcvh = (time_cvh × T) – (tskew1 + tskew2)	time_cvh
—	ton toff	ton = time_on × T – tskew1 toff = time_off × T – tskew1	—

3.6.3 Digital Audio Mux (AUDMUX) Timing

The AUDMUX provides a programmable interconnect logic for voice, audio, and data routing between internal serial interfaces (SSI and SAP) and external serial interfaces (audio and voice codecs). The AC timing of AUDMUX external pins is governed by the SSI modules. For more information, see Section 3.6.17, “Synchronous Serial Interface (SSI) Timing.”

3.6.4 CMOS Sensor Interface (CSI) Timing

The CSI enables the chip to connect directly to external CMOS image sensors, which are classified as dumb or smart as follows:

- Dumb sensors only support traditional sensor timing (vertical sync (VSYNC) and horizontal sync (HSYNC)) and output-only Bayer and statistics data.
- Smart sensors support CCIR656 video decoder formats and perform additional processing of the image (for example, image compression, image pre-filtering, and various data output formats).

The following subsections describe the CSI timing in gated and ungated clock modes.

3.6.4.1 Gated Clock Mode Timing

Figure 20 and Figure 21 shows the gated clock mode timings for CSI, and Table 36 describes the timing parameters (P1–P7) shown in the figures. A frame starts with a rising/falling edge on VSYNC, then HSYNC is asserted and holds for the entire line. The pixel clock is valid as long as HSYNC is asserted.

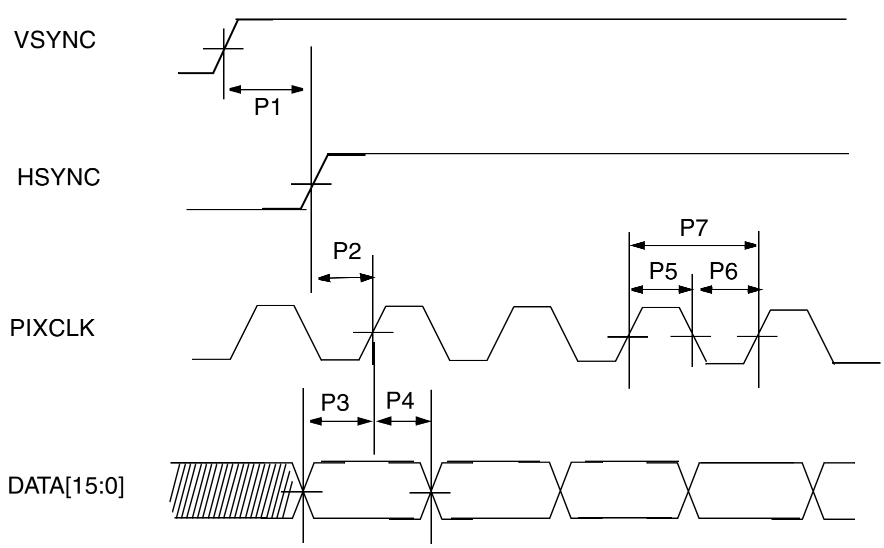


Figure 20. CSI Gated Clock Mode—Sensor Data at Falling Edge, Latch Data at Rising Edge

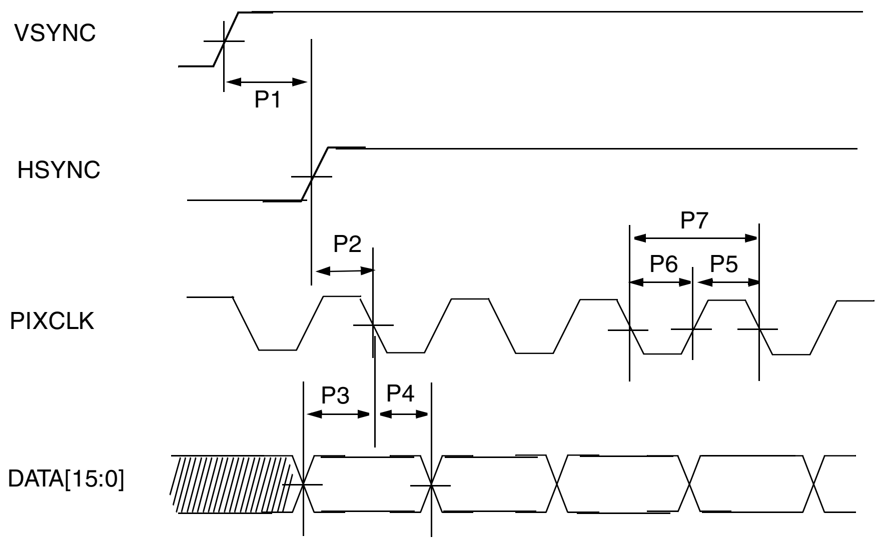


Figure 21. CSI Gated Clock Mode—Sensor Data at Rising Edge, Latch Data at Falling Edge

Table 36. CSI Gated Clock Mode Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
P1	CSI VSYNC to HSYNC time	tV2H	67.5	—	ns
P2	CSI HSYNC setup time	tHsu	1	—	ns
P3	CSI DATA setup time	tDsu	1	—	ns
P4	CSI DATA hold time	tDh	1	—	ns
P5	CSI pixel clock high time	tCLKh	10	—	ns
P6	CSI pixel clock low time	tCLKl	10	—	ns
P7	CSI pixel clock frequency	fCLK	—	48 ± 10%[1]	MHz

[1] Will be verified during qualification

3.6.4.2 Ungated Clock Mode Timing

Figure 22 shows the ungated clock mode timings of CSI, and Table 37 describes the timing parameters (P1–P6) that are shown in the figure. In ungated mode the VSYNC and PIXCLK signals are used, and the HSYNC signal is ignored.

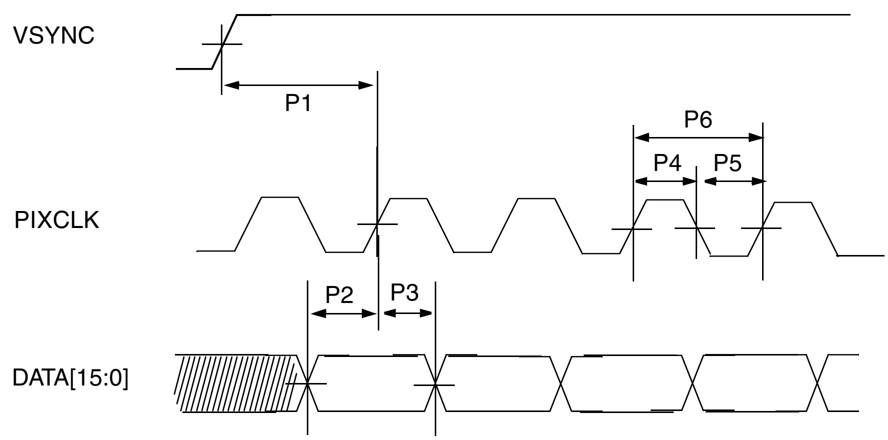


Figure 22. CSI Ungated Clock Mode—Sensor Data at Falling Edge, Latch Data at Rising Edge

Table 37. CSI Ungated Clock Mode Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
P1	CSI VSYNC to pixel clock time	tVSYNC	67.5	—	ns
P2	CSI DATA setup time	tDsu	1	—	ns
P3	CSI DATA hold time	tDh	1	—	ns
P4	CSI pixel clock high time	tCLKh	10	—	ns
P5	CSI pixel clock low time	tCLKl	10	—	ns
P6	CSI pixel clock frequency	fCLK	—	48 ± 10%[1]	MHz

[1] Will be verified during qualification

3.6.5 Configurable Serial Peripheral Interface (CSPI) Timing

Figure 23 and Figure 24 provide CSPI master and slave mode timing diagrams, respectively. Table 38 describes the timing parameters (t1–t14) that are shown in the figures. The values shown in timing diagrams were tested using a worst-case core voltage of 1.1 V, slow pad voltage of 2.68 V, and fast pad voltage of 1.65 V.

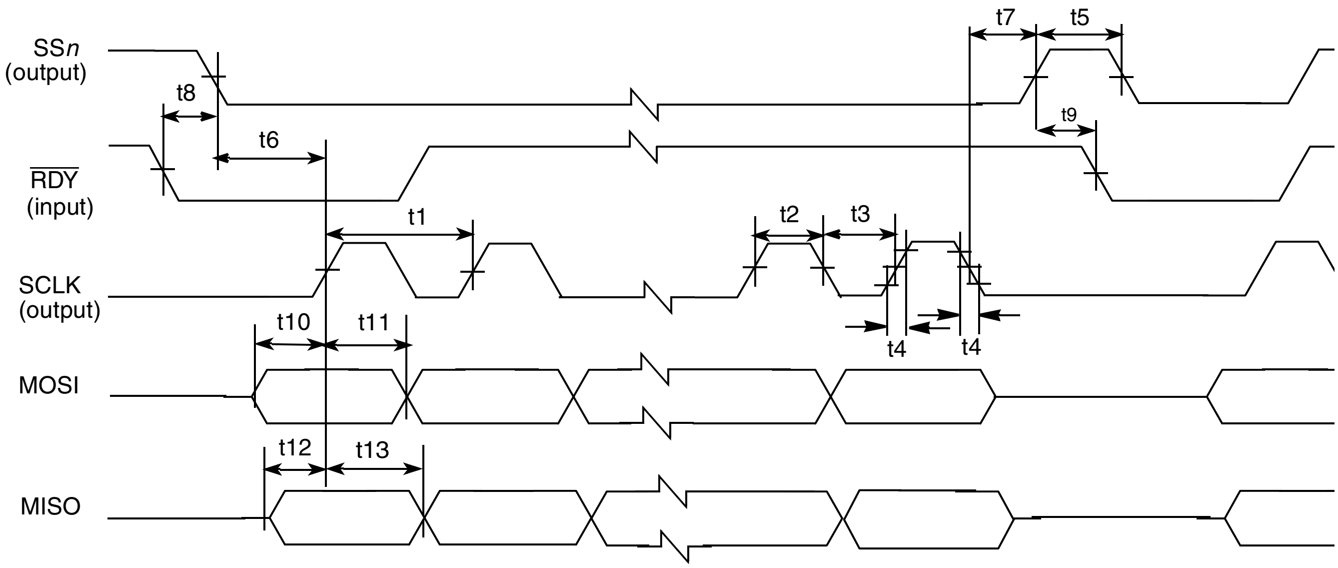


Figure 23. CSPI Master Mode Timing Diagram

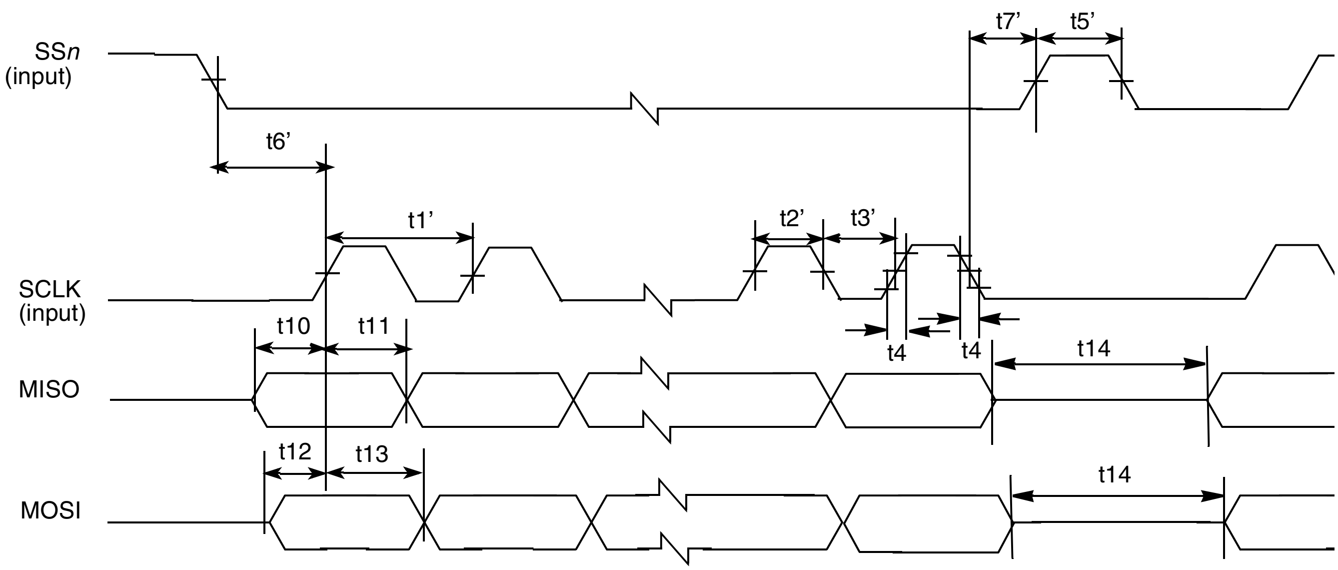


Figure 24. CSPI Slave Mode Timing Diagram

Table 38. CSPI Interface Timing Parameters

ID	Parameter Description	Symbol	Minimum	Maximum	Units
t1	CSPI master SCLK cycle time	t_{clko}	60.2	—	ns
t2	CSPI master SCLK high time	t_{clkoH}	22.65	—	ns
t3	CSPI master SCLK low time	t_{clkoL}	22.47	—	ns
t1’	CSPI slave SCLK cycle time	t_{clki}	60.2	—	ns
t2’	CSPI slave SCLK high time	t_{clkiH}	30.1	—	ns
t3’	CSPI slave SCLK low time	t_{clkiL}	30.1	—	ns

Table 38. CSPI Interface Timing Parameters (continued)

ID	Parameter Description	Symbol	Minimum	Maximum	Units
t4	CSPI SCLK transition time	t_{pr}[1]	2.6	8.5	ns
t5	SS*n* output pulse width	t_{Wsso}	$2T_{sclk}$[2] $+T_{wait}$[3]	—	—
t5'	SS*n* input pulse width	t_{Wssi}	T_{per}[4]	—	—
t6	SS*n* output asserted to first SCLK edge (SS output setup time)	t_{Ssso}	$3T_{sclk}$	—	—
t6'	SS*n* input asserted to first SCLK edge (SS input setup time)	t_{Sssi}	T_{per}	—	—
t7	CSPI master: Last SCLK edge to SS*n* negated (SS output hold time)	t_{Hsso}	$2T_{sclk}$	—	—
t7'	CSPI slave: Last SCLK edge to SS*n* negated (SS input hold time)	t_{Hssi}	30	—	ns
t8	CSPI master: CSPI1_RDY low to SS*n* asserted (CSPI1_RDY setup time)	t_{Srdy}	$2T_{per}$	$5T_{per}$	—
t9	CSPI master: SS*n* negated to CSPI1_RDY low	t_{Hrdy}	0	—	ns
t10	Output data setup time	t_{Sdatao}	$(t_{clkoL}$ or t_{clkoH} or t_{clkiL} or $t_{clkiH}) - T_{ipg}$[5]	—	—
t11	Output data hold time	t_{Hdatao}	t_{clkoL} or t_{clkoH} or t_{clkiL} or t_{clkiH}	—	—
t12	Input data setup time	t_{Sdatai}	$T_{ipg} + 0.5$	—	ns
t13	Input data hold time	t_{Hdatai}	0	—	ns
t14	Pause between data word	t_{pause}	0	—	ns

1 The output SCLK transition time is tested with 25 pF drive.
2 T_{sclk} = CSPI clock period
3 T_{wait} = Wait time, as specified in the sample period control register
4 T_{per} = CSPI reference baud rate clock period (PERCLK2)
5 T_{ipg} = CSPI main clock IPG_CLOCK period

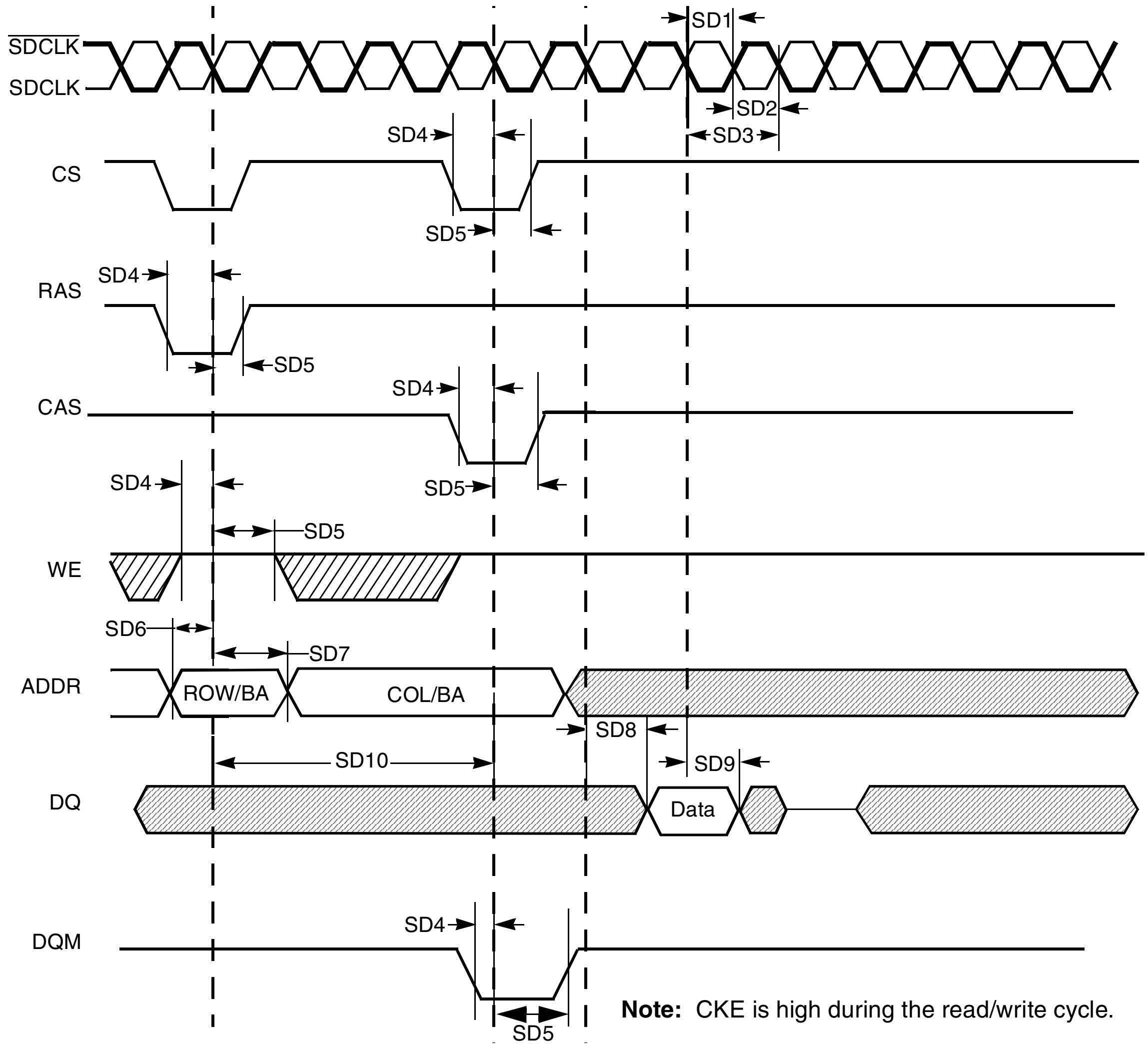
3.6.6 External Memory Interface (EMI) Timing

The EMI module includes the enhanced SDRAM/LPDDR memory controller (ESDCTL), NAND Flash controller (NFC), and wireless external interface module (WEIM). The following subsections give timing information for these submodules.

3.6.6.1 ESDCTL Electrical Specifications

3.6.6.1.1 SDRAM Memory Controller

The following diagrams and tables specify the timings related to the SDRAMC module which interfaces SDRAM.



Note: CKE is high during the read/write cycle.

Figure 25. SDRAM Read Cycle Timing Diagram

Table 39. DDR/SDR SDRAM Read Cycle Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Unit
SD1	SDRAM clock high-level width[1]	tCH	3.4	4.1	ns
SD2	SDRAM clock low-level width[1]	tCL	3.4	4.1	ns
SD3	SDRAM clock cycle time	tCK	7.5	—	ns
SD4	CS, RAS, CAS, WE, DQM, CKE setup time	tCMS	2.0	—	ns
SD5	CS, RAS, CAS, WE, DQM, CKE hold time	tCMH	1.8	—	ns
SD6	Address setup time	tAS	2.0	—	ns
SD7	Address hold time	tAH	1.8	—	ns
SD8	SDRAM access time	tAC	—	6.47	ns

Table 39. DDR/SDR SDRAM Read Cycle Timing Parameters (continued)

ID	Parameter	Symbol	Min.	Max.	Unit
SD9	Data out hold time[2]	tOH	1.2	—	ns
SD10	Active to read/write command period	tRC	10	—	clock

[1] SD1 + SD2 does not exceed 7.5 ns for 133 MHz.

[2] Timing parameters are relevant only to SDR SDRAM. For the specific DDR SDRAM data related timing parameters, see Table 43 and Table 44.

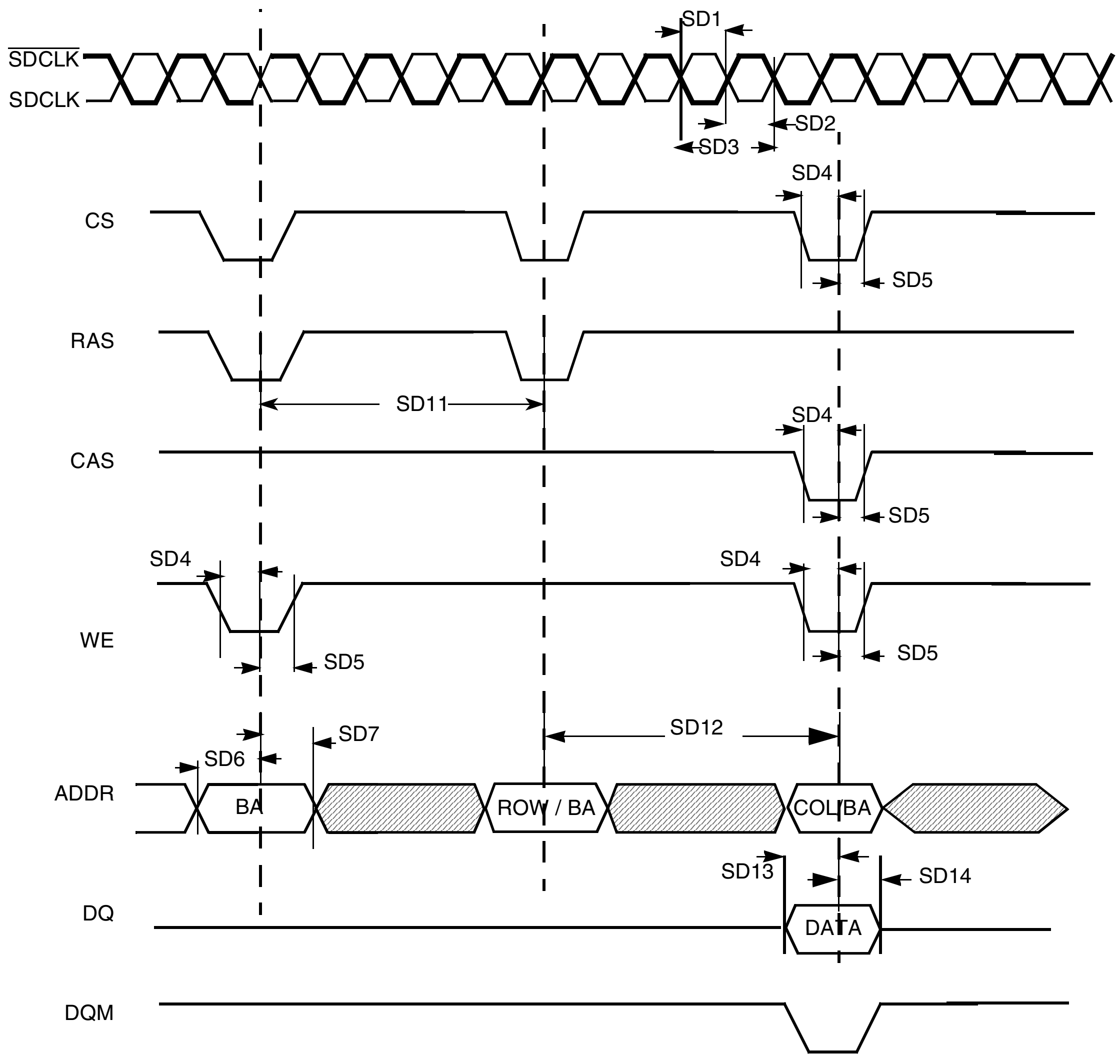


Figure 26. SDR SDRAM Write Cycle Timing Diagram

Table 40. SDR SDRAM Write Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Unit
SD1	SDRAM clock high-level width	tCH	3.4	4.1	ns
SD2	SDRAM clock low-level width	tCL	3.4	4.1	ns
SD3	SDRAM clock cycle time	tCK	7.5	—	ns
SD4	CS, RAS, CAS, WE, DQM, CKE setup time	tCMS	2.0	—	ns
SD5	CS, RAS, CAS, WE, DQM, CKE hold time	tCMH	1.8	—	ns
SD6	Address setup time	tAS	2.0	—	ns
SD7	Address hold time	tAH	1.8	—	ns
SD11	Precharge cycle period[1]	tRP	1	4	clock
SD12	Active to read/write command delay[1]	tRCD	1	8	clock
SD13	Data setup time	tDS	2.0	—	ns
SD14	Data hold time	tDH	1.3	—	ns

1 SD11 and SD12 are determined by SDRAM controller register settings.

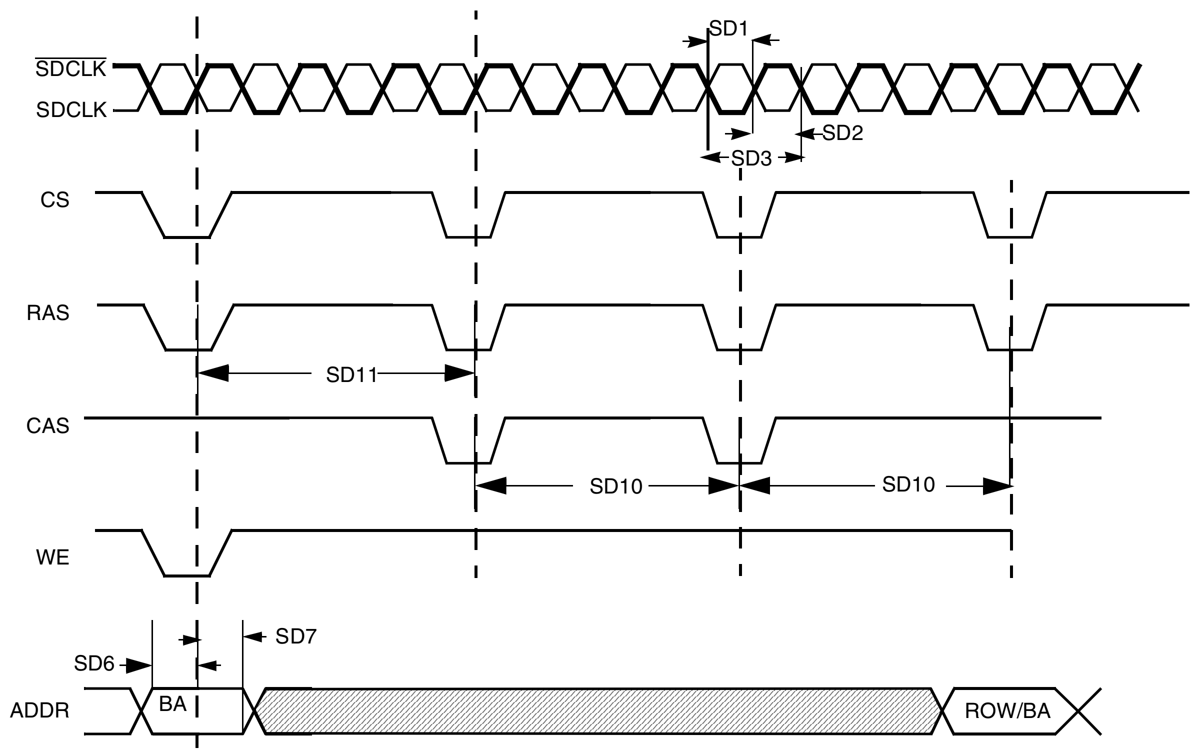


Figure 27. SDRAM Refresh Timing Diagram

Table 41. SDRAM Refresh Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Unit
SD1	SDRAM clock high-level width	tCH	3.4	4.1	ns
SD2	SDRAM clock low-level width	tCL	3.4	4.1	ns
SD3	SDRAM clock cycle time	tCK	7.5	—	ns
SD6	Address setup time	tAS	1.8	—	ns
SD7	Address hold time	tAH	1.8	—	ns
SD10	Precharge cycle period[1]	tRP	1	4	clock
SD11	Auto precharge command period[1]	tRC	2	20	clock

[1] SD10 and SD11 are determined by SDRAM controller register settings.

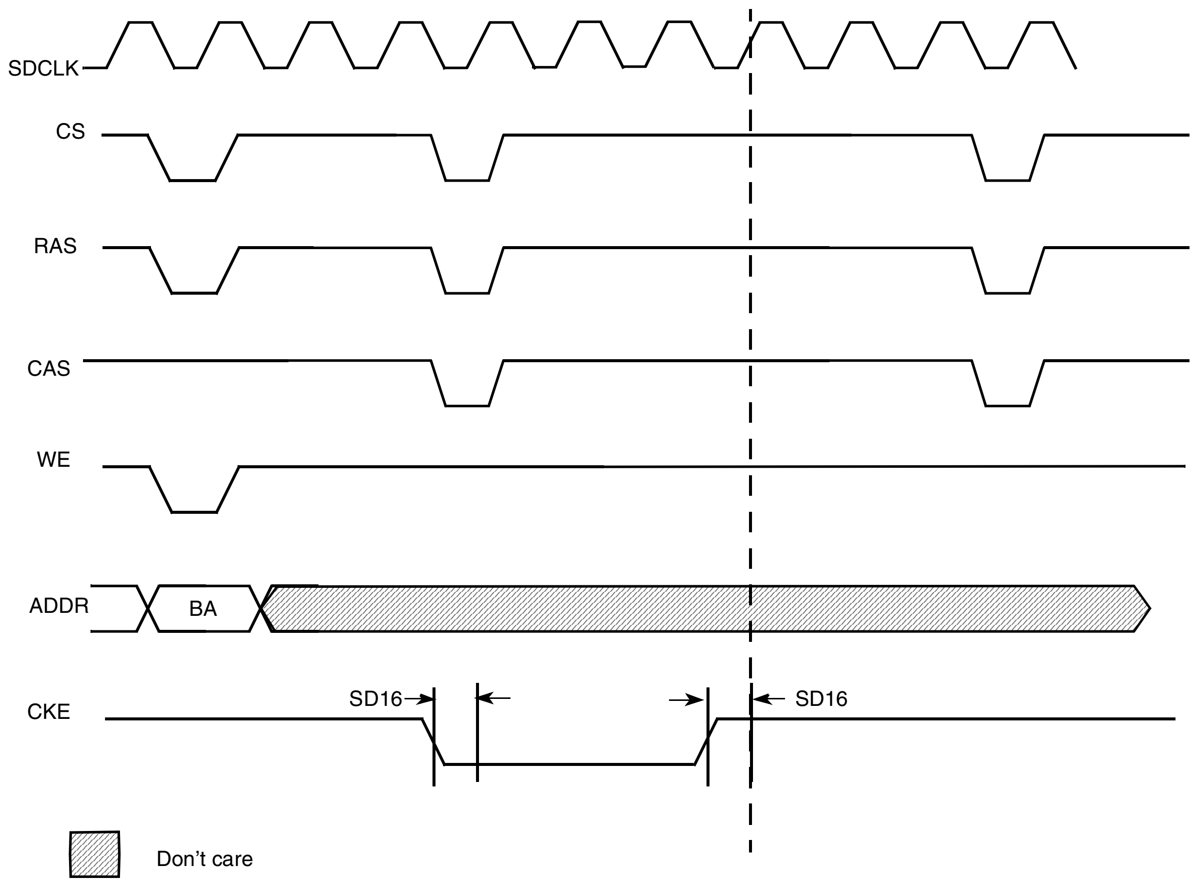


Figure 28. SDRAM Self-Refresh Cycle Timing Diagram

NOTE

The clock continues to run unless CKE is low. Then the clock is stopped in low state.

Table 42. SDRAM Self-Refresh Cycle Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Unit
SD16	CKE output delay time	tCKS	1.8	—	ns

3.6.6.1.2 Mobile DDR SDRAM–Specific Parameters

The following diagrams and tables specify the timings related to the SDRAMC module which interfaces with the mobile DDR SDRAM.

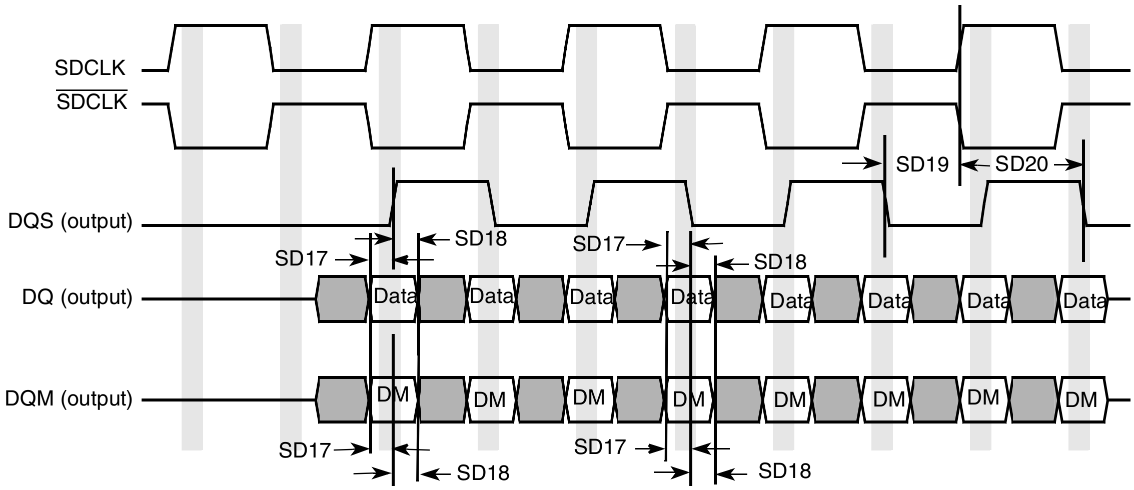


Figure 29. Mobile DDR SDRAM Write Cycle Timing Diagram

Table 43. Mobile DDR SDRAM Write Cycle Timing Parameters[1]

ID	Parameter	Symbol	Min.	Max.	Unit
SD17	DQ and DQM setup time to DQS	tDS	0.95	—	ns
SD18	DQ and DQM hold time to DQS	tDH	0.95	—	ns
SD19	Write cycle DQS falling edge to SDCLK output delay time	tDSS	1.8	—	ns
SD20	Write cycle DQS falling edge to SDCLK output hold time	tDSH	1.8	—	ns

1 Test condition: Measured using delay line 5 programmed as follows: ESDCDLY5[15:0] = 0x0703.

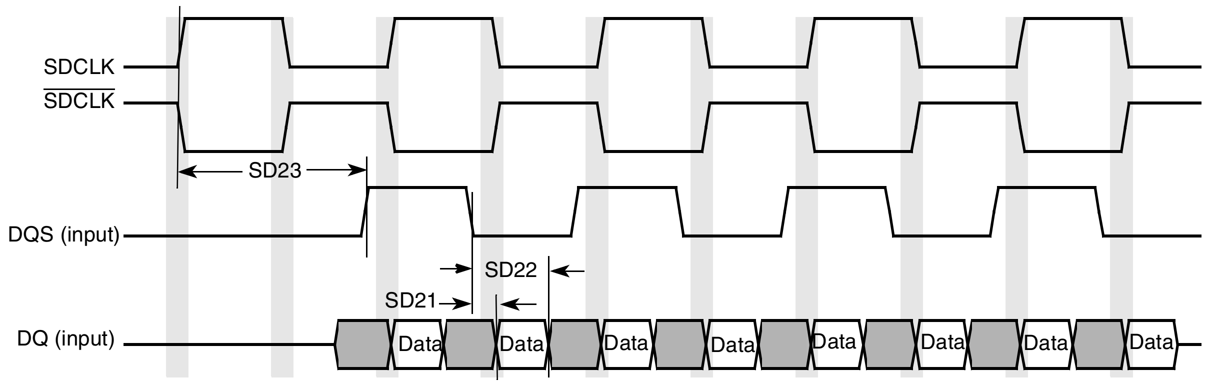


Figure 30. Mobile DDR SDRAM DQ versus DQS and SDCLK Read Cycle Timing Diagram

Table 44. Mobile DDR SDRAM Read Cycle Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Unit
SD21	DQS – DQ Skew (defines the data valid window in read cycles related to DQS)	tDQSQ	—	0.85	ns
SD22	DQS DQ HOLD time from DQS	tQH	2.3	—	ns
SD23	DQS output access time from SDCLK posedge	tDQSCK	—	6.7	ns

3.6.6.1.3 DDR2 SDRAM–Specific Parameters

The following diagrams and tables specify the timings related to the SDRAMC module which interfaces DDR2 SDRAM.

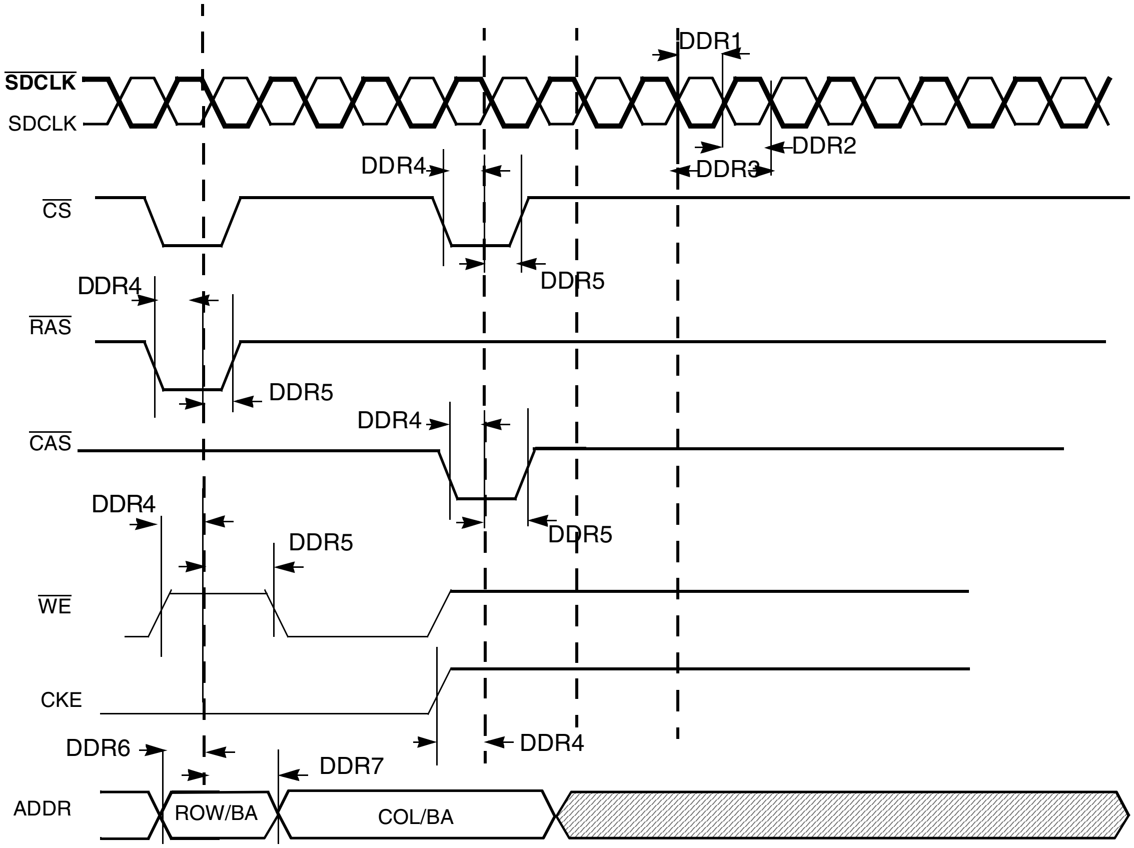


Figure 31. DDR2 SDRAM Basic Timing Parameters

Table 45 provides values for a command/address slew rate of 1 V/ns and an SDCLK, SDCLK_B differential slew rate of 2 V/ns. For additional values, use Table 46, “tlS, tlH Derating Values for DDR2-400, DDR2-533.”

Table 45. DDR2 SDRAM Timing Parameter Table

ID	Parameter	Symbol	DDR2-400		Unit
			Min.	Max.	
DDR1	SDRAM clock high-level width	tCH	0.45	0.55	tCK
DDR2	SDRAM clock low-level width	tCL	0.45	0.55	tCK
DDR3	SDRAM clock cycle time	tCK	7.5	8	ns
DDR4	CS, RAS, CAS, CKE, WE setup time	tIS	0.35	—	ns
DDR5	CS, RAS, CAS, CKE, WE hold time	tIH	0.475	—	ns
DDR6	Address output setup time	tIS	0.35	—	ns
DDR7	Address output hold time	tIH	0.475	—	ns

Table 45 shows values for a command/address slew rate of 1 V/ns and an SDCLK, SDCLK_B differential slew rate of 2 V/ns. Table 46 shows additional values for DDR2-400 and DDR2-533.

Table 46. tIS, tIH Derating Values for DDR2-400, DDR2-533

Command/ Address Slew Rate (V/Ns)	CK, CK Differential Slew Rate						Units
	2.0 V/ns		1.5 V/ns		1.0 V/ns		
	∆tIS	∆tIH	∆tIS	∆tIH	∆tIS	∆tIH	
4.0	+187	+94	+217	+124	+247	+154	ps
3.5	+179	+89	+209	+119	+239	+149	ps
3.0	+167	+83	+197	+113	+227	+143	ps
2.5	+150	+75	+180	+105	+210	+135	ps
2.0	+125	+45	+155	+75	+185	+105	ps
1.5	+83	+21	+113	+51	+143	+81	ps
1.0	0	0	+30	+30	+60	+60	ps
0.9	–11	–14	+19	+16	+49	+46	ps
0.8	–25	–31	+5	–1	+35	+29	ps
0.7	–43	–54	–13	–24	+17	+6	ps
0.6	–67	–83	–37	–53	–7	–23	ps
0.5	–110	–125	–80	–95	–50	–65	ps
0.4	–175	–188	–145	–158	–115	–128	ps
0.3	–285	–292	–255	–262	–225	–232	ps
0.25	–350	–375	–320	–345	–290	–315	ps
0.2	–525	–500	–495	–470	–465	–440	ps
0.15	–800	–708	–770	–678	–740	–648	ps
0.1	–1450	–1125	–1420	–1095	–1390	–1065	ps

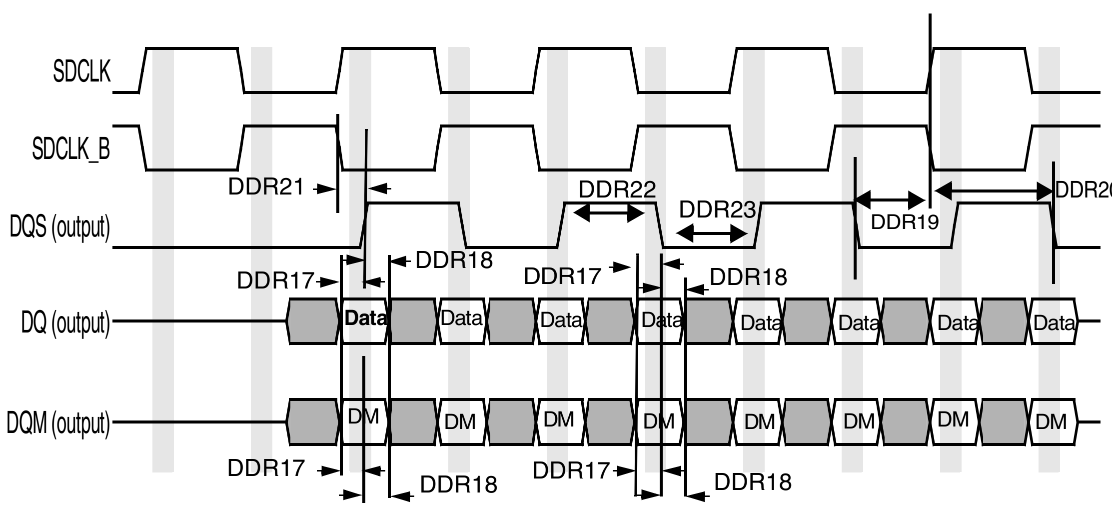


Figure 32. DDR2 SDRAM Write Cycle Timing Diagram

Table 47. DDR2 SDRAM Write Cycle Parameter Table

ID	Parameter	Symbol	DDR2-400		Unit
			Min.	Max.	
DDR17	DQ & DQM setup time to DQS (single-ended strobe)[1]	tDS1(base)	0.025	—	ns
DDR18	DQ & DQM hold time to DQS (single-ended strobe)[1]	tDH1(base)	0.025	—	ns
DDR19	Write cycle DQS falling edge to SDCLK output setup time	tDSS	0.2	—	tCK
DDR20	Write cycle DQS falling edge to SDCLK output hold time	tDSH	0.2	—	tCK
DDR21	DQS latching rising transitions to associated clock edges	tDQSS	-0.25	0.25	tCK
DDR22	DQS high-level width	tDQSH	0.35	—	tCK
DDR23	DQS low-level width	tDQSL	0.35	—	tCK

1 These values are for a DQ/DM slew rate of 1 V/ns and a DQS slew rate of 1 V/ns. For additional values use Table 48, “DtDS1, DtDH1 Derating Values for DDR2-400, DDR2-533.”

Table 48. ∆tDS1, ∆tDH1 Derating Values for DDR2-400, DDR2-533[1,2,3]

		DQS Single-Ended Slew Rate																	
		2.0 V/ns		1.5 V/ns		1.0 V/ns		0.9 V/ns		0.8 V/ns		0.7 V/ns		0.6 V/ns		0.5 Vns		0.4 V/ns	
		∆tD S1	∆tD H1	∆tD S1	∆tD H1	∆tD S1	∆tD H1	∆tD S1	∆tD H1	∆tD S1	∆tD H1	∆tD S1	∆tD H1	∆tD S1	∆tD H1	∆tD S1	∆tD H1	∆tD S1	∆tD H1
DQ Slew Rate V/ns	2.0	188	188	167	146	125	63	—	—	—	—	—	—	—	—	—	—	—	—
	1.5	146	167	125	125	83	42	81	43	—	—	—	—	—	—	—	—	—	—
	1.0	63	125	42	83	0	0	–2	1	–7	–13	—	—	—	—	—	—	—	—
	0.9	—	—	31	69	–11	–14	–13	–13	–18	–27	–29	–45	—	—	—	—	—	—
	0.8	—	—	—	—	–25	–31	–27	–30	–32	–44	–43	–62	–60	–86	—	—	—	—
	0.7	—	—	—	—	—	—	–45	–53	–50	–67	–61	–85	–78	–109	–108	–152	—	—
	0.6	—	—	—	—	—	—	—	—	–74	–96	–85	–114	–102	–138	–132	–181	–183	–246
	0.5	—	—	—	—	—	—	—	—	—	—	–128	–156	–145	–180	–175	–223	–226	–288
	0.4	—	—	—	—	—	—	—	—	—	—	—	—	–210	–243	–240	–286	–291	–351

1 All units in ‘ps’.

2 Test conditions are at capacitance=15pF for DDR PADS. Recommended drive strengths are medium for SDCLK and high for address and controls.

3 SDRAM CLK and DQS related parameters are measured from the 50% point. That is, high is defined as 50% of the signal value, and low is defined as 50% of the signal value. DDR SDRAM CLK parameters are measured at the crossing point of SDCLK and SDCLK (inverted clock).

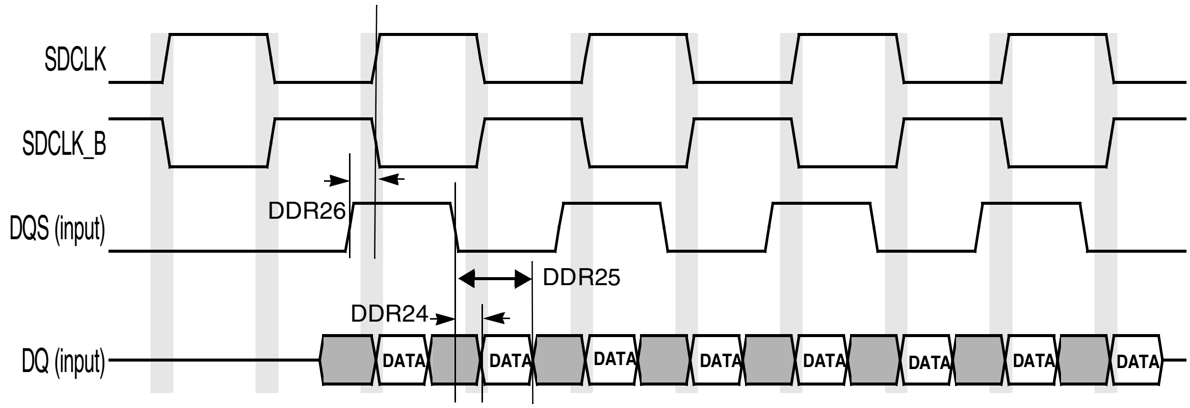


Figure 33. DDR2 SDRAM DQ vs. DQS and SDCLK READ Cycle Timing Diagram

Table 49. DDR2 SDRAM Read Cycle Parameter Table[1,2]

ID	Parameter	Symbol	DDR2-400		Unit
			Min.	Max.	
DDR24	DQS - DQ Skew (defines the Data valid window in read cycles related to DQS)	tDQSQ	—	0.35	ns
DDR25	DQS DQ in HOLD time from DQS[3]	tQH	2.925	—	ns
DDR26	DQS output access time from SDCLK posedge	tDQSCK	–0.5	0.5	ns

[1] Test conditions are at capacitance=15 pF for DDR PADS. Recommended drive strengths are medium for SDCLK and high for address and controls.

[2] SDRAM CLK and DQS-related parameters are measured from the 50% point. That is, high is defined as 50% of the signal value, and low is defined as 50% of the signal value. DDR SDRAM CLK parameters are measured at the crossing point of SDCLK and SDCLK (inverted clock).

[3] The value was calculated for an SDCLK frequency of 133 MHz, by the formula tQH = tHP - tQHS = min (tCL,tCH) - tQHS = 0.45*tCK - tQHS = 0.45 * 7.5 - 0.45 = 2.925 ns

3.6.6.2 NAND Flash Controller (NFC) Timing

The i.MX25 NFC supports normal timing mode, using two Flash clock cycles for one access of $\overline{\text{RE}}$ and $\overline{\text{WE}}$. AC timings are provided as multiplications of the clock cycle and fixed delay. Figure 34 through Figure 37 depicts the relative timing between NFC signals at the module level for different operations under normal mode. Table 50 describes the timing parameters (NF1–NF17) that are shown in the figures.

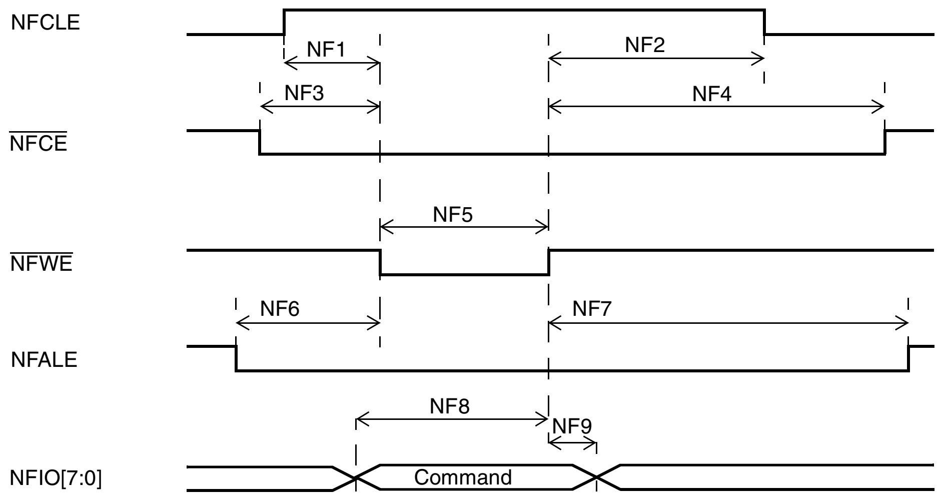


Figure 34. Command Latch Cycle Timing Diagram

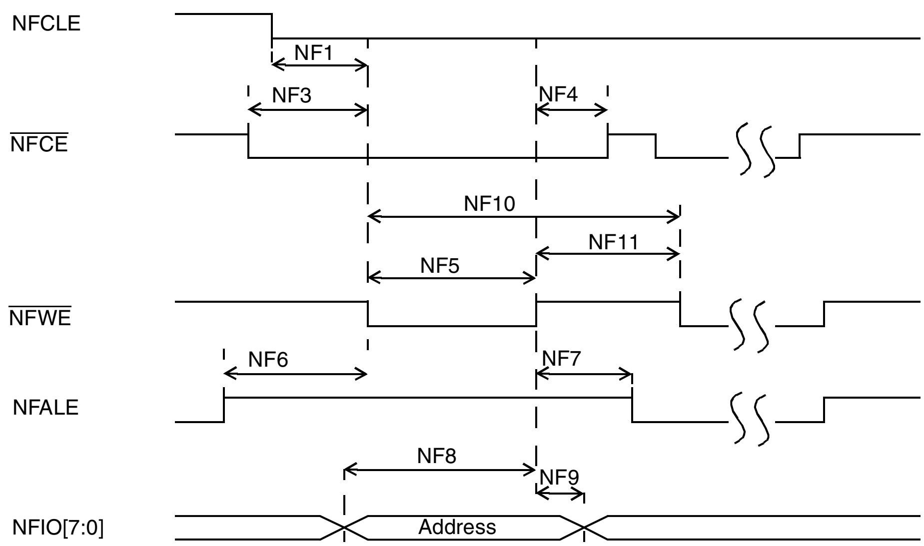


Figure 35. Address Latch Cycle Timing Diagram

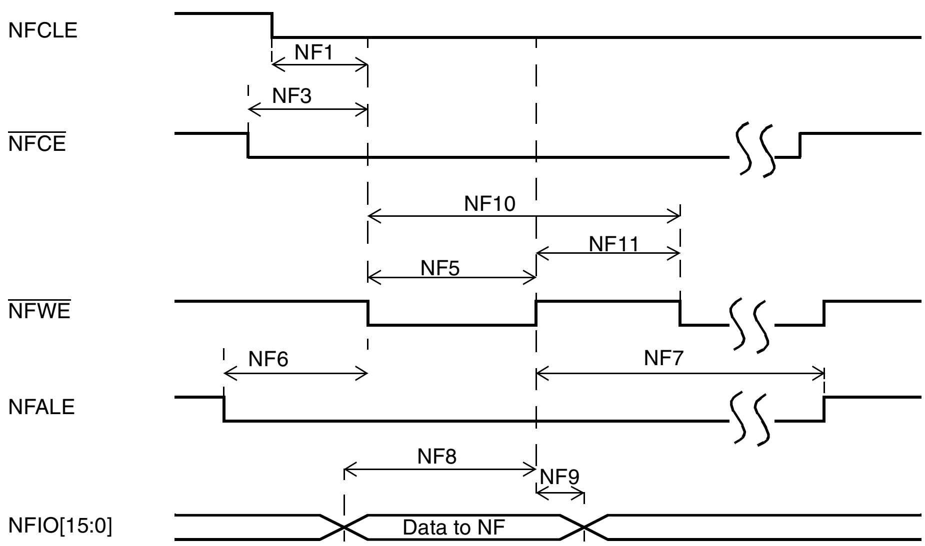


Figure 36. Write Data Latch Cycle Timing Diagram

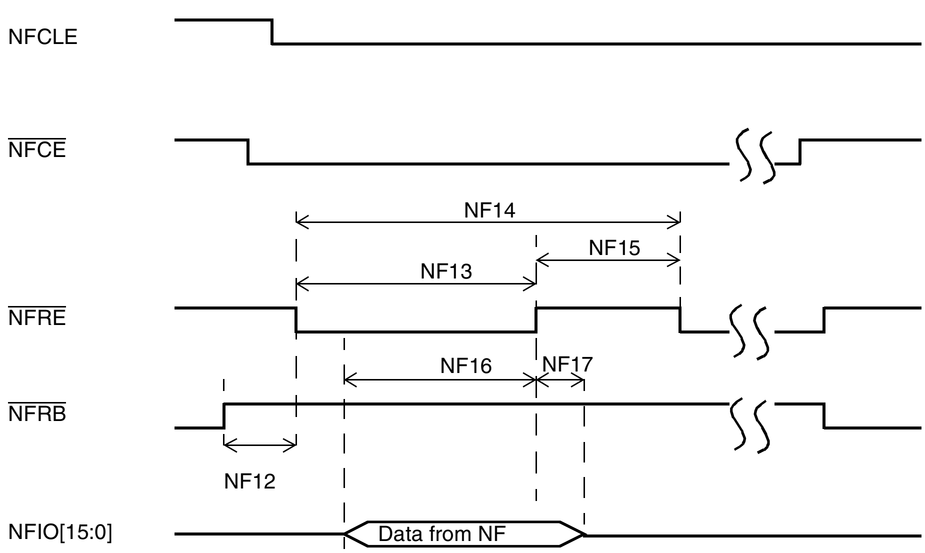


Figure 37. Read Data Latch Cycle Timing Diagram

Table 50. NFC Timing Parameters[1]

ID	Parameter	Symbol	Timing T = NFC Clock Cycle		Example Timing for NFC Clock ≈ 33 MHz T = 30 ns		Unit
			Min.	Max.	Min.	Max.	
NF1	NFCLE setup time	tCLS	T–1.0 ns	—	29	—	ns
NF2	NFCLE hold time	tCLH	T–2.0 ns	—	28	—	ns
NF3	NFCE setup time	tCS	T–1.0 ns	—	29	—	ns
NF4	NFCE hold time	tCH	T–2.0 ns	—	28	—	ns

Table 50. NFC Timing Parameters[1] (continued)

ID	Parameter	Symbol	Timing T = NFC Clock Cycle		Example Timing for NFC Clock ≈ 33 MHz T = 30 ns		Unit
			Min.	Max.	Min.	Max.	
NF5	NF_WP pulse width	tWP	T–1.5 ns		28.5		ns
NF6	NFALE setup time	tALS	T	—	30	—	ns
NF7	NFALE hold time	tALH	T–3.0 ns	—	27	—	ns
NF8	Data setup time	tDS	T	—	30	—	ns
NF9	Data hold time	tDH	T–5.0 ns	—	25	—	ns
NF10	Write cycle time	tWC	2T		60		ns
NF11	NFWE hold time	tWH	T–2.5 ns		27.5		ns
NF12	Ready to NFRE low	tRR	6T	—	180	—	ns
NF13	NFRE pulse width	tRP	1.5T	—	45	—	ns
NF14	READ cycle time	tRC	2T	—	60	—	ns
NF15	NFRE high hold time	tREH	0.5T–2.5 ns		12.5	—	ns
NF16	Data setup on read	tDSR	N/A		10	—	ns
NF17	Data hold on read	tDHR	N/A		0	—	ns

[1] The Flash clock maximum frequency is 50 MHz.

NOTE

For timing purposes, transition to signal high is defined as 80% of signal value; while signal low is defined as 20% of signal value.

Timing for HCLK is 133 MHz. The internal NFC clock (Flash clock) is approximately 33 MHz (30 ns). All timings are listed according to this NFC clock frequency (multiples of NFC clock phases), except NF16 and NF17, which are not related to the NFC clock.

3.6.6.3 Wireless External Interface Module (WEIM) Timing

Figure 38 depicts the timing of the WEIM module, and Table 51 describes the timing parameters (WE1–WE27) shown in the figure.

All WEIM output control signals may be asserted and negated by internal clock relative to BCLK rising edge or falling edge according to corresponding assertion/negation control fields. Address always begins relative to BCLK falling edge, but may be ended on rising or falling edge in muxed mode according to the control register configuration. Output data begins relative to BCLK rising edge except in muxed mode, where rising or falling edge may be used according to the control register configuration. Input data, ECB and DTACK are all captured relative to BCLK rising edge.

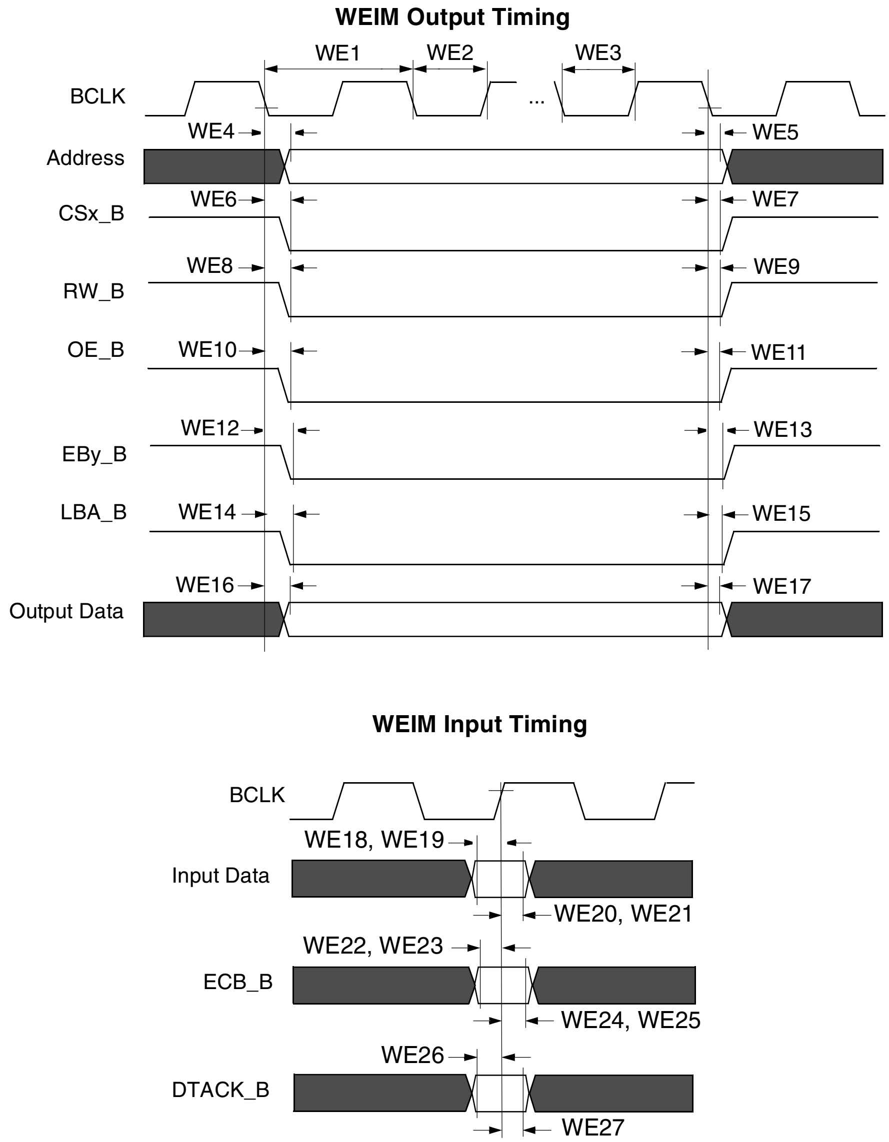


Figure 38. WEIM Bus Timing Diagram

Table 51. WEIM Bus Timing Parameters[1]

ID	Parameter	Min.	Max.	Unit
WE1	BCLK cycle time[2]	7.5	—	ns
WE2	BCLK low-level width[2]	3.0	—	ns
WE3	BCLK high-level width[2]	3.0	—	ns
WE4	Clock fall to address valid	0.7	2.0	ns
WE5	Clock rise/fall to address invalid	0.7	2.5	ns
WE6	Clock rise/fall to CSx_B valid	0.4	2.3	ns
WE7	Clock rise/fall to CSx_B invalid	0.4	2.3	ns

Table 51. WEIM Bus Timing Parameters[1] (continued)

ID	Parameter	Min.	Max.	Unit
WE8	Clock rise/fall to RW_B valid	0.9	2.6	ns
WE9	Clock rise/fall to RW_B invalid	0.9	2.6	ns
WE10	Clock rise/fall to OE_B valid	1.2	2.5	ns
WE11	Clock rise/fall to OE_B invalid	1.2	2.5	ns
WE12	Clock rise/fall to EBy_B valid	0.7	2.4	ns
WE13	Clock rise/fall to EBy_B invalid	0.7	2.4	ns
WE14	Clock rise/fall to LBA_B valid	1.0	2.8	ns
WE15	Clock rise/fall to LBA_B invalid	1.0	2.8	ns
WE16	Clock rise/fall to output data valid	1.0	3.0	ns
WE17	Clock rise to output data invalid	1.0	3.0	ns
WE18	Input data valid to clock rise, FCE=1	1.2	—	ns
WE19	Input data valid to clock rise, FCE=0	6.9	—	ns
WE20	Clock rise to input data invalid, FCE=1	0.2	—	ns
WE21	Clock rise to input data invalid, FCE=0	2.4	—	ns
WE22	ECB_B setup time, FCE=1	1.1	—	ns
WE23	ECB_B setup time, FCE=0	7.2	—	ns
WE24	ECB_B hold time, FCE=1	0	—	ns
WE25	ECB_B hold time, FCE=0	0	—	ns
WE26	DTACK_B setup time	5.4	—	ns
WE27	DTACK_B hold time	–3.2	—	ns

1 High is defined as 80% of signal value; low is defined as 20% of signal value.

2 BCLK parameters are being measured from the 50% point. For example, high is defined as 50% of signal value and low is defined as 50% as signal value.

NOTE

The test condition load capacitance was 25 pF. Recommended drive strength for all controls, address, and BCLK is maximum drive.

Recommended drive strength for all controls, address and BCLK is maximum drive.

Figure 39 through Figure 44 give examples of basic WEIM accesses to external memory devices with the timing parameters described in Table 51 for specific control parameter settings.

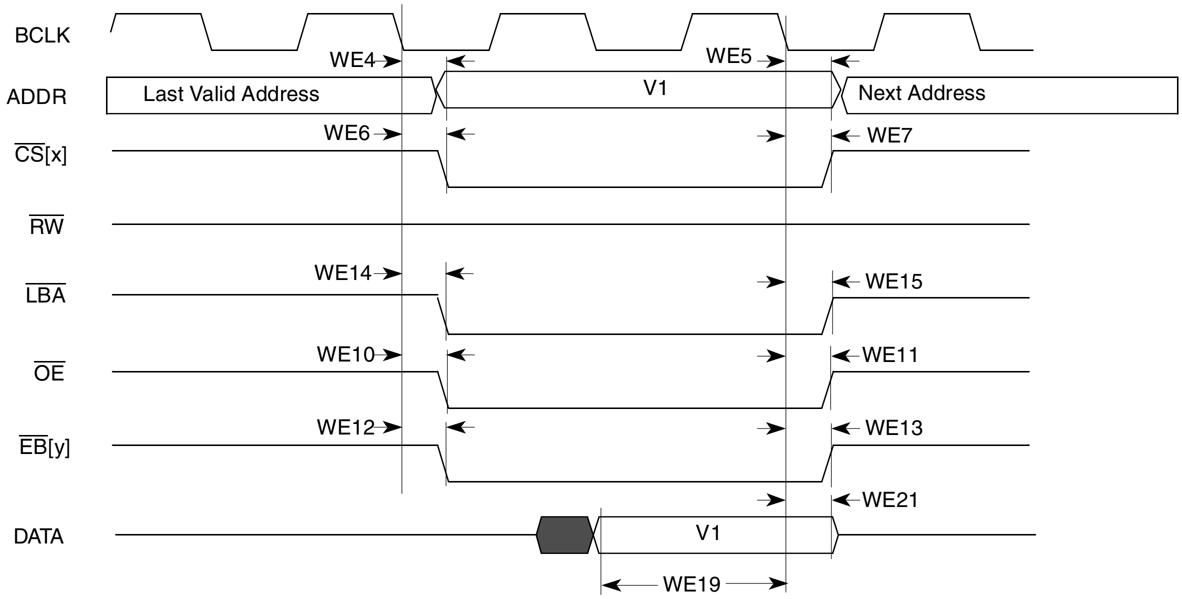


Figure 39. Synchronous Memory Timing Diagram for Read Access—WSC=1

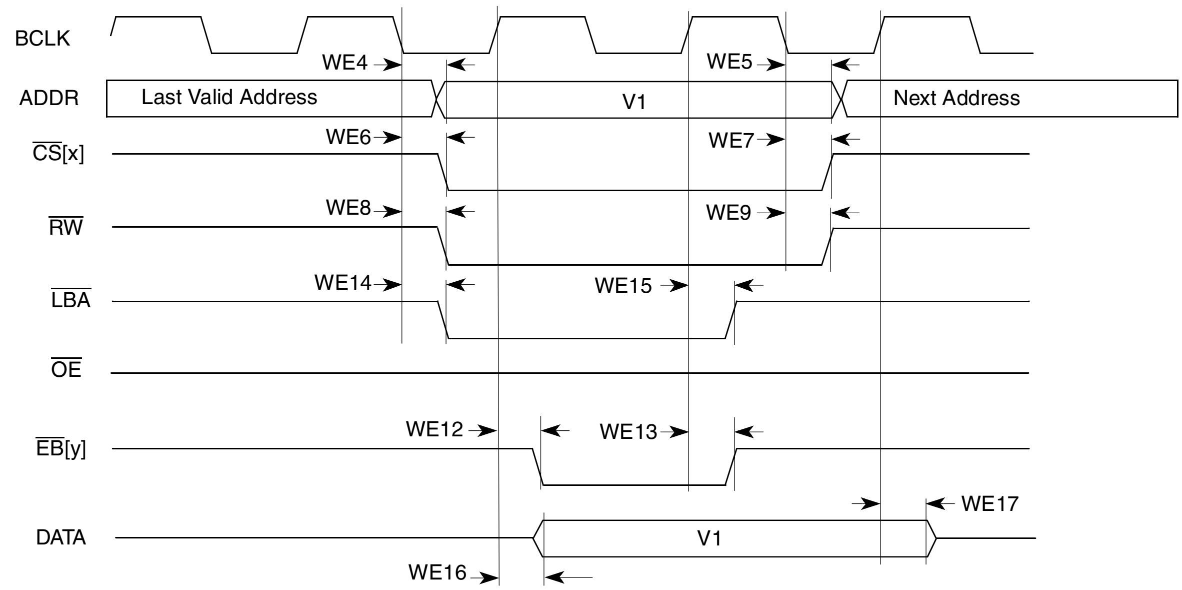


Figure 40. Synchronous Memory Timing Diagram for Write Access—WSC=1, EBWA=1, EBWN=1, LBN=1