Document Number: MC34700
Rev. 4, 6/2008

RoHS

9 to 18V, Quad Output, Integrated MOSFET Power Supply

34700

POWER SUPPLY

EP SUFFIX (Pb FREE)
98ASA10800D
32-Pin QFN
5 x 5mm

The 34700 is a compact, high efficiency power supply, with on-chip power MOSFETs that feature three step down switching regulators and one low dropout linear regulator. The switching regulators utilize voltage mode control with external compensation, allowing flexibility in optimizing the performance of the 34700 for a given application.

The 34700 is ideal for space constrained applications where multiple power rails are required and simplicity of design and implementation of the power supply is necessary. Over-voltage, under-voltage, over-current, and over-temperature protection features ensure robust and reliable operation. Fixed switching frequency, internal soft start, and internal power MOSFETs enable rapid power supply design and development.

The 34700 is well suited for power supply designs in wide variety of applications, including set top boxes, cable modems, laser printers, fax machines, point of sale terminals, small appliances, telecom line cards, and DVD players.

ORDERING INFORMATION		
Device	**Temperature Range (T_A)**	**Package**
MC34700EP/R2	-40°C to 85°C	32 QFN

Features

- Three switching regulators: 2 synchronous and 1 non-synchronous
- One low dropout linear regulator
- Input current capability:
  - 1.5A continuous on channel 1
  - 1.25A continuous on channels 2 and 3
  - 400mA continuous on channel 4
  - Internal power MOSFETs on all channels
- Voltage feed forward on channel 1
- ±1.5% Output voltage accuracy on all channels
- Cycle-by-cycle current limit and short-circuit protection
- Fixed 800kHz switching frequency
- Internal soft start
- Over-voltage, under-voltage, and over-temperature protection
- Open-drain power good output signal
- Separate active-high enable input for each channel
- Pb-free packaging designated by suffix code EP

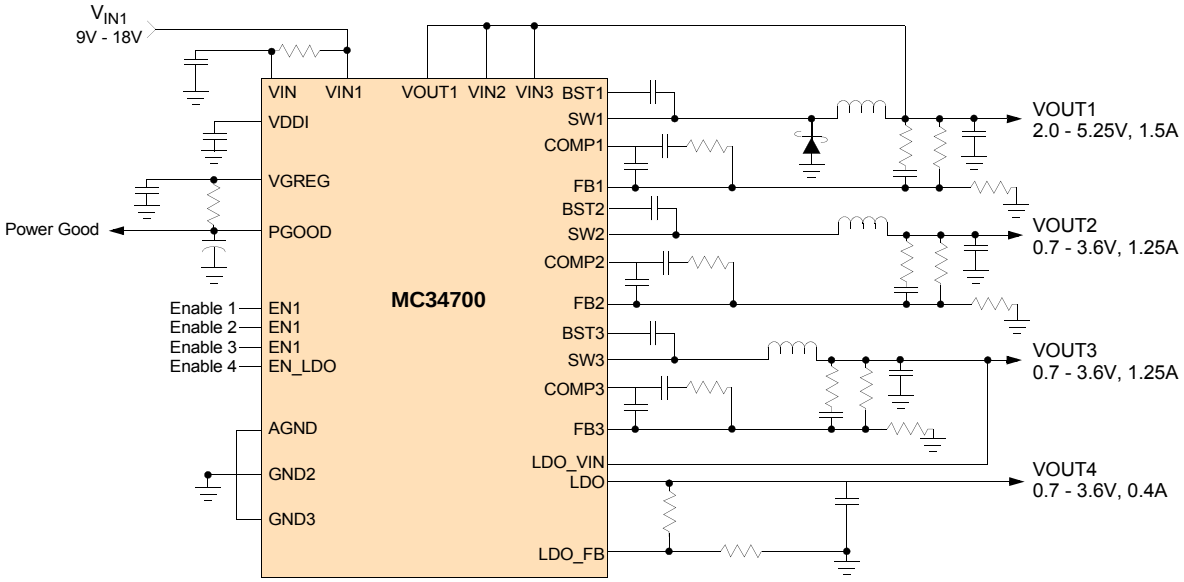


Figure 1. MC34700 Simplified Application Diagram

freescale semiconductor

INTERNAL BLOCK DIAGRAM

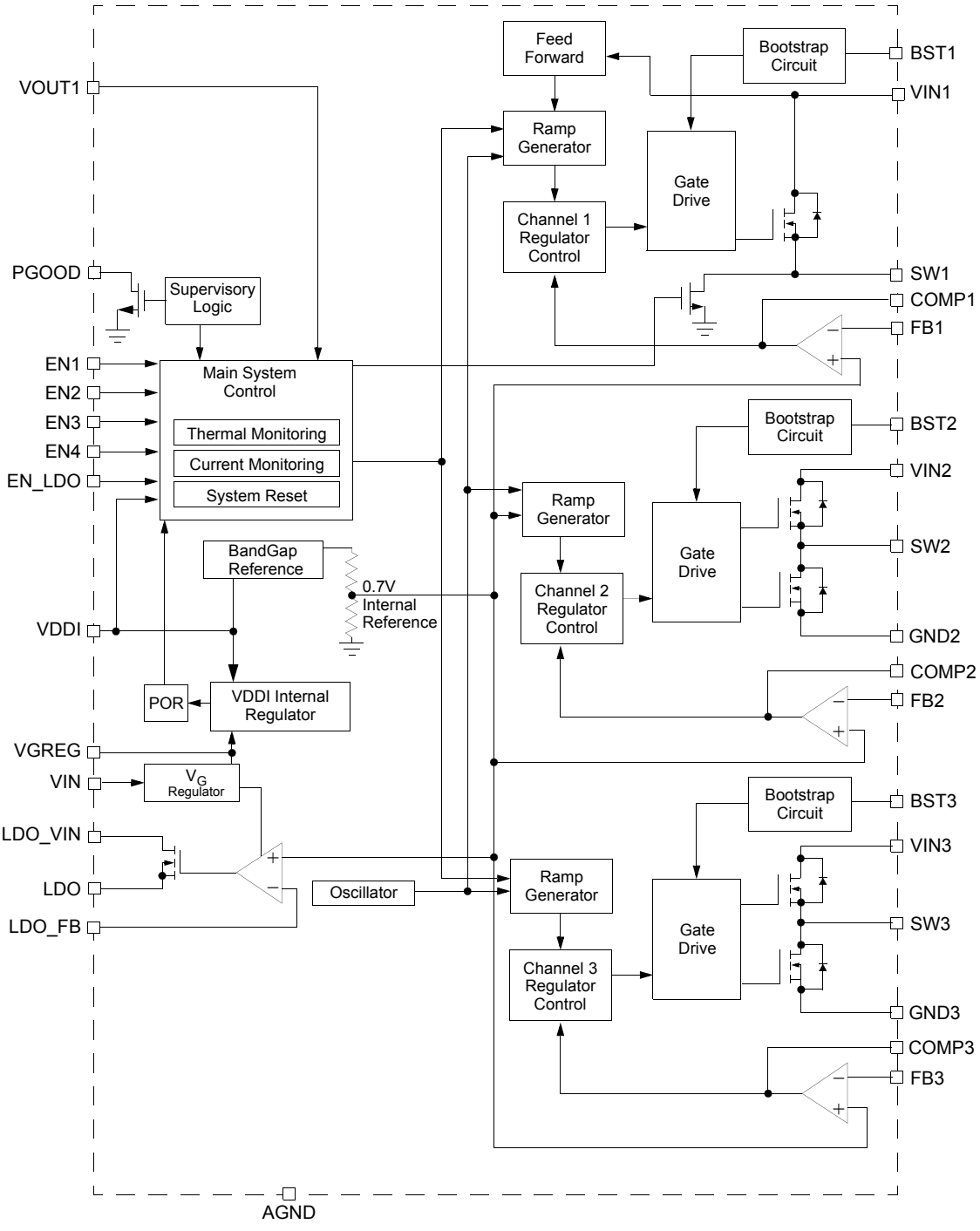


Figure 2. 34700 Simplified Internal Block Diagram

PIN CONNECTIONS

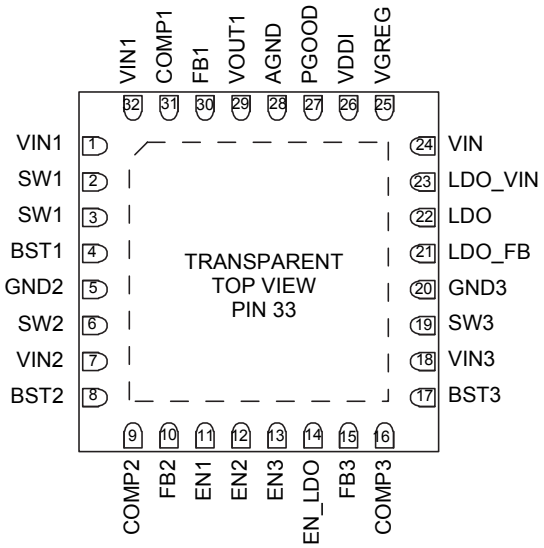


Figure 3. 34700 Pin Connections

Table 1. 34700 Pin Definitions

Pin Number	Pin Name	Pin Function	Formal Name	Definition
1,32	VIN1	Power Input	DC/DC1 Power Input	Buck regulator #1 power input. VIN1 is connected to the drain of DC/DC1's high side MOSFET.
2,3	SW1	Power Output	Switch 1 Output	Buck regulator #1 switching node. SW1 is connected to the source of DC/DC1's high side MOSFET.
4	BST1	Input	Bootstrap1	Bootstrap capacitor input for DC/DC1.
5	GND2	Power Ground	Power Ground	Buck regulator #2 power ground. GND2 is connected to the source of DC/DC2's low side MOSFET.
6	SW2	Power Output	Switch 2 Output	Buck regulator #2 switching node. SW2 is connected to the source of the high side MOSFET and the drain of the low side MOSFET.
7	VIN2	Power Input	DC/DC2 Power Input	Buck regulator #2 power input. VIN2 is connected to the drain of DC/DC2's high side MOSFET.
8	BST2	Input	Bootstrap2	Bootstrap capacitor input for DC/DC2.
9	COMP2	Output	DC/DC2 Compensation Output	Buck regulator #2 compensation output. COMP2 is connected to the error amplifiers output.
10	FB2	Input	DC/DC2 Feedback Input	Buck regulator #2's error amplifier inverting input. Connect the output voltage feedback resistor divider and compensation network to this pin.
11	EN1	Input	Enable DC/DC1	Enables buck regulator #1. Asserting EN1 turns on DC/DC1.
12	EN2	Input	Enable DC/DC2	Enables buck regulator #2. Asserting EN2 turns on DC/DC2.
13	EN3	Input	Enable DC/DC3	Enables buck regulator #3. Asserting EN3 turns on DC/DC3.
14	EN_LDO	Input	Enable LDO	Enables the LDO. Asserting EN_LDO turns on the LDO.
15	FB3	Input	DC/DC3 Feedback Input	Buck regulator #3's error amplifier inverting input. Connect the output voltage feedback resistor divider and compensation network to this pin.

Table 1. 34700 Pin Definitions (continued)

Pin Number	Pin Name	Pin Function	Formal Name	Definition
16	COMP3	Output	DC/DC3 Compensation Output	Buck regulator #3 compensation output. COMP3 is connected to the error amplifiers output.
17	BST3	Input	Bootstrap3	Bootstrap capacitor input for DC/DC3.
18	VIN3	Power Input	DC/DC3 Power Input	Buck regulator #3 power input. VIN3 is connected to the drain of DC/DC3's high side MOSFET.
19	SW3	Output	Switch 3 Output	Buck regulator #3 switching node. SW3 is connected to the source of the high side MOSFET and the drain of the low side MOSFET.
20	GND3	Power Ground	Power Ground	Buck regulator #3 power ground. GND3 is connected to the source of DC/DC3's low side MOSFET.
21	LDO_FB	Input	LDO Feedback Input	The LDO's error amplifier inverting input. Connect the output voltage feedback resistor divider to this pin.
22	LDO	Output	Linear Regulator Output	LDO output connection.
23	LDO_VIN	Power Input	Input supply for the Linear Regulator	The LDO's power input. LDO_VIN is connected to the drain of the linear regulator's MOSFET.
24	VIN	Input	Input Supply Voltage	The IC's supply voltage input.
25	VGREG	Output	Gate driver Supply Voltage Output	Internal regulator used to supply the gate drivers of the buck regulators.
26	VDDI	Output	Internal Core Voltage Output	Internal regulator used to supply the internal logic and analog blocks.
27	PGOOD	Output	Power Good Output Signal	Status signal used to indicate that all the regulators' output voltages are good. Upon a fault occurrence this output goes low.
28	AGND	Ground	Ground	Analog ground of the IC. All signals are referenced to this pin.
29	VOUT1	Input	VOUT1 Shunt	Buck regulator #1's shunt input. VOUT1 is connected to a discharge MOSFET.
30	FB1	Input	DC/DC1 Feedback Input	Buck regulator #1's error amplifier inverting input. Connect the output voltage feedback resistor divider and compensation network to this pin.
31	COMP1	Output	DC/DC1 Compensation Output	Buck regulator #1 compensation output. COMP1 is connected to the error amplifiers output.
33	GND	Ground	Thermal Pad	Thermal pad for heat transfer. Connect the thermal pad to the analog ground and ground plane for heat sinking.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			
Input Voltages			V
Input Voltage	V_{IN}	-0.3 to 20	
Input DC/DC1 Voltage, I_{Vin} = 0	V_{IN1}	-0.3 to 20	
Input DC/DC 2, 3, and LDO Voltage	V_{IN2}, V_{IN3}, V_{INLDO}	-0.3 to 7.0	
Switch Node Voltages			V
Switch Node DC/DC1	V_{SW1}	-0.3 to 20	
Switch Node DC/DC2, and 3	V_{SW2}, V_{SW3}	-0.3 to 7.0	
Bootstrap Voltages			V
Bootstrap DC/DC1	V_{BST1}	-0.3 to 25	
Bootstrap DC/DC2, and 3	V_{BST2}, V_{BST3}	-0.3 to 14	
Bootstrap Voltage referenced to Switch Node Voltage	V_{BST}-V_{SW}	-0.3 to 7.0	
Compensation (COMP1, 2, and 3), Feedback (FB1, 2, 3, LDO_FB), VDDI	-	-0.3 to 3	V
All Other Pins (EN1, 2, 3, EN_LDO, PGOOD, VGREG, LDO, VOUT1)	-	-0.3 to 7	V
ESD Voltage[1]	V_{ESD}		V
Human Body Model (HBM) All Pins		±2000	
THERMAL RATINGS			
Operating Temperature			°C
Ambient	T_A	-40 to +85	
Junction	T_J	-40 to +125	
Peak Package Reflow Temperature During Reflow[2],[3]	T_{PPRT}	300	°C
Storage Temperature	T_{STG}	-40 to +150	°C
THERMAL RESISTANCE			
Thermal Resistance[2]			°C/W
Junction-to-Case	$T_{\Theta JC}$	6.7	
Junction-to-Ambient	$T_{\Theta JA}$	37	
Power Dissipation	P_D		W
T_A = 25°C		2.5	
T_A = 70°C		1.3	
T_A = 85°C		1.0	

Notes

1. ESD testing is performed in accordance with the Human Body Model (HBM) (C_{ZAP} = 100pF, R_{ZAP} = 1500Ω).
2. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
3. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics noted under conditions 9.0V ≤ V_{IN} ≤ 18V, -40°C ≤ T_A ≤ 85°C, GND = 0V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER SUPPLY					
VIN Voltage Maximum Minimum	V_{IN}	 - -	 18 9.0	 - -	V
Standby Current V_{EN1} = V_{EN2} = V_{EN3} = V_{EN_LDO} = 0V	I_{SDB}	-	8.95	15	mA
Operating Current V_{EN1} = V_{EN2} = V_{EN3} = V_{EN_LDO} = 5.0V, V_{VIN} = 9.0V, Load = 0A	I_{IN}	-	15.4	-	mA
Internal Supply Voltage	V_{DDI}	2.3	2.5	2.7	V
POWER-ON RESET					
VGREG Rising Threshold Voltage	V_{VGREG_RISE}	3.5	4.0	4.5	V
VGREG Falling Threshold Voltage	V_{VGREG_FALL}	3.0	3.4	4.0	V
VGREG Hysteresis Voltage	V_{VGREG_HYS}	0.2	0.55	1.0	V
VGREG LINEAR REGULATOR					
On Resistance I_{VGREG} = 80mA	$R_{VGREGIN}$	-	30	-	Ω
Output Voltage	V_{VGREG}	4.75	5.25	5.5	V
BIAS VOLTAGES					
VGREG Decoupling VGREG = 5V	C_{VGREG}	-	1.0	-	µF
VDDI Decoupling VDDI = 2.5V	C_{VDDI}	-	1.0	-	µF
ENABLE					
Output Enable Logic High Threshold Voltage	$V_{EN1,2,3}$ V_{EN_LDO}	0.78	-	-	V
Output Enable Logic Low Threshold Voltage	$V_{EN1,2,3}$ V_{EN_LDO}	-	-	0.61	V
EN Input Resistance to Ground	R_{EN_IN}	-	1.5	-	MΩ
REFERENCE					
DC/DC 1, 2, 3 Reference Voltage	$V_{REF1,2,3}$	0.690	0.700	0.710	V
LDO Reference Voltage	V_{REF_LDO}	0.690	0.700	0.710	V

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 9.0V ≤ V_{IN} ≤ 18V, -40°C ≤ T_A ≤ 85°C, GND = 0V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER GOOD					
OV Threshold, all regulators Percentage of setpoint	Δ_{OV_TH}	-	-	108	%
UV Threshold, all regulators Percentage of setpoint	Δ_{UV_TH}	92	-	-	%
PGOOD Output Low Level I_{SINK} = 6.0mA	V_{OL_PGOOD}	-	0.4	-	V
BUCK CONVERTER 1					
Maximum VIN1 Input Voltage	V_{IN1_MAX}	-	18	-	V
Minimum VIN1 Input Voltage	V_{IN1_MIN}	-	9.0	-	V
Maximum Output Voltage V_{IN} = 9.0V	$V_{DC1VOUTMAX}$	-	5.25	-	V
Minimum Output Voltage V_{IN} = 9.0V	$V_{DC1VOUTMIN}$	-	2.0	-	V
Maximum Output Current	$IOUT_{DC1MAX}$	-	1.5	-	A
Total System Accuracy	ΔV_{OUT1}	-1.5	-	1.5	%
Peak Short-circuit Current Limit	I_{SHORT1}	2.5	-	4.5	A
High Side On Resistance	$R_{DS(ON)\_HS}$	-	150	-	mΩ
Equivalent Dropout Resistance V_{IN1} = 5.5V, V_{OUT} = 3.3V, I_{LOAD} = 2A	R_{DO}	-	183	-	mΩ
BUCK CONVERTER 2					
Maximum VIN2 Input Voltage	V_{IN2_MAX}	-	6.0	-	V
Minimum VIN2 Input Voltage	V_{IN2_MIN}	-	1.5	-	V
Maximum Output Voltage	$V_{DC2VOUTMAX}$	-	3.6	-	V
Minimum Output Voltage	$V_{DC2VOUTMIN}$	-	0.7	-	V
Maximum Output Current	$IOUT_{DC2MAX}$	-	1.25	-	A
Total System Accuracy	ΔV_{OUT2}	-1.5	-	1.5	%
Peak Short-circuit Current Limit	I_{SHORT2}	2.0	-	4.5	A
High Side On Resistance	$R_{DS(ON)\_HS}$	-	175	-	mΩ
Low Side On Resistance	$R_{DS(ON)\_LS}$	-	150	-	mΩ
Equivalent Dropout Resistance V_{IN2} = 1.7V, V_{OUT} = 1.25V, I_{LOAD} = 1.25A	R_{DO}	-	150	-	mΩ
SW2 Leakage Current V_{IN} = 12V, V_{IN2} = 0V, EN2 = 0V	I_{SW2}	-	400	-	μA

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 9.0V ≤ V_{IN} ≤ 18V, -40°C ≤ T_A ≤ 85°C, GND = 0V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
BUCK CONVERTER 3					
Maximum VIN3 Input Voltage	V_{IN3_MAX}	-	6.0	-	V
Minimum VIN3 Input Voltage	V_{IN3_MIN}	-	1.5	-	V
Maximum Output Voltage	$V_{DC3VOUTMAX}$	-	3.6	-	V
Minimum Output Voltage	$V_{DC2VOUTMIN}$	-	0.7	-	V
Maximum Output Current	$IOUT_{DC3MAX}$	-	1.25	-	A
Total System Accuracy	ΔV_{OUT3}	-1.5	-	1.5	%
Peak Short-circuit Current Limit	I_{SHORT3}	2.0	-	4.5	A
High Side On Resistance	$R_{DS(ON)\_HS}$	-	160	-	mΩ
Low Side On Resistance	$R_{DS(ON)\_LS}$	-	140	-	mΩ
Equivalent Dropout Resistance V_{IN2} = 1.7V, V_{OUT} = 1.25V, I_{LOAD} = 1.25A	R_{DO}	-	150	-	mΩ
SW3 Leakage Current V_{IN} = 12V, V_{IN3} = 0V, EN3 = 0V	I_{SW3}	-	400	-	μA
LINEAR REGULATOR					
Maximum LDO Input Voltage	$V_{INLDOMAX}$	-	6.0	-	V
Minimum LDO Input Voltage	$V_{INLDOMIN}$	-	1.5	-	V
Maximum LDO Output Voltage	V_{LDOMAX}	-	3.6	-	V
Minimum LDO Output Voltage	V_{LDOMIN}	-	0.7	-	V
Maximum LDO Output Current	I_{LDO}	-	400	-	mA
Total System Accuracy	ΔV_{LDO}	-1.5	-	1.5	%
Maximum Dropout Voltage I_{LDO} = 400mA	V_{DROP}	-	250	-	mV
Maximum LDO Power Dissipation	P_{DISS_LDO}	-	375	-	mW
Maximum Output Current	I_{SHORT_LDO}	-	1100	-	mA
Minimum Output Current	I_{SHORT_LDO}	-	500	-	mA
Required Output Decoupling	C_{LDO}	-	10	-	μF
THERMAL SHUTDOWN					
Maximum Thermal Shutdown Threshold	T_{SD_MAX}	-	160	-	°C
Typical Thermal Shutdown Threshold	T_{SD}	-	140	-	°C
Minimum Thermal Shutdown Threshold	T_{SD_MIN}	-	120	-	°C
Thermal Shutdown Hysteresis	T_{SD_HYS}	-	25	-	°C

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions 9.0V ≤ V_{IN} ≤ 18V, -40°C ≤ T_A ≤ 85°C, GND = 0V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
OSCILLATOR					
Switching Frequency	f_{SW}	760	800	840	kHz
VGREG LINEAR REGULATOR					
Maximum Input dV/dT VIN1 = VIN	$V_{IN\_dV/dT}$	-	10	-	V/µs
ENABLE					
Delay from Enable to Soft Start DC1	t_{DELAY1}	-	1.0	-	ms
Delay from Enable to Soft Start DC2, DC3	$t_{DELAY2,3}$	-	160	-	µs
SOFT START					
Soft Start Duration DC1, 2, 3	$t_{SS\_BUCKREG}$	2.5	3.5	4.5	ms
Soft Start Duration LDO	t_{SS_LDO}	0.3	0.5	0.7	ms
RAMP GENERATORS					
Ramp Amplitude (DC/DC1) Typical Voltage Range V_{FF_GAIN1} x VIN1, VIN1 = 18V	V_{RAMP_AMP1}	-	1.0	-	V_{P-P}
VFF Gain (DC/DC1)	V_{FF_GAIN1}	-	0.055		V/V
Ramp Amplitude (DC/DC2,3) Typical Voltage Range V_{FF_GAIN2} x VIN2, VIN2 = 6.0V	$V_{RAMP\_AMP2,3}$	-	1.25	-	V_{P-P}
VFF Gain (DC/DC2,3)	$V_{FF\_GAIN2,3}$	-	0.208		V/V
Ramp Bottom/Offset (DC/DC1,2,3)	V_{RAMP_OS}	-	0.2	-	V
Min Duty Cycle (DC/DC1) I_{LOAD1} = 0A	D_1	-	-	16	%
Max Duty Cycle (DC/DC1) I_{LOAD1} = 0A	D_1	68.4	-	-	%
Min Duty Cycle (DC/DC2,3) I_{LOAD1} = 0A	$D_{2,3}$	-	0	0	%
Max Duty Cycle (DC/DC2,3) I_{LOAD1} = 0A	$D_{2,3}$	83.6	-	-	%
POWER-GOOD					
PGOOD Reset Delay	$t_{PG-RESET}$		100		µs
PGOOD Glitch Rejection	$t_{PG-FILTER}$		10		µs

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions $9.0V \le V_{IN} \le 18V$, $-40°C \le T_A \le 85°C$, GND = 0V, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A = 25°C$ under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
BUCK CONVERTER 1					
Error Amplifier DC Gain	A_{EA}	-	110	-	dB
Error Amplifier Unity-gain Bandwidth	GBW	-	4.0	-	MHz
Error Amplifier Slew Rate @ 15pF	SR	-	1.8	-	V/µs
Current Limit Timer	t_{LIM1}	-	10	-	ms
Current Limit Retry Timeout Period	$t_{TIMEOUT1}$	-	100	-	ms
BUCK CONVERTER 2					
Error Amplifier DC Gain	A_{EA}	-	110	-	dB
Error Amplifier Unity-gain Bandwidth	GBW	-	4.0	-	MHz
Error Amplifier Slew Rate	SR	-	1.8	-	V/µs
Current Limit Timer	t_{LIM2}	-	10	-	ms
Current Limit Retry Timeout Period	$t_{TIMEOUT2}$	-	100	-	ms
BUCK CONVERTER 3					
Error Amplifier DC Gain	A_{EA}	-	110	-	dB
Error Amplifier Unity-gain Bandwidth	GBW	-	4.0	-	MHz
Error Amplifier Slew Rate	SR	-	1.8	-	V/µs
Current Limit Timer	t_{LIM3}	-	10	-	ms
Current Limit Retry Timeout Period	$t_{TIMEOUT3}$	-	100	-	ms
LINEAR REGULATOR					
Current Limit Retry Timeout Period	$t_{TIMEOUT\_LDO}$	-	100	-	ms

FUNCTIONAL DESCRIPTION

INTRODUCTION

When products and technologies are first introduced, the power needs are generally met with individual regulators. These regulators can be changed or adjusted to match the ever changing requirements. As products and technologies mature, the requirements become more defined, and the individual regulators can be replaced with a multiple output power IC. The integrated solution is cost effective, and offers size reduction and reliable operation.

The 34700 is a high efficiency, four output, integrated power regulator. It includes three switching buck regulators and an LDO. The first buck regulator, DC/DC1, uses a non-synchronous, voltage mode topology and can operate over a wide external supply voltage range of 9V to 18V. It is capable of delivering 1.5A of continuous current. The other buck regulators, DC/DC 2 and DC/DC3, use a synchronous rectifier, voltage mode topology, and operate from an external supply voltage range of 1.5V to 6V. They are each capable of delivering 1.25A of continuous current. The LDO has a separate input that can be connected to any of the buck regulators' outputs, or to an external supply, depending on the application. The LDO is capable of delivering 400mA of continuous current.

The 34700 includes control, supervisory, and protection features. It has individual enables for each regulator. This allows the power up and power down sequencing to be controlled by the user. The 34700 monitors each of the regulators' output voltage for an over-voltage or under-voltage condition. If any of the outputs are out of regulation, either too high or too low, the "power good" status signal will go low. The 34700 includes cycle by cycle current limiting and short-circuit protection, as well as thermal shutdown protection.

By integrating the control, supervisory and protection features along with the four regulators into a single 5 x 5mm QFN package, all of the functions that four individual regulators can perform are now available in the 34700.

FUNCTIONAL PIN DESCRIPTION

INPUT SUPPLY VOLTAGE (VIN)

IC supply voltage input. This pin should be de-coupled from the VIN1 supply voltage. Filtering is required for proper device operation.

POWER INPUT VOLTAGE (VIN1, VIN2, VIN3, LDO_VIN)

Buck regulators and LDO power input voltage. VIN1, 2, 3 is connected to the drain of the respective DC/DC's high side MOSFET. LDO_VIN is connected to the drain of the linear regulator's pass device. Local bypass capacitors are recommended.

SWITCH NODE (SW1, SW2, SW3)

Buck regulator's switching node. SW1 is connected to the source of the high side MOSFET. Connect this pin to the cathode of the catch diode and the output inductor. SW2 and SW3 are connected to source of the high side and the drain of the low side MOSFET. Connect this pin to the output inductor.

BOOTSTRAP INPUT (BST1, BST2, BST3)

Bootstrap capacitor input. Connect a capacitor between the BST and SW pin of the respective DC/DC to enhance the gate of the high side MOSFET during switching.

ERROR AMPLIFIER INVERTING INPUT (FB1, FB2, FB3, LDO_FB)

Buck regulator and LDO error amplifier inverting input. Connect the output voltage feedback resistor divider to this pin.

COMPENSATION INPUT (COMP1, COMP2, COMP3)

Buck regulators compensation input. COMP is connected to the error amplifier's output of the respective DC/DC regulator. Connect the external compensation components between the COMP pin and the FB pin of the respective buck regulator.

POWER GROUND (GND2, GND3)

Buck regulator power ground. GND is connected to the source of the low side MOSFET of the respective DC/DC regulator. Connect this pin to the DC/DC regulator's power return path.

ANALOG GROUND (AGND)

Analog ground of the IC. Internal analog and logic signals are referenced to this pin.

REGULATOR ENABLE (EN1, EN2, EN3, EN_LDO)

These inputs enable the buck regulators and the LDO. Asserting EN turns on the respective regulator. Control logic remains active as long as VIN is present.

VOUT1 SHUNT (VOUT1)

DC/DC1 shunt input. VOUT1 is connected to a discharge MOSFET. This MOSFET is used to discharge the output of DC/DC1 when there is a fault condition, such as thermal shutdown or a short-circuit. It is also used to provide a pre-load to maintain a minimum duty. Connect this pin to the output of DC/DC1.

LINEAR REGULATOR OUTPUT (LDO)

LDO regulator output. Connect this pin to the feedback resistor divider and output capacitor.

GATE DRIVE SUPPLY VOLTAGE OUTPUT (VGREG)

Internal regulator used to supply the gate drivers. VGREG is driven from the input supply voltage VIN, and is used to drive the gates of the low side MOSFETs of regulators DC/DC2 and DC/DC3. It is also used to supply the LDO. Connect this pin to a low ESR, 1µF bypass capacitor.

INTERNAL SUPPLY VOLTAGE (VDDI)

The internal regulator used to supply the internal logic and analog blocks. VDDI is driven from the gate drive supply voltage, VGREG. Connect this pin to a 1µF, low ESR decoupling filter capacitor.

POWER GOOD OUTPUT SIGNAL (PGOOD)

Status signal used to indicate that all the regulators' output voltages are good. Upon a fault occurrence, this output signal goes low. PGOOD is an open drain output, and must be pulled up by an external resistor to a supply voltage suitable for I/O.

FUNCTIONAL INTERNAL BLOCK DESCRIPTION

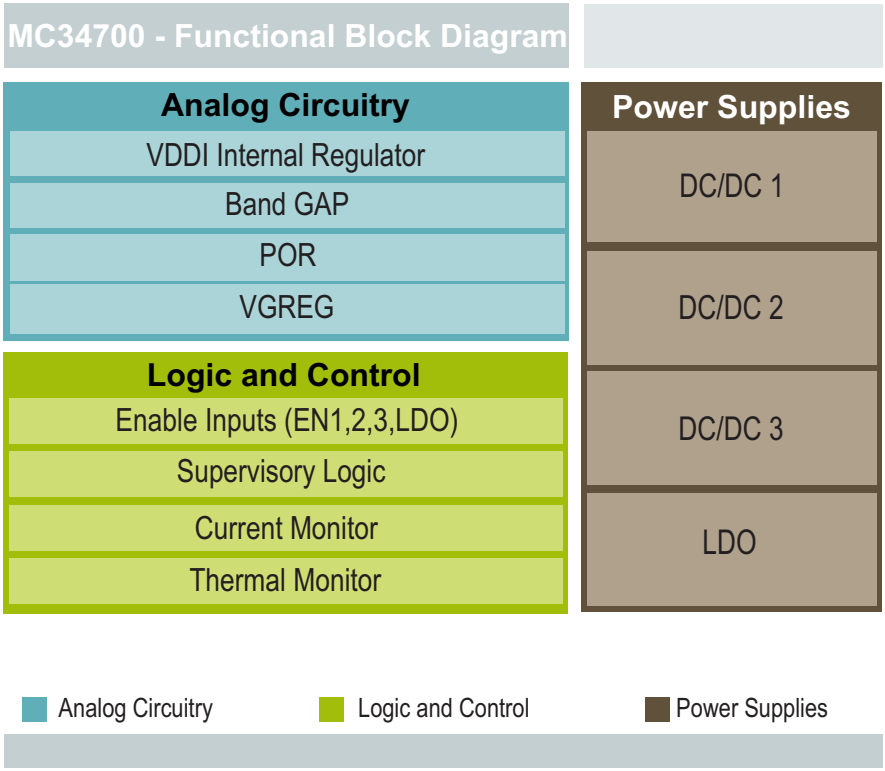


Figure 4. Functional Internal Block Diagram

ANALOG CIRCUITRY

VDDI Internal Regulator

This internal voltage regulator supplies 2.5V for the internal logic and analog circuitry. VDDI is driven from the gate drive supply voltage, VGREG.

Bandgap

The internal voltage reference provides the required precision value needed for the on-chip circuitry. This block is driven from the VDDI internal regulator, and generates a highly accurate 0.7V reference voltage for the internal comparators and regulators.

POR

This internal Power On Reset (POR) monitors the internal voltage regulators (VDDI, VGREG). If the internal regulators are above the specified rising threshold voltage, critical internal blocks are enabled. If the internal supplies are out of regulation, the internal blocks are disabled.

VGREG

This internal regulator supplies 5V for the gate drivers. VGREG is driven from the input supply voltage VIN, and is used to drive the gates of the low side MOSFETS of DC/DC 2 and DC/DC3. It is also used to supply the LDO block.

LOGIC AND CONTROL

Enable Inputs (EN1, 2, 3, and EN_LDO)

These 4 input control, logic level signals will turn the appropriate voltage regulator outputs on and off. Asserting EN turns on the respective regulator and begins a soft start ramp of the output voltage. Control logic remains active as long as VIN is present.

Supervisory Logic

This logic function will monitor the internal system control functions, and controls the PGOOD output to signal (logic 0) of any fault occurrence. Conditions monitored include output regulation, over-current, and over-temperature.

Current Monitor

This block detects over-current in the power MOSFET of each regulator. If an over-current condition is detected the regulator will turn off the MOSFET and wait for a timeout period before attempting a soft start retry.

Thermal Monitor

This block detects the temperature of the device and protects against overheating. If the temperature reaches the thermal shutdown threshold, the regulator will shutdown until the temperature has decreased by the hysteresis.

POWER SUPPLIES

DC/DC1

This is a non-synchronous switching buck regulator, utilizing a feed forward voltage mode control, with external compensation. This is the only converter in this IC that will regulate from a wide input supply voltage of 9V to 18V. It is capable of generating a 2V to 5.25V output at 1.5A.

DC/DC2

This is a synchronous switching buck regulator whose input can be fed from DC/DC1, or an external 1.5V to 6V source. It utilizes voltage mode control with external compensation. It is capable of generating a 0.7V to 3.6V output at 1.25A.

DC/DC3

This buck regulator is identical to DC/DC2. Note that all three switching regulators switch at 800kHz, and are 120° out of phase to help reduce system noise and input surge currents.

LDO

This low drop out regulator can feed off of any of the switching regulators or from an external 1.5V to 6V source. The dropout voltage is 250mV at the rated load. It is capable of generating a 0.7V to 3.6V output at 400mA.

FUNCTIONAL DEVICE OPERATION

OPERATIONAL MODES

Each regulator of the 34700 has three basic modes of operation.

NORMAL MODE

In normal mode, the regulator is fully operational. To be in this mode, the 34700 input supply, VIN, needs to be present and within its operating range. The regulator's power input voltage also needs to be present and in range. The ENABLE pin for the regulator needs to be asserted, and the output voltage needs to be in regulation. No over-current or thermal faults are present in normal mode.

STANDBY MODE

In standby mode, the ENABLE pin for the regulator is held low and the regulator is disabled. VIN needs to be present and within its operating range. The regulator's power input is not needed in this mode, but needs to be present and stable before transitioning to normal mode. The power good signal is low since the regulator's output is disabled. Note that the standby mode consumes the least amount of power.

FAULT MODE

In fault mode, the output is no longer in regulation, or an over-current or a thermal fault is present. To be in this mode the 34700 input supply, VIN needs to be present and within its operating range. The regulator's power input voltage also needs to be present and in range. However, if the power input is outside the operating range, a regulation fault may occur. The ENABLE pin for the regulator needs to be asserted and the power good signal is low.

START-UP SEQUENCE

When power is first applied to the 34700, the internal regulators and bias circuits need to be up and stable before the power on reset (POR) signal is released. The POR waits until the gate drive regulator's voltage, V_{GREG}, has reached about 4V before it allows the rest of the internal blocks to be enabled.

Each regulator has an independent enable pin. This allows the user to program the power up sequence to suit the application. As each regulator is turned on, it will execute a soft start ramp of the output voltage. This is done to prevent the output voltage from overshooting the regulation point. Without a soft start ramp, the output voltage will ramp up faster than the control loop can typically respond, resulting in overshoot. As a result, the soft start periods for the switching regulators are longer (3.5ms) than for the linear regulator (0.5ms). The soft start is active each time the regulator is enabled, after a fault retry, or when the IC power is recycled.

After a successful start-up sequence, where all the regulators are enabled, no faults have occurred, and the output voltage is in regulation, the power good signal goes open drain after a 100μs reset delay. A power good true indicates that all the regulators are functioning in normal operation mode.

PROTECTION FUNCTIONS

The 34700 monitors the regulators for several fault conditions to protect both the system load and the IC from overstress. The response of the 34700 to a fault condition is described as follows.

OUTPUT OVER-VOLTAGE

An over-voltage (OV) condition occurs when the output voltage exceeds the over-voltage threshold, Δ_{OV_TH}. This can occur if the regulator's output is shorted to a supply with a higher output voltage. In this case, the power good signal is pulled low, alerting the host that a fault is present, but the regulator remains active. The regulator will continue to try to regulate the output: DC/DC1 will pulse skip; DC/DC2, 3 will go to minimum duty; and the LDO pass device will go high impedance.

To avoid false trips of the OV monitor, the power good circuit has a 10μs glitch filter. Once the output voltage falls below the OV threshold and back into regulation, the fault is cleared and the power good signal goes high.

OUTPUT UNDER-VOLTAGE

An under-voltage (UV) condition occurs when the output voltage falls below the under-voltage threshold, Δ_{UV_TH}. This can occur if the regulator's output is shorted to ground, overloaded, or the power input voltage has decreased. In this case, the power good signal is pulled low, alerting the host that a fault is present, but the regulator remains active. The regulator will continue to try to regulate the output: DC/DC1, 2, 3 will go to maximum duty or current limit; and the LDO pass device will go low resistance.

To avoid false trips of the UV monitor, the power good circuit has a 10μs glitch filter. Once the output voltage rises above the UV threshold and back into regulation, the fault is cleared and the power good signal goes high.

CURRENT LIMIT

A current limit condition for the switching regulators' occurs when the peak current in the high side power MOSFET exceeds the current limit threshold. The switch current is monitored using a sense FET and a comparator. The sense FET acts as a current detecting device by sampling a fraction of the current in the power MOSFET. This sampled current is compared to an internal reference to determine if the regulator is exceeding the current limit or not.

If the peak switch current reaches the peak current limit threshold (I_{SHORT}), the regulator will start the cycle by cycle

current limit operation, the power good signal is pulled low after the 10μs glitch filter, and a 10ms current limit timer (t_{LIM}) begins. The regulator will stay in this mode of operation until one of the following occur:

- The current is reduced back to normal levels before the current limit timer expires and normal operation is resumed.
- The current limit timer expires without regaining normal operation, at which time the regulator turns off. The regulator remains off for a 100ms retry timeout period ($t_{TIMEOUT}$), after which the regulator will attempt a soft start cycle.
- The switch current continues to increase until it exceeds the cycle by cycle current limit by approximately 1A. At this point the regulator shuts down immediately. The regulator remains off for a 100ms retry timeout period ($t_{TIMEOUT}$), after which the regulator will attempt a soft start cycle.
- The device reaches the thermal shutdown limit (T_{SD}), the regulator turns off.

THERMAL SHUTDOWN

A thermal limit condition occurs when a power device reaches the thermal shutdown threshold (T_{SD}). The temperature of the power MOSFETs in the switching regulators and the LDO are monitored using a thermal sensing transistor located near the power devices.

If the temperature of a switcher or an LDO reaches the thermal shutdown threshold, the switcher or LDO regulator will switch off and the PGOOD output would indicate a fault by pulling low. The regulator will stay in this mode of operation until the temperature of the die has decreased by the hysteresis value, and the regulator will attempt a soft start cycle.

TYPICAL APPLICATIONS

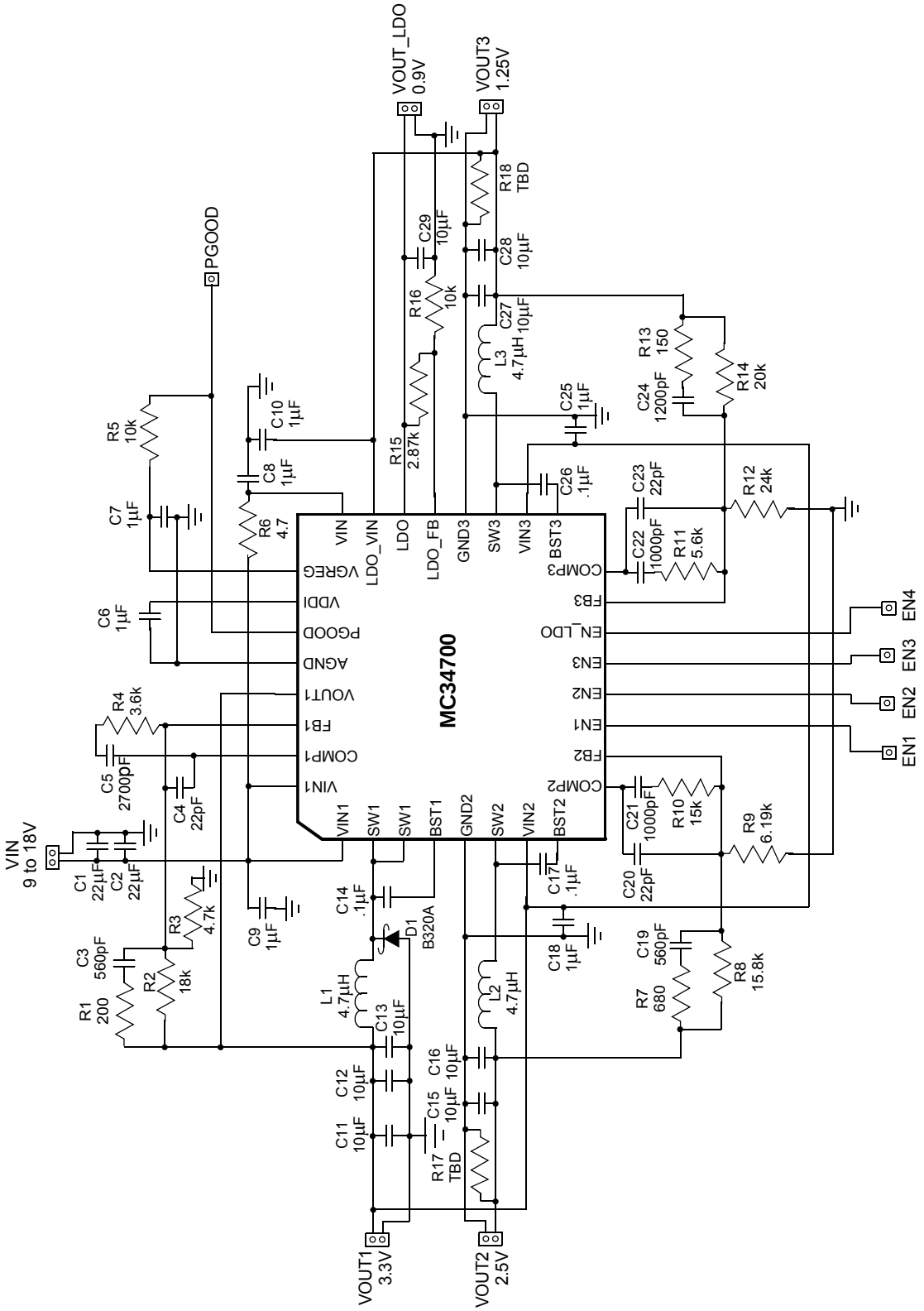


Figure 5. Typical Application Diagram

DESIGN CONSIDERATIONS

INPUT/OUTPUT CONFIGURATION

The 34700 has independent inputs for each regulator. This allows a high degree of flexibility as far as how the IC can be configured.

First, consider what supplies are available in the application, and the input voltage range that each regulator has. Only Buck Converter 1 has a 9V to 18V input voltage range. All the other regulators have a 1.5V to 6V input voltage range.

Next, consider the output voltages and currents required, and how best to match them to the 34700. Buck Converter 1 is capable of 2V to 5.25V at 1.5A, while Buck Converters 2 and 3 are capable of 0.7V to 3.6V at 1.25A each. The LDO is capable of 0.7V to 3.6V at a 400mA output.

Some sample configurations are show in Figures 6 thru 8. Note that not all combinations are shown, and all the regulators require an input voltage higher than the output voltage.

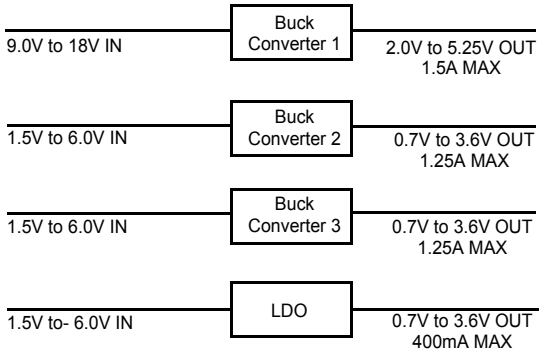


Figure 6. General Configuration

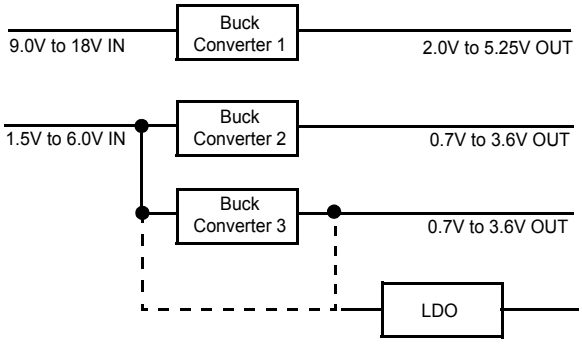


Figure 7. Dual Input Supply Configuration

MINIMUM/MAXIMUM DUTY LIMIT

Based on the application specifications, the minimum and maximum duty cycle of the buck converters need to be checked against the limits. For Buck Converter 1, there is a minimum limit of 16% and a maximum limit of 68.4%. For

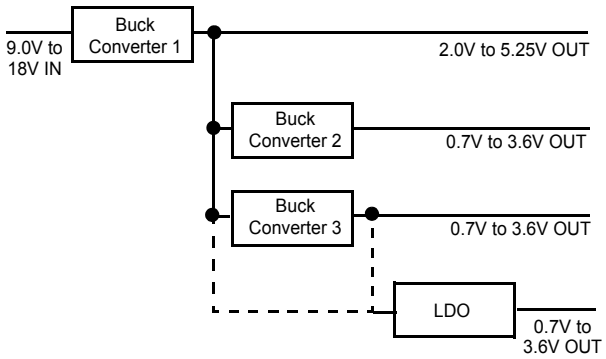


Figure 8. Single Input Supply Configuration

INPUT/OUTPUT POWER

Based on the application specifications and the regulator's configuration, the input and output power requirements need to be checked. For the LDO, the input and output powers are calculated:

$$P_{OUT(LDO)} = V_{OUT} \times I_{OUT}$$
$$P_{IN(LDO)} = V_{IN} \times I_{IN}$$
$$I_{IN} = I_{OUT}$$

For the buck converters, the input and output powers are calculated:

$$P_{OUT(BUCK)} = V_{OUT} \times I_{OUT}$$
$$P_{IN(BUCK)} = \frac{P_{OUT(BUCK)}}{\eta}$$
$$I_{IN} = \frac{P_{IN(BUCK)}}{V_{IN}}$$

Where η is the estimated efficiency of the buck converters, use 0.85 for the initial estimate.

When making the power calculations, be sure to include any input currents from regulators that are connected to the converter as part of the output current. For example, the input currents of Buck Converters 2 and 3 should be added to the system load current of Buck Converter 1 shown in Figure 8. After completing the calculations for all the regulators, check to make sure there are no violations of the power budget – input currents exceeding supply current capabilities, or output currents exceeding the regulator's rating.

Buck Converters 2 and 3 there is a maximum limit of 83.6%. The duty cycle for a buck converter is calculated using:

$$D = \frac{V_{OUT}}{V_{IN}} \times 100\%$$

This equation works for calculating the minimum duty cycle, however, the above formula does not take into account load currents and losses. A more accurate equation for calculating the maximum duty under load follows:

$$D_{MAX} = \frac{V_{OUT} + (R_{DO} + R_{DC}) \times I_{OUT}}{V_{IN(MIN)}} \times 100\%$$

Where R_{DO} is the equivalent dropout resistance of the buck converter and R_{DC} is the DC resistance of the inductor.

Check to make sure all the buck converters are within the duty cycle limit. Converters, where the calculated maximum duty cycle exceeds the limit, run the risk of dropping out of regulation under load. Conversely, the maximum duty cycle limit can be used to predict the maximum load current that can be drawn without the output dropping out of regulation.

$$I_{OUT(MAX)} = \frac{\frac{D_{MAX} \times V_{IN}}{100\%} - V_{OUT}}{(R_{DO} + R_{DC})}$$

LDO DROPOUT AND POWER DISSIPATION

The input of the LDO needs to exceed the output voltage by a minimum of 250mV, in order to maintain regulation. If the input voltage falls below the dropout level, the output voltage will also start to fall and begin to track the input voltage down. However, choosing an input voltage that exceeds the output voltage by a large amount is not recommended either. This is due to increased power dissipation. The linear regulators power dissipation is calculated using:

$$P_{DISS} = (V_{OUT} - V_{IN}) \times I_{OUT}$$

Since the maximum power dissipation for the LDO is 375mW, the user can determine what the limits are for the LDO's input voltage.

$$V_{OUT} + 0.25V \le V_{IN} \le V_{OUT} + \frac{0.375}{I_{OUT}}$$

CASCADED OPERATION, SEQUENCING, AND LEAKAGE

When the 34700 is configured for cascaded operation, where the output of one regulator powers the input of another regulator (see Figure 8), the startup sequence also needs to be cascaded. The output voltage of the first regulator needs to be up and stable before enabling the downstream regulator, otherwise startup overshoot can occur.

Even without being configured for cascaded operation, the user may prefer the cascaded sequence to prevent startup latch-up or race conditions. With the four independent enables provided, the user can program any power up sequence that the application requires. The enable pins can be controlled by a host processor, a programmable logic device, or a power supply sequencer IC. If the application requires a simpler implementation of the cascaded sequence startup, a single enable signal can be used to start the first regulator in the sequence. When the first regulator is near or in regulation, its output is used to enable the next regulator in the sequence. See Figure 9. Note that there is a time delay from when the enable signal is asserted, until when the soft start ramp begins. For Buck Converter 1, the delay is typically 1ms. For Buck Converter 2 and 3, the delay is typically 160μs.

When sequencing the regulators on, one parameter that must be considered is the leakage specification. Buck Converters 2 and 3 exhibit 400μA of leakage current between VIN and the switch node. This results in the output voltage floating up if the load impedance is high. In cases where the output voltage is floating, it is recommended adding a 1K Ohm resistor between the output and ground.

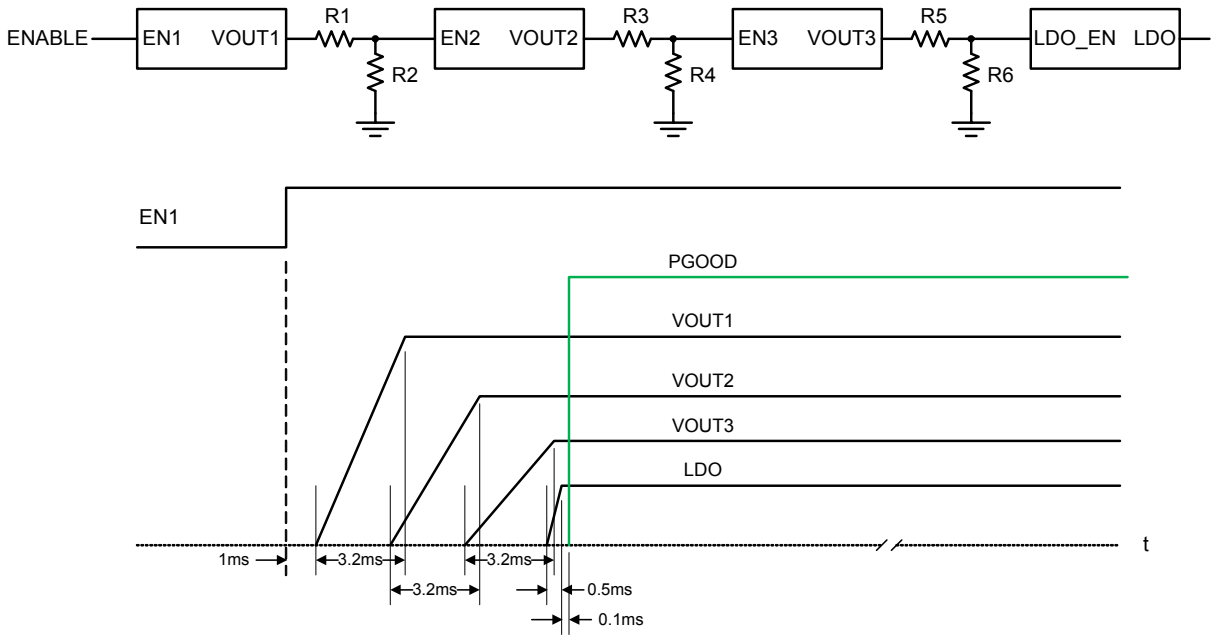


Figure 9. 34700 Cascade Sequence

SHUTDOWN SEQUENCE

The shutdown sequence is controlled by the enable pins. By pulling the ENABLE pin low or letting it float, the corresponding regulator is disabled. If the application is being controlled by the host processor or programmable logic device, the regulators can be shutdown in any order. Most power supply sequencer ICs shutdown the regulators in the reverse order of their startup. The first regulator that is turned on is the last regulator to be turned off. For the single ENABLE pin sequencer shown in Figure 9, the shutdown order is the same as for startup; the first regulator that is turned on, is the first regulator turned off.

LAYOUT GUIDELINES

The layout of any switching regulator requires careful consideration. First, there are high di/dt signals present, and the traces carrying these signals need to be kept as short and as wide as possible to minimize the trace inductance, and therefore reduce the voltage spikes they can create. To do this, an understanding of the major current carrying loops is important. See Figure 10. These loops, and their associated components, should be placed in such a way as to minimize the loop size to prevent coupling to other parts of the circuit. Also, the current carrying power traces and their associated return traces should run adjacent to one another, to minimize the amount of noise coupling. If sensitive traces must cross the current carrying traces, they should be made perpendicular to one another to reduce field interaction.

Second, small signal components which connect to sensitive nodes need consideration. The critical small signal components are the ones associated with the feedback circuit. The high impedance input of the error amp is especially sensitive to noise, and the feedback and compensation components should be placed as far from the switch node, and as close to the input of the error amplifier as possible. Other critical small signal components include the bypass capacitors for VIN, VGREG, and VDDI. Locate the bypass capacitors as close to the pin as possible.

The use of a multi-layer printed circuit board is recommended. Dedicate one layer, usually the layer under the top layer, as a ground plane. Make all critical component ground connections with vias to this layer. Make sure that the power grounds, GND2 and GND3, are connected directly to the ground plane and not routed through the thermal pad or analog ground. Dedicate another layer as a power plane and split this plane into local areas for common voltage nets.

The IC input supply (VIN) should be connected through an RC filter to the 9V to 18V input supply, to prevent noise from Buck Regulator 1's power input (VIN1) from injecting switching noise into the analog circuitry. If possible, further isolation can be made by routing a dedicated trace for VIN, and a separate trace for VIN1.

In order to effectively transfer heat from the top layer to the ground plane and other layers of the printed circuit board, thermal vias need to be used in the thermal pad design. It is recommended that 5 to 9 vias be spaced evenly and have a finished diameter of 0.3mm.

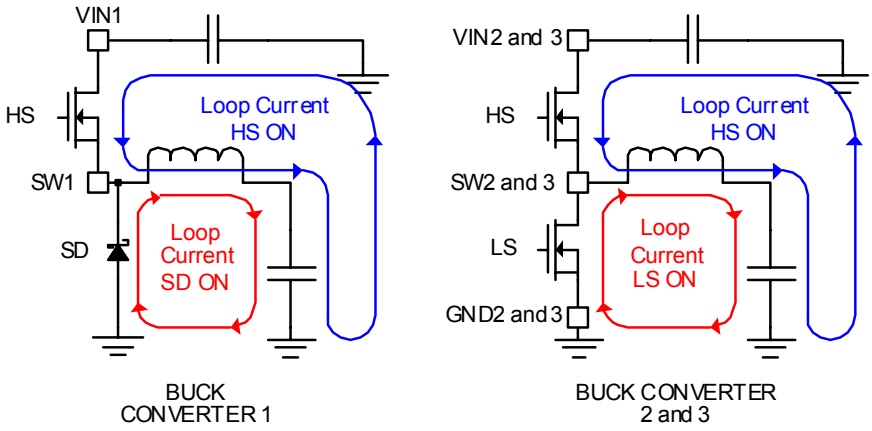


Figure 10. Current Loops

COMPONENT SELECTION

Setting the Output Voltage

For all the regulators, the feedback resistor divider sets the output voltage. See Figure 11 for the feedback and compensation components referred to in the equations. For the buck regulators, choose a value of about 20K for the upper resistor, and calculate the lower resistor using the following equations:

$$R_{BOT} = \frac{R_{TOP} \times V_{REF}}{V_{OUT} - V_{REF}}$$

$$V_{OUT} = V_{REF}\left(\frac{R_{TOP}}{R_{BOT}} + 1\right)$$

where, V_{REF} = 0.7V

For the LDO regulator, choose a value of about 10K for the lower resistor, and calculate the upper resistor using the following equations:

$$R_{TOP} = R_{BOT}\left(\frac{V_{OUT}}{V_{REF}} - 1\right)$$

$$V_{OUT} = V_{REF}\left(\frac{R_{TOP}}{R_{BOT}} + 1\right)$$

where, V_{REF} = 0.7V

Choose the closest standard resistance values, check the output voltage by using the equations above, and adjust the values if necessary.

Setting the Enable for Cascade Sequencing

For the cascaded startup sequence shown in Figure 9, the resistor divider sets the output voltage level where the next the next regulator in the sequence will start or shutdown. For top resistors R1, R3, and R5, choose a value of 10K, and calculate the value for the bottom resistors R2, R4, and R6, using the following equation:

$$R_{BOT} = \frac{0.78 \times R_{TOP}}{0.95V_{OUT} - 0.78}$$

where, V_{OUT} is the value calculated above using standard value resistors.

Choose the closest standard resistance values and check the output voltage levels that enable and disable the regulator in sequence, using the following equations, and adjust if necessary:

$$V_{OUT(EN)} = 0.78\left(\frac{R_{TOP} + R_{BOT}}{R_{BOT}}\right)$$

$$V_{OUT(DISABLE)} = 0.61\left(\frac{R_{TOP} + R_{BOT}}{R_{BOT}}\right)$$

These equations should give an enable of ~95% of V_{OUT}, and a disable of ~75% of V_{OUT}.

Catch Diode

An external catch diode is required for Buck Converter 1 to provide a return path for the inductor current when the high side switch is off. The catch diode should be located close to the 34700 and connected using short, wide traces. See the Layout Guidelines for more details.

It is recommended to use a Schottky diode, due to their low forward voltage drop and fast switching speed. This provides the best efficiency and performance, and is especially true when the output voltage is less than 5V. Choose a Schottky with a 2A to 3A average output current rating and a reverse voltage specified for 30V.

Inductor

The output inductor is sized to meet the output voltage ripple requirements, and to minimize the load transient response time. For continuous conduction mode (CCM) operation, where the inductor does not fully discharge during the switch off time, and assuming an ideal switch and catch diode, the following equation is used:

$$L = \left(V_{IN(MAX)} - V_{OUT}\right) \times \frac{V_{OUT}}{V_{IN(MAX)}} \times \frac{1}{f_{SW}} \times \frac{1}{N \times I_{OUT(MAX)}}$$

where, f_{SW} is the switching frequency and N is the ripple current to output current ratio.

A high ripple current to output current ratio gives improved load transient response, but also increases output ripple, and results in lower efficiency. A value of 0.3 to 0.4 for N represents a good trade off between efficiency, ripple, and load transient response.

After calculating a value for the inductor, choose the closest standard value and then determine the ripple current and peak current using the following equations:

$$\Delta I_L = \frac{\left(V_{IN(MAX)} - V_{OUT}\right)}{L} \times \frac{V_{OUT}}{V_{IN(MAX)}} \times \frac{1}{f_{SW}}$$

$$I_{PEAK} = I_{OUT(MAX)} + \frac{\Delta I_L}{2}$$

The peak inductor current determines the required saturation current rating of the inductor. Choose an inductor with a saturation current rating that's large enough to compensate for circuit tolerances. The minimum acceptable margin for this purpose is at least 20% above the calculated rating.

To minimize copper losses, choose an inductor with the lowest possible DCR. As a general rule of thumb, look for a DCR of approximately 5mOhms per μH of inductance.

Output Capacitor

The output capacitor is required to minimize the voltage overshoot and undershoot in response to load transients, and to reduce the ripple present at the output of a buck regulator. The same holds true for the linear regulator.

For the LDO, a 10μF, low ESR capacitor is required as the output capacitor. Smaller values may result in instability. Make sure the capacitor has good temperature characteristics, and a suitable voltage rating. As a general rule, choose ceramic capacitors with a X5R, or X7R dielectric and a voltage rating of 1.5 to 2 times the output voltage, but check with the manufacturer for detailed information.

For the buck converters, large transient load overshoots and large voltage ripple are caused by insufficient capacitance as well as high equivalent series resistance (ESR) and high equivalent series inductance (ESL) in the capacitor. To meet the application requirements, the output capacitor must be specified with ample capacitance and low ESR and ESL.

To deal with overshoot, where the output voltage overshoots its regulated value when a full load is removed from the output, the output capacitor must be large enough to prevent the energy stored in the inductor from causing the voltage to spike above the specified maximum output voltage. The amount of capacitance required can be estimated using the following equation:

$$C_{OUT} = \frac{L\left(I_{PEAK}\right)^2}{\left(\Delta V + V_{OUT}\right)^2 - {V_{OUT}}^2}$$

where, ΔV is the maximum output voltage overshoot.

Allow a 20% capacitance tolerance and choose the closest standard value.

The ESR of the output capacitor also contributes to the transient overshoot. The maximum ESR can be estimated using the equation:

$$C_{ESR} = \frac{\Delta V}{\Delta I_{TRANSIENT}}$$

where, $\Delta I_{TRANSIENT}$ is the magnitude of the load transient, and ΔV is the maximum output voltage overshoot.

The ESR of the output capacitor usually dominates the output voltage ripple. The maximum ESR can be calculated using the equation:

$$C_{ESR} = \frac{V_{RIPPLE}}{\Delta I_L}$$

where, V_{RIPPLE} is the specified ripple voltage allowed.

Note that most capacitor vendors do not specify the ESL of the capacitor and board layout also contribute to the ripple and overshoot. Consult the manufacturer for more information on the characteristics and selection of output capacitors. Use these calculations as a design guideline. After selecting the output capacitors, make adjustments based on actual test results.

Input Capacitor

Generally, a mix of bypass capacitors is used for the input supply. Use a small ceramic capacitor for high frequency decoupling, and bulk capacitors to supply the surge of current required each time the high side MOSFET turns on. Place the small ceramic capacitor close to the power input pins.

For reliable operation, select the bulk input capacitors with voltage and RMS ripple current ratings above the maximum input voltage, and the largest RMS current required by the application. As a general guideline, the capacitor's voltage rating should be around 1.5 times the maximum input voltage, but the manufacturer's de-rating information should be followed. The RMS ripple current rating that the bulk input capacitors require can be estimated by the following equation:

$$I_{IN(RMS)} = I_{OUT}\sqrt{D - D^2}$$

where D = V_{OUT}/V_{IN}.

The worst case occurs when V_{IN} = 2 x V_{OUT}, yielding a worst case ripple current of $I_{IN(RMS)} = I_{OUT}/2$.

The bulk input capacitance required for a buck converter depends on the impedance of the input supply. For common laboratory supplies, 10μF to 20μF of capacitance per ampere of input ripple current is usually sufficient. Use this general guideline as a starting point and adjust the input capacitance based on actual test results.

Tantalum capacitors can be used as input capacitors, but proper de-rating must be used or they can fail "short" and present a fire hazard. Ceramic capacitors and aluminum electrolytic capacitors don't have this failure mechanism, making them a preferred choice. However, ceramic capacitors can exhibit piezo effect and emit an audible buzz. Polymer capacitors do not have this audible noise problem, but they can also fail "short". However, polymer capacitors are much more robust than tantalums, and therefore are suitable as input capacitors. Consult the manufacturer for more information on the use and de-rating of capacitors.

Bootstrap Capacitor

The external bootstrap capacitor is part of a charge pump circuit which is used to drive the gate of the high side N-MOSFET. This capacitor develops a floating voltage supply which is referenced to the switch node (SW) or the source of the high side MOSFET. The bootstrap capacitor is charged every cycle, when the low side MOSFET or the catch diode conducts, to a voltage of about V_{GREG}. To turn the high side switch on, the bootstrap capacitor needs to be large enough to charge the gate-source capacitance of the N-MOSFET without a significant drop in voltage. For the 34700 the bootstrap capacitor should be 0.1μF.

Compensation

The voltage mode buck converters used in the 34700 require a Type III compensation network as shown in Figure 11. The Type III network utilizes two zeroes to give a phase boost of 180°. This phase boost is necessary to counteract the double pole of the output LC filter.

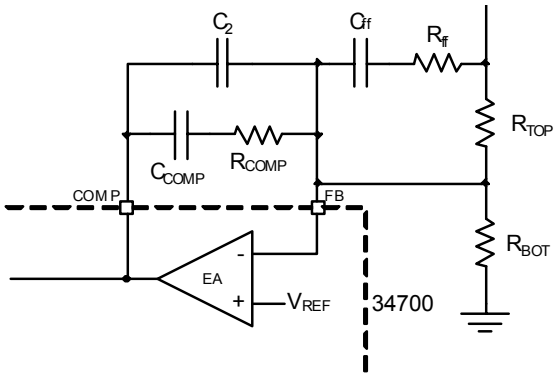


Figure 11. Type III Compensation Network

The closed loop transfer function is comprised of the modulator, the filter, and the compensation transfer functions. Before we can determine the compensation we need to first calculate the gains and break frequencies of the modulator and filter.

$$G_{MOD} = \frac{D_{MAX} \times V_{IN}}{V_{RAMP}}$$

where, G_{MOD} is the modulator gain, and D_{MAX} and V_{RAMP} are given in the electrical table.

$$f_{LC} = \frac{1}{2\pi\sqrt{L \times C}}$$

where, f_{LC} is the location of the LC filter double pole.

$$f_{ESR} = \frac{1}{2\pi \times C \times ESR}$$

where, f_{ESR} is the location of the ESR zero, and ESR is the equivalent series resistance of the output capacitors.

As shown in Figure 11, the compensation network consists of the error amplifier (internal to the 34700), and the external resistors and capacitors. If designed properly, the compensation network will yield a closed loop transfer function with a high crossover (0dB) frequency, and adequate phase margin to be stable. Use the following steps to calculate the compensation components.

1. Using the value for R_{TOP} and R_{BOT}, selected in the Setting the Output Voltage section, calculate the value

of R_{COMP} for the desired converter bandwidth, f_0. Typically f_0 is chosen to be 1/10th of the switching frequency.

$$R_{COMP} = \frac{V_{RAMP} \times R_{TOP} \times f_0}{D_{MAX} \times V_{IN} \times f_{LC}}$$

This will set the high frequency gain of the error amplifier (R_{COMP}/R_{TOP}), and shift the open loop gain up to give the desired bandwidth.

2. Using the value for R_{COMP}, calculate the value of C_{COMP}, to place a zero, to cancel one of the double poles. This zero (f_{Z1}) is placed at a fraction of the LC double pole frequency.

$$C_{COMP} = \frac{1}{2\pi \times R_{COMP} \times K_{LC} \times f_{LC}}$$

where, K_{LC} is the fraction of the LC filter frequency = f_{Z1}/f_{LC}. Typical values for K_{LC} are 0.2 to 0.7, but begin with 0.5.

3. Using the values of R_{COMP} and C_{COMP}, calculate the value of C_2 to place a pole (f_{P1}) at the ESR zero frequency. Note that if ceramic capacitors are used for the output capacitors, the ESR zero will be at a very high frequency, making the calculated value of C_2 very small. If this is the case, C_2 may not be needed, saving a component and space.

$$C_2 = \frac{C_{COMP}}{(2\pi \times R_{COMP} \times C_{COMP} \times f_{ESR}) - 1}$$

4. Calculate the value of R_{ff} and C_{ff}, to place a zero (f_{Z2}) at the LC double pole frequency, and a pole (f_{P2}) at half the switching frequency.

$$R_{ff} = \frac{R_{TOP}}{\left(\frac{f_{SW}}{2 \times f_{LC}}\right) - 1}$$

$$C_{ff} = \frac{1}{\pi \times R_{ff} \times f_{SW}}$$

Choose the closest standard value for the compensation components. Although precision components are not required, do not use poor quality components that have large tolerances over-temperature. As a double check, it is recommended to use a mathematical model to plot the closed loop response. Check that the closed loop gain is within the error amplifier's open loop gain, and there is enough phase margin, and make adjustments as necessary. A stable control loop has a gain crossing with close to -20dB/decade, and a phase margin of at least 45°. The following equations describe the frequency response of the modulator, feedback compensation, and the closed loop.

$$G_{MOD}(f) = \frac{D_{MAX} \times V_{IN}}{V_{RAMP}} \cdot \frac{1 + s(f) \cdot ESR \cdot C}{1 + s(f) \cdot (ESR + DCR) \cdot C + s^2(f) \cdot L \cdot C}$$

$$H_{COMP}(f) = \frac{1 + s(f) \cdot R_{COMP} \cdot C_{COMP}}{s(f) \cdot R_{TOP} \cdot (C_{COMP} + C_2)} \cdot \frac{1 + s(f) \cdot (R_{TOP} + R_{ff}) \cdot C_{ff}}{1 + s(f) \cdot R_{ff} \cdot C_{ff} \cdot \left(1 + s(f) \cdot R_{COMP} \cdot \left(\frac{C_{COMP} \cdot C_2}{C_{COMP} + C_2}\right)\right)}$$

$$G_{CL}(f) = G_{MOD}(f) \cdot H_{COMP}(f)$$

where, $s(f) = j \cdot 2\pi \cdot f$

A more intuitive representation of the mathematical model, is an asymptotic bode plot of the buck converter's gain versus frequency, as shown in Figure 12. Use of the previous steps should result in a compensation gain similar to the one shown in the bode plot. The open loop error amplifier gain bounds the compensation gain. Check the compensation gain at f_{P1} or f_{P2}, whichever is greater, against the capabilities of the error amplifier. For reference, the equations for the compensation break frequencies are given.

$$f_{Z1} = \frac{1}{2\pi \times R_{COMP} \times C_{COMP}}$$

$$f_{P1} = \frac{1}{2\pi \times R_{COMP} \times \left(\frac{C_{COMP} \times C_2}{C_{COMP} + C_2} \right)}$$

$$f_{Z2} = \frac{1}{2\pi \times (R_{TOP} + R_{ff}) \times C_{ff}}$$

$$f_{P2} = \frac{1}{2\pi \times R_{ff} \times C_{ff}}$$

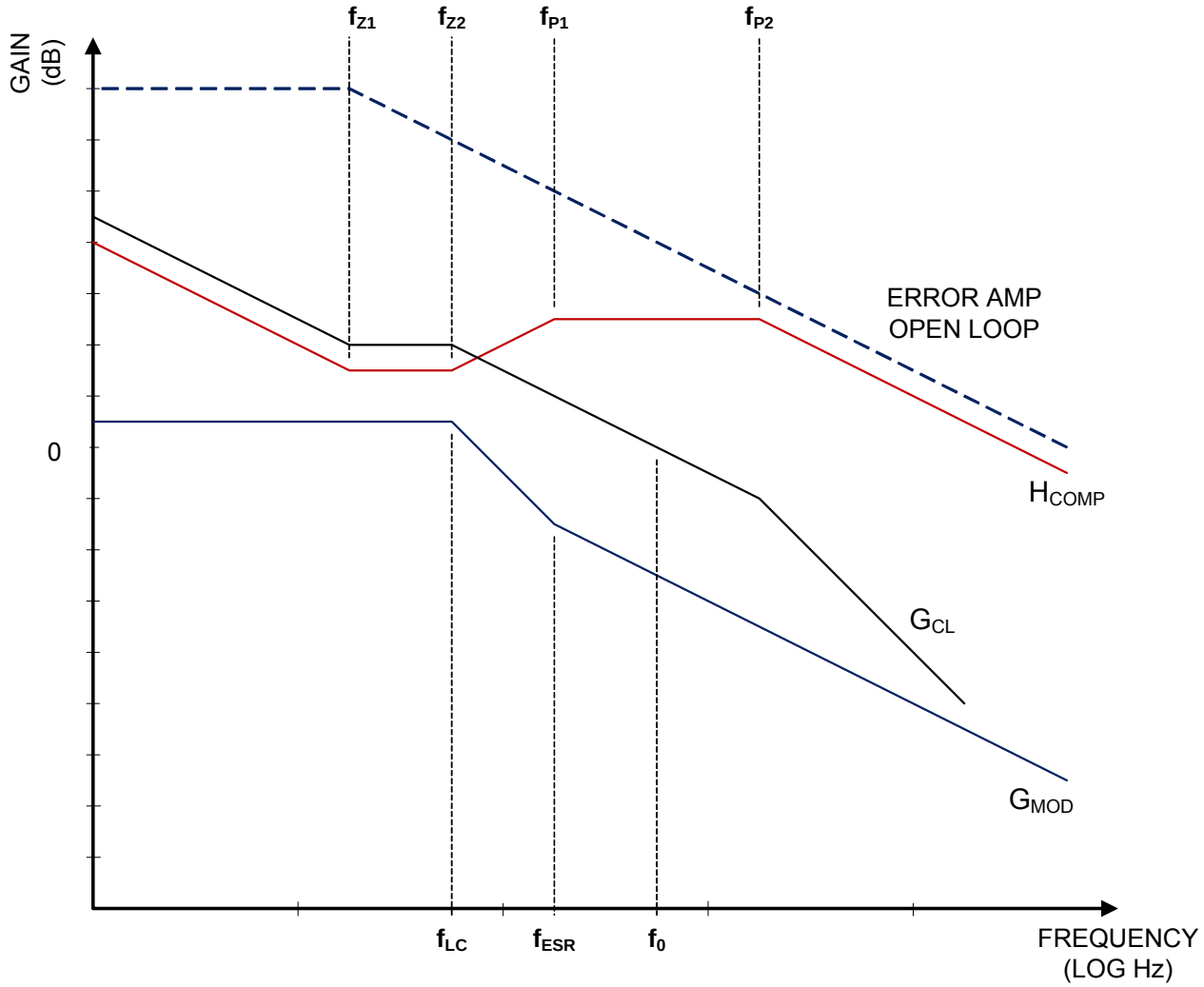
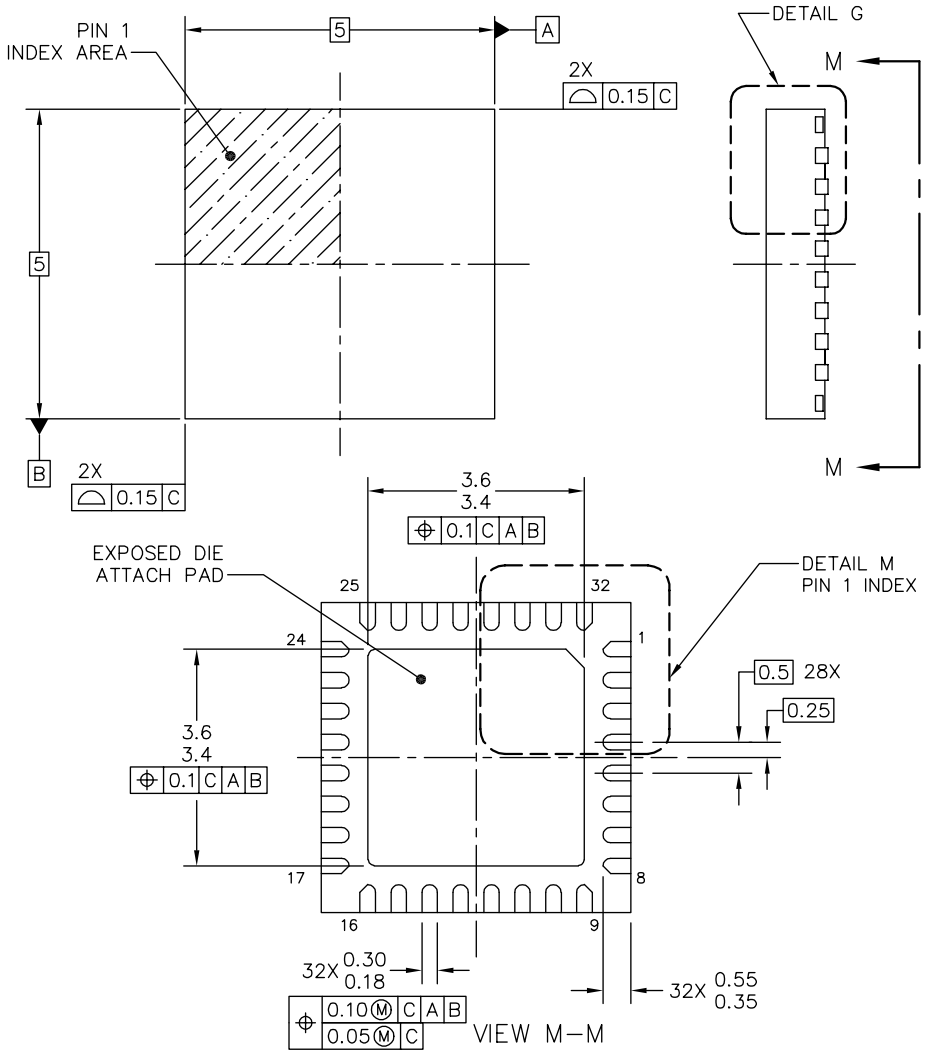


Figure 12. Bode Plot of the Buck Converter

PACKAGING

PACKAGE DIMENSIONS

For the most current package revision, visit **www.freescale.com** and perform a keyword search using the “98A” listed below.



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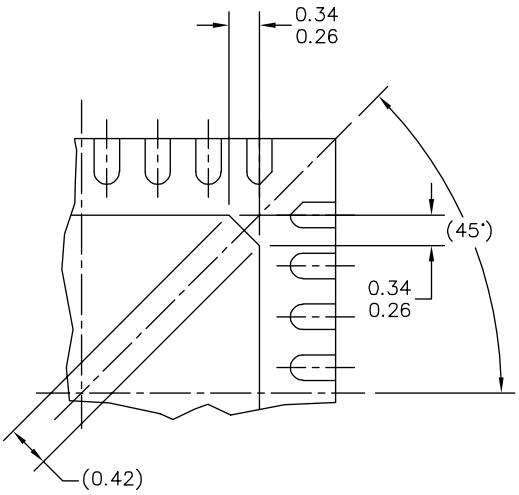
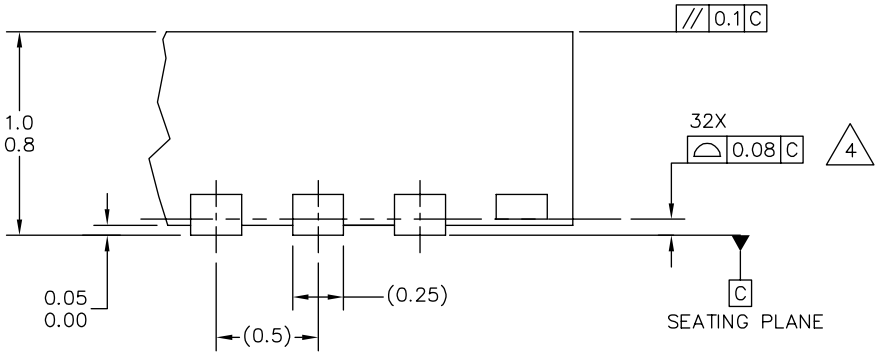
TITLE: THERMALLY ENHANCED QUAD FLAT NON–LEADED PACKAGE (QFN) 32 TERMINAL, 0.50 PITCH (5 X 5 X 1) 3.5 X 3.5 EP, CASE OUTLINE	DOCUMENT NO: 98ASA10800D	REV: O
	CASE NUMBER: 1972–01	29 AUG 2007
	STANDARD: NON–JEDEC	

EP SUFFIX (Pb FREE)
32-PIN
98ASA10800D
REVISION D

34700



DETAIL M
PIN 1 BACKSIDE IDENTIFIER



DETAIL G
VIEW ROTATED 90°CW

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34700

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. RADIUS ON TERMINAL IS OPTIONAL.
4. COPLANARITY APPLIES TO LEADS, AND DIE ATTACH PAD.
5. MINIMUM METAL GAP SHOULD BE 0.2 MM.

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REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
1.0	4/2008	• Initial release
2.0	4/2008	• Changed the 98A package drawing from **98ARE10566D to 98ASA10800D**
3.0	5/2008	• Corrected error on MC34700 Simplified Application Diagram on page 1
4	6/2008	• Changed category from “Advance Information” to “Technical Data”

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